A Simple Switching Loss Model for Buck Voltage Regulators with Current Source Drive

Wilson Eberle, Zhiliang Zhang, Yan-Fei Liu, and Paresh Sen
Queen's Power Group, www.queenspowergroup.com
Department of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, Canada, K7L 3N6
wilson.eberle@ece.queensu.ca, zhiliang.zhang@ece.queensu.ca, yanfei.liu@queensu.ca and senp@queensu.ca

Abstract - A review of switching loss mechanisms for synchronous buck voltage regulators is presented. Following the review, a new simple analytical switching loss model is proposed for voltage regulators with current source drive. The model includes the impact of common source inductance and parasitic inductance on switching loss. It uses simple equations to calculate the rise and fall times and piecewise linear approximations of the MOSFET voltage and current waveforms to allow quick and accurate calculation of switching loss. Spice is used to demonstrate the accuracy of the model operating in a 1MHz synchronous buck voltage regulator at 12V input, 1.3V output. Experimental results are presented to demonstrate the accuracy of the proposed model.

I. Introduction

In order to optimally design a high frequency switching converter, engineers and researchers begin their design by estimating the losses in a design file that is typically created using a spreadsheet, or other mathematical software. Device data sheet values and analytical models are used to calculate the losses. Using the loss models, many design parameters and components are compared to achieve a design with the optimal combination of efficiency and cost.

One of the most popular analytical switching loss models is the piecewise linear model presented in [1]. This model is referred to as the conventional model and is used as a benchmark later for comparison purposes with the proposed model. This model enables simple and rapid estimation of switching loss, however, the main drawback is that it neglects the switching loss dependences due to parasitic inductances. Typically, this model predicts that turn on and turn off loss are nearly similar in magnitude, however in a real converter operating at a high switching frequency, the model is highly inaccurate since turn off loss is much larger due to parasitic inductances, so it does not predict switching loss accurately.

A comprehensive analytical switching loss model for voltage source drive is presented in [2] and a model for current source drive is presented in [3]. These models are an extension of the model presented in [4], with the advantage that they provide accurate characterization of switching loss when common source inductance is included. Common source inductance is inductance in the source lead of a power MOSFET that is common to the powertrain circuit and driver. The main drawback of the models in [2]-[4] is their complexity.

The synchronous buck remains the topology of choice for voltage regulators (VRs) in today's computers [5]-[10]. However, in order to properly model switching loss in a buck VR, a detailed understanding of the impact of MOSFET gate capacitance, common source inductance, other parasitic inductance and load current on switching loss is necessary. This is most easily accomplished through careful examination of waveforms through simulation and experiments, which are included in section II following the approach presented in [5].

In section III, a new switching loss model is proposed with the goal of maintaining the relative simplicity of the very popular conventional model in [1], while improving the accuracy for high frequency synchronous buck with parasitic circuit inductances, including common source inductance. The proposed model is an extension of the model presented in [10] for the current source drivers presented in [8],[9]. These drivers are designed to operate with nearly constant current supplied to the power MOSFET gate. The advantage of this class of drivers is that they eliminate the back voltage, v_{Ls1}, in the gate circuit that reduces the gate current in conventional voltage source gate drivers. In particular, the model predicts the large decrease in turn on loss and increase in turn off loss that occurs as undesired circuit parasitic inductance increases.

II. Impact of Parasitic Inductance and Load

A synchronous buck converter is illustrated in Fig. 1. It includes parasitic drain and source inductances for the HS MOSFET, M_1, and SR MOSFET, M_2. It can be assumed that the source inductances, L_{s1} and L_{s2} are common to their respective drive signals. Any other inductance in the source that is not common to the source is assumed to be lumped with the drain inductances, L_{d1} and L_{d2}. These inductances have a significant impact on the switching loss behavior in high frequency synchronous buck voltage regulators.

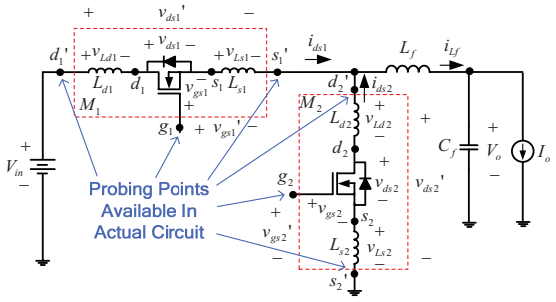


Fig. 1. Synchronous buck voltage regulator with parasitic inductances

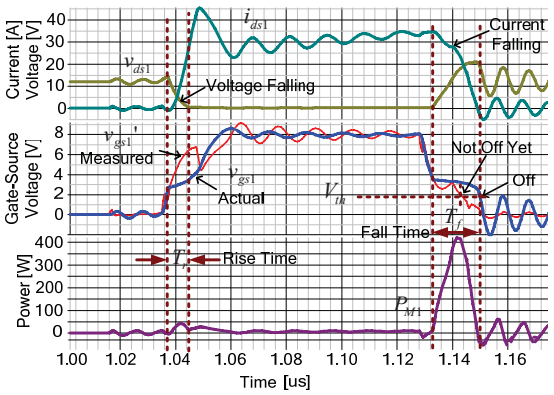


Fig. 2. Synchronous buck voltage regulator HS MOSFET waveforms (top: actual drain-source voltage, v_{ds1} and drain current, i_{ds1}; middle: measured gate-source voltage, v_{gs1}' and actual gate-source voltage (bold), v_{gs1}; bottom: HS MOSFET power, $v_{ds1}i_{ds1}$)

During the switching transitions, the HS MOSFET operates in the saturation (linear) mode as a dependent current source simultaneously supporting the current through the device and voltage across it. At turn on and turn off, the gate-source voltage, v_{gs1}, is held at the plateau voltage, V_{pl}, by the feedback mechanism provided by the voltage across the common source inductance, v_{Ls1}.

Simulation waveforms are illustrated in Fig. 2 for a buck voltage regulator at 12V input, 30A load, 8V drive voltage and 1MHz switching frequency. The top curves are the HS MOSFET switch current, i_{ds1} and actual drain-to-source voltage, v_{ds1}. The second set of curves are the v_{gs1} (Actual) and v_{gs1}' (Measured; $v_{gs1}'=v_{gs1}+v_{Ls1}$) waveforms, which are included to demonstrate that measuring v_{gs1}' in the lab provides an inaccurate representation of the switching times. The bottom curve is the power loss in the MOSFET, $P_{M1}=v_{ds1}i_{ds1}$. Typical, parasitic inductance values for common package types are provided by the semiconductor manufacturers in application notes [6]-[7] and range from approximately 250pH-1nH, depending on the package type. Matched inductances of 500pH each for the four inductances were used in the simulation.

As can be observed from the circuit in Fig. 1 and the waveforms in Fig. 2, at turn on, as the HS MOSFET current increases, v_{Ls1} is positive in the direction noted, so this voltage subtracts from the V_{cc} voltage applied to the gate, enabling $v_{gs1}=V_{pl}$ while the MOSFET operates in the saturation mode. At the same time, the four parasitic inductances provide a current snubbing effect, which virtually eliminates turn on switching loss enabling a near zero current switching (ZCS) turn on. During this transition, the rise time, T_r, is dictated by the gate driver's ability to charge the MOSFET gate capacitances (C_{iss} from V_{th} to V_{pl} and C_{gd} to V_{in}), which is the time for v_{ds1} to fall to zero. Then, it is assumed that this time is independent of the time it takes i_{ds1} to rise to the buck inductor current.

At turn off, as the HS MOSFET current decreases, v_{Ls1} is negative in the direction noted Fig. 1, so this voltage subtracts from the low impedance source voltage (ideally zero volts) applied to the gate enabling $v_{gs1}=V_{pl}$ while the MOSFET operates in the saturation mode. During this transition, the fall time, T_f, is the time for the HS MOSFET current to fall from the buck inductor current to zero. This time is dictated by both the gate driver's ability to discharge the MOSFET gate capacitances (C_{gd} from V_{in}, and C_{iss} from V_{pl} to V_{th}) and by the four parasitic inductances, which prolong the time for i_{ds1} to fall to zero by limiting the di_{ds}/dt.

As alluded to in the two paragraphs above, the MOSFET and trace parasitic inductances have vastly different effects at turn on and turn off. At turn on, the inductances provide a current snubbing effect, which decreases turn on switching loss. At turn off, the inductances increase the turn off loss by prolonging T_f. In addition, as load current increases, T_f increases, so turn off losses increase proportionally to I_o^2 (i.e. proportional to I_o and $T_f(I_o)$). In contrast, at turn on, the load current magnitude has ideally no effect on the T_r. Therefore, in real circuits, turn off loss is much greater than turn on loss, which is clearly evident in the P_{M1} power loss waveform in Fig. 2.

Another important point to note from Fig. 1 and Fig. 2 is that in a real circuit, the board mounted packaged inductances are distributed within the MOSFET devices. Therefore, when probing in the lab, one only has access to the external terminals, g_1, s_1' and d_1' for the HS MOSFET and g_2, s_2' and d_2' for the SR. However, the actual nodes that provide waveform information relevant to the switching loss are at the unavailable internal nodes s_1 and d_1 for the HS MOSFET. Using the plateau portion of the measured gate-source voltage, v_{gs1}' to determine the switching loss times is misleading since the induced voltage across L_{s1} is included. Probing v_{gs1}' in the lab, one would observe a negligible T_r at turn on, and at turn off, T_f less than one half of the actual T_f. The actual v_{gs1} waveform, which cannot be measured in a real circuit, more clearly illustrates the plateau portions in T_r and T_f.

To demonstrate the effects of load current and common source inductance, experimental testing was done at a reduced frequency of 200kHz, with the source connection cut and a wire inserted in the common source path to measure the MOSFET current. Measurement waveforms are illustrated in Fig. 3, and Fig. 4, where the load current has been increased from 0A to 5A. With this method, the inductance of the wire (approximately 20nH) is much greater than the approximate total package inductance of 1nH, so the package inductance can be neglected allowing for measurement of v_{gs1} and v_{ds1}. As stated previously, it is noted that as load current increases from 0 to 5A, T_r remains nearly unchanged from 20ns to 22ns, but T_f increases significantly from 48ns to 96ns. In addition, at a constant load current of 5A, as illustrated in Fig. 5, as L_{s1} increases to 30nH (using a longer 3 inch wire), T_r remains relatively unchanged from 22ns to 24ns, while T_f further increases from 96ns to 160ns.

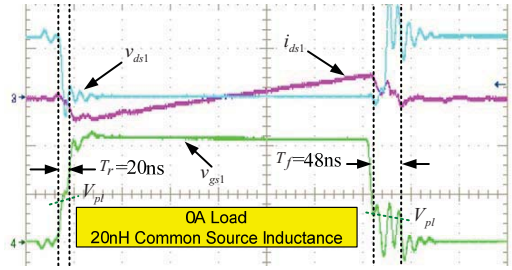


Fig. 3. Switching waveforms at 0A load and 20nH common source inductance (80ns/div; v_{ds1}: 10V/div; i_{ds1}: 5A/div; v_{gs1}: 5V/div)

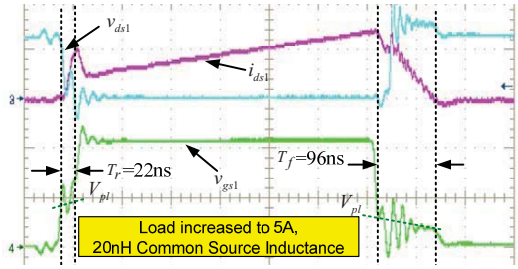


Fig. 4. Switching waveforms at 5A load and 20nH common source inductance (80ns/div; v_{ds1}: 10V/div; i_{ds1}: 5A/div; v_{gs1}: 5V/div)

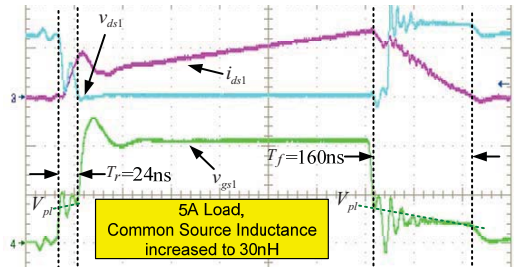


Fig. 5. Switching waveforms at 5A load with 30nH common source inductance (80ns/div; v_{ds1}: 10V/div; i_{ds1}: 5A/div; v_{gs1}: 5V/div)

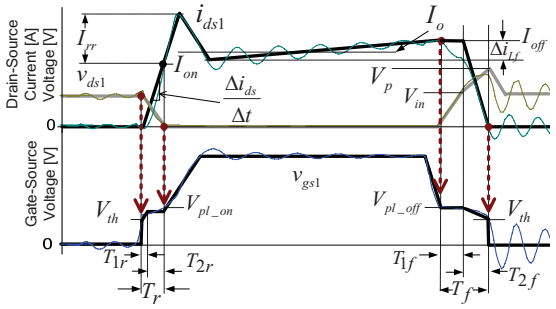


Fig. 6. Synchronous buck HS MOSFET waveforms with piecewise linear approximations of these waveforms in bold

III. Proposed Switching Loss Model

Typical switching waveforms for a synchronous buck VR are illustrated in Fig. 6. The proposed model uses the piecewise linear approximations (noted with thicker bold lines) of the switching waveforms in Fig. 6. Turn on switching loss occurs during T_r and turn off switching loss occurs during T_f. The key to the model is prediction of the turn on current, I_{on}, the rise and fall times, T_r and T_f, the reverse recovery current, I_{rr}, the magnitude of the rising current slope, $\Delta i_{ds}/\Delta t$, and the current drop, Δi_{1f}, when v_{ds1} rises to V_{in} at turn off. The goal of the model is to calculate the switching loss with respect to load current, driver gate current and total circuit inductance in a simple manner.

The MOSFET parasitic capacitances are required in the model. They are estimated using the effective values as follows in (1)-(3) using datasheet specification values for V_{ds1_spec}, C_{rss1_spec}, and C_{iss1_spec} [1]. The C_{ds1} capacitor of the synchronous buck HS MOSFET is neglected in the proposed model.

$$C_{gd1} = 2C_{rss1\_spec}\sqrt{\frac{V_{ds1\_spec}}{V_{in}}} \tag{1}$$

$$C_{iss1} = C_{iss1\_spec} \tag{2}$$

$$C_{gs1} = C_{iss1} - C_{gd1} \tag{3}$$

In the following sub-sections, derivations of the model for the turn on and turn off switching loss are presented.

A. Turn On Switching Loss Model

Piecewise linear turn on waveforms of i_{ds1}, v_{ds1}, v_{gs1} and the power loss in M_1, P_{M1}, are provided in Fig. 7. These waveforms and knowledge of the circuit operation are used extensively in this sub-section in order to derive the turn on loss, P_{on}.

By definition, P_{on}, is derived using the simple integral in (4), representing the average power over one switching period.

$$P_{on} = f_s \int_0^{T_r} v_{ds1} i_{ds} dt \tag{4}$$

Using the piecewise linear geometry for the voltage and current waveforms at turn on in Fig. 7, v_{ds1} is given by (5) and i_{ds} can be expressed by (6), allowing P_{on} to be given by (7), which evaluates to the expression given in (8).

$$v_{ds1} = V_{in} - \frac{V_{in}}{T_r}t \tag{5}$$

$$i_{ds} = \frac{I_{on}}{T_r}t \tag{6}$$

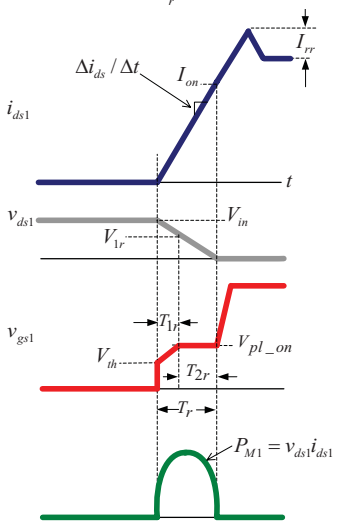


Fig. 7. Synchronous buck HS MOSFET waveforms at turn on with piecewise linear approximations

$$P_{on} = f_s \int_0^{T_r} \left[\left(\frac{I_{on}}{T_r} t \right) \left(V_{in} - \frac{V_{in}}{T_r} t \right) \right] dt \tag{7}$$

$$P_{on} = \frac{1}{6} V_{in} I_{on} T_r f_s \tag{8}$$

The power loss in (8) is the product of V_{in}, I_{on}, fs and T_r. The turn on current, I_{on} is the HS MOSFET drain current when v_{ds1}=0. The two parameters that are key to accurate prediction of P_{on} are the current at turn on, I_{on} and T_r. The remainder of this sub-section provides a simple procedure to calculate I_{on} and T_r, to enable calculation of P_{on}.

As discussed in section II, T_r is dictated by the gate driver's ability to charge the MOSFET gate capacitances, which is the time for v_{ds1} to fall to zero. This time is assumed independent of the time it takes i_{ds1} to rise to its final value. Under this assumption, T_r consists of two intervals, T_{1r} and T_{2r}.

1) Rise Time Interval T_{1r}: Charging C_{gs1} and C_{gd1}

The HS MOSFET equivalent circuit during T_{1r} is given in Fig. 8. R_g represents the internal gate resistance of the MOSFET.

During T_{1r}, the C_{gs1} capacitance is charged from V_{th} to V_{pl_on}, while the gate side of C_{gd1} charges from V_{th} to V_{pl_on} and the drain side of the C_{gd1} capacitance discharges from V_{in} to V_{1r}. Therefore, the change in voltage across C_{gd1} during T_{1r} is $[(V_{in}-V_{1r})+(V_{pl\_on}-V_{th})]$. Then, T_{1r} is given by (9), assuming an average gate charging current I_g. V_{pl_on} represents the plateau voltage at turn on and is given by (10), where Δi_{Lf} represents the buck output inductor ripple current. Since the peak MOSFET current at turn on is lower than at turn off, the plateau voltage at turn on differs slightly than at turn off. In (9), $\Delta V_{gsr}=V_{pl\_on}-V_{th}$.

$$T_{1r} = \frac{C_{gs1}\Delta V_{gsr} + C_{gd1}[\Delta V_{gsr} + (V_{in} - V_{1r})]}{I_g} \tag{9}$$

$$V_{pl\_on} = V_{th} + \frac{I_o - 0.5\Delta i_{Lf}}{g_{fs}} \tag{10}$$

The drain-source voltage during T_{1r} is given by (11), where $L_{loop}= L_{s1}+L_{d1}+L_{s2}+L_{d2}$.

$$v_{ds1} = V_{in} - L_{loop} \frac{di_{ds1}}{dt} \tag{11}$$

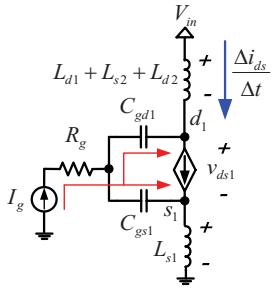


Fig. 8. Synchronous buck HS MOSFET equivalent circuit during T_{1r}

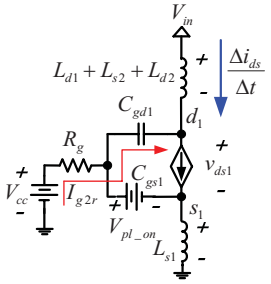


Fig. 9. Synchronous buck HS MOSFET equivalent circuit during T_{2r}

$$\frac{di_{ds1}}{dt} = \frac{dg_{fs}(v_{gs1} - V_{th})}{dt} = \frac{g_{fs} dv_{gs1}}{dt} \tag{12}$$

$$\frac{di_{ds}}{dt} \approx \frac{\Delta i_{ds}}{\Delta t} \tag{13}$$

$$\frac{\Delta i_{ds}}{\Delta t} = \frac{g_{fs}\Delta v_{gs1}}{\Delta t} = \frac{g_{fs}\Delta V_{gsr}}{T_{1r}} \tag{14}$$

Using (12)-(14), the intermediate voltage, V_{1r} is given by (15).

$$V_{1r} = V_{in} - L_{loop} \frac{g_{fs}\Delta V_{gsr}}{T_{1r}} \tag{15}$$

Using (9), and (14)- (15), solving for T_{1r} yields (16).

$$T_{1r} = \frac{C_{iss1} + \sqrt{(\Delta V_{gsr} C_{iss1})^2 + 4 I_g \Delta V_{gsr} C_{gd1} L_{loop} g_{fs}}}{2 I_g} \tag{16}$$

2) Rise Time Interval T_{2r}: Charging C_{gd1}

The HS MOSFET equivalent circuit during T_{2r} is given in Fig. 9. During T_{2r}, the gate voltage of the C_{gd1} capacitance remains constant at V_{pl_on}, while the drain node of C_{gd1} is discharged by current I_g, allowing T_{2r} to be given by (17).

$$T_{2r} = \frac{C_{gd1} V_{1r}}{I_g} \tag{17}$$

Using (14), (15) and (17), solving for T_{2r} yields (18).

$$T_{2r} = \frac{C_{gd1}\left(V_{in} - L_{loop} g_{fs} \frac{\Delta V_{gsr}}{T_{1r}} \right)}{I_g} \tag{18}$$

The total T_r is the sum of T_{1r} and T_{2r} as given by (19). The total turn on switching loss can be calculated using (8), (24) and (19).

$$T_r = T_{1r} + T_{2r} \tag{19}$$

The final step to determine the turn on loss is to estimate the current I_{on} at the end of T_r. Depending on the load current and parasitic inductances, calculating I_{on} can require estimation of the reverse recovery current, I_{rr}. The waveform in Fig. 10 is used to estimate I_{rr}. When the HS MOSFET turns on, the SR body diode cannot reverse block, so the SR current goes negative and the HS current spikes by the same magnitude. The total reverse recovery time is T_{rr}. The rising slope magnitude is $\Delta i_{ds}/\Delta t$ and the reverse recovery charge is Q_{rr}, which represents the shaded area as given by (20). Using the geometry, the reverse recovery current as a function of T_{rr} is given by (21). Then, eliminating T_{rr} from (20) and (21), (23) is derived, which represents I_{rr} as a function of

Q_{rr} and the known slope. In addition, since reverse recovery charge increases with load current, Q_{rr} is approximated using (22), where Q_{rr_spec} and I_{rr_spec} are the datasheet specification values.

$$Q_{rr} = \frac{1}{2} I_{rr} T_{rr} \tag{20}$$

$$I_{rr} = \frac{\Delta I_{ds}}{\Delta t} \frac{1}{2} T_{rr} \tag{21}$$

$$Q_{rr} = \frac{Q_{rr\_spec}}{I_{rr\_spec}} I_o \tag{22}$$

$$I_{rr} = \sqrt{\frac{\Delta I_{ds}}{\Delta t} Q_{rr}} \tag{23}$$

Since the rise time is dictated by the time for the HS MOSFET voltage, v_{ds1}, to fall to zero, the current at the end of T_r can be at any value equal to, or less than the inductor current plus the reverse recovery current. Therefore, the turn on current is determined by the slope of the current at turn on multiplied by T_r as given by the first condition in (24).

$$\begin{aligned} I_{on} &= \frac{\Delta i_{ds}}{\Delta t} T_r \quad \text{if} \quad \frac{\Delta i_{ds}}{\Delta t} T_r < I_o - 0.5\Delta i_{Lf} + I_{rr} \\ &= I_o - 0.5\Delta i_{Lf} + I_{rr} \quad \text{otherwise} \end{aligned} \tag{24}$$

The first condition holds true as long as the calculated value is less than the inductor current (I_o-0.5Δi_{Lf}) plus I_{rr}. Under light load and/or conditions where the parasitic inductances are small, using the current slope times T_r would yield a turn on current greater than the peak current. In this case, the current is capped at maximum value of the inductor current plus reverse recovery current as given by the second condition in (24).

B. *Turn Off Switching Loss Model*

Piecewise linear turn off waveforms of i_{ds1}, v_{ds1}, v_{gs1} and the power loss in M_1, P_{M1}, are provided in Fig. 11. These waveforms and knowledge of the circuit operation are used extensively in this sub-section in order to derive the turn off loss, P_{off}. The turn off transition consists of two intervals, T_{1f} and T_{2f}.

During T_{1f}, the Miller capacitor, C_{gd1} is discharged while v_{gs1} remains at V_{pl_off} and i_{ds1} is assumed to remain constant. In a real circuit, it is noted that i_{ds1} begins to fall during T_{1f}, however the current slope is limited due to the discharging of the C_{gd2} and C_{ds2} capacitors of the SR. During this interval, v_{ds1} increases from zero to V_{in}. Therefore, from the geometry, the turn off power loss, P_{1off}, during T_{1f} is given by (25).

$$P_{1off} = \frac{1}{2} V_{in} I_{off} T_{1f} f_s \tag{25}$$

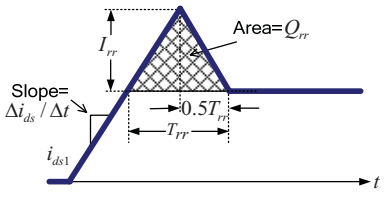


Fig. 10. Synchronous buck HS MOSFET current waveform approximation during reverse recovery at turn on

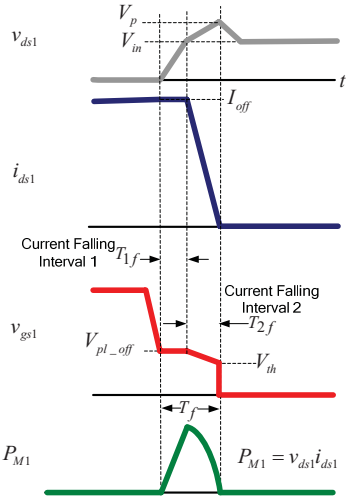


Fig. 11. Synchronous buck HS MOSFET waveforms at turn off with piecewise linear approximations

During T_{2f}, C_{gs1} is discharged from V_{pl_off} to V_{th}, while the gate node of C_{gd1} is also discharged from V_{pl_off} to V_{th} and the drain node of C_{gd1} is charged from V_{in} to the peak voltage at turn off, V_p. During this interval, i_{ds1} falls from I_{off} to zero, while v_{ds1} rises from V_{in} to V_p. Using a simple integral with the procedure presented in section III, the turn off loss during T_{2f} is approximated as P_{2off}, given by (26).

$$P_{2off} = \left(\frac{1}{6}(V_p - V_{in}+) I_{off} + \frac{1}{2} V_{in} I_{off} \right) T_{2f} f_s \tag{26}$$

The total turn off loss, P_{off}, is the sum of P_{1off} and P_{2off} as given by (27).

$$P_{off} = P_{1off} + P_{2off} \tag{27}$$

The key parameters to accurate prediction of the turn off loss are the HS MOSFET current at turn off, I_{off}, the intervals T_{1f}, and T_{2f}, and the peak overshoot voltage of v_{ds1}, V_p. The turn off current is the load current, I_o, plus half of the filter inductor peak-to-peak ripple current, Δi_{Lf}, as given by (28).

$$I_{off} = I_o + \frac{1}{2} \Delta i_{Lf} \tag{28}$$

The plateau voltage at turn off, V_{pl_off}, is given by (30). It differs slightly from V_{pl_on} at turn on due to the larger switch current during the transition.

$$V_{pl\_off} = V_{th} + \frac{I_o + 0.5\Delta i_{Lf}}{g_{fs}} \tag{29}$$

The turn off loss estimated using (27) is a function of T_f. During T_f, the current falls from I_{off} to zero and v_{ds1} rises from zero to V_p. It is a function of the driver's capability to discharge C_{gd1} and C_{iss1}, but in addition, it is a function of circuit parasitic inductances which limit the current falling slope and therefore, the falling time.

1) *Fall Time Interval T_{1f}: Discharging C_{gd1}*

The HS MOSFET equivalent circuit during T_{1f} is given in Fig. 12. Since i_{ds1} remains constant at I_{off}, the $\Delta i_{ds}/\Delta t$=0, so the parasitic inductors can be neglected. T_{1f}

is the time required to discharge the C_{gd1} capacitance by gate current I_g as given by (30).

$$T_{1f} = \frac{C_{gd1} V_{in}}{I_g} \tag{30}$$

2) Fall Time Interval T_{2f}: Current Falling and Discharging C_{gs1} and C_{gd1}

The HS MOSFET equivalent circuit during T_{2f} is given in Fig. 13. During T_{2f}, the C_{gs1} capacitance is discharged from V_{pl_off} voltage to V_{th}, while the voltage at the drain side of the C_{gd1} capacitance charges from V_{in} to V_p and the voltage at the gate side of C_{gd1} discharges from V_{pl_off} to V_{th}. Therefore, the change in voltage across C_{gd1} during T_{2f} is $[(V_p\text{-}V_{in})+(V_{pl\_off}\text{-}V_{th})]$. Then, T_{2f} is given by (31) , where $\Delta V_{gsf}=V_{pl\_off}\text{-}V_{th}$.

$$T_{2f} = \frac{C_{gs1}\Delta V_{gsf} + C_{gd1}[(V_p - V_{in}) + \Delta V_{gsf}]}{I_{g2f}} \tag{31}$$

The drain-source voltage during T_{2f} is given by (32), where $L_{loop}= L_{s1}+L_{d1}+L_{s2}+L_{d2}$.

$$v_{ds} = V_{in} + L_{loop}\frac{di_{ds1}}{dt} \tag{32}$$

Following the approach of the approximations made in (12) and (13), the peak overshoot voltage, V_p is given by (33).

$$V_p = V_{in} + L_{loop}\frac{g_{fs}\Delta V_{gsf}}{T_{2f}} \tag{33}$$

Using (31) and (33), solving for T_{2f} yields (34), where V_{gs2f}=0.5(V_{pl_off}+V_{th}).

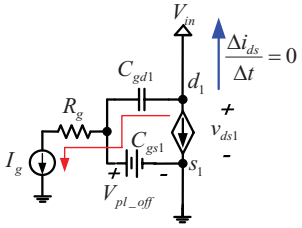


Fig. 12. Synchronous buck HS MOSFET equivalent circuit during T_{1f}

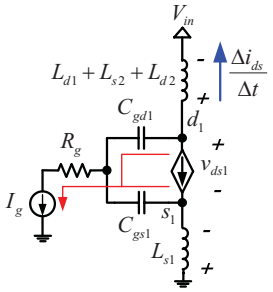


Fig. 13. Synchronous buck HS MOSFET equivalent circuit during T_{2f}

$$T_{2f} = \frac{\Delta V_{gsf} C_{iss1} + \sqrt{(\Delta V_{gsf} C_{iss1})^2 + 4 I_g \Delta V_{gsf} C_{gd1} L_{loop}\, g_{fs}}}{2 I_g} \tag{34}$$

T_f is the sum of T_{1f} and T_{2f} as given by (35).

$$T_f = T_{1f} + T_{2f} \tag{35}$$

C. Total Switching Loss Model

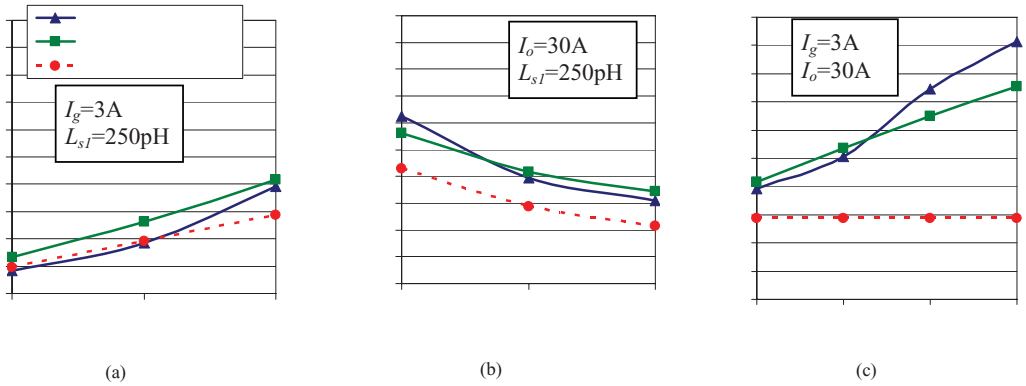
The total switching loss, given by (36).

$$P_{tot\_sw} = P_{on} + P_{off} \tag{36}$$

IV. Simulation Results

The analytical switching loss model with a voltage source drive was compared to SIMetrix Spice simulation and the conventional model in [1]. Simulation results were conducted at 12V input, 1MHz switching frequency, and 10A peak-to-peak buck output inductor ripple (100nH), R_g=1Ω. MOSFET parameters: M_1: Si7860DP, g_{fs}=60S, V_{th}=2V, C_{iss1_spec}=1800pF (@V_{ds1_spec}=15V), C_{oss1_spec}=600pF (@V_{ds1_spec}=15V), C_{rss1_spec}=200pF (@V_{ds1_spec}=15V) and M_2: Si7336ADP SR, Q_{rr_spec}=30nC, I_{rr_spec}=25A .

Curves of total switching loss as a function of: (a) load current, (b) driver supply current and (c) common source inductance (assuming $L_{s1}=L_{d1}=L_{s2}=L_{d2}$) for the proposed model, Spice simulation and the conventional model are given in Fig. 14(a)-(c). The proposed model follows the trends of the Spice simulation results very well. The accuracy of the proposed model total switching loss is within 0.5W under all conditions.



(a) (b) (c)

Fig. 14. Total switching loss at 1MHz, 12V input as a function of: (a) load current (I_g=3A, L_{s1}=250pH), (b) driver supply current (I_o=30A, L_{s1}=250pH) and (c) common source inductance (I_g=3A, I_o=30A)

V. Experimental Results

Given the constraints on measuring actual switching loss, a method to gauge the accuracy of the proposed model is to use it in a loss analysis file that estimates the switching loss, other loss and total loss for a synchronous buck voltage regulator and compare it to the total loss in the real circuit. This analysis has been completed and the total loss in the design file has been compared to the total measured loss of the circuit. Circuit parameters: 1MHz switching frequency; 12V input; 1.3V output; 330nH buck inductor; V_{cc}=10V; IRF6617 HS MOSFET: g_{fs}=39S, V_{th}=1.85V, C_{rss1_spec}=160pF (@V_{ds1_spec}=15V) , C_{oss_spec1}=450pF (@V_{ds1_spec}=15V), C_{iss1_spec}=1300pF (@V_{ds1_spec}=15V); and IRF6691 SR MOSFET; L_{s1}=L_{d1}=L_{s2}=L_{d2}=500pH (model). Current source driver parameters: 3A gate current for the HS MOSFET, 1.3A gate current for the SR.

The estimated synchronous buck VR losses and model predicted switching loss as a function of load current is compared to the experimentally measured loss in Fig. 15. Good agreement is achieved between the loss predicted by the model and the actual loss of the voltage regulator, with the accuracy within 1W over the entire load range.

A loss breakdown of the estimated losses used to generate the model predicted loss in Fig. 15 is given in Fig. 16 for 25A load current.

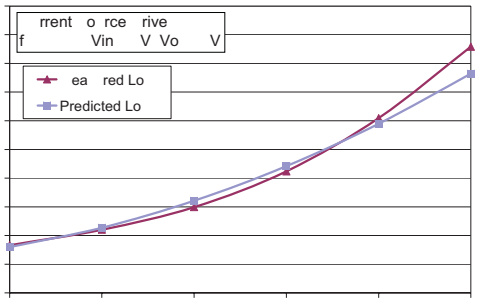


Fig. 15. Comparison of total loss predicted and measured for current source drive (f_s=1MHz, V_{in}=12V and V_o=1.3V)

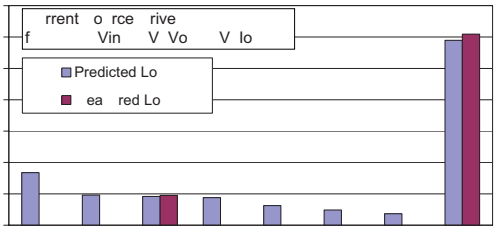


Fig. 16. Loss breakdown of the losses predicted and comparison to the measured gate and total losses for current source drive (f_s=1MHz, V_{in}=12V and V_o=1.3V)

VI. Conclusions

The switching loss characteristics and behavior in a high frequency synchronous buck VR have been reviewed. Following the demonstrated switching loss characteristics, a new practical analytical switching loss model has been proposed for current source drivers. The model can accurately predict the switching loss in a high frequency synchronous buck voltage regulator using relatively simple closed-form equations. This enables engineers to use a spreadsheet design file to estimate losses in their designs.

To validate the proposed model, it was compared to Spice simulation results. It was demonstrated that the proposed model follows the trends in turn on and turn off switching loss for variations in load current, driver supply current and total circuit inductance. The accuracy of the proposed models was demonstrated to be within 0.5W. Following the simulation results, the proposed model was used in a loss analysis file to accurately predict the total circuit loss. The total predicted circuit loss was within 1.0W of the measured loss.

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