A Novel Non-Isolated ZVS Asymmetrical Buck Converter for 12 V Voltage Regulators

Zhiliang Zhang, *Student Member*, *IEEE*, Wilson Eberle, *Member*, *IEEE*, Yan-Fei Liu, *Senior Member, IEEE* and Paresh C. Sen, *Fellow IEEE*
Department of Electrical and Computer Engineering,
Queen's University at Kingston, Ontario, Canada K7L 3N6
zhiliang.zhang@ece.queensu.ca, wilson.eberle@ece.queensu.ca, yanfei.liu@queensu.ca and senp@post.queensu.ca

***Abstract*—This paper presents a new non-isolated asymmetrical buck converter. The transformer is used to extend the extremely low duty-cycle of a conventional buck converter. The turn-off loss can be significantly reduced due to the extension of duty-cycle and there is no turn-on loss owing to zero-voltage turn-on condition. At the same time, the voltage stress over the synchronous rectifier (SR) MOSFETs is also reduced. Therefore, the reverse recovery losses of the body diode can also be reduced. Furthermore, MOSFETs with the lower voltage rating and lower $R_{ds(on)}$ can be used to reduce the conduction loss further. To further reduce the turn-off loss above the switching frequency of 1MHz, current-source gate driver can be also applied to this topology. A prototype at switching frequency of 1MHz was implemented and the preliminary experimental results verify the functionality of the new circuit.**

I. Introduction

With fast development of microprocessors technology, the output voltage of a Voltage Regulator (VR) keeps reducing while the output current is increasing further due to the high power consumption of the processors. In order to meet the strict transient requirements [1] and achieve high power density on the mother board (MB), the switching frequency of a Voltage Regulator (VR) has moved into the megahertz (MHz) range recently [2]-[5].

Multiphase buck converters are very popular for 12 V VRs, however, the buck converter suffers from an extremely low duty cycle, which increases the switching losses and the reverse recovery loss of the body diode significantly. More importantly, it has been noticed that the parasitic inductance, especially, the common source inductance has a serious propagation effect during the switching transition and thus leads the switching loss to increase even higher [6]-[7]. Furthermore, the excessive gate driver losses also come to a penalty at switching frequency of several MHz, especially for the synchronous rectifier (SR) MOSFETs with high total gate charge [8]. Therefore, frequency-dependent losses become one of the barriers to push the switching frequency above several MHz.

In order to extent the extremely low duty cycle, the tapped inductor buck converter is proposed in [9]. A non-isolated half-bridge (NHB) converters with extended duty cycle is proposed in [10]-[11] and similarly, a family of buck-type dc-dc converters taking advantages of the autotransformers are proposed in [12]. For the forward, push-pull, half-bridge topologies with autotransformers, though the duty cycle is extended, the power MOSFETs are still under hard-switching condition, which results in high switching losses at high frequency (>1 MHz). 12 V non-isolated full-bridge (FB) topologies featuring zero-voltage-switching (ZVS) and reduced SR MOSFET conduction loss are proposed in [13]. Furthermore, an improved self-driven 12 V VR topology is proposed based on the phase-shift buck (PSB) converter to recovery the gate drive loss of the SR FETs [14]-[15]. However, these non-isolated FB topologies need four control switches, which results in complex control. In order to solve the above problems, a new non-isolated asymmetrical buck converter is proposed for a 12 V VR in this paper.

II. Proposed Non-Isolated ZVS Asymmetrical Buck Converter

Figure 1 shows the proposed non-isolated ZVS asymmetrical buck converter. In the circuit, Q_1-Q_2 are control MOSFETs and Q_3-Q_4 are SR MOSFETs. C_b is the blocking capacitor. L_1 and L_2 are output filter inductors. T_r is the power transformer.

The key waveforms are shown in Figure 2. The two control MOSFETs (Q_1 and Q_2) are controlled complementarily with the dead time set to achiever ZVS.

The advantage is that due to the direct-energy transfer capability, part of the energy directly transfers to the output capacitor, which helps to improve the efficiency. At the same time, during energy transfer stage, the primary winding and the secondary winding form an autotransformer structure, which reduces both current stress of the primary-side and secondary-side significantly.

There are four switching modes in a switching period and the equivalent circuits are given in Figure 3 accordingly. D_1-D_2 and C_1-C_2 are the body diodes and the intrinsic capacitors of Q_1 and Q_2 respectively.

1) Mode 1 [t_0, t_1] [Figure 3 (a)]: Prior to t_0, Q_1 and Q_3 are on, the energy transfers from the input to the output through the autotransformer, which reduces the both copper loss of the primary side winding and the secondary side winding. At t_0, Q_1 turns off, the primary current i_p charges C_1 and discharges C_2. As C_1 and C_2 limit the rise rate of the voltage of C_1, Q_1 is under zero-voltage turn-off condition. During this stage, the energy to discharge C_2 is from the leakage inductance and the output inductor L_2. L_2 is large enough to be regarded as a constant current source so that the primary current i_p keeps the value $I_{p1}=I_{L2}/(n+1)$, where I_{L2} is the output current and n is the ratio of the primary and secondary windings of the transformer. The voltage C_1 rises linearly and the voltage of C_2 decays linearly. The inductor current i_{L1} freewheels through Q_3.

2) Mode 2 [t_1, t_3] [Figure 3 (b)]: At t_1, D_2 conducts, which provide zero-voltage turn-on condition for Q_2. As i_p is not enough to power the load, the body diode of Q_4 conduct and Q_4 turns on, both primary and secondary

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voltage are zero. The voltage v_{cb} of the blocking capacitor is applied on the leakage inductance of the transformer and cause i_p to decrease linearly. At t_6, i_p increases inversely but is still not enough to power the load. Q_3 and Q_4 continue freewheeling.

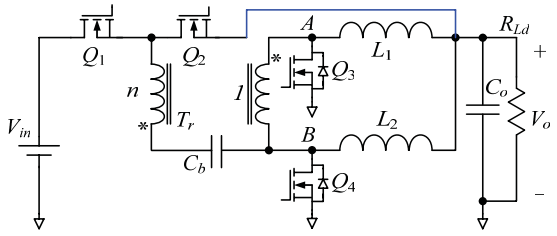

Figure 1 Proposed new asymmetrical buck converter

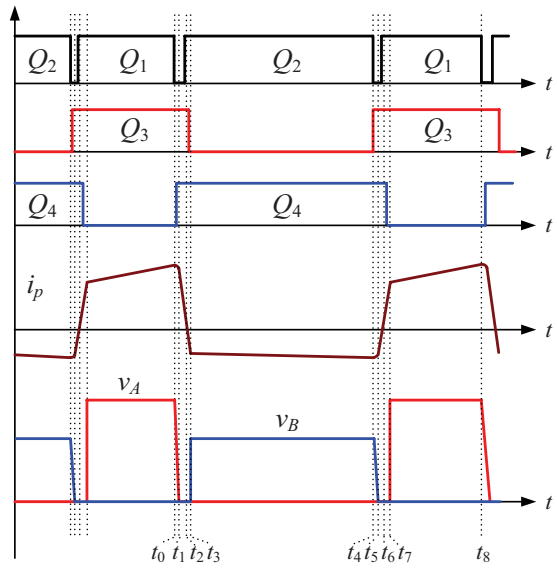

Figure 2 Key waveforms

3) Mode 3 [t_3, t_4] [Figure 3 (c)]: At t_3, i_p rises to the reflected load current, Q_3 turns off. During this stage, part of the energy directly transformers through the primary-side winding to the output capacitors instead of passing through the output inductor L_1, which reduces the inductor loss further.

4) Mode 4 [t_4, t_5] [Figure 3 (d)]: At t_3, Q_2 turns off, the primary current i_p charges C_2 and discharges C_1. As C_1 and C_2 limit the rise rate of the voltage of C_2, Q_2 is under zero-voltage turn-off condition. During this stage, the energy to discharge C_1 is also from the leakage inductance and L_1. L_1 is large enough to be regarded as a constant current source so that the primary current i_p keeps the value $I_{p2}=I_{L1}/(n+1)$, where I_{L1} is the average current of L_1. The voltage C_2 rises linearly and the voltage of C_2 decays linearly. i_{L2} freewheels through Q_4.

5) Mode 5 [t_5, t_7] [Figure 3 (e)]: At t_5, D_1 conducts, which provide zero-voltage turn-on condition for Q_1. As i_p is not enough to power the load, the body diode of Q_4 conduct and Q_4 turns on, both primary and secondary voltage are zero. V_{in}-v_{cb} is applied on the leakage inductance of the transformer and cause i_p to decrease linearly. At t_6, i_p increases inversely but is still not enough to power the load. Q_3 and Q_4 continue freewheeling.

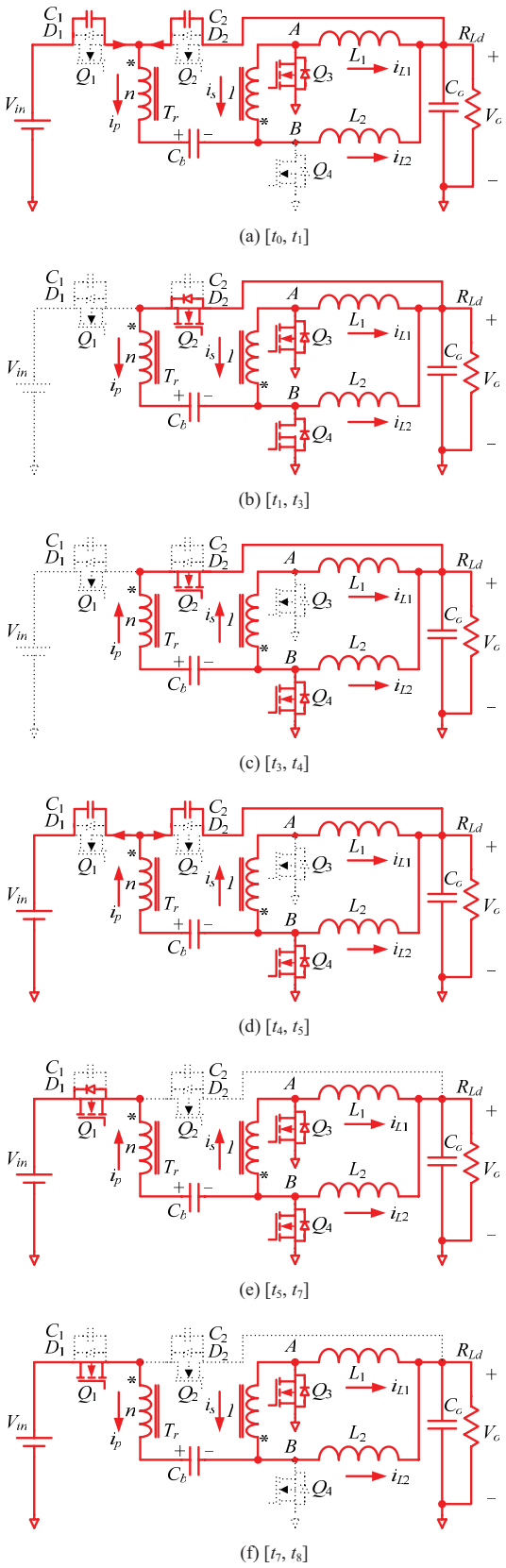

Figure 3 Equivalent circuits of operation

6) Mode 6 [t_7, t_8] [Figure 3 (f)]: At t_7, i_p rises to the reflected load current, Q_4 turns off. The energy transfer through an autotransformer structure again. At t_8, the next switching cycle starts.

III. Steady- Stage Analysis and Advantages of the New Converter

A. Analysis of Steady- State

The voltage transfer ratio can be derived from the volt-second balance condition across the output inductors L_1 and L_2.

For L_1, the volt-second balance is

$$(\frac{V_{cb}-V_o}{n}-V_o)\cdot D\cdot T_s = V_o\cdot(1-D)\cdot T_s \quad (1)$$

Where V_{cb} is the voltage over the C_b, D is the duty-cycle of Q_2 and equals T_{on_Q2}/T_s, T_s is the switching period, V_o is the output voltage and n is the transformer primary to secondary turns ratio.

For L_2, the volt-second balance is

$$(\frac{V_{in}-V_{cb}}{n+1}-V_o)\cdot(1-D)\cdot T_s = V_o\cdot D\cdot T_s \quad (2)$$

Solving (1) and (2), the voltage gain of the converter is expressed as

$$\frac{V_o}{V_{in}} = \frac{(1-D)\cdot D}{2\cdot D\cdot(1-D)+n} \quad (3)$$

B. Advantages of New Asymmetrical Buck Converter

Based on the principle of operation, the advantages of the non-isolated asymmetrical buck converter are highlighted as follows:

1) Extend the extremely low duty-cycle of buck converter

According to the voltage gain of Equation (3), in order to achieve V_{in}=12 V, and V_o=1 V, n=1, the required duty cycle is D=0.25. However, for the same output voltage and input voltage, the duty-cycle of a buck converter is only 0.1. Therefore, the duty-cycle is extended by 2.5 times, which leads to better ripple cancellation and lower output inductor could be used to keep the same amount of output bulk capacitors.

For a buck converter, the switching loss of the control FET is expressed as

$$P_{Q1} = \frac{1}{2}\cdot V_{in}\cdot I_{(on)\_Q1}\cdot t_{sw(on)\_Q1}\cdot f_s + \frac{1}{2}\cdot V_{in}\cdot I_{(off)\_Q1}\cdot t_{sw(off)\_Q1}\cdot f_s \quad (4)$$

where $I_{(on)\_Q1}$ and $I_{(off)\_Q1}$ are the turn-off currents, $t_{sw(on)\_Q1}$ is the turn-on time and $t_{sw(off)\_Q1}$ is the turn-off time.

For the non-isolated asymmetrical buck converter, due to the zero-voltage turn-on, there is no turn-on loss. The switching loss is expressed as

$$P_{Q1} = \frac{1}{n+1}\cdot\frac{1}{2}\cdot V_{in}\cdot I_{(off)\_Q1}\cdot t_{sw(off)\_Q1}\cdot f_s \quad (5)$$

In a practical design, with n=1, at least 50% of the total switching loss is saved. As a specific example, when V_{in}=12 V, V_o=1 V, switching frequency 1 MHz, output inductance L_f=300 nH, total output current I_o=60 A, for two phase buck converters, the turn-off current of each control MOSFETs is 34 A. However, for the new converter, the turn-off currents of control MOSFETs and are 25 A (Q_1, a reduction of 26%) and 10 A (Q_2, a reduction of 70%) respectively, which means a significant reduction of turn-off losses due to the duty-cycle extension.

2) ZVS of the control MOSFETs

The voltage stresses of the primary side MOSFETs are given by Equation (4)

$$V_{DS\_Q1} = V_{in} - V_o \quad (6)$$

In order to realize ZVS for the control MOSFETs, we need enough energy to charge C_1 to V_{DS_Q1} and discharge C_2 to zero. We can take advantage of the energy of the leakage inductance of the transformer, which is very similar to the ZVS condition of the lagging leg of the traditional full-bridge converter. Therefore, no additional resonant inductor is required. However, in order to reduce the duty-cycle loss, the leakage inductance should be reduced. In a practical design, the trade-off between the ZVS range and the duty-cycle loss should be compromised for the transformer design.

3) Reduced body diode reverse recovery loss of SR MOFETs

For a conventional buck converter, due to the reverse recovery of the body diode with the circuit parastics and variation of the input voltage, the peak voltage of the switching node with the ringing is more than 20 V and therefore, 30 V rated MOSFETs is generally used for the SR MOSFETs and control MOSFETs. However, due to duty cycle extension of the asymmetrical buck converter, the voltage stresses of the SR MOSFETs including the ringing are reduced to less than 15 V and 10 V respectively. Therefore, according to the equation P_{rr}=Q_{rr}·V_s·f_s, where V_s is the peak voltage of the switching node, the reverse recovery losses are reduced by 37.5% and 58.3% respectively. Moreover, the voltage stress of the control MOSFETs in the new converter are reduced to 12 V. Therefore, 20 V rated MOSFETs and 10V rated MOSFET with lower $R_{ds(on)}$ can be used for the control MOSFETs and SR MOSFETs respectively.

IV. Asymmetrical Buck Converters with Proposed New Current-Source Driver

Though there is no turn-on loss due to ZVS and the turn-off loss is also reduced significantly by the factor of turn ratio n, the turn-off loss is still the dominant loss in the total loss breakdown. It would be expected even higher at above 1 MHz due to the parasitic inductance in the PCB traces and packing. So in order to push switching frequency above 1 MHz, a new current source drive is proposed to further reduce the turn-off loss due to the parasitics. At the same time, the gate energy at high frequency will also be recovered.

Figure 4 shows the new asymmetrical buck converter with current-source gate drive circuit. The key idea is to use current-source driver to reduce the turn-off loss due to the parasitics further, which is still dominant loss for a MOSFETs with ZVS capability.

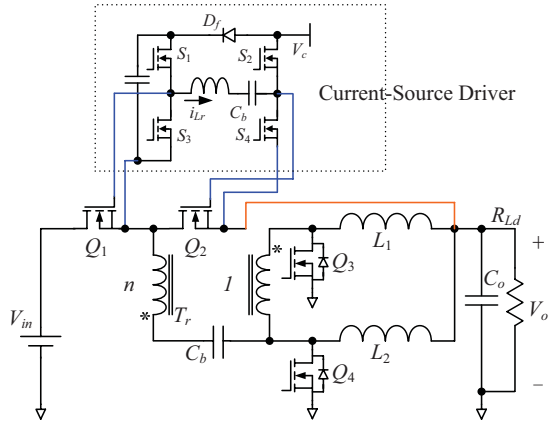

Figure 4 The asymmetrical buck converter with proposed new current-source driver

V. Experimental Verification And Discussion

In order to verify the functionality of the new circuit, the asymmetrical buck converter was built. Initial testing has just begun. The specifications are as follows: input voltage V_{in}=12 V; output voltage V_o=1.0 V; output current I_o=50 A, fs = 1 MHz. The PCB is six-layer with 2 oz copper. The components used in the circuit are listed as follows: control MOSFET Q_1: Si7368DP (20 V N-channel, $R_{DS(on)}$=8.5 mΩ@V_{GS}=4.5 V, Vishay); SR MOSFET Q_2: Si7866ADP (20 V N-channel, $R_{DS(on)}$=3 mΩ@V_{GS}=4.5 V, Vishay); output filter inductance: L_1=L_2 =330 nH (R = 1.3 mohm, IHLP-5050CE-01, Vishay).

Figure 5 shows the gate waveforms of the four switches (Q_1- Q_4) according to the control strategy of Figure 2. Figure 6 gives the drain-to-source voltages of the SR FETs Q_3 and Q_4. The oscillation of the voltage is due to the reverse recovery of the body diode. It is observed that the drain-to-source voltages of Q_3 and Q_4 are less than 15 V and 10 V respectively, therefore the SR MOSFETs can use the MOSFETs with lower voltage rating and lower $R_{ds(on)}$. At the same time, the reverser-recovery losses are also reduced significantly.

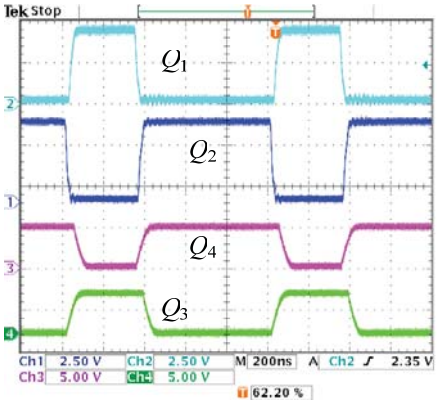

Figure 5 Gate signals (control MOSFET Q_1 and Q_2, SR MOSFET Q_3 and Q_4)

Figure 7 shows the drain-to-source voltage and gate drive voltage of Q_2. The drain-to-source voltage drops to zero before the gate voltage begins to rise and ZVS is achieved.

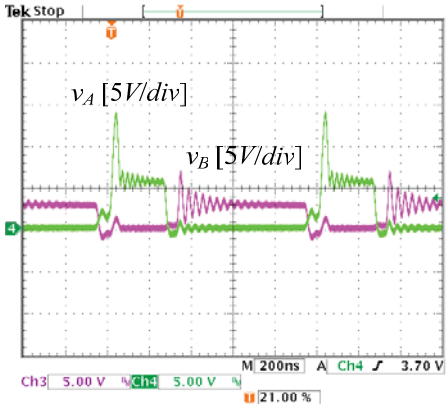

Figure 6 Drain-to-source voltages of SR MOSFET Q_3 and Q_4

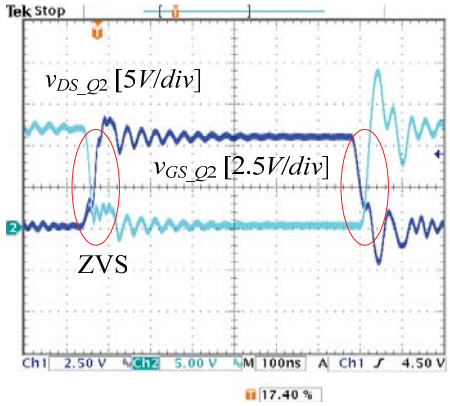

Figure 7 Drain-to-source voltage and gate voltage of Q_2

VI. Conclusion

A new non-isolated asymmetrical buck converter is proposed in this paper. The transformer is used to extend the extremely low duty-cycle of a conventional buck converter. The turn-off loss can be significantly reduced due to the extension of duty-cycle and there is no turn-on loss owing to zero-voltage turn-on condition. At the same time, the voltage stress over the SR MOSFETs is also reduced. Therefore, the reverse-recovery losses of the body diode can also be reduced. Furthermore, MOSFETs with the lower voltage rating and the lower $R_{ds(on)}$ can be used to reduce the conduction loss further. The preliminary experimental results verify the functionality of the new circuit. Under the desired control, the extension of the duty-cycle and ZVS has been achieved for the control MOSFETs. Further experiment result will be reported in the future work.

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