A New Hybrid Gate Drive Scheme for High Frequency Buck Voltage Regulators

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Abstract— **This paper presents a new hybrid drive scheme for a synchronous buck voltage regulator (VR). The proposed current-source driver is used to drive the control MOSFET to achieve fast switching speed and reduce the switching loss significantly due to the parasitic inductance in addition to gate energy recovery. Conventional voltage driver is used for synchronous rectifier (SR) MOSFET for its simplicity and good immunity and alleviation of *dv*/*dt* effect. The experimental results prove the advantages of the new drive scheme and a significant efficiency improvement has been achieved. At 1.3 V output, the new driver improves the efficiency from 82.8% using a conventional driver to 85.6% (an improvement of 2.8%) at 20 A, and at 25 A, from 80.5% to 83.0% (an improvement of 2.5%). The new drive can also be integrated into a standard drive integrated circuit (IC) and replace the conventional voltage drive IC directly. Overall, the new driver scheme is very promising from the standpoints of both performance and cost-effectiveness.**

I. INTRODUCTION

In order reduce the expensive output capacitors and reduce the high output inductance to achieve high power density and fast dynamic response, there is a strong trend toward pushing has the switching frequency of a voltage regulator (VR) into MHz range for meet the stringent future microprocessors [1] -[4].

For today's VR solution, the multi-phase synchronous buck converters are used nearly exclusively as dc-dc converters to power microprocessors due to its simplicity and low component count. The switching frequency of the commercial buck VRs available presently is around 500 KHz to 700 KHz. Many semiconductor companies such as International rectifier (IR), Intersil and Linear Technology etc offer commercial synchronous buck driver chips up to 2MHz. Generally, these driver chips use voltage-source gate drivers for both control MOSFET and synchronous rectifier (SR) MOSFET. However, the major concern of the voltage source gate driver is slow drive speed due to R-C type gate charging/ discharging and the parasitic inductance, especially, the common source inductance, which increases the switching loss of the control MOSFET significantly in a buck VR at high frequency (>1MHz).

One of the interesting topics of VR technology is resonant gate driver technique. In the last fifteen years, resonant gate drive circuits have originally been proposed with the objective of recovering gate energy lost in a conventional gate driver [5]-[11]. The resonant drivers using a coupled inductor [12] and using a transformer [13] are able to drive two MOSFETs. A full-bridge topology drive circuit with one inductor is proposed to drive two ground-sharing MOSFETs in a 1MHz Boost converter in [14]. An assessment of resonant drive techniques for use in low power dc/dc converters is presented in [15] and the mathematical model is built to estimate the power loss of the drive circuit in [16]. However, these investigations are generally emphasizing gate energy savings by the resonant driver and concentrating on the drive topologies, but ignore the potential switching loss savings that are much more dominant in a high frequency buck VR.

In order to reduce the negative impact of the parasitics, several different resonant gate drive circuits are proposed in [17]- [19]. In addition to the gate energy recovery capability, the most important feature of these new drive circuits is that the switching loss is significantly reduced due to the parasitic inductance by using a constant current to charge and discharge the input capacitor of a power MOSFET to achieve fast switching transition. A detailed switching loss model considering the parasitics is reported in [20]and with the optimal design method, a significant efficiency improvement is achieved. Actually, these proposed drive circuits can be called as current-source gate drivers.

Figure 1 shows the loss breakdown of buck converter with the conventional voltage gate driver. Carefully investigating the switching behavior of the MOSFETs in a synchronous buck converter, it is interesting to observe that the switching loss of the control MOSFET is dominant among the total loss breakdown. For the control MOSFET, the common source inductance results in significant increase of the switching losses, especially, turn-off losses, which makes the fast turn-off transition more desirable. However, on the other hand, for the SR MOSFET, it almost has no switching loss basically since its output capacitor has been discharged to zero voltage before it turns on, which can be regarded to achieve zero-voltage-switching (ZVS). Moreover, due to the ZVS condition, no miller charge is needed and the gate charge is saved around 30%. Also, the common-source inductance could help to improve the *dv*/*dt* immunity of the SR MOSFET [21].

Overall, the point is that control MOSFET and the SR MOSFET have different switching behavior due to the parasitics respectively. Therefore, a new hybrid gate drive scheme is proposed for a buck converter in this paper. A new current-source gate driver is adopted for the control MOSFET to achieve the fast switching transition and

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reduce the switching loss significantly due to the parasitics, while the conventional driver is used for the SR MOSFET for its simplicity and good *Cdv/dt* immunity. Moreover, only one small inductor is needed in the new driver scheme, which reduces the cost and profile.

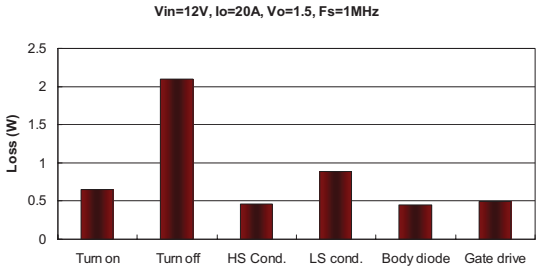


Figure 1 Loss breakdown of a buck converter with the conventional voltage gate driver (L_s=1 nH, L_D=2 nH, control MOSFET: Si7860DP, SR MOSFET: Si7336ADP)

II. Proposed Hybrid Gate Driver and Principle of Operation

Figure 2 shows the buck converter with the proposed hybrid drive circuit. The key waveforms are shown in Figure 3. Essentially, the new high-side current-source driver is used for the control MOSFET to achieve fast switching transition. It consists of two driver MOSFETs S_1 and S_2, a bipolar transistor pair S_3 and S_4, the resonant inductor L_r, the bootstrap capacitor C_f , diode D_f and the blocking capacitor C_b. V_c are the drive voltages. C_{gs1} and C_{gs2} are the input gate capacitors of MOSFETs Q_1 and Q_2 respectively. S_1 and S_2 are switched out of phase with complimentary control respectively.

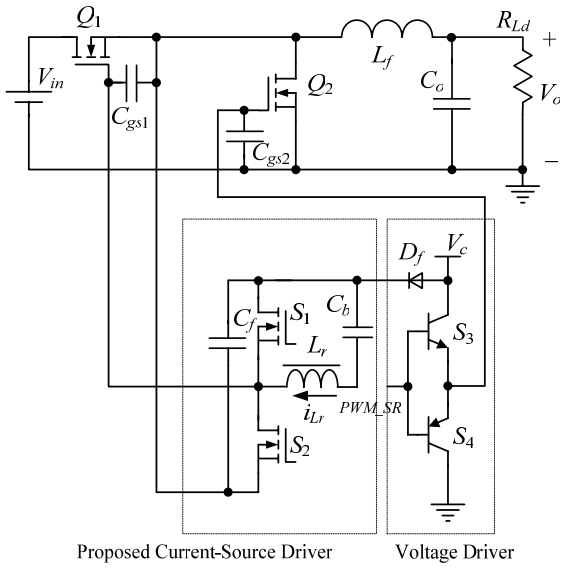


Figure 2 Buck VR with proposed current-source driver

For the SR MOSFET, the conventional voltage driver is used, which is the bipolar totem-pole drive structure featuring low cost and simplicity. PWM_SR is the signal fed into the bipolar totem-pole pair.

It is noted that the object of this paper is to verify the functionality of the proposed new gate drive scheme and significant efficiency improvement. Therefore, the discrete devices were used to build the new driver. Actually, from the perspective of driver integrated circuit (driver IC), the new hybrid driver will be implemented as a drive IC as shown in Figure 4 through standard CMOS or BiCMOS technology. The integrated current-drive IC can achieve low profile and high power density with low footprint packages such as small outline integrated circuit (SOIC) package or Quad Flat No-lead (QFN) package, which are pin-to pin compatible with conventional drive IC. Compared to the conventional voltage drive IC, the new driver improves the efficiency greatly while achieves the same packaging size in a simple and low cost manner.

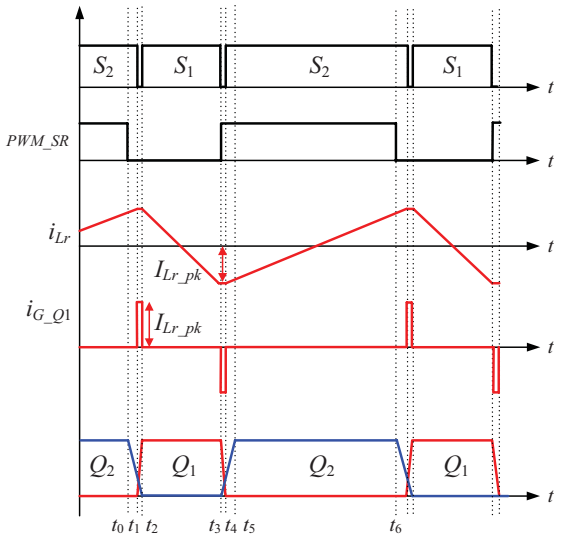


Figure 3 Key waveforms

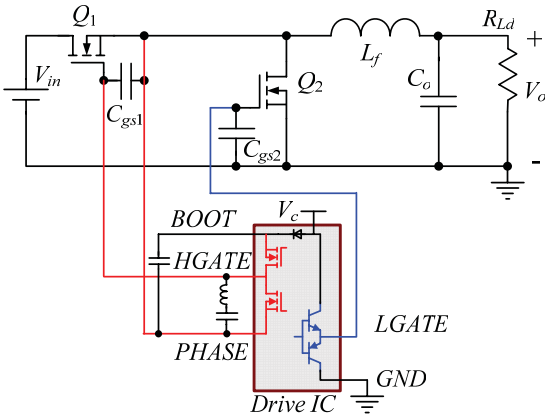


Figure 4 Buck VR with the hybrid drive scheme as a drive IC

The switching transitions of charging and discharging C_{gs1} and C_{gs2} are during the interval of [t_0, t_2] and [t_3, t_5]. The peak currents i_{G_Q1} during [t_0, t_2] and [t_3, t_5] are constant during switching transition, which ensure fast charging and discharging of the MOSFET gate, including the miller capacitor of Q_1. For the SR MOSFET Q_2, the conventional voltage driver is used since SR MOSFET Q_2 is switched under ZVS condition.

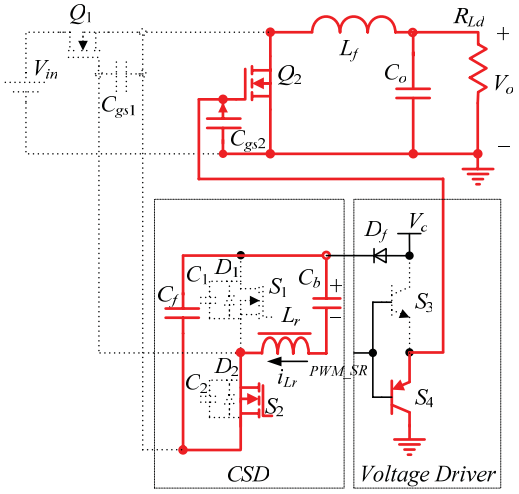
There are four switching modes in a switching period and the equivalent circuits are given in Figure 5 accordingly. D_1-D_2 are the body diodes and C_1-C_2 are the intrinsic capacitors of S_1-S_2 respectively.

1) Mode 1 [t_0, t_1] [Figure 5 (a)]: Prior to t_0, the gate voltage of Q_2 is clamped to V_c by S_3. S_2 conducts and the inductor current i_{Lr} increases in the positive direction. At t_0, S_3 turns off and S_4 turns on at the same time. C_{gs2} begins to be discharged through S_4.

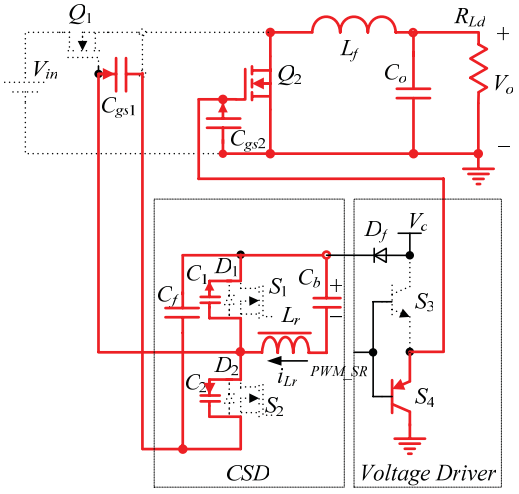
2) Mode 2 [t_1, t_2] [Figure 5 (b)]: At t_1, S_2 turns off. i_{Lr} charges C_2 plus the input capacitor C_{gs1} and discharges C_1 simultaneously. Due to C_1 and C_2, S_2 is zero-voltage turn-off. The voltage of C_2 rises linearly and the voltage of C_1 decays linearly. C_{gs2} continues to be discharged through S_4.

3) Mode 3 [t_2, t_3] [Figure 5 (c)]: At t_2, v_{c2} rises to V_c and v_{c1} decays to zero. The body diode D_1 conducts and S_1 turns on under zero-voltage condition. The gate-to-source voltage of Q_2 is clamped to ground through S_4.

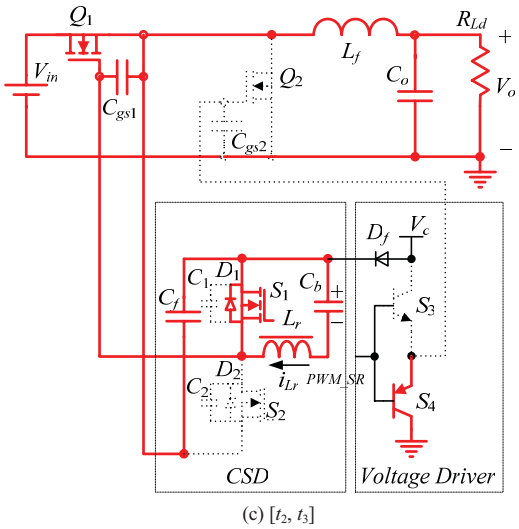
4) Mode 4 [t_3, t_4] [Figure 5 (d)]: Before t_3, i_{Lr} has changed its polarity to the negative direction. At t_3, S_1 turns off. i_{Lr} charges C_1 and discharges C_2 plus C_{gs1} simultaneously. Due to C_1 and C_2, S_1 is zero-voltage turn-off. The voltage of C_1 rises linearly and the voltage of C_2 decays linearly. S_4 turns off and S_3 turns on at the same time. C_{gs2} begins to be charged through S_3.



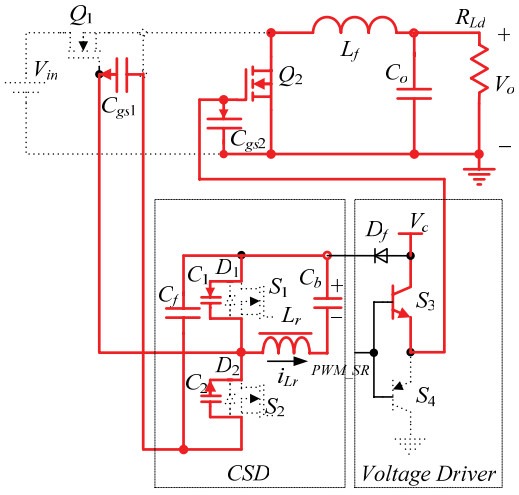
(a) [t_0, t_1]



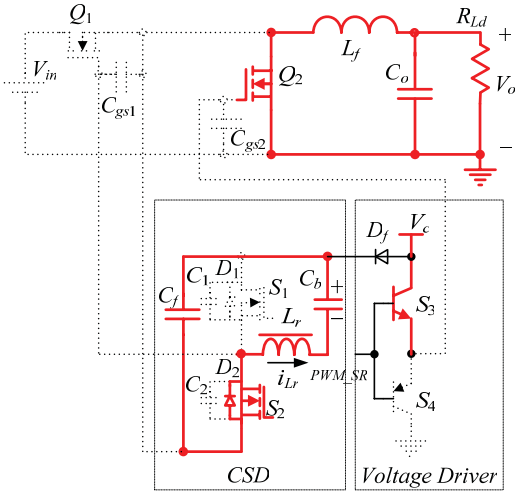
(b) [t_1, t_2]



(c) [t_2, t_3]



(d) [t_3, t_4]



(e) [t_4, t_6]

Figure 5 Equivalent circuits of operation

5) Mode 5 [t_4, t_6] [Figure 5 (e)]: At t_4, v_{c1} rises to V_c and v_{c2} decays to zero. The body diode D_2 conducts and S_2 turns on under zero-voltage condition. The gate-to-source voltage of Q_1 is clamped to zero through S_2. At t_5, the gate-to-source voltage of Q_2 is charged and clamped to V_c through S_3 and Q_2 is on. i_{Lr} begins to increase until t_6.

III. Loss Analysis and Optimal Design

A. Loss Analysis

From the volt-second balance condition across the resonant inductor, the DC voltage v_{cb} across the blocking capacitor C_b is derived as Equation (1)

$$v_{Cb} = (1-D)\cdot V_c \tag{1}$$

where D is the duty cycle of S_1 and V_c is the drive voltage.

The blocking capacitor value can be found using the following calculation:

$$C_b = \frac{I_{Lr\_pk}}{4\cdot k\cdot V_c\cdot f_s} \tag{2}$$

where k is the percent ripple on C_b. For example, when V_c=7 V, I_{Lr_pk}=1.5 A, k=5% and f_s=1 MHz, then C_b =1.0 uF should be used.

The relationship of the inductor value L_r and the peak inductor current I_{Lr_pk} is given by Equation (3)

$$L_r = \frac{V_c\cdot D\cdot(1-D)}{2\cdot I_{Lr\_pk}\cdot f_s} \tag{3}$$

where D is the duty cycle of S_1, V_c is the drive voltage and f_s is the switching frequency. By choosing the proper peak inductor current (drive current for MOSFET), the resonant inductor value can be obtained by Equation (2).

As seen from the principle of operation in Figure 3, the peak current I_{Lr_pk} of the resonant inductor L_r is actual gate drive current for the power MOSFET and can be regarded as a constant current source. So the higher I_{Lr_pk} is, the shorter of switching transition is, thus more switching loss can be saved. On the other hand, higher I_{Lr_pk} will result in a larger RMS value of the inductor circulating current i_{Lr} since the waveform of i_{Lr} is triangular, which increases the resistive circulating loss in the drive circuit and decreases the gate energy recovery efficiency. Therefore it is critical to decide I_{Lr_pk} properly so that the maximum loss saving can be achieved. The optimal design to choose I_{Lr_pk} will be given in next section.

The inductor current waveform indicated in Figure 3 can be regarded as a triangular waveform since the charging/ discharging time [t_0, t_2] and [t_3, t_5] are very small and can be neglected. Therefore, the RMS value of the inductor current I_{Lr_RMS} is $I_{Lr\_pk}/\sqrt{3}$.

The RMS currents flowing through the switches S_1 can be derived as

$$I_{s1\_RMS} = I_{Lr\_pk1}\cdot\sqrt{\frac{D}{3}} \tag{4}$$

The RMS currents flowing through switches S_2 is

$$I_{s2\_RMS} = I_{Lr\_pk1}\cdot\sqrt{\frac{1-D}{3}} \tag{5}$$

Assuming same type of MOSFETs is used for S_1 and S_2, the conduction loss of S_1 and S_2 is expressed as

$$P_{cond} = {I_{s1\_RMS}}^2\cdot R_{ds(on)} + {I_{s2\_RMS}}^2\cdot R_{ds(on)} \tag{6}$$

Substituting (4) and (5) into (6) yields

$$P_{cond} = \frac{1}{3}\cdot {I_{Lr\_pk1}}^2\cdot R_{ds(on)} \tag{7}$$

The copper loss of the inductor winding is expressed as

$$P_{copper} = R_{ac}\cdot I^2{}_{Lr\_RMS1} \tag{8}$$

where R_{ac} is the AC resistance of the inductor winding. I_{Lr_RMS1} is the RMS value of the inductor current.

Core loss of the resonant inductor should be also included. So the total inductor loss is given in (9):

$$P_{ind} = P_{copper} + P_{core} \tag{9}$$

Both the charge and discharge currents flow through the internal gate mesh resistance R_G of the power MOSFET and cause resistive loss. The charge and discharge current is the peak value of the inductor current.

Thus the total loss caused by the internal resistance of the power MOSFET Q_1 during turn-on (t_{on1}) and turn-off (t_{off1}) is expressed as

$$P_{RG} = R_{G1}\cdot I^2{}_{Lr\_pk1}\cdot(t_{on1}+t_{off1})\cdot f_s \tag{10}$$

where R_{G1} is the internal gate resistors of Q_1 and f_s is the switching frequency.

The gate drive loss of S_1 and S_2 is expressed as

$$P_{gate} = 2\cdot Q_{g\_s}\cdot V_{gs\_s}\cdot f_s \tag{11}$$

where Q_{g_s} is the total gate charge of a drive switch and V_{gs_s} is the drive voltage, which is typically 5 V.

In conclusion, the total loss of the gate drive circuit of #1 is expressed as

$$P_{Drvie} = P_{cond} + P_{ind} + P_{RG} + P_{gate} \tag{12}$$

B. Optimal Design

For the control MOSFET Q_1, the optimal design involves a trade off between the switching loss reduction and the drive circuit loss. Following optimal design procedure based on the analytical loss model in [20], the gate drive current can be decided. The sum of the switching loss and drive circuit loss can be plotted as $P_{Q1\_Optimal}$ and the optimal gate current, I_{G_Q1} can be determined from the graph (at the minimum point of $P_{Q1\_Optimal}$). For the given application and parameters in the experimental results section, the curves are given in Figure 5.

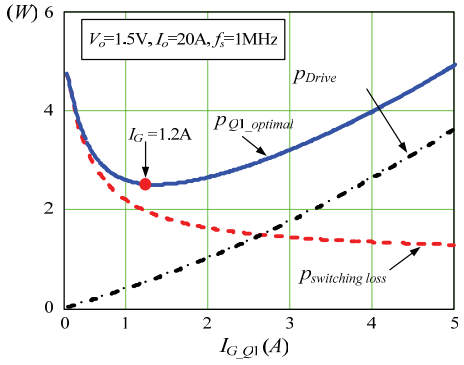


Figure 6 Optimization curves for the control MOSFET Q_1: power loss vs. gate current

In Figure 5, the optimal gate current is 1.2 A and the resonant inductor value is 1.0 μH according to Equation (3). In this case, $P_{switching}$=2.3 W and P_{Drive}=0.5 W.

IV. Experimental Verification And Discussion

In order to verify the performance of the new hybrid drive scheme, a synchronous buck converter was built. The specifications are as follows: input voltage V_{in}=12 V; output voltage V_o=1.5 V- 1.0 V; output current I_o=25 A; switching frequency f_s=1 MHz; gate driver voltage V_c=6 V. The PCB uses six-layer 2 oz copper. The components used in the circuit are listed as follows: Q_1: Si7860DP; Q_2: Si7866ADP; output filter inductance: L_f=300 nH (IHLP-5050CE-01, Vishay); resonant inductors: L_r= 1.0 μH (SMT DO1608C series, Coilcraft).

Figure 7 shows the photo of the synchronous buck VR prototype with the hybrid current-source driver. The driver was built using discrete components with an Altera Max II EPM240 CPLD used to generate the control signals as shown in Figure 7. In order to simply the level-shift circuit and the logic circuit, we use the integrated level-shift circuit in a conventional drive chip from ISL6208 from Intersil so that we can drive the drive MOSFETs (S_1 and S_2 see Figure 2) with floating source. For the SR MOSFET, the conventional voltage gate driver in ISL6208 is used in the experiment.

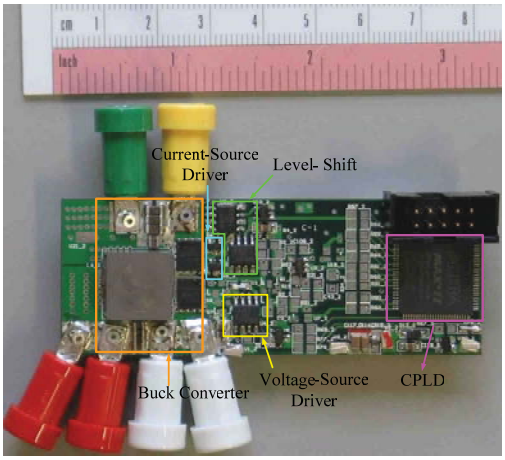


Figure 7 Prototype photo of the synchronous buck VR with the hybrid gate driver

Figure 8 shows the gate drive signals v_{gs_Q1} (control MOSFET) and v_{gs_Q2} (synchronous MOSFET). It is observed that v_{gs_Q1} is very smooth and no miller plateau is observed as the miller charge is removed fast by the constant inductor drive current. Moreover the rise time and fall time of v_{gs_Q1} is less than 15ns, which means quick switching speed. The dead time between two drive voltages is fixed to avoid shoot-through and is minimized to reduce the body diode loss of SR MOSFET. It should be also noted that adaptive control or predictive of the conventional driver can also be applied to the hybrid gate driver easily when it is integrated into a drive chip.

Figure 9 shows gate drive signals v_{gs_Q1} (control MOSFET) and the resonant inductor current i_{Lr}. Its peak current value is 1.2 A, which is the optimized value of the drive current.

Figure 10 shows the drain-source voltage v_{ds_Q2} and the gate signal v_{gs_Q2} of the synchronous FET at the load current of 25 A. It can bee seen from v_{ds_Q2} that the body diode conduction time is small, which reduces the conduction loss and the reverse recovery loss of the body diode greatly.

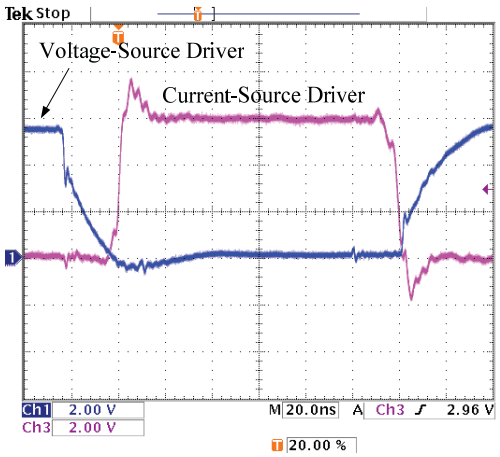


Figure 8 Gate signals v_{gs_Q1} (control FET) and v_{gs_Q2}(synchronous FET)

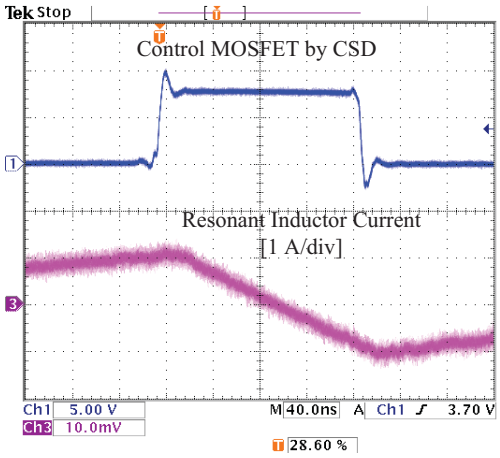


Figure 9 Gate signals v_{gs_Q1}, v_{gs_Q2} and resonant inductor current i_{Lr}

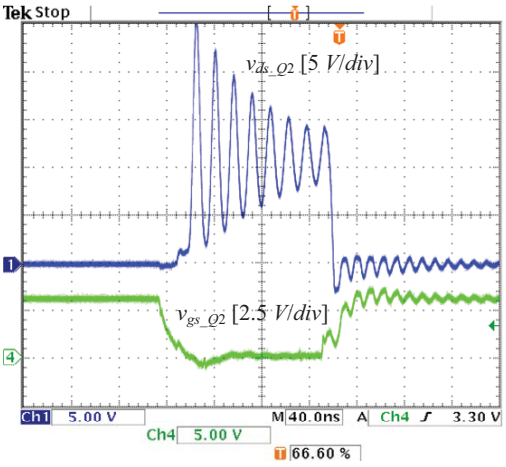


Figure 10 Drain-source voltage v_{ds_Q2} and the gate signal v_{gs_Q2} (synchronous FET) at load current of 25 A

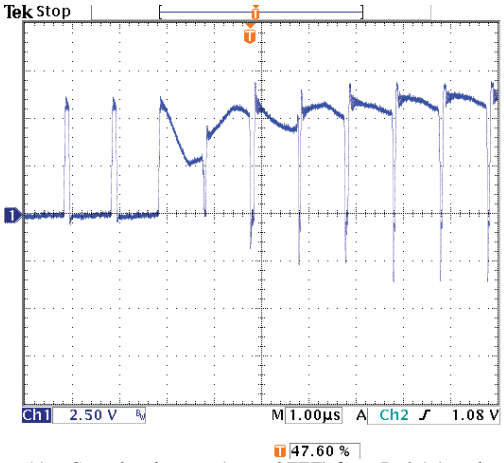


Figure 11 Gate signals v_{gs_Q1} (control FET) from D=0.1 (steady state) to D=0.9

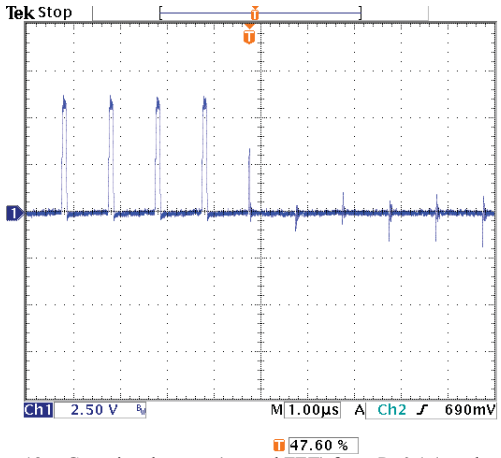


Figure 12 Gate signals v_{gs_Q1} (control FET) from D=0.1 (steady state) to D=0

Figure 11 and Figure 12 show the steady-state duty-cycle with step change from D=0.1 to D=0.9 and from D=0.9 to D=0 respectively. It is observed that the current-source gate drive has fast response when duty-cycle has a step change.

A benchmark of a synchronous buck converter with the conventional gate driver was built. A Predictive Gate Drive UCC 27222 from Texas Instruments was used as the conventional voltage driver.

Figure 13 shows the measured efficiency comparison for the hybrid gate driver and the conventional gate driver at 1.3 V output. It is observed that at 20 A, the efficiency is improved from 82.8% to 85.6% (an improvement of 2.8%) and at 25 A, the efficiency is improved from 80.5% to 83% (an improvement of 2.5%).

Figure 14 shows the measured efficiency with the hybrid gate driver at different output voltages and load currents. It is observed that at 1.0 V/ 25 A, the efficiency is 80.3% and it is almost the same as 82.5% (see Figure 13) of the conventional driver at 1.3 V/20 A, which means that we can reduce the output voltage from 1.3 V to 1.0 V by the hybrid gate driver without penalizing the efficiency.

Figure 15 shows the measured efficiency for the hybrid gate driver at different switching frequencies. It should be pointed here that during this test, all the components used and specifications are kept same. It is observed that at f_s=600 KHz, at 1.3 V/ 25 A, the efficiency is 85.6 %, and at 1.3 V/ 15 A, the efficiency is 89.5%.

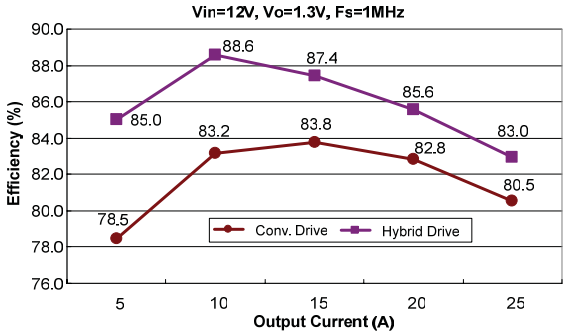


Figure 13 Efficiency comparison: top: hybrid driver; bottom: conventional driver (Conv.)

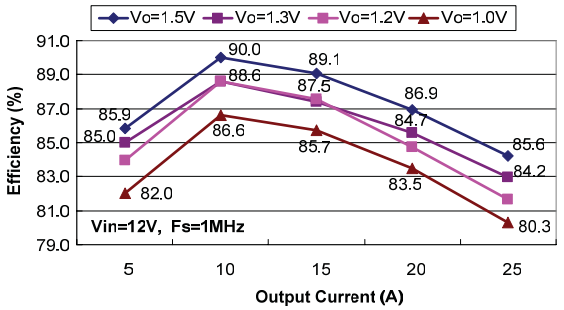


Figure 14 Efficiency with different output voltages and currents with the resonant driver

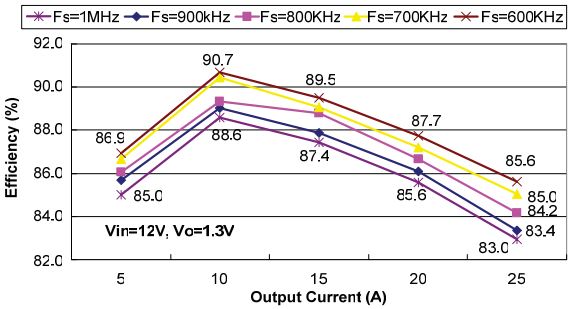


Figure 15 Efficiency with different switching frequencies

V. Conclusion

This paper presents a new hybrid current-source drive scheme for a synchronous buck voltage regulator. The proposed hybrid drive scheme use current-source driver to drive the control MOSFET to achieve significant switching loss reduction due to the parasitic inductance in addition to gate energy recovery. Conventional voltage driver is used for the synchronous MOSFET for its simplicity and good immunity and alleviation of *dv/dt* effect. The new hybrid drive scheme need only one small inductor (600 nH to 1 µH at 1MHz typically) featuring low cost and low profile.

The experimental results verify the advantages of the new drive scheme and a significant efficiency improvement has been achieved. At 1.3 V output, the new driver improves the efficiency from 82.8% using a conventional driver to 85.6% (an improvement of 2.8%) at 20 A, and at 25 A, from 80.5% to 83% (an improvement of 2.5%).

The future work will achieve the IC implementation of the proposed new drive circuit with standard CMOS technology for VR applications.

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