# A Novel Non-Isolated Full Bridge Topology for VRM Applications

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***Abstract*—In this paper, a new non-isolated full bridge (NFB) topology is introduced to solve the narrow duty cycle and hard switching problems of the Buck converter in low output voltage, high output current applications. In comparison to the Buck converter, it operates at a significantly wider duty cycle and can achieve zero voltage switching for the high side MOSFETs. The NFB significantly reduces the input peak current and transfers a portion of the primary side energy directly to the load thereby reducing the stress on the synchronous rectifiers and filter inductors. Using self-driven synchronous rectifiers, the body diode conduction loss is reduced since no dead time is required between the primary side MOSFETs and the synchronous rectifiers. Given these significant advantages, the NFB can achieve higher efficiency than a two and three phase interleaved Buck at the same power level. The efficiency gain enables the NFB to operate at a high switching frequency thereby enabling smaller output inductors to be used to achieve improved dynamic performance.**

**Experimental results and analysis demonstrate that the new NFB can significantly improve the performance of a voltage regulator. The prototype built operated at 500 kHz, 12 V input, 1 V output, up to 30 A load and achieved an efficiency of 84.4% at 30 A load. A 1 MHz prototype achieved a full load efficiency of 82.1%. In comparison, the efficiency of a two and three phase Buck prototype was 79.7% and 82.6% at 30 A load and at 500 kHz switching frequency.**

***Index Terms*—Full bridge (FB), non-isolated full bridge (NFB), phase shifted FB, voltage regulation module (VRM).**

## I. Introduction

With the continued improvements in integrated circuit technology, next generation CPUs will operate at much higher clock frequencies, and consume more power. In the future, to reduce power consumption, CPUs will operate at supply voltages below 1 V, with tight voltage tolerance, large current demand (above 100 A), and require fast dynamic response (above 100 A/$\mu$s) [1].

To meet these requirements for next generation CPUs, the voltage regulation modules (VRMs) will need to achieve: 1) high efficiency at high switching frequency, 2) fast dynamic response, and 3) low component cost. The most popular topology for this application is the multiphase interleaved Buck. The major obstacle for the multiphase Buck to achieve these three goals is its extremely narrow duty cycle for output voltages at and below 1 V. Narrow duty cycles yield high switching loss which limits the Buck switching frequency, making it difficult to design a Buck based VRM that can achieve high efficiency at a high switching frequency. Presently, the only solution for the conventional Buck type VRM is to use up to eight phases in parallel, which is not an optimized economic solution [2]–[4].

To solve the aforementioned problems several new topologies have been proposed. The topologies proposed in [5]–[10] are Buck based topologies that use a coupled-inductor to extend the duty cycle. The major drawback of these topologies is that the voltage stress of the control MOSFET is higher than the input voltage, so an auxiliary circuit is often required to limit the voltage stress on the switches. Furthermore, these topologies operate in hard switching mode, so switching losses prevent them from being suitable candidates at very high switching frequencies.

To solve the problems of the conventional Buck and coupled inductor Buck topologies, in this paper a new non-isolated full bridge (NFB) topology is proposed with significant advantages, including soft-switching, reduced synchronous rectifier voltage stress and current stress. Compared with the topologies proposed in [11], the NFB has reduced current stress for the synchronous rectifiers and output inductors since a portion of the energy is transferred directly to the load, so some of the output current does not need to go through the output inductors. In [11], the output inductor is connected between the primary side and secondary side, so all of the output current conducts through the output inductor, which increases both the copper loss in the inductor and the physical size of the inductor core. One advantage of the topology proposed in [11] is that it uses a simple circuit to drive the synchronous rectifiers.

The proposed topology is presented and analyzed in the following sections.

## II. Derivation and Operation of the NFB Converter

The conventional FB and proposed NFB are shown in Fig. 1, which illustrates the evolution of the new topology. For the conventional FB, the voltage at points A and C are stable dc voltages. The points B and D are primary and secondary ground, respectively. Since A and C are stable dc voltages, we can remove the connection between point A and B and connect A to C, and B to D, yielding the new NFB topology. There are three significant benefits of these topology changes:

1) The input current conducts directly to the load side, so the current stress on the synchronous rectifiers and inductors is reduced.
2) A portion of the load energy is not transferred by the transformer, so its associated losses decrease.

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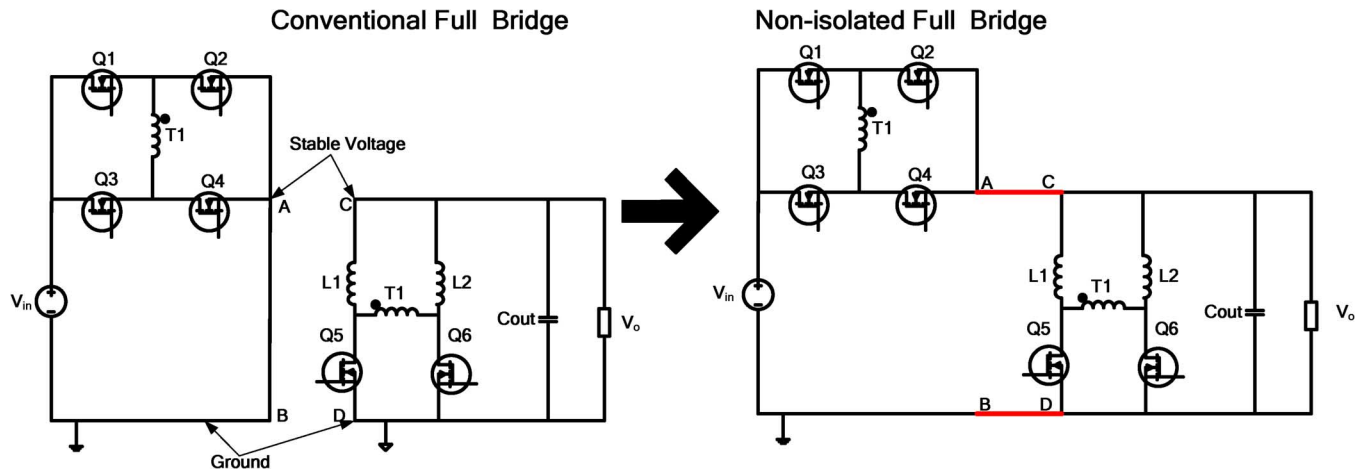


Fig. 1. Evolution of the conventional FB to the new NFB converter.

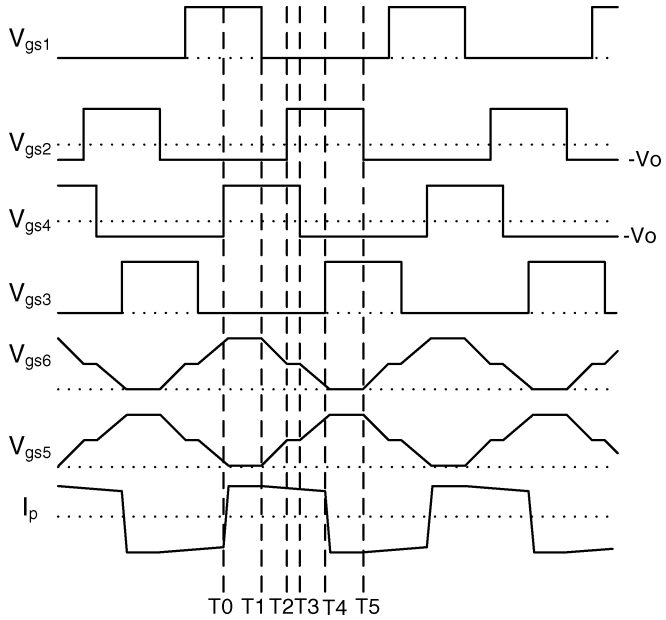


Fig. 2. Key waveforms of the five modes of operation.

3) When the two primary low side MOSFETs, Q2, Q4, turn off, their gate voltage is $-V_o$, so they can turn off faster reducing turn off loss.

The modes of operation of the NFB operating in phase-shift mode are presented in the following sub-sections. The key waveforms illustrating the five modes of operation from T0–T5 are illustrated in Fig. 2.

In Fig. 2 Q5 and Q6 are driven by using the SR drive method proposed in [12]; further details are explained in Section IV. It is also noted that the source of MOSFETs Q2 and Q4 are directly connected to the output so, they are turned off by $-V_o$, which allows them to be turned off faster to reduce switching loss.

### A. *Mode 1* $[T0 \sim T1]$

The first mode is illustrated in Fig. 3. From time T0 to T1, Q1, Q4 and Q6 are on. Q2, Q3 Q5 are off; the voltage across Q2 and

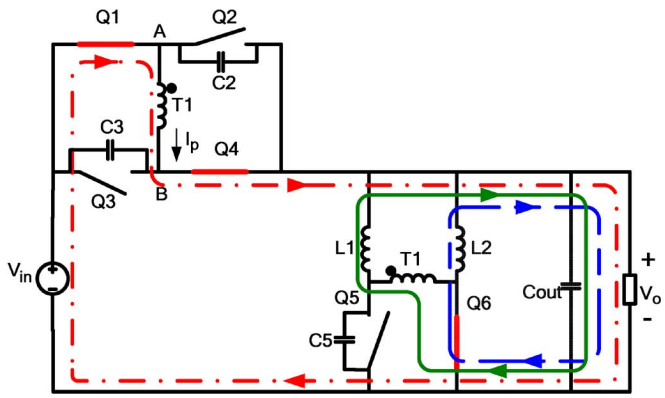


Fig. 3. Operation mode of NFB during time interval T0–T1.

Q3 is $V_{\text{in}} - V_o$. The current in L1 increases and the current in L2 decreases. Energy flows from the input to the load. In Fig. 3 we can see that the input current goes directly to the load side, and the current stress of the synchronous rectifier is reduced as a result.

### B. *Mode 2* $[T1 \sim T2]$

The second mode is illustrated in Fig. 4. From time $T1$ to $T2$, $Q1$ is turned off at $T1$ to prepare the zero voltage turn on of $Q2$. The current reflected from the secondary side charges $C1$ and discharges $C2$. The currents decrease in both $L1$ and $L2$. During this time interval, the voltage at point A decreases from $V_{\text{in}}$ to $V_o$. When the voltage at point A decreases to $V_o$, the voltage across $Q2$ is zero. If $Q2$ is turned on at this time, zero voltage turn on can be achieved. $Q5$ also is turned on during this transition, and it begins to share the load current after the voltage across $Q2$ is reduced to zero. If the self-driven circuit proposed in [12] is used, $Q5$ is turned on before it begins to conduct the inductor current, so its body diode does not conduct during this transition. During this time interval the current reflected from the secondary side is used to charge and discharge the output capacitors of $Q1$ and $Q2$. It is easier for $Q1$ and $Q2$ to achieve zero voltage switching (ZVS) compared to the lagging leg ($Q3$ and $Q4$).

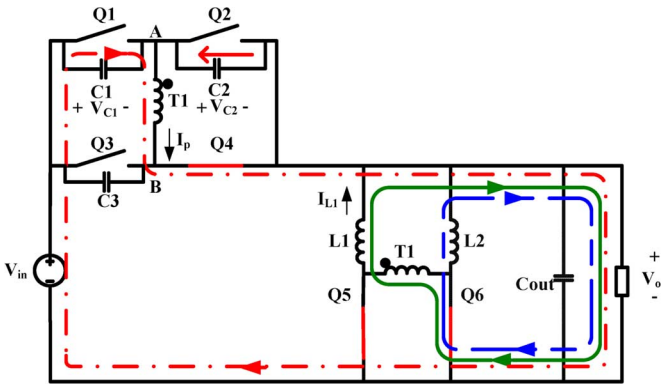


Fig. 4. Operation mode of NFB during time interval T1–T2.

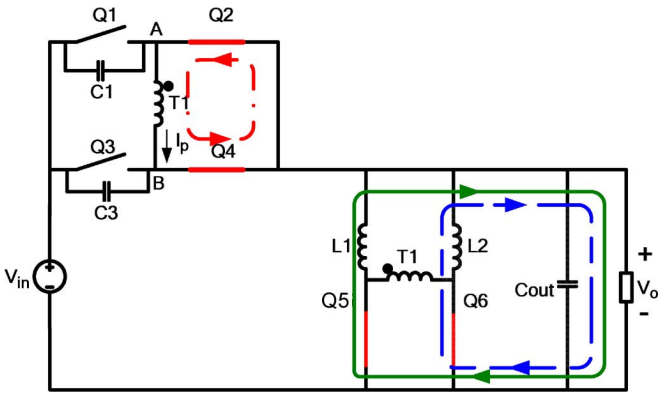


Fig. 5. Operation mode of NFB during time interval T2–T3.

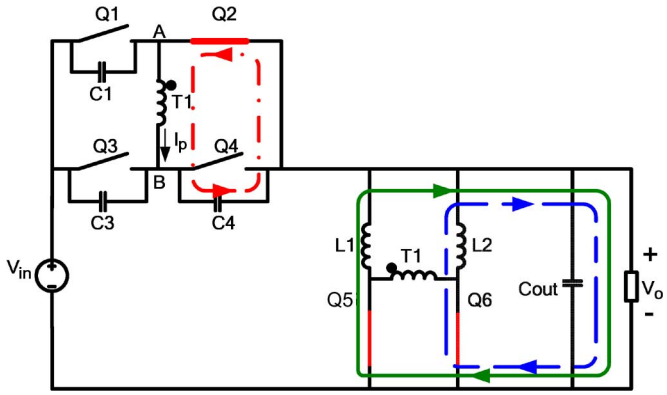


Fig. 6. Operation mode of NFB during time interval $T3$–$T4$.

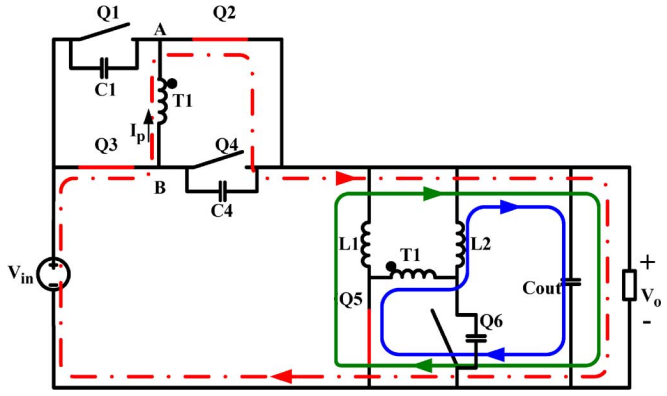


Fig. 7. Operation mode of NFB during time interval $T4$–$T5$.

### C. *Mode 3* $[T2 \sim T3]$

The third mode is illustrated in Fig. 5, for time $T2$ to $T3$. After the voltage across $Q2$ reaches zero, $Q2$ is turned on at $T2$. Since at this time the secondary side of the transformer is shorted, the primary and secondary sides of the transformer are decoupled, and the current in both inductors decreases. The load energy is provided by the output capacitance and output inductors.

### D. *Mode 4* $[T3 \sim T4]$

The fourth mode is illustrated in Fig. 6. From time $T3$ to $T4$, $Q4$ is turned off at $T4$ to prepare the zero voltage turn on of $Q3$. The energy stored in the leakage inductance of the transformer charges $C4$ and discharges $C3$, and voltage at point B increases from $V_o$ to $V_{\text{in}}$. After the voltage increase to $V_{\text{in}}$, $Q3$ can achieve ZVS turn on. In order to achieve ZVS turn on of $Q3$, the energy stored in the leakage inductance must be sufficient to charge $C4$ to $(V_{\text{in}} - V_o)$ and discharge $C3$ to 0 V.

### E. *Mode 5* $[T4 \sim T5]$

The final mode is illustrated in Fig. 7. From time $T4$ to $T5$, once the voltage across $Q3$ becomes zero, $Q3$ is turned on at $T4$. The primary current can not change direction instantly due to the transformer leakage inductance. During the interval, the primary current increases in the opposite direction of $I_p$, and the current in $Q5$ begins to increase and the current in $Q6$ begins to decrease. If $Q6$ is turned off before the primary current changes from $I_p$ to $-I_p$, its body diode begins to conduct. After the primary current changes from $I_p$ to $-I_p$, the primary side begins to provide energy to the secondary side, and $Q5$ begins to conduct the full current in $L1$ and $L2$ and $Q6$ is turned off. At the end of $T5$, one switching period is complete.

### F. *Steady-State Equations of the NFB*

The output voltage of the NFB is derived using the inductor volt–seconds balance in the steady-state as given by (1), where $N = Np/Ns$ and $D$ is duty cycle. $(D = Ton/Ts)$. From (1) we can see that after adding a transformer, the duty cycle can be easily adjusted. For example when $V_{\text{in}} = 12$ V, $V_o = 1$ V, $N = 3$, the duty cycle is $D = 0.545$, which, compared with the Buck, the duty cycle increase five times

$$V_o = \frac{V_{\text{in}} D}{2N + D}. \tag{1}$$

The average current in the two output inductors is given by (2), where, $I_o$ is the output current, $I_{\text{in}}$ is the average input current given by (3) (assuming 100% efficiency). The ripple current through the output inductor is given by (4)

$$I_{Lavg} = \frac{(I_o - I_{\text{in}})}{2} \tag{2}$$

$$I_{\text{in}} = \frac{P_{\text{out}}}{V_{\text{in}}} \tag{3}$$

$$\Delta I_L = \frac{V_o}{L}(1 - D/2)Ts. \tag{4}$$

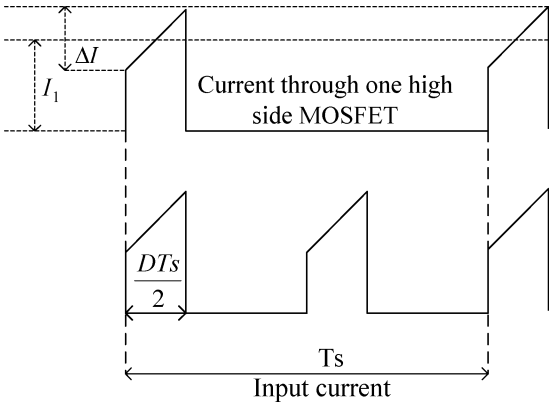


Fig. 8. Waveforms of current through the high side MOSFET and input current.

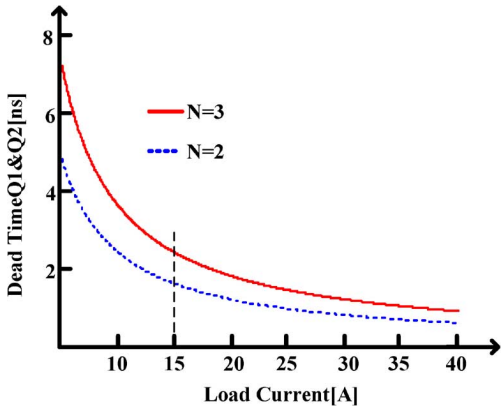


Fig. 9. Dead time between $Q1$ and $Q2$ required to achieve ZVS for the leading bridge leg as a function of load current.

The voltage stresses of the primary and secondary side MOSFETs are given by (5) and (6), respectively

$$V_{PMOSFET} = V_{\text{in}} - V_o \tag{5}$$
$$V_{SR} = (V_{\text{in}} - V_o)/N. \tag{6}$$

Waveforms of the input current and current through high side MOSFET are shown in Fig. 8. The root mean square (RMS) current stress of the primary side MOSFETs is given by (7) using (8). Equations (7)–(9) can be used to calculate the RMS current through the synchronous rectifiers when the inductor ripple current is small

$$I_{PMOSFET\_RMS} = \sqrt{(D/2)\left((I_1+\Delta I/2)^2+(I_1-\Delta I)\Delta I+\frac{\Delta I^2}{3}\right)} \tag{7}$$
$$I_1 = I_{Lavg}\frac{1}{N}, \quad \Delta I = \frac{\Delta I_L}{N} \tag{8}$$
$$I_{syn\_RMS} = \sqrt{(1-D)I_{Lavg}^2 + \frac{D}{2}(2I_{Lavg})^2}. \tag{9}$$

## III. Zero Voltage Switching Analysis

In this section, the ZVS requirements for the NFB are analyzed in detail for the leading and lagging legs.

### A. Leading Leg Transition: Mode 2 [T1–T2]

The transition paths of the leading leg are shown in Fig. 4. $Q1$ is turned off to prepare for the zero voltage turn on of $Q2$. The current reflected from the secondary side charges $C1$ and discharges $C2$. During this transition, the time needed to charge $C1$ to $V_{\text{in}} - V_o$ and discharge $C2$ from $V_{\text{in}} - V_o$ to zero voltage is dependent on the load current. Since this time interval is very short we can assume the charge current is constant during the transition. Equations (10) and (11) can be used to calculate the voltage across $C1$ and $C2$, if $C1 = C2$, (12) can be used to calculate the dead time needed to achieve ZVS. Equation (12) is derived based on the assumption that during the transaction of the Mode 2 $[T1 \sim T2]$, the current is constant to charge $C1$ and discharge $C2$. $I_{L1}$ in (10)–(12) is the average current in $L1$ and can be calculated using (2). In Fig. 9, the minimum dead time is calculated using (12) as a function of load current with $V_{\text{in}} = 12$ V, $Np : Ns = 3 : 1$ and $Np : Ns = 2 : 1$, $C1 = 250$ pF. From Fig. 9 we can observe that heavy load and a low turn's ratio can help the NFB achieve ZVS and at 15 A load, $Td = 2.4$ ns for $N = 3$ and 1.6 ns for $N = 2$

$$V_{C1}(t) = \frac{I_{L1}t}{2C1N} \tag{10}$$
$$V_{C2}(t) = (V_{\text{in}} - V_o) - \frac{I_{L1}t}{2C2N} \tag{11}$$
$$t_{dead\_Q12} > \frac{2C1(V_{\text{in}} - V_o)N}{I_{L1}}. \tag{12}$$

### B. Lagging Leg Transition: Mode 4 [T3–T4]

The transition paths of the lagging leg are shown in Fig. 6. Initially, $Q4$ is turned off to prepare the zero voltage turn on of $Q3$. If the energy stored in the leakage inductance of the transformer is sufficient to charge C4 to $V_{\text{in}} - V_o$ and discharge $C3$ from $V_{\text{in}} - V_o$ to zero, $Q3$ can achieve zero voltage turn on.

In this transition the leakage inductance resonates with $C3$ and $C4$. The equivalent circuit is shown in Fig. 10. If the voltage at point B can be charged to $V_{\text{in}}$, the body diode of $Q3$ will turn on and clamp the voltage to $V_{\text{in}}$, then the equivalent circuit becomes that shown in Fig. 11. In order to achieve ZVS turn on, $Q3$ must turn on before the current through the leakage inductance decreases to zero. The voltages across $C3$ and $C4$ can be calculated using (13)–(16) assuming $C3 = C4$. The leakage current, $I_{\text{Leakage}}$ in (13) is the current at the instant $Q4$ is turned on and can be estimated using (18), where $I_p$ is the primary side current. From (13) it can be observed that in order to achieve ZVS, (17) must be satisfied. Fig. 12 shows the minimum dead time between $Q3$ and $Q4$ calculated using (17), with $V_{\text{in}} = 12$ V, $V_o = 1$ V, $C3 = C4 = 250$ pF, $L_{\text{Leakage}} = 30$ nH. It is clear that it is more difficult for the lagging leg to achieve zero voltage turn on in comparison to the leading leg. Form Fig. 12 we can see that at 15 A load $Td = 3.1$ ns for $N = 3$ and 1.7 ns for $N = 2$

$$V_{C3}(t) = Z_o I_{\text{Leakage}} \sin \omega t - (V_{\text{in}} - V_o) \tag{13}$$
$$I_p(t) = I_{\text{Leakage}} \cos \omega t \tag{14}$$
$$V_{C4}(t) = Z_o I_{\text{Leakage}} \sin \omega t \tag{15}$$

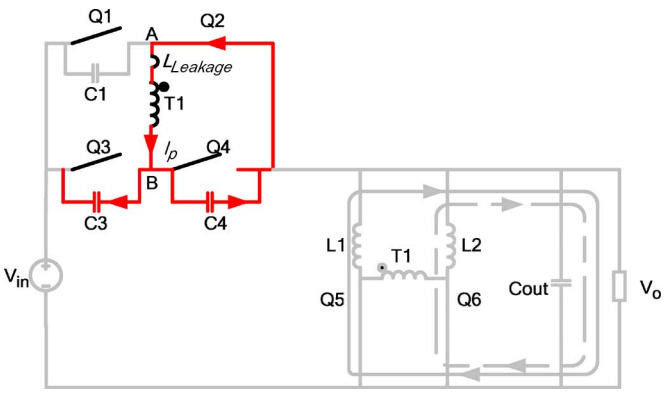


Fig. 10. Equivalent circuit for lagging leg.

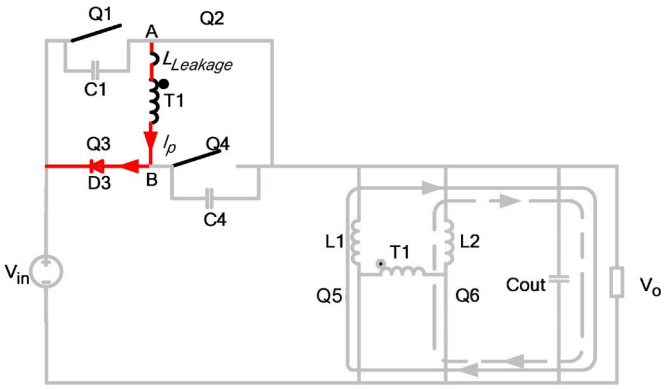


Fig. 11. Equivalent circuit for lagging leg after $V_{C3}$ is zero.

$$Z_o = \sqrt{L_{\text{Leakage}}/2C_3}$$
$$\omega = 1/\sqrt{2L_{\text{Leakage}}C_3}$$
$$t_X = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{\text{in}} - V_o}{Z_o}\right) \tag{16}$$
$$\begin{cases} Z_o I_{\text{Leakage min}} > (V_{\text{in}} - V_o) \\ \frac{1}{\omega}\sin^{-1}\left(\frac{V_{\text{in}}-V_o}{Z_o I_{\text{Leakage}}}\right) < t_{dead\_Q34} \\ \quad < \frac{(I_{\text{Leakage}} L_{\text{Leakage}})\cos\omega t_X}{(V_{\text{in}}-V_o)} + t_X \end{cases} \tag{17}$$
$$I_{Leakage} = I_{Lavg}/N. \tag{18}$$

## IV. Loss Analysis and Comparison

In this section, a brief comparison is given between the proposed NFB and the benchmark two and three phase Buck topologies. Following the comparison, the losses of a two phase synchronous Buck converter and the NFB are compared. It is demonstrated that NFB is able to achieve higher efficiency than a two phase Buck. In the comparison, the components used for the two phase Buck and NFB and their operating conditions are the same.

### A. Topology Comparison Overview

A comparison of the components count, efficiency and cost is given in Table I for the NFB in comparison to a two and three phase Buck.

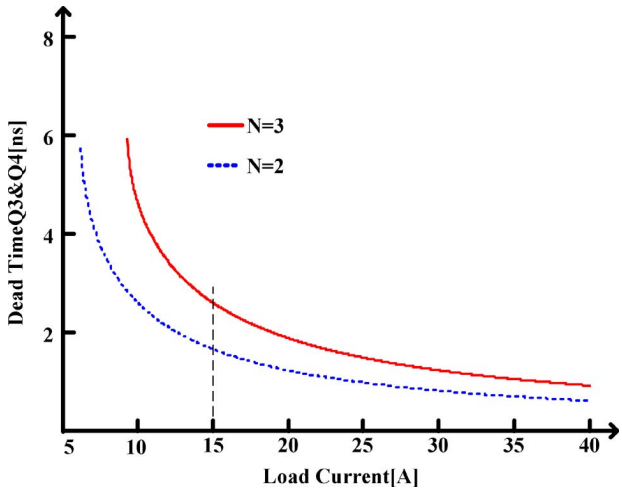


Fig. 12. Lagging leg dead time between $Q3$ and $Q4$.

TABLE I
Design Comparison Between the Two-Phase Buck, Three-Phase Buck and NFB

| | 2 phase Buck | 3 phase Buck | NFB |
|---|---|---|---|
| Total MOSFETs | 4 | 6 | 6 |
| Control MOSFETs | 2 | 3 | 4 |
| SR MOSFETs | 2 | 3 | 2 |
| Magnetics | 2 | 3 | 3 |
| Inductors | 2 | 3 | 2 |
| Transformers | 0 | 0 | 1 |
| Controllers | 1 | 1 | 1 |
| Drivers | 2 | 3 | 2 |
| Efficiency | Lowest | Medium | Highest |
| Cost | Lowest | High | High |

From the table above, the NFB and three phase Buck have the same number of MOSFETs, magnetics and one controller. However, the NFB with self driven synchronous rectification only requires two gate drivers, while the three phase Buck requires three drivers. On the other hand, the two phase Buck and NFB each have two inductors, two SR MOSFETs and two drivers.

In terms of cost, the total cost of the NFB and three phase Buck should be similar. The NFB has a lower cost for the drivers and MOSFETs since SR MOSFETs are typically more expensive than control MOSFETs. However, the NFB phase shift controller is more expensive than the multiphase Buck controllers available in the market. Depending on the transformer implementation, the magnetics cost for the NFB and three phase Buck should be similar. The component cost of the two phase Buck is lower than the NFB, but the two additional control MOSFETs and transformer enable the NFB to achieve improved efficiency through ZVS which reduces utility costs.

In the analysis that follows, the NFB is compared to the two phase Buck since they both require two synchronous MOSFETs and two power inductors.

### B. Switching Loss Saved by ZVS and Duty Cycle Extension

In comparison to the two phase Buck, the NFB operates with extended duty cycle, so the primary peak current through the MOSFETs is significantly reduced thereby also reducing the

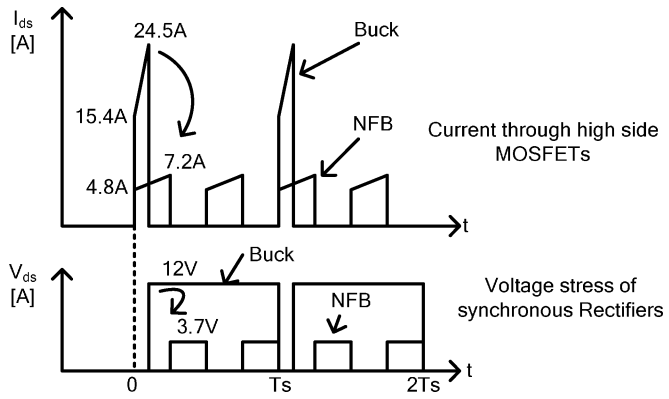


Fig. 13. Peak current and voltage stress reduced by extend the duty cycle.

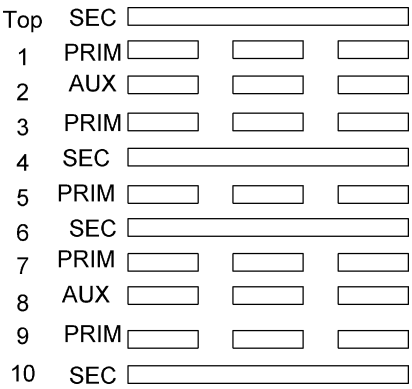


Fig. 14. Transformer winding layer structure illustrating interleaving.

switching loss. Fig. 13 illustrates an example with the input voltage at 12 V, output at 1 V/40 A, output inductor of 100 nH and $Np : Ns = 3 : 1$. From the example, it is clear that the primary peak current is reduced from 24.5 A for the Buck to 7.2 A for the NFB. Furthermore, the voltage stress of the synchronous rectifiers is reduced from 12 V for the Buck to 3.7 V for the NFB.

As previously discussed, when operated in phase shift mode and if the control circuit is properly designed, the primary MOSFETs of the NFB can achieve ZVS at turn on. Another benefit of the ZVS turn on is that the gate driving loss can be reduced since the Qgd charge is eliminated [15]. This can reduce the gate loss by at least 30% for the primary MOSFETs. The turn on and turn off loss can be calculated by (19) and (20), where $f_s$ represents the switching frequency, $V_{\rm ds}$ represents the switch voltage, $I_{\rm PKon}$ represents the peak turn on current, $t_r$ represents the rise time, $I_{\rm PKoff}$ represents the peak turn off current and $t_f$ represents the fall time. It is expected that at least 66% of the switching loss energy can be saved in comparison to the Buck as in [11].

$$P_{\rm on} = \frac{1}{2} f_s V_{ds} I_{PKon} t_r \tag{19}$$

$$P_{\rm off} = \frac{1}{2} f_s V_{ds} I_{PKoff} t_f. \tag{20}$$

For example if we assume the turn on time is 14 ns and the turn off time is 10 ns then the switching loss for a two phase

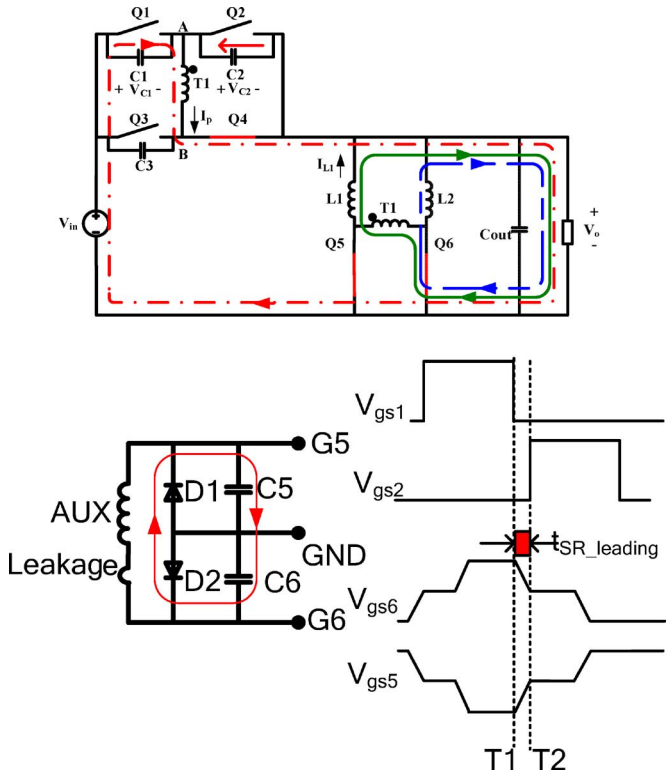


Fig. 15. Leading leg transition for the self-driven synchronous rectifiers.

Buck is 5.527 W and 1.584 W for the NFB leading to a savings of 3.943 W. The calculation is as follows:

$$\begin{aligned} P_{\rm SW\_BUCK} &= 0.5(1\ {\rm MHz})(12\ {\rm V}) \\ &\quad \times [(15.4\ {\rm A})(14\ {\rm ns}) + (24.5\ {\rm A})(10\ {\rm ns})]\ (2) \\ &= 5.527\ {\rm W} \\ P_{\rm SW\_NFB} &= 0.5(1\ {\rm MHz})(12\ {\rm V} - 1\ {\rm V})(7.2\ {\rm A})(10\ {\rm ns})(4) \\ &= 1.584\ {\rm W}. \end{aligned}$$

In real circuits, the switching loss can be slightly higher due to the parasitic source inductance [14], which is neglected in this analysis. However, by using these simple calculations, it is clear that the NFB can save switching loss energy in comparison to the interleaved Buck due to the lower peak current and zero voltage turn on with the NFB.

For the synchronous rectifiers, their reverse recovery loss for each switch can be calculated using (21), where $Q_{\rm rr}$ represents the reverse recovery charge of the body diode. Since the voltage stress for the synchronous rectifiers in the NFB is significantly reduced as compared with the Buck, the reverse recovery loss is also reduced. For the example previously given, the reverse recovery losses of the NFB would be approximately 1/3 of those for the Buck, calculated as below. From the calculation, 0.868 W can be saved

$$\begin{aligned} P_{reverse} &= Q_{rr} V_{DS} f_s \\ {\rm P_{RE\_BUCK}} &= (1\ {\rm MHz})(12\ {\rm V})\,[(52\ {\rm nC})]\,(2) = 1.248\ {\rm W} \\ {\rm P_{RE\_NFB}} &= (1\ {\rm MHz})(3.7\ {\rm V})(52\ {\rm nC})(2) = 0.38\ {\rm W} \end{aligned} \tag{21}$$

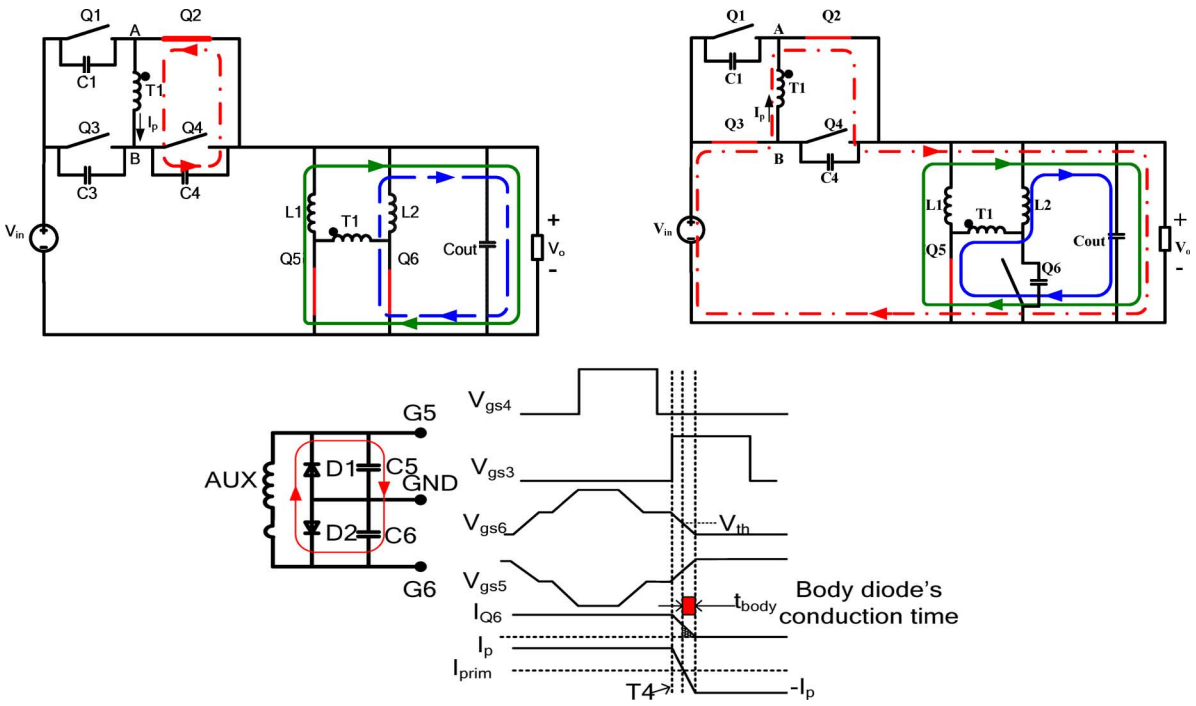


Fig. 16. Lagging leg transition for the self-driven synchronous rectifiers.

### C. Synchronous Rectifier Body Diode Loss Savings

With the conventional Buck, a dead time must be added between the primary control MOSFET and the synchronous MOSFET to prevent a short circuit. For the NFB, when self-driven synchronous rectification is used, the body diode conduction loss is significantly reduced since there is no need to add dead time to prevent a short circuit. To drive the synchronous rectifiers, the self-driven circuit proposed in [12] was used for the NFB. The transformer windings were interleaved to achieve good coupling between the primary, secondary and AUX windings as illustrated in Fig. 14.

In the following sub-sections, the body diode conduction loss of the two phase Buck and NFB are compared.

*1) Leading Leg Transition for Rectification:* The first mode shown in Fig. 15 correspond to the transitions shown in Fig. 4. Q1 is turned off to prepare for the ZVS turn on of $Q2$. Synchronous rectifier $Q6$ is already on since the voltage across the primary winding is decreasing. The voltage across the AUX winding also begins to decrease, so the energy stored in $C6$ begins to charge $C5$. After the voltage across the primary winding reaches zero, $Q2$ is turned on with ZVS and the voltage across the AUX wingding is also zero, so $V_{\rm gs5}$ equals $V_{\rm gs6}$. The transition time of this interval is determined by the load current and can be calculated using (13). When the primary winding voltage is zero, the secondary winding voltage is zero and $Q5$ begins to share the current initially handled by $Q6$, so the current in $Q5$ begins to increase, while the current in $Q6$ begins to decrease. Since $Q5$ is turned on before it begins to take over the current in $Q6$, its body diode does not conduct during this interval [17].

*2) Lagging Leg Transition for Rectification:* The second mode is shown in Fig. 16. $Q4$ is turned off to prepare for the ZVS turn on of $Q3$. The states of this mode are shown in Figs. 6 and 7. The energy stored in the leakage inductance of the transformer charges $C4$ and discharges $C3$. Since the two synchronous rectifiers are conducting, the primary windings and secondary windings are decoupled. After $Q3$ is turned on, $V_{\rm gs5}$ begins to increase and $V_{\rm gs6}$ begins to decrease. Meanwhile, the current in $Q5$ begins to increase and the current in $Q6$ begins to decrease while the primary side current begins to change direction. Before the primary current changes from $I_p$ to $-I_p$, $V_{\rm in} - V_o$ is applied across the leakage inductance reflected to primary. The body diode of $Q6$ begins to conduct when its gate voltage is reduced below the threshold voltage. After the primary side current changes to $-I_p$, the current in $Q6$ is reduced to zero and $Q5$ begins to conduct the full inductor current.

To simplify the analysis we will assume the gate voltages of $Q5$ and $Q6$ change linearly. This assumption is valid as long as the synchronous rectifier gate resistances and the leakage inductance of the AUX winding can be neglected. Based on this assumption, when the primary side current linearly changes from $I_p$ to $-I_p$, $V_{\rm gs6}$, changes linearly from $(V_{\rm in}-V_o)N_{\rm AUX}/2N_p$ to zero. Then, (22) can be used to calculate the body diode's conduction time

$$t_{body} = \frac{2V_{th}(I_o - I_{\rm in})L_{leak}N_s}{N_{AUX}(V_{\rm in} - V_o)^2}. \tag{22}$$

If a two phase Buck operates at 1 MHz, 1 V/40 A load, the body diode's forward voltage drop is 0.7 V and the dead time between top and bottom switch is 20 ns, total conduction loss for the body diode is [18]

$$P_{\rm diode\_Buck} = (20\ {\rm A})(2)(20\ {\rm ns})(0.7\ {\rm V})(1\ {\rm MHz}) = 0.56\ {\rm W}.$$

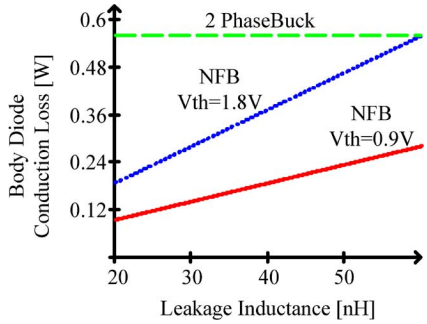


Fig. 17. Body diode conduction loss as a function of leakage inductance reflected to the primary.

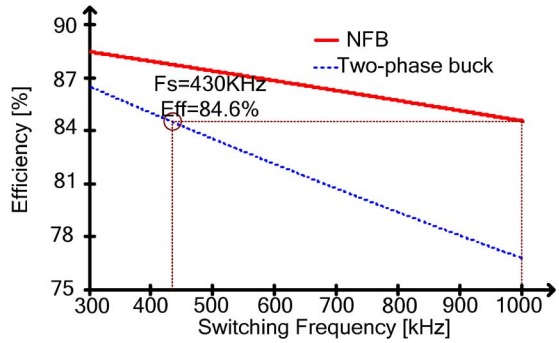


Fig. 18. Calculated efficiency of a two phase Buck and NFB at 1 V/40 A.

For the NFB, the threshold voltage is $V_{\rm th} = 0.9$ V, and other parameters are, $L_{\rm leak} = 30$ nH, $I_o = 40$ A, $I_{\rm in} = 3.4$ A, $Ns =$ a, $N_{\rm AUX} = 3$, then the conduction time for the body diode is 4.3 ns as calculated using (22)

$$\mathrm{P_{diode\_Buck}} = (18.35\ \mathrm{A})(2)(4.3\ \mathrm{ns})(0.7\ \mathrm{V})(1\ \mathrm{MHz}) = 0.11\ \mathrm{W}.$$

From the above calculation 0.45 W energy is saved on the body diode's conduction loss.

Fig. 17 illustrates the body diode's conduction losses as a function of leakage inductance reflected to primary side. From the figure it is clear that reducing the leakage inductance and/or the threshold voltage can reduce the body diode's conduction loss. Leakage inductance can be minimized by interleaving the transformer windings. However, reducing the threshold voltage increases susceptibility to MOSFET false triggering due to noise.

### D. Summary

From the analysis in the previous sub-sections, the major advantages of new topology are that it can reduce switching loss and body diode's conduction loss, yielding improved efficiency. Since the duty cycle of the NFB is extended and the primary switches can achieve ZVS turn on, its switching loss is significantly reduced compared with the two phase Buck. Shorter body diode conduction time and lower voltage stress for the synchronous rectifiers also helps to improve the efficiency.

The efficiencies of the two phase Buck and NFB have been calculated. The efficiency curves are shown in Fig. 18. In the analysis it was assumed that 75% of the turn on loss was saved for the NFB. For the NFB the gate voltage of the two low side MOSFETs, $Q2$ and $Q4$, is $-V_o$ when turned off, so it is assumed that they can be turned off faster (8 ns turn off and 15 ns turn on). In the calculations, IRF7821 was used for the primary MOSFETs and FDS6162N7 was used for the synchronous rectifiers. The output is 1 V/40 A. As shown in Fig. 18, the NFB is able to achieve the same efficiency, 84.6% as a two phase Buck but at more than double the switching frequency (i.e., 430 kHz for the Buck and 1 MHz for the NFB).

A loss breakdown comparison is illustrated in Fig. 19 at 1 V/40 A load and 1 MHz switching frequency. It is clear that the most significant savings for the NFB is from the switching loss reduction. The other loss components in Fig. 19 consist

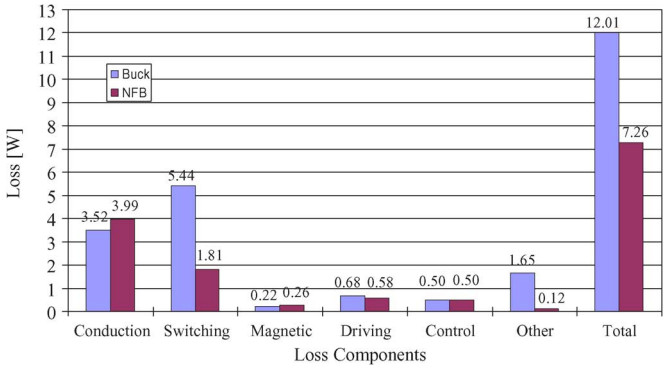


Fig. 19. Loss breakdown comparison between the two phase Buck and NFB at 1 MHz switching frequency and 1 V/40 A load.

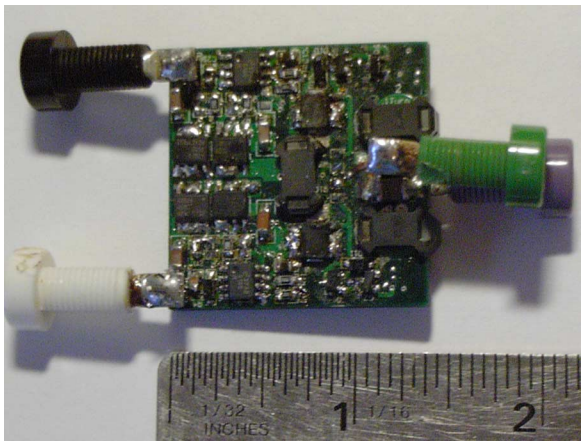


Fig. 20. Photo of the prototype; size $1.41'' \times 1.41''$ (3.6 × 3.6 cm).

of the MOSFET output loss, body diode conduction loss and reverse recovery loss.

## V. Experimental Results

Prototypes of the NFB and two phase synchronous Buck at 12 V input and 1 V/40 A output were designed and built to operate at frequencies between 500 kHz and 1 MHz. The NFB prototype was built on a 1.41 in × 1.41 in, 12 layer, 2oz copper printed circuit board. A photo of the prototype is shown in Fig. 20. In the design, three pairs of RM4 cores were used. One pair was used for the transformer and the other two pairs were used for the current doubler inductors. The turns ratio, primary to secondary for the transformer was 3:1. In the steady state

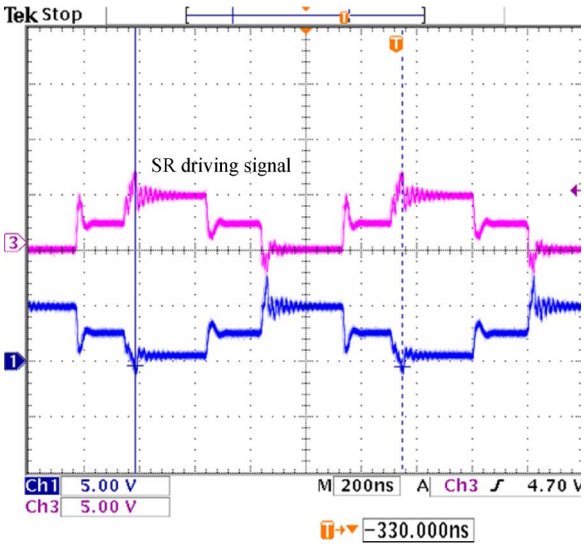


Fig. 21. Gate drive signals of the synchronous rectifiers at 1 MHz switching frequency.

the effective duty cycle was 54.5%. Phase shift control was used to reduce the switching loss at the primary side. In order to demonstrate the advantages of this topology, the efficiency of the new topology was measured at 1 V output and 500 kHz, 700 kHz, and 1 MHz switching frequencies.

The high side MOSFETs used in the design were IRF7821 since they have very low gate charge to minimize switching loss. The synchronous rectifier MOSFETs used were FDS6162N7 since they have very low on resistance which minimizes conduction loss. The UCC3895 phase shift controller and two LM5100 drivers were used. The dead time was optimized at half load (15 A) to 20 ns by adding a resistor between pins 9 and 10 of the UCC3895 controller.

Waveforms of the synchronous rectifier gate signals are shown in Fig. 21. In Fig. 21, we can see that when all four primary MOSFETs are turned off, both SRs are turned on as desired. In Fig. 21 there is some ringing on the SR gate signals, which is caused by leakage inductance on the AUX winding. Care must be taken in the transformer design since large ringing can cause the false turn off of the SR. In addition, a small gate resistor can be added to damp the ringing. In order to reduce the leakage inductance on the driving winding, the AUX winding must have good coupling with the primary winding. The interleaving method shows in Fig. 14 was used to achieve this goal.

From the testing results shown in Figs. 22 and 23, we can see that both the lagging and leading legs are able to achieve ZVS turn on at 20 A load.

The efficiency as a function of load for the NFB was measured and is illustrated in Fig. 24 for switching frequencies of 500 kHz, 700 kHz, and 1 MHz. In addition, a comparison is given in Fig. 25 for the efficiency as a function of load for the NFB and a two phase and three phase synchronous Buck at 500 kHz switching frequency. From the test results shown in Figs. 24 and 25, it is observed that at 30 A load the NFB can achieve 82.1% efficiency at 1 MHz and 84.4% at 500 kHz, but

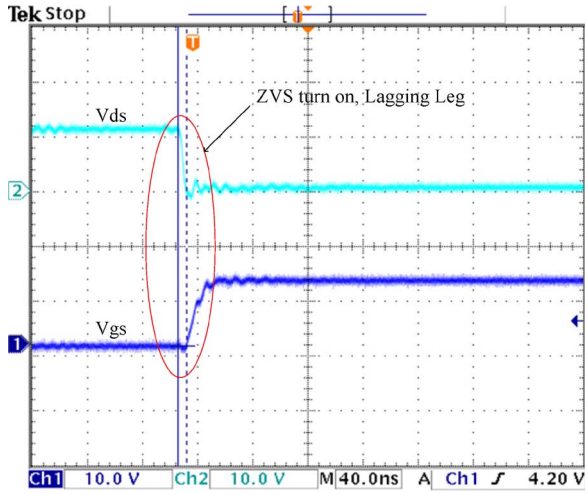


Fig. 22. Drain voltage (top) and gate voltage (bottom); ZVS achieved at turn on for the lagging leg at 1 V/20 A load and 1 Mhz switching frequency.

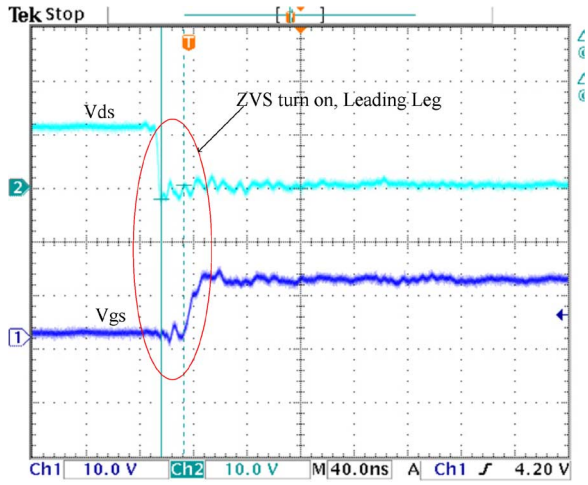


Fig. 23. Drain voltage (top) and gate voltage (bottom); ZVS achieved at turn on for the leading leg at 1 V/20 A load and 1 Mhz switching frequency.

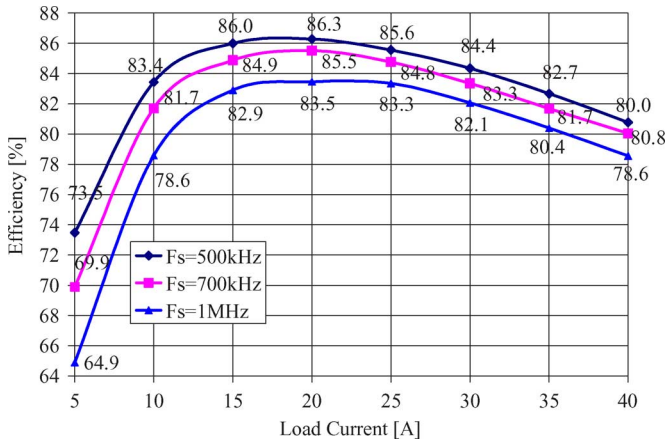


Fig. 24. NFB efficiency as a function of load at 1 V output.

the two phase and three phase Buck topologies achieve only 79.7% and 82.6%, respectively, at 500 kHz. Therefore, compared to the two phase Buck, at 30 A load, a 2.4% efficiency improvement (82.1% for NFB versus 79.7% for two phase Buck) is

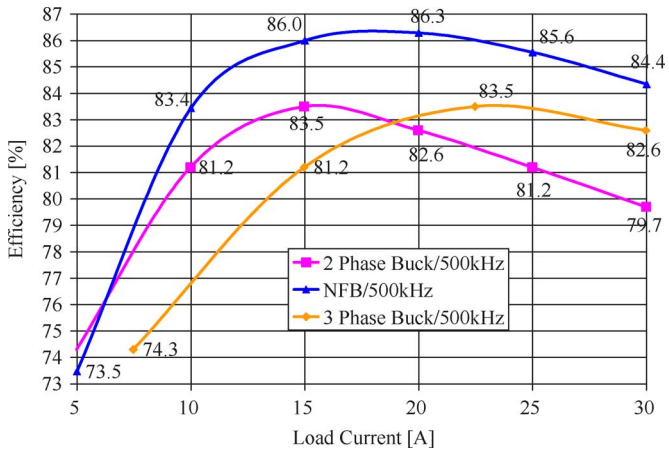


Fig. 25. Efficiency comparison as a function of load between the NFB and the two phase and three phase Buck operating at 500 kHz and 1 V output.

achieved with the NFB at double the switching frequency. Compared to the three phase Buck the efficiency of the three phase Buck at 82.1% is nearly equal to that of the three phase Buck of 82.6% at double the switching frequency, which is a very significant improvement. Furthermore, at 500 kHz and 30 A a 4.7% efficiency improvement (84.4% for NFB versus 79.7% for two phase Buck) is achieved compared with two phase Buck and a 1.8% improvement (84.4% for NFB versus 82.6% for two phase Buck) is achieved compared to the three phase Buck.

## VI. Conclusion

A new NFB topology was proposed. The primary side of this topology is derived from the FB, however the conventional ground points of the primary side are connected directly to the positive point of the output. This topology improvement allows the input current to flow directly to the load without going through the transformer, so the current stress of synchronous rectifiers and filter inductors are both reduced.

Compared with the traditional multiphase Buck topology, the switching loss can be dramatically reduced with the NFB since it operates with extended duty cycle. Furthermore, with the proposed topology, ZVS can be achieved when the high side is operated in phase shift mode. These advantages enable the NFB to achieve higher efficiency than both the two phase and three phase synchronous Buck topologies. These lower losses can also permit the NFB to operate at much higher switching frequencies than the Buck. In addition, smaller output inductors and capacitors can be used to improve the dynamic response and reduce the component cost.

To demonstrate the advantages of this topology, a VRM module has been built and tested at 12 V input and 1 V output. At 30 A load and 500 kHz switching frequency, the NFB achieves 84.4% efficiency, which is 4.7% higher than that of two phase Buck converter (79.7%). Furthermore, at 1 MHz, the NFB achieves 82.1% efficiency, which is 2.4% higher than that of two phase Buck converter operating at 500 kHz.

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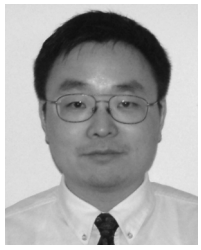

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