A Novel Two Phase Nonisolated Full Bridge With Shared Primary Switches

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***Abstract*—In this paper, a new full bridge topology called the two-phase nonisolated full bridge (NFB) is introduced. The proposed two-phase NFB can handle the same power as two parallel NFB converters, but with less MOSFETs, better efficiency, and lower cost. To demonstrate the advantages of the new topology, two prototypes are built on a 12-layer 2-oz PCB board, one with four inductors, the other with three inductors. Two prototypes achieve 82.3% and 82% efficiency at 1-MHz full load (1 V/80 A), respectively. This is compared to 81.8% efficiency of the two paralleled NFB converters. At light load (1 V/10 A), a 4% efficiency improvement is achieved. Experimental results demonstrate that compared with two paralleled NFB converters, the two-phase NFB converter is able to achieve better efficiency with a simplified power train circuit and reduced cost.**

***Index Terms*—Nonisolated full bridge (NFB), two-phase NFB, voltage regulation module, voltage regulator module (VRM).**

I. Introduction

With the continued improvements in integrated circuit technology, next-generation CPUs will operate at much higher clock frequencies and consume more power. To reduce power consumption, CPUs will operate at supply voltages below 1 V with tight voltage tolerance, large current demand (above 100 A), and fast dynamic response (above 100 A/μs) [1].

The multiphase interleaved Buck converter is the most popular topology for VRM design because of its low cost. However this topology also has some drawbacks.

1) If an output current of 100 A is required, assuming 20 A/phase, a five-phase buck converter is required. If the output current keeps increasing, more phases would be needed. Eventually, the multiphase Buck will become overly complex and will no longer be cost effective.
2) The Buck converter has an extremely narrow duty cycle for output voltages at and below 1 V. Narrow duty cycles yield high switching loss which limits the Buck's switching frequency and makes it difficult to design a Buck based VRM that can achieve high efficiency at a high switching frequency. A narrow duty cycle also reduces the effectiveness of current ripple cancellation by using phase shift control.
3) Using too many phases in parallel makes current sharing complex.

To solve the aforementioned problems, several new topologies have been proposed. The topologies proposed in [2]–[7] are Buck-based topologies that use coupled-inductors or transformers to extend the duty cycle. The major drawback of these topologies is that the voltage stress of the control MOSFET is higher than the input voltage, so an auxiliary circuit is often required to limit the voltage stress on the switches. Furthermore, these topologies operate in hard switching mode, so switching losses prevent them from being suitable candidates at very high switching frequencies.

To solve the problems of the conventional Buck, a new single phase nonisolated full bridge is proposed in [8]. It demonstrates significant advantages over the conventional multiphase Buck; however, if 80 A or more output current is required, two parallel nonisolated full bridges (NFBs) would be required; this solution is complex and not cost effective.

In this paper, a new two-phase nonisolated full bridge (NFB) topology is proposed with significant advantages over two parallel NFB converters. It can reduce the cost and double the output current with better efficiency. The detailed analysis is shown in the following sections: the derivation of the new topology is shown in Section II. In Section III, the operation modes will be analyzed. Section IV is the design equations for the new topology. Section V and VI will analyze the SR driving circuit and zero voltage transition. In Section VII, losses of the new topology will be analyzed. Finally, the experimental results are presented in Section VIII, and the conclusions are presented in Section IX.

II. Derivation and Operation of the Two-Phase Nonisolated Full Bridge

Fig. 1 illustrates the evolution of the two-phase nonisolated full bridge from two paralleled one-phase NFB converters. Fig. 1(a) illustrates two one-phase NFB converters in parallel. Since the conduction loss of the SR is the most significant loss in low-voltage high-current applications [9], [10], we simply parallel the two rectifier stages, and this forms the rectifier stage of the two-phase NFB shown in Fig. 1(b).

When the rectifier stage is in parallel, the primary side should also operate in parallel; this is illustrated in Fig. 1(b). Since the primary side operates in parallel, point B and D shown in Fig. 1(b) can be connected together. When the two primary side windings are connected at B as show in Fig. 1(c), it is observed that QA, Q3, and Q4, QB actually operate in parallel. Considering the conduction loss at the primary side is usually not large, four MOSFETs (Q3, Q4, QA, and QB) can be combined to two

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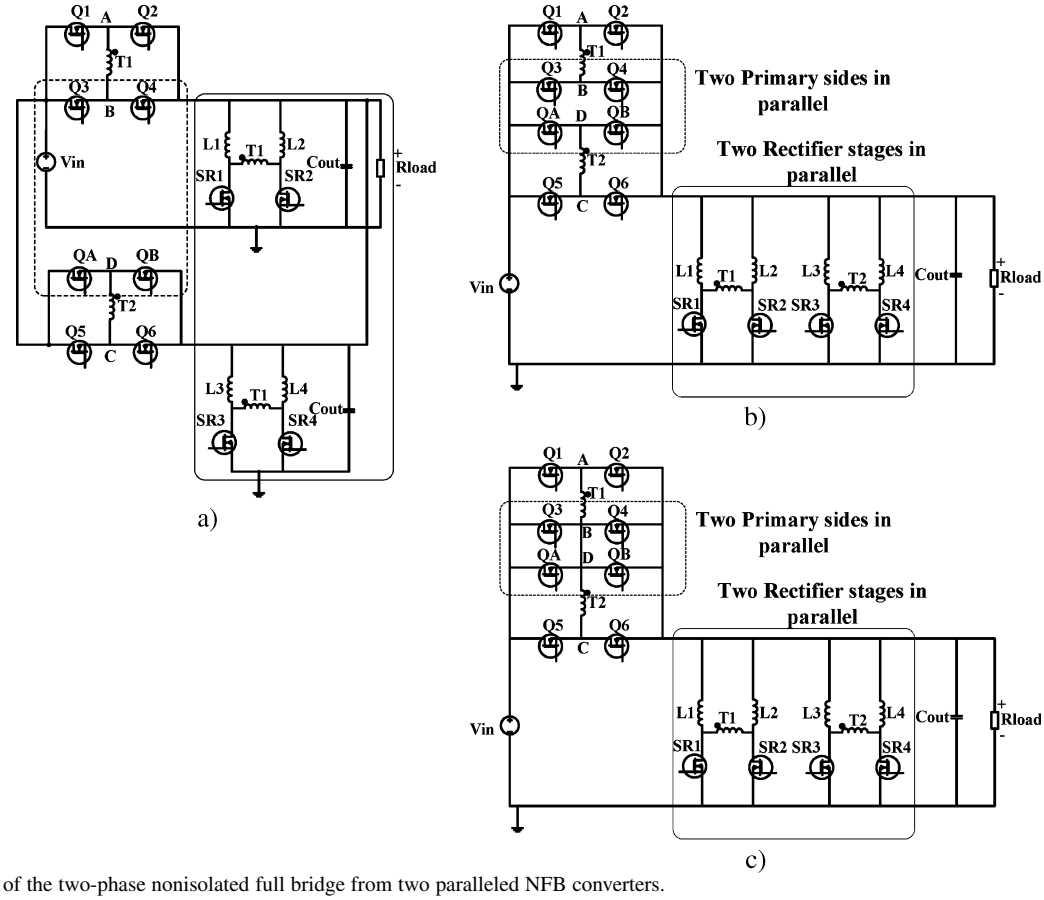

Fig. 1. Evolution of the two-phase nonisolated full bridge from two paralleled NFB converters.

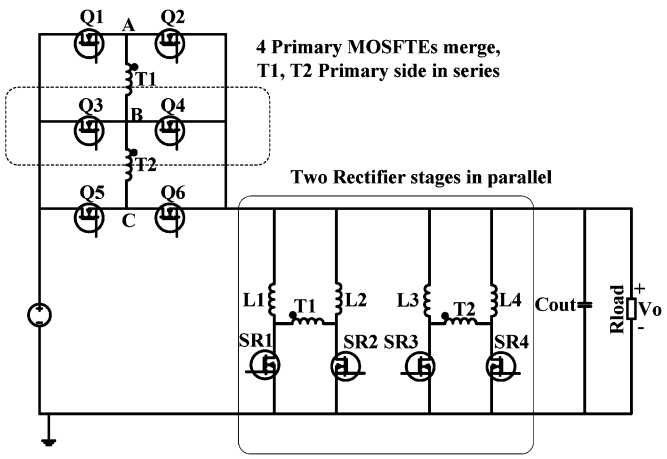

Fig. 2. Proposed new two-phase nonisolated full bridge.

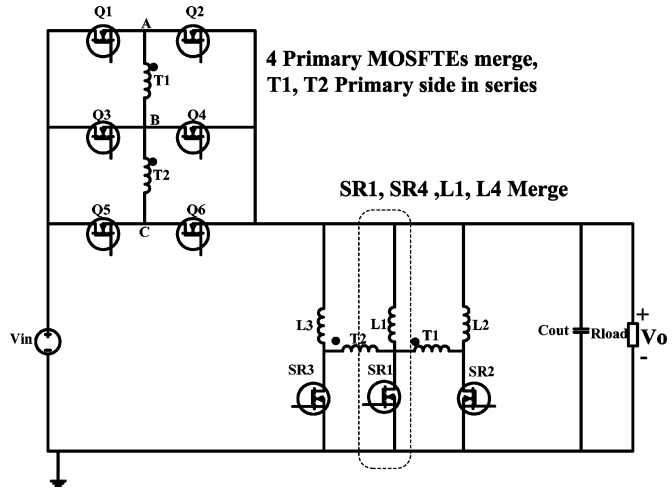

Fig. 3. Two-phase nonisolated full bridge with simplified rectifier stage.

MOSFETs (Q3 and Q4) to simplify the circuit. After making the aforementioned modifications, a new topology is created, as shown in Fig. 2.

The primary side windings of T1 and T2 in Fig. 2 are connected at B, which means for the secondary side windings there are two points that have the same voltage and can be connected together. It is observed that the GS voltages of SR1 and SR4 are exactly the same, so SR1 and SR4 can be driven by the same driver. This means that SR4 and L4 may be removed without effecting the operation of the topology. The further simplified two-phase NFB is show in Fig. 3. This change will result in higher conduction loss for the rectifier stage; however, the total gate loss and cost is reduced.

Using the proposed topology many benefits can be achieved; a more detailed analysis of those benefits will be shown in the following sections.

1) Components cost is reduced.
2) Better efficiency is achieved. A more detailed analysis is shown in Section VII.
3) Current sharing is simplified due to the sharing leg (Q3, Q4) which makes two power stages coupled with each other.

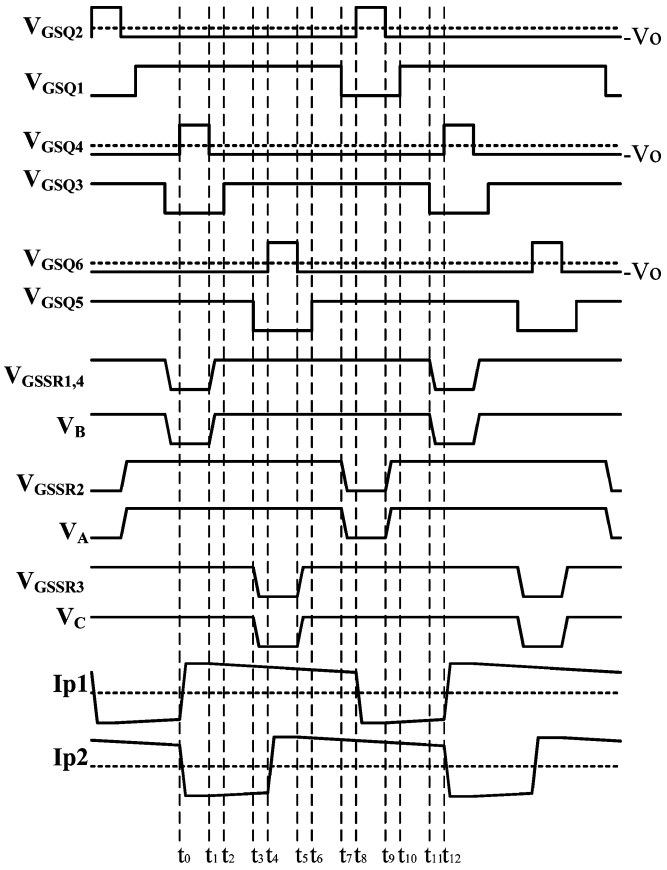

Fig. 4. Key waveforms of the two-phase NFB converter operating in phase shift mode.

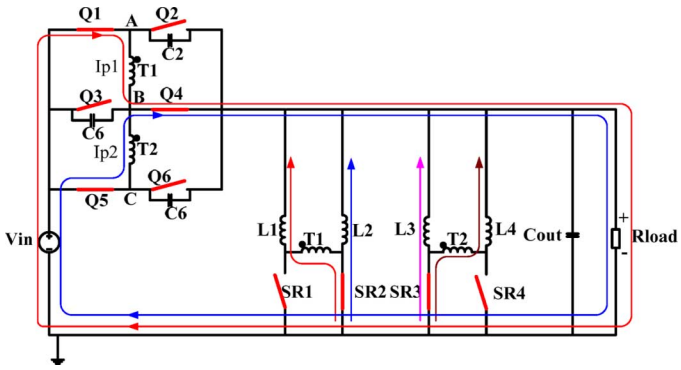

Fig. 5. t0–t1.

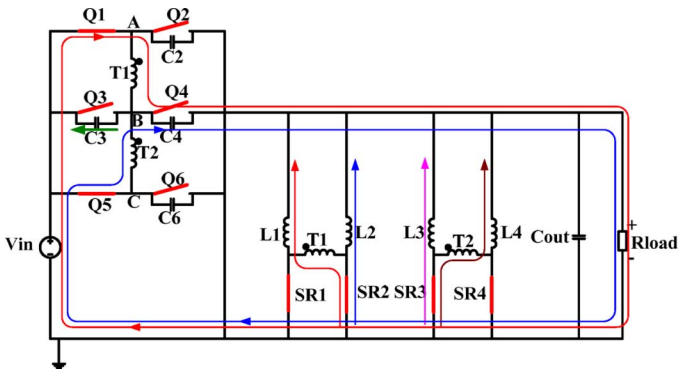

Fig. 6. t1–t2.

4) Compared with the single phase topology [11], a smaller output capacitor and inductor can be used to improve dynamic performance.
5) Since SR1 and SR4 operate in parallel, the number of SRs and inductors can be reduced from four to three if necessary. The further simplified two-phase NFB is shown in Fig. 3.
6) Compared with the topology proposed in [11], the two-phase NFB has reduced current stress for the synchronous rectifiers and output inductors, since a portion of the energy is transferred to the load directly.

Fig. 4 depicts the key waveforms of the two-phase NFB converter. There are 13 operation modes and they will be analyzed in detail in Section III. In Fig. 4, $V_{GSQ1} - V_{GSQ6}$ are the gate driving signals of corresponding MOSFETs in Fig. 2. Q1, Q3, and Q5 are leading leg MOSFETs. Their duty cycles are 1-D and are shifted 120° from each other. Q2, Q4, and Q6 are lagging leg MOSFETs. Their duty cycles are D and are shifted 120° from each other. Ip1 and Ip2 represent the current which conducts through the primary windings of transformer T1 and T2, respectively, shown in Fig. 2.

The synchronous MOSFET driving signal $V_{GSSR1\&SR4}$, V_{GSSR2}, and V_{GSSR3} are generated by the voltages V_A, V_B, and V_C from points A, B, and C, respectively, as shown in Fig. 2. SR1 and SR4 are driven by the same driver because they operate in parallel. The detailed analysis of the SR driving circuit will be analyzed in Section V. It is also noted that the source of MOSFETs Q2, Q4, and Q6 are directly connected to the output; thus, they are turned off by $-Vo$, which allows them to be turned off faster to reduce switching loss.

III. Operation Modes

In this section, the operation modes of the new topology are analyzed in detail, and the impact of transformer's leakage inductance on the SR body diode conduction time will also be discussed. There are a total of 13 operation modes. The 13 operation modes are in correspondence with the key waveforms shown in Fig. 4. In the analysis, T1 and T2 represent the two transformers in Fig. 2, and Ip1 and Ip2 represent the current goes through the primary windings of transformer T1 and T2, and $+/-$ are used to indicate the direction of the current in correspondence with the key waveforms shown in Fig. 4.

The first state is shown in Fig. 5 from t0–t1. In this operation mode Q1, Q4, Q5, SR2, and SR3 are on. Q2, Q3, Q6, SR1, and SR4 are off. Energy is transferred by transformer T1 and T2 from the primary side to the secondary side. Two transformers operate in parallel and the input current flows to the load side directly. The current stress of the output inductors and the SRs is reduced as a result. During this time interval, the current in Q1 and Q5 both conduct through Q4 causing the current stress of Q4 to be doubled compared to that of Q1 and Q5, as shown in Fig. 18.

The second state t1–t2 is shown in Fig. 6. In this operation mode, Q4 is turned off at t1 to prepare for the zero voltage turn-on of Q3. The load current reflected from the secondary

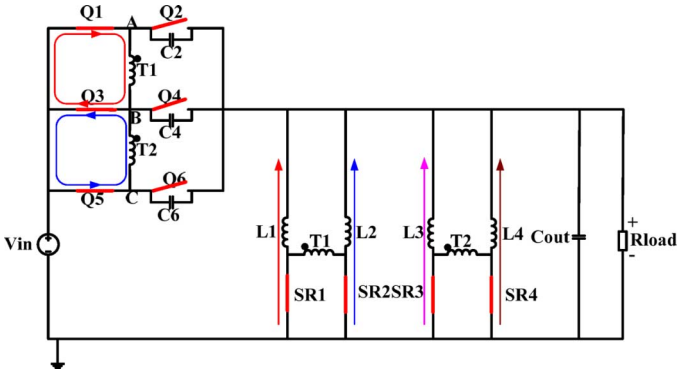

Fig. 7. t2–t3.

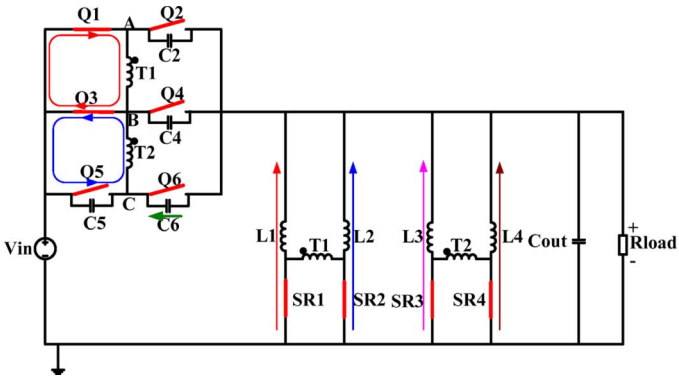

Fig. 8. t3–t4.

side begins charging C4 while discharging C3. The voltage at point $\mathrm{B}(\mathrm{V_B})$ increases linearly from Vo to Vin. The gate voltage of SR1 and SR4 also begins to increase, and SR1 and SR4 will be turned on after their gate voltage increases above the threshold. However, due to the leakage inductance, SR1 and SR4 will not conduct the load current after they are turned on. In this transition, the gate capacitors of SR1 and SR4 are charged by a constant current source and their gate loss can be reduced. This will be analyzed in Section V.

The third mode t2–t3 is shown in Fig. 7. When the voltage across Q3 equals zero, Q3 is turned on with ZVS at t2. At this time, both the primary windings of T1 and T2 are shortened, and their primary sides and secondary sides are decoupled. SR1 and SR4 begin to conduct the load current after Q3 is turned on.

The fourth state is shown in Fig. 8. Q5 is turned off at t3 to prepare for the ZVS turn-on of Q6. The energy stored in the leakage inductance of T2 charges C5 and discharges C6. The voltage at point C $(\mathrm{V_C})$ decreases from Vin to Vo. The gate voltage of SR3 also begins to decrease, and its body diode begins conducting for a short period of time after its gate voltage reduces below the threshold. This time interval should be as small as possible the detailed analysis is shown in Section V.

The fifth state is shown in Fig. 9. Q6 is turned on at t4 after the voltage across it becomes zero. The primary side current of T2 cannot change direction instantly after Q6 is turned on. Thus Vin-Vo is applied across the leakage inductance of T2 before the primary side current $-\mathrm{I_{p2}}$ changes to $+\mathrm{I_{p2}}$. The body diode of SR3 is conducting and will be turned off after $-\mathrm{I_{p2}}$ changes to $+\mathrm{I_{p2}}$.

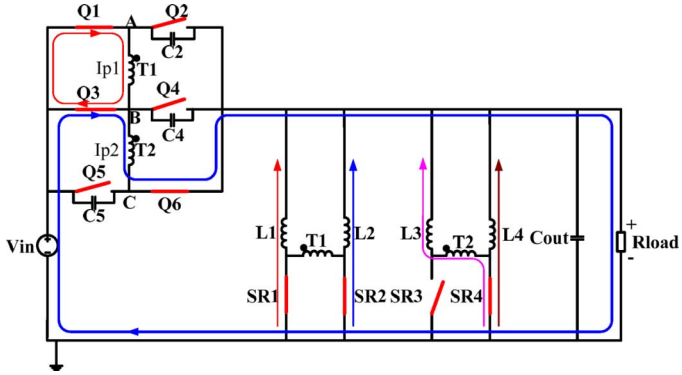

Fig. 9. t4–t5.

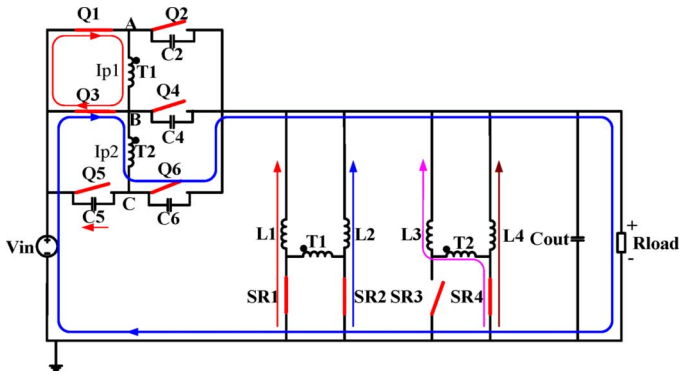

Fig. 10. t5–t6.

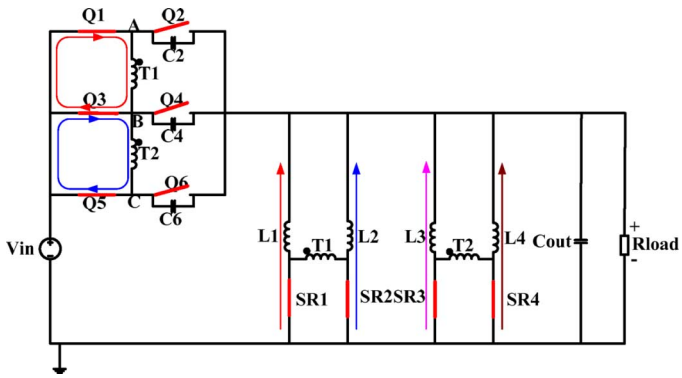

Fig. 11. t6–t7.

The sixth state is shown in Fig. 10. Q6 is turned off at t5 to prepare for the ZVS turn-on of Q5. The load current reflected from secondary side charges C6 and discharges C5. $\mathrm{V_C}$ increases from Vo to Vin. The gate voltage of SR3 also increases. SR3 is turned on after its gate voltage increases above the threshold; however, SR3 will not conduct the load current immediately after it is turned on due to the leakage inductance.

The seventh state is shown in Fig. 11. Q5 is turned on at t6 after the voltage across it becomes zero. At this time, the primary side and the secondary side of T2 are both shortened and SR3 begins to conduct the load current.

The eighth state is shown in Fig. 12. Q1 is turned off at t7 to prepare for the ZVS turn-on of Q2. The energy stored in the leakage inductance of T1 charges C1 and discharges C2. The voltage at point A $(\mathrm{V_A})$ decreases from Vin to Vo. The gate

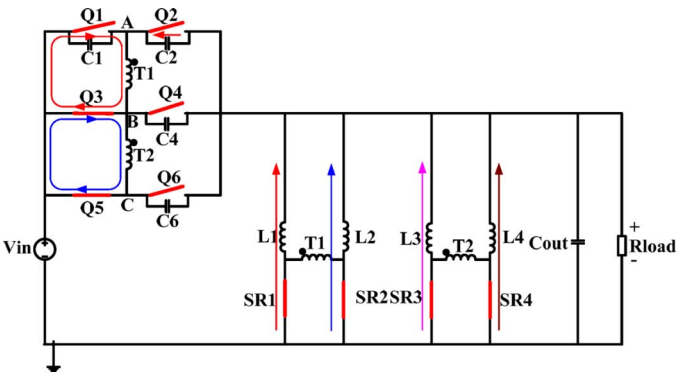

Fig. 12. t7–t8.

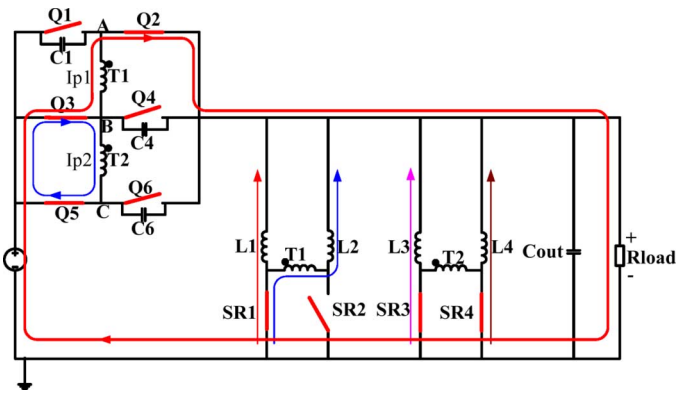

Fig. 13. t8–t9.

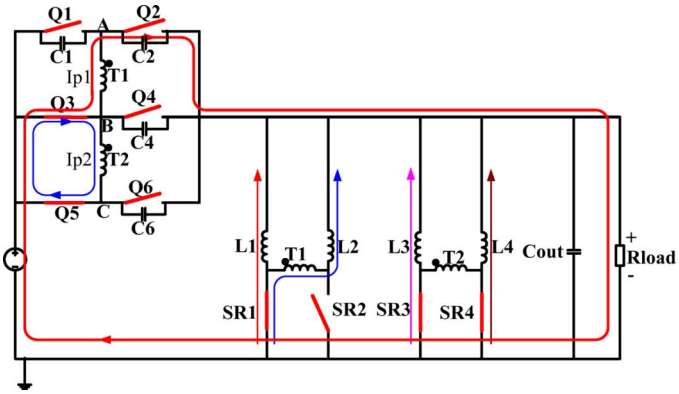

Fig. 14. t9–t10.

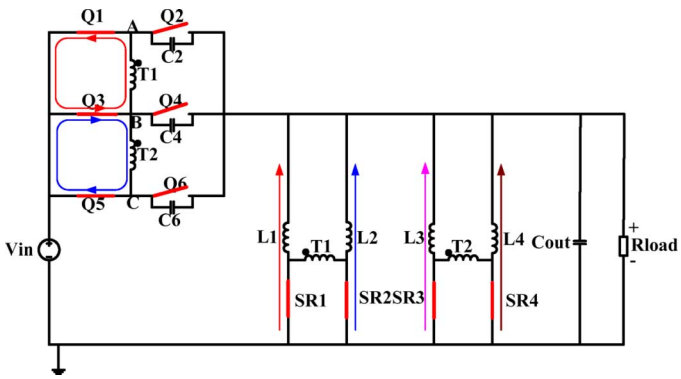

Fig. 15. t10–t11.

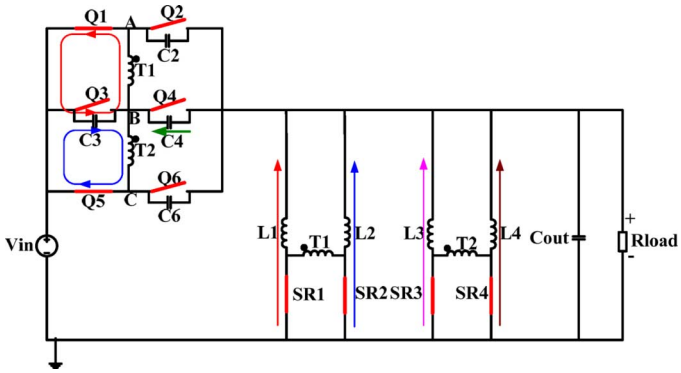

Fig. 16. t11–t12.

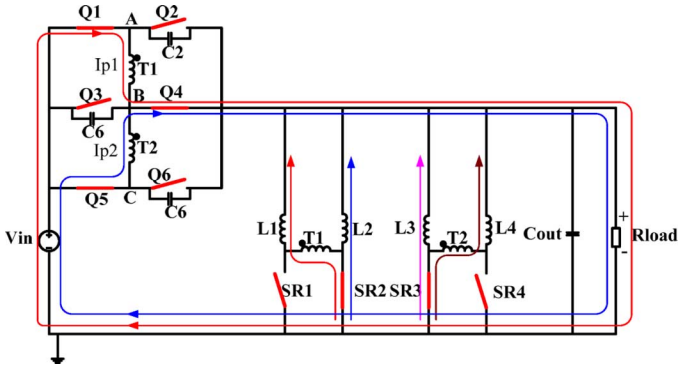

Fig. 17. t12–t13.

voltage of SR2 also decreases, and its body diode begins to conduct for a very short time after its gate voltage reduces below the threshold.

The ninth state is shown in Fig. 13. Q2 is turned on at t8 after V_A decreases to Vo. Due to the leakage inductance the primary current I_{p1} cannot change direction instantly; Vin-Vo will be applied across the leakage inductance of T1 before I_{p1} completely changes to $-I_{p1}$. After Ip1 changes to $-I_{p1}$, SR2 is turned off completely and T1 begins to transfer energy to the secondary side.

The tenth state is shown in Fig. 14. Q2 is turned off at t9 to prepare for the ZVS turn-on of Q1, the load current reflected from the secondary side charges C2 and discharges C1. V_A increases from Vo to Vin. The gate voltage of SR2 also begins to increase and SR2 is turned on after its gate voltage increases above the threshold; However, SR2 will not conduct the load current after it is turned on due to the leakage inductance.

The 11th state is shown in Fig. 15. Q1 is turned on at t10 after the voltage across it becomes zero. The primary windings of T1 are shortened, the primary side and secondary side are decoupled, and SR2 begins to conduct the load current.

The 12th operation state is shown in Fig. 16. Q3 is turned off at t11 to prepare for the ZVS turn-on of Q4. The energy stored in the leakage inductance of T1 and T2 charges C3 and discharges C4. V_B decreases from Vin to Vo. The gate voltage of SR1 and SR4 also begins to decrease, and their body diodes begin to conduct for a very short time after their gate voltages reduce below the threshold.

The 13th state is shown in Fig. 17. After the voltage across Q4 becomes zero, Q4 is turned on with ZVS at t12. Due to the

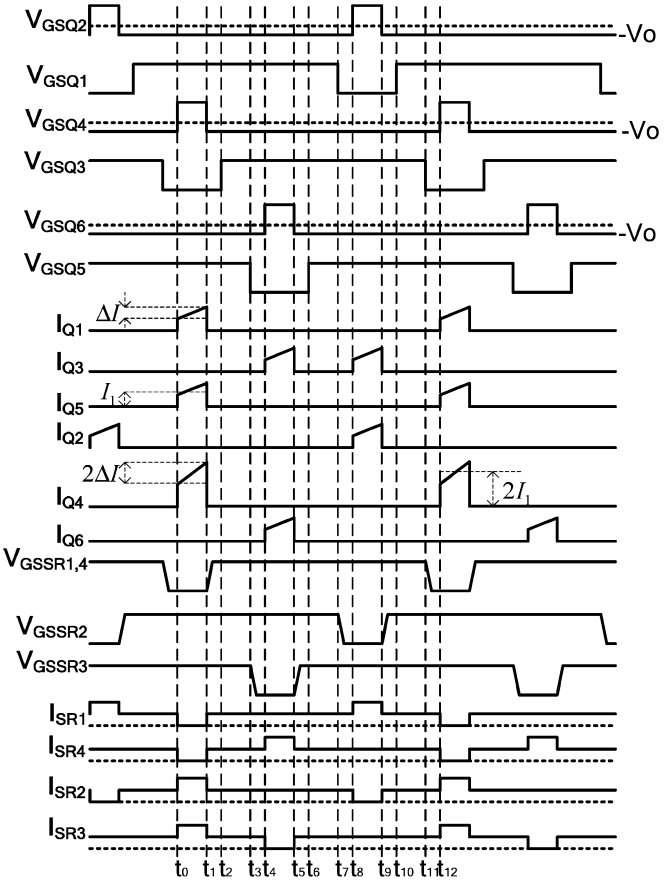

Fig. 18. Current waveforms of major switches in two-phase NFB.

leakage inductance, the primary current cannot change its direction instantly. Vin-Vo is applied across the leakage inductance of T1 and T2 and the primary current of T1: $-\mathrm{I_{p1}}$ changes to $+\mathrm{I_{p1}}$ and T2: $+\mathrm{I_{p2}}$ changes to $-\mathrm{I_{p2}}$. SR1 and SR4 are turned off completely after the primary currents of T1 and T2 change direction completely and both transformers T1 and T2 begin to transfer energy to the secondary side. At this point, one cycle is completed. Based on the analysis, the key current waveforms are shown in Fig. 18, more detailed analysis of major switches' current stress will be shown in Section IV.

IV. Design Equations

In this section, the key equations of the new topology will be derived. Those equations can be used to analyze and design the proposed two-phase nonisolated full bridge topology.

1) Output Voltage Gain: Equation (1) is derived using the output inductor volt-seconds in steady-state, D is duty cycle. Equation (2) is derived from (1). Equation (2) is the voltage gain of the two-phase NFB, if 12 V to 1 V is required. $Np = 3$ $Ns = 1$ should be selected and $D = 0.27$ is calculated by using (2) ($N = Np/Ns$, $D = Ton/Ts$)

$$V_o(1-D)T_s + \left(V_o - (V_{\mathrm{in}} - V_o)\frac{N_s}{N_p}\right)DT_s = 0 \tag{1}$$

$$\frac{V_o}{V_{\mathrm{in}}} = \frac{D}{N+D}. \tag{2}$$

2) Voltage Stress: The primary MOSFET stress can be calculated by (3), and (4) can be used to calculate the SR voltage stress. When the input voltage is 12 V, output voltage 1 V, and $Np/Ns = 3$, the calculated SR voltage stress is 3.6 V. This is considerably less than the input voltage which means that low voltage rating SRs (such as 8-V MOSFETs) can be used to improve efficiency. As we know for multiphase Bucks, the voltage stress of the SR equals input voltage, which means a 20-V MOSFET must be used.

$$V_{\mathrm{PMOS}} = V_{\mathrm{in}} - V_o \tag{3}$$

$$V_{\mathrm{SR}} = (V_{\mathrm{in}} - V_o)\frac{N_s}{N_p}. \tag{4}$$

3) Current Stress of the Power Inductor: Equation (5) can be used to calculate the average input current, assuming efficiency is 100%

$$I_{\mathrm{in}} = \frac{P_{\mathrm{out}}}{V_{\mathrm{in}}}. \tag{5}$$

Since the input current goes directly to the load side, the currents through the four output inductors is Io-Iin; therefore, (6) can be used to calculate the average inductor current

$$I_{\mathrm{Lavg}} = \frac{I_o - I_{\mathrm{in}}}{4}. \tag{6}$$

The SR will conduct (1-D)Ts, and the output voltage is applied to the output inductor during this period thus (7) can be used to calculate the inductor current ripple

$$\Delta I_L = \frac{V_o(1-D)T_s}{L}. \tag{7}$$

Equation (8) can be used to calculate the minimum and maximum inductor current

$$I_{L\_\min} = I_{\mathrm{Lavg}} - \frac{\Delta I}{2} \qquad I_{L\_\max} = I_{\mathrm{Lavg}} + \frac{\Delta I}{2}. \tag{8}$$

The root mean square (RMS) current through the output inductor can be calculated as

$$I_{\mathrm{Lrms}} = \sqrt{I_{\mathrm{Lavg}}^2 + \frac{\Delta I^2}{12}}. \tag{9}$$

4) Current Stress of Synchronous Rectifier Power MOSFET: Fig. 18 illustrates the current waveforms of the SRs when the ripple current is neglected. It is observed from Fig. 18 that the RMS current of all synchronous MOSFETs are the same and can be calculated by using (10). When calculating the current stress of the SR the current ripple is neglected to simplify the calculation. $\mathrm{I_{Lavg}}$ is the average inductor current

$$I_{\mathrm{SR\_rms}} = \sqrt{I_{\mathrm{Lavg}}^2(1-2D) + D(2I_{\mathrm{Lavg}})^2}. \tag{10}$$

5) Current Stress of the Primary Power MOSFETs Q1, Q2, Q5, Q6: Fig. 18 illustrates the current waveform through major switches in the two-phase NFB, the circulating current and ripple current of SRs are neglected to simplify the analysis. In Fig. 18 $\mathrm{V_{GSQ1}} - \mathrm{V_{GSQ6}}$ represent the gate signal of MOSFETs Q1–Q6 in Fig. 2, $\mathrm{V_{GSSR1}} - \mathrm{V_{GSSR4}}$ represent the gate signal

of synchronous MOSFETs SR1–SR4. $I_{Q1} - I_{Q6}$, $I_{SR1} - I_{SR4}$ represent the current through MOSFETs Q1–Q6 and SR1–SR4. I1 is the average inductor current reflected to the primary side and ΔI is the inductor ripple current reflected to the primary side. They can be calculated using (13).

The circulating current of the primary side is neglected as shown in Fig. 18. In this case Q1, Q2, Q5, and Q6 will have the same RMS current stress while Q3 and Q4 will have higher RMS current stress. The peak turn-on and turn-off current of the primary MOSFETs Q1, Q2, Q5, and Q6 can be calculated using (11). The RMS current through Q1, Q2, Q5, and Q6 can be calculated as

$$I_{\text{peak\_off}} = I_{L\_\max}\frac{N_S}{N_p} \quad I_{\text{peak\_on}} = I_{L\_\min}\frac{N_S}{N_p} \tag{11}$$

$$I_{\text{Q1\_RMS}} = \sqrt{D\left(I_1^2 + \frac{\Delta I^2}{12}\right)} \tag{12}$$

$$I_1 = I_{\text{L\_avg}}\frac{1}{N} \quad \Delta I = \frac{\Delta I_L}{N} \quad N = \frac{N_p}{N_S}. \tag{13}$$

For example, if $Vin = 12$ V, $Vo = 1$ V, Io $= 80$ A, $Fs =$ 1 MHz, and Inductor $= 100$ nH, then Ipeak_on $= 4.8$ A, Ipeak_off $= 7.2$ A, $I_{Q1RMS} = 3.6$ A. (Q2, Q5, Q6 will have the same RMS current and peak current stress as Q1).

6) Current Stress of Q4: The current stress of Q4 is the highest of the six primary side MOSFETs, since $I_{Q4} = I_{Q1} + I_{Q5}$ as shown in Fig. 18. Q4's current stress is double as compared with that of Q1, Q2, Q5, and Q6. Its peak turn-on and turn-off current can be calculated using (14). Its RMS current can be calculated using (15). I_1, and ΔI can be calculated using (13). For example, if $Vin = 12$ V, $Vo = 1$ V, Io $= 80$ A, $Fs = 1$ MHz, and Inductor $= 100$ nH, then Ipeak_on $= 9.6$ A, Ipeak_off $= 14.5$ A, $I_{Q4RMS} = 7.2$ A

$$I_{\text{Q4peak\_off}} = 2I_{L\_\max}\frac{N_S}{N_p}$$

$$I_{\text{Q4peak\_on}} = 2I_{L\_\min}\frac{N_S}{N_p} \tag{14}$$

$$I_{\text{Q4\_RMS}} = 2\sqrt{D\left(I_1^2 + \frac{\Delta I^2}{12}\right)} = 2I_{\text{Q1\_RMS}}. \tag{15}$$

7) Current Stress of Q3: It can be observed from Fig. 18 that the RMS current stress of Q3 is less than that of Q4, but higher than that of Q1, Q2, Q5, and Q6. Iq3 $=$ Iq2 $+$ Iq6, but Iq3 and Iq6 are 120° out of phase with each other as shown in Fig. 18, so the peak current of Q3 is not increased, and it can be calculated using (11). In addition, Q3 is turned on at t2 and turned off at t11 only so Q3's switching loss will also be the same as Q1 (Section VII will provide a more detailed analysis.) This is one of the benefits of phase shift control, which reduces the current stress of the shared leg MOSFETs in the two-phase NFB. The RMS current through Q3 can be calculated using (16). I_1 and ΔI can be calculated using (13)

$$I_{\text{Q3\_RMS}} = \sqrt{2D\left(I_1^2 + \frac{\Delta I^2}{12}\right)} = \sqrt{2}I_{\text{Q1\_RMS}}. \tag{16}$$

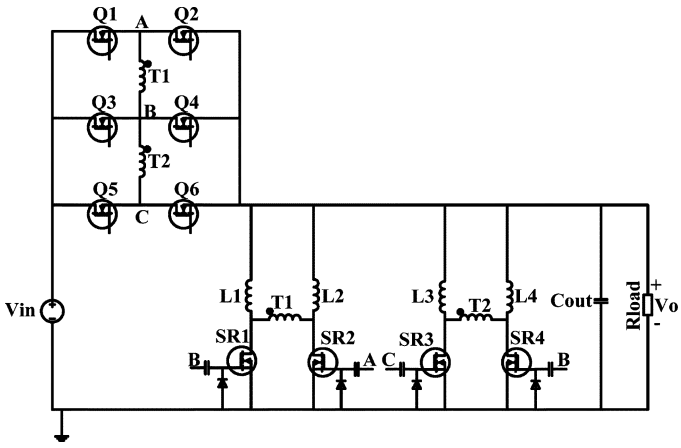

Fig. 19. Synchronous MOSFETs drive signal connection.

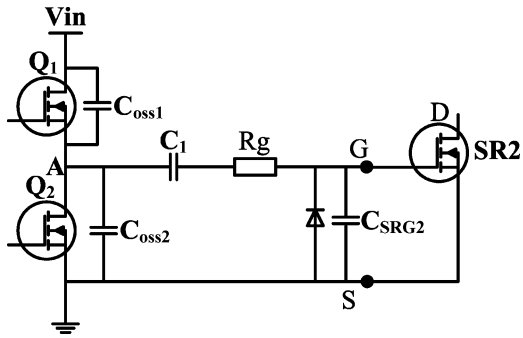

Fig. 20. Synchronous MOSFET equivalent driving circuit.

For example, if $Vin = 12$ V, $Vo = 1$ V, Io $= 80$ A, $Fs = 1$ MHz, and Inductor $= 100$ nH, then Ipeak_on $= 4.8$ A, Ipeak_off $= 7.2$ A, $I_{Q3RMS} = 5.1$ A.

V. Synchronous MOSFET Driving

Compared with an external driver, the self-driven method reduces the cost, simplifies the timing control of the SR turn-on and turn-off transition and saves some of the gate energy. In this section, the synchronous MOSFET driving method proposed in [11] is extended to drive the synchronous MOSFETs in the two-phase NFB. A new linear method will be used to analyze the SR turn-on and turn-off transition and calculate the SR body diode's conduction time.

It can be observed from Fig. 4 that voltage V_A, V_B, and V_C can be used to drive SR MOSFETs. For example, V_A can be used to drive SR2, V_B can be used to drive SR1 and SR4, and V_C can be used to drive SR3. Fig. 19 shows the connection of the SR driving signals. The voltage signals from points A, B, and C are connected directly to synchronous MOSFETs gate through a dc block capacitor. The detailed driving circuit is shown in Fig. 20.

It is observed from Fig. 20 that the voltage across Q2 is used to drive SR2. Coss1 and Coss2 represent the output capacitors of Q1 and Q2, respectively. C_{SRG2} represents the gate capacitor of SR2 while C1 represents the dc block capacitor. Rg is the gate resistance of the synchronous MOSFET. From Fig. 20 it is observed that C_{SRG2} is in parallel with Coss2 which means that

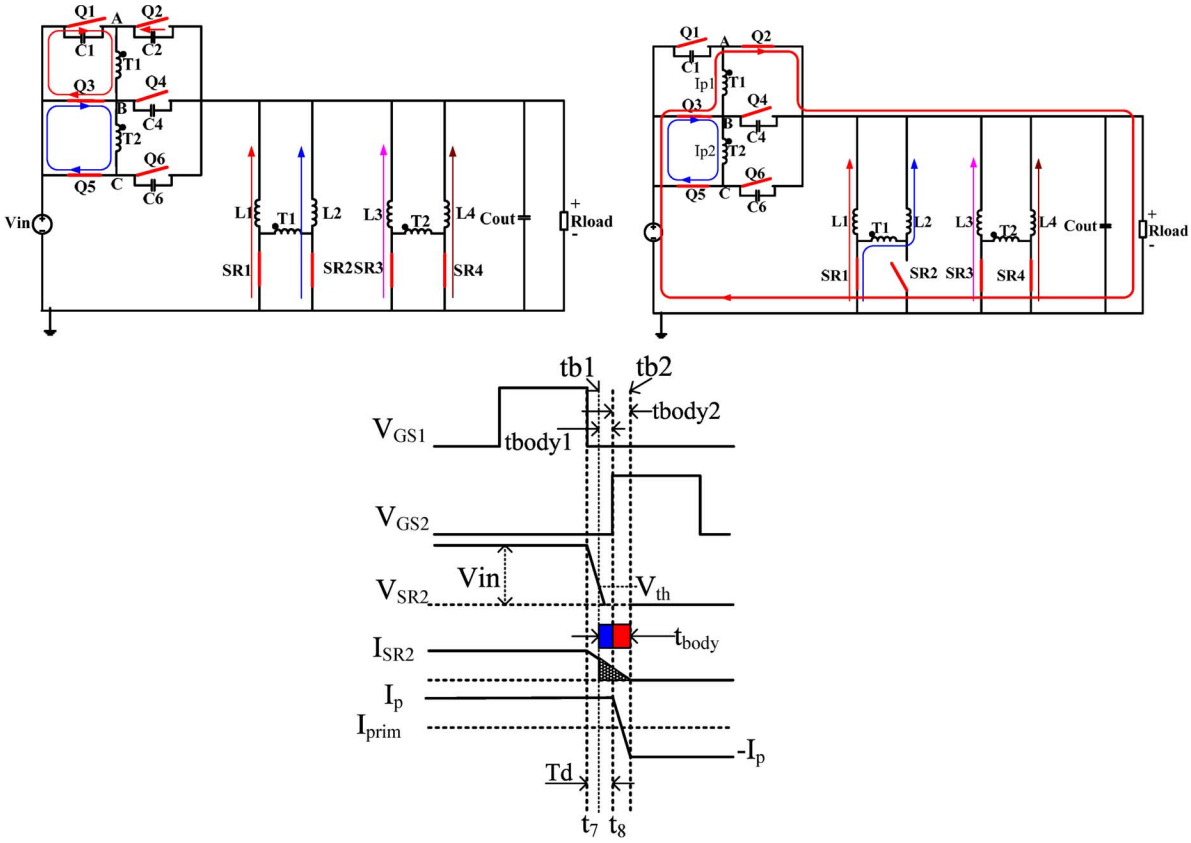

Fig. 21. Lagging leg transition of the self-driven synchronous rectifiers.

the output capacitor of Q2 is equivalently increased and thus requires more energy in order for Q2 to achieve ZVS turn-on.

A. Synchronous MOSFET Turn-On Transition [t9–t10]

SR2 is used to analyze the detailed operation of synchronous rectifiers. The SR2 turn-on transition begins at t9, when Q2 is turned off at t9 to prepare for the ZVS turn-on of Q1. At this point, the synchronous MOSFET's gate voltage V_{GSR2} begins to increase. The load current reflected from the secondary side charges Coss2 + C_{SRG2} and discharges Coss1. The voltage at point A linearly increases from Vo to Vin. During the synchronous MOSFETs turn-on transition shown in Fig. 14 [t9–t10], SR2 is turned on after its gate voltage increases above the threshold voltage; however, it will not conduct the load current, this is because that the secondary side winding of T1 conducts the current of L2 before SR2 is turned on. After Q2 is turned off the current in the leakage inductance will not change instantly, and SR2 is turned on while L2's current continues through the transformer winding. It is noticed that SR2 is turned on before it begins to conduct any current; thus, its body diode will not conduct any current during the turn-on transition. Therefore, the body diode conduction during the turn-on transition is eliminated.

B. Synchronous MOSFET Turn-Off Transition [t7–t8]

In this section, a linear method is used to analyze the SR turn-off transition. SR2 is used as an example. The detailed transition waveform is illustrated in Fig. 21. In order to simplify the analysis it is assumed that the gate voltage of SR2 (V_{SR2}) changes linearly. The assumption is valid as the synchronous rectifier gate resistances and the leakage inductance of the power transformer winding are very small.

The lagging leg transition begins when Q1 is turned off at t7 to prepare for the ZVS turn-on of Q2. After Q1 is turned off, the transformer leakage inductor begins to resonate with Coss1 and Coss2 + C_{GSR2}. V_{SR2} and I_{SR2} will begin to decrease. After V_{SR2} decreases linearly below the gate threshold voltage at tb1, the body diode of SR2 will begin to conduct the load current. The SR body diode's conducting time during this stage is from tb1 to t8 and is equal to t_{body1}. t_{body1} can be calculated using (17). (N is the turn's ratio of the power transformer $Np : Ns$, Td is the dead time between Q1 and Q2, Vth is the gate threshold voltage of SR2).

$$t_{\text{body1}} = Td - \frac{4(2\text{Coss} + C_{GSR})N(V_{\text{in}} - V_{th})}{I_o}. \quad (17)$$

After the voltage across Q2 reduces to zero, Q2 is turned on with zero voltage at t8. Due to the transformer leakage inductance, the primary side current cannot change direction instantly; Vin-Vo is applied across the leakage inductance of the power transformer and forces the primary side current to change direction linearly. After the primary side current changes direction completely at tb2, I_{SR2} reduces to zero, and SR1 will conduct the load current in L1 and L2. The body diode's conduction time during this stage is dependant on the time required for the primary current to change direction. The conduction time is from t8 to tb2 and is equal to tbody2. t_{body2} can be

calculated using (18), where N is the transformer turn's ratio $N = Np/Ns$.

$$t_{\text{body2}} = \frac{I_o L_{\text{leakage}}}{2N(V_{\text{in}} - V_o)} \tag{18}$$

$$t_{\text{body}} = t_{\text{body1}} + t_{\text{body2}}. \tag{19}$$

The total body diode conduction time is equal to tbody1 + tbody2 and can be calculated using (19). From (17) and (18) it is clear that reducing the leakage inductance, threshold voltage, or the dead time can reduce the body diode's conduction loss. Leakage inductance can be minimized by interleaving the transformer windings. However, reducing the dead time could also cause non ZVS turn-on of the lagging legs and increase the switching loss. Reducing the threshold voltage may increase the susceptibility to MOSFET false triggering due to noise. From Fig. 21 it is also observed that we can reduce the body diode's conduction time by turning off the SR slower. One way to achieve this is to add an external gate resistor which will also increase the gate loss.

When Io = 40 A, $L_{\text{leakage}} = 30$ nH, $Vth = 0.7$ V, $Td = 10$ ns, Csr = 5 nF, Coss = 250 pF, $N = 3$ using (17) and (18) the calculated body diode's conduction time is 11 ns.

Compared with a multiphase Buck, the SRs's body diodes in the two-phase NFB only conduct during the turn-off transition while the SR's body diodes in the Buck conduct during both turn-on and turn-off transition [12], [13]. Therefore, the body diode's conduction loss will be smaller for the two-phase NFB converter, and the switching loss and gate loss can be further reduced if the method proposed in [12] is used.

VI. Zero Volatge Turn-On Transition

From the analysis in the previous sections, it is shown that Q1, Q3, and Q5 are leading leg MOSFETs. Q2, Q4, and Q6 are lagging leg MOSFETs. The output capacitors of the lagging leg MOSFETs are discharged by the energy stored in the leakage inductance, so it is more difficult for them to achieve zero voltage turn-on.

From the previous section it is observed that the SR's gate capacitor is in parallel with the output capacitor of Q2, Q4, and Q6. This equivalently enlarges the output capacitors of the primary side MOSFETs, and as a result increases the dead time and energy needed to achieve ZVS turn-on. The detailed analysis will be discussed in this section.

A. Leading Legs, Transition During [t9–t10] (Q1,Q3, Q5)

The transition paths of the leading leg are shown in Fig. 14. Q2 is turned off at t9 to prepare for the zero voltage turn-on of Q1. The current reflected from the secondary side charges C2 and discharges C1. During this transition, the time required to charge C2 from Vo to Vin and discharge C1 from Vin to Vo is dependent on the load current. Since this time interval is very short, it can be assumed that the charge current is constant during the transition. Equations (20) and (21) can be used to calculate the voltage across C1 and C2, assume $C1 = C2$. Equation (22) can be used to calculate the dead time needed to achieve zero voltage turn-on. Equation (22) is derived based on the assumption that during the duration of [t9–t10], the current is constant to charge C2 and discharge $C1$. I_{Lavg}, in (20)–(22), represents the average current in L2 and can be calculated using (23) as follows:

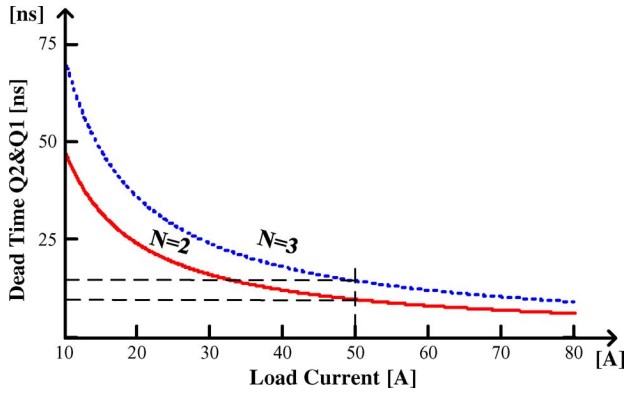

Fig. 22. Dead time between Q2&Q1 required for Q1 to achieve ZVS for the leading leg as a function of load current.

$$V_{C1}(t) = (V_{\text{in}} - V_o) - \frac{I_{\text{Lavg}} t}{2C2N} \tag{20}$$

$$V_{C2}(t) = \frac{I_{\text{Lavg}} t}{2C1N} \tag{21}$$

$$t_{\text{dead\_Q12}} > \frac{2C1(V_{\text{in}} - V_0)N}{I_{\text{Lavg}}} \tag{22}$$

$$I_{\text{Lavg}} = \frac{(I_o - I_{\text{in}})}{4}. \tag{23}$$

Fig. 22 shows the minimum dead time required to achieve ZVS turn-on. This figure is calculated using (22) as a function of the load current. The operating parameters are as follows: Vin = 12 V, $N = 3$, and $N = 2$, $C1 = C2 = 2.5$ nF (since the SR gate capacitor is in parallel with C2, it equivalently increases the value of C1 and C2). From Fig. 22 it is observed that a heavy load and a low turn's ratio can help the NFB achieve ZVS. As shown in Fig. 22, for a 50-A load, $Td = 14.4$ ns for $N = 3$, and $Td = 9.6$ ns for $N = 2$.

B. Lagging Legs, Transition During [t7–t8] (Q2 Q4 Q6)

The transition paths of the lagging leg are shown in Fig. 12. Initially, Q1 is turned off at t7 to prepare for the zero voltage turn-on of Q2. If the energy stored in the leakage inductance of the transformer is sufficient to charge C1 to V_{in} and discharge C2+C_{GSR2} from V_{in} to Vo, Q2 can achieve zero voltage turn-on.

In this transition, the leakage inductance resonates with C1 and C2 + C_{GSR2}. The equivalent circuit is shown in Fig. 23. If the voltage at point A can be discharged from Vin to Vo, the body diode of Q2 will be turned on. Q2 must be turned on before the current through the leakage inductance decreases to zero. The voltages across C1 and C2 can be calculated using (24)–(27). The leakage current I_{Leakage}, in (24) represents the current at the instant Q1 is turned off and can be estimated using (29), where Ip is the primary side current. From (24) it is observed that in order to achieve ZVS turn-on, (28) must be satisfied as

$$V_{C2}(t) = Z_o I_{\text{Leakage}} \sin \omega t - (V_{\text{in}} - V_o) \tag{24}$$

$$I_p(t) = I_{\text{Leakage}} \cos \omega t \tag{25}$$

$$V_{C1}(t) = Z_o I_{\text{Leakage}} \sin \omega t \tag{26}$$

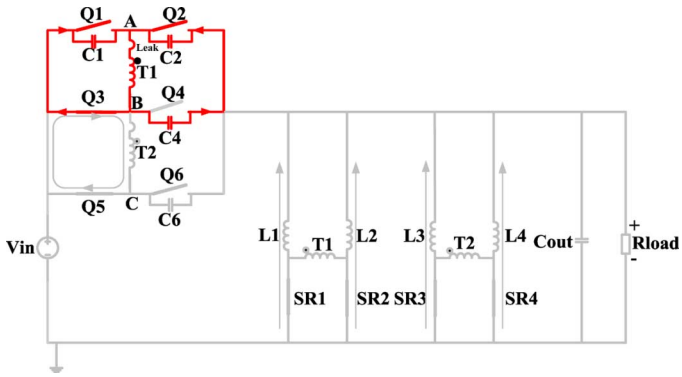

Fig. 23. Lagging leg transition equivalent circuit.

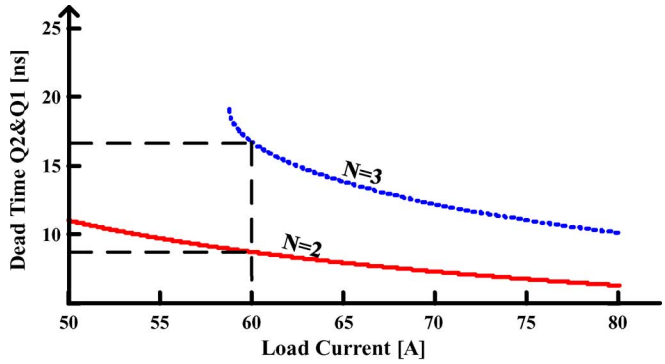

Fig. 24. Dead time between Q1&Q2 required for Q2 to achieve ZVS for the lagging leg as a function of load current.

$$Z_o = \sqrt{L_{\text{Leakage}}/2C_1}\ \omega = 1/\sqrt{2L_{\text{Leakage}}C_1}$$

$$t_X = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{\text{in}} - V_o}{Z_o}\right) \tag{27}$$

$$\begin{cases} Z_o I_{\text{Leakage}\,\min} > (V_{\text{in}} - V_o) \\ \frac{1}{\omega}\sin^{-1}\left(\frac{V_{\text{in}} - V_o}{Z_o I_{\text{Leakage}}}\right) < t_{\text{dead\_Q34}} \\ \quad < \frac{(I_{\text{Leakage}} L_{\text{Leakage}})\cos\omega t_X}{(V_{\text{in}} - V_o)} + t_X \end{cases} \tag{28}$$

$$I_{\text{Leakage}} = (I_o - I_{\text{in}})/4N. \tag{29}$$

Fig. 24 shows the minimum dead time required to achieve ZVS turn-on of the lagging leg transition between Q1 and Q2 as a function of the load. The curve is calculated using (28) with $V_{\text{in}} = 12$ V, $V_{\text{o}} = 1$ V, C1 = C2 = 2.5 nF (since the SR gate capacitor is paralleled with C2, it equivalently increases the value of C1 and C2), $L_{\text{Leakage}} = 30$ nH. Comparing the results shown in Fig. 22 with Fig. 24, it is observed that when the load current is less than 50 A, the lagging leg will lose ZVS turn-on when $N = 3$.

Based on the data shown in Fig. 24, to achieve ZVS turn-on at 60-A load for the lagging leg, $Td = 16.8$ ns for $N = 3$, and $Td = 8.7$ ns for $N = 2$.

VII. Loss Comparison Between Two Paralleled One-Phase NFB and the New Two-Phase NFB

In this section, the losses of two paralleled NFB converters and the new proposed two-phase NFB converter will be compared. It will demonstrate that the new proposed two-phase NFB has better efficiency. The comparison conditions are: $Vin = 12$ V, $Vo = 1$ V, $Iout = 80$ A, $Fs = 1$ MHz, $Np : Ns = 3 : 1$ primary side MOSFETs IFR7821 [14], SR IRF6619 [15]. The output inductor is 100-nH SMD inductor from ICE Components.

TABLE I
Current Stress Comparison Between Two NFB Converters and Two-Phase NFB Converter

Two-Phase NFB	Q1,Q2,Q5,Q6	Q3	Q4	Q7,Q8
Ipkoff	7.2A	7.2A	14.5A	Not needed
Ipkon	4.8A	4.8A	9.6A	Not needed
Vds	11V	11V	11V	Not needed
Fs	1MHz	1MHz	1MHz	Not needed
Two NFB Converters in Parallel	Q1,Q2,Q5,Q6	Q3	Q4	Q7,Q8
Ipkoff	7.2A	7.2A	7.2A	7.2A
Ipkon	4.8A	4.8A	4.8A	4.8A
Vds	11V	11V	11V	11V
Fs	1MHz	1MHz	1MHz	1MHz

A. Switching Loss

The switching loss can be calculated using (30) and (31). In a real circuit, the switching loss may be larger due to parasitic components [16]–[21], but using (30) and (31) still can be used to estimate the switching loss as follows:

$$P_{\text{on}} = \frac{1}{2} f_s V_{ds} I_{\text{PKon}} t_r \tag{30}$$

$$P_{\text{off}} = \frac{1}{2} f_s V_{ds} I_{\text{PKoff}} t_f. \tag{31}$$

Table I lists the current stress comparison between two paralleled one-phase NFBs and the two-phase NFB (the circulating current is neglected in the calculation). Form the table it is noticed that the current stress of Q4 is doubled compared with other MOSFETs. For Q3, since $\text{Iq3} = \text{Iq2} + \text{Iq6}$, and Iq2 and Iq6 are 120° out of phase, Q3 has the same peak current as Q1, Q2, Q5, and Q6.

Solely considering switching loss, the two-phase NFB saves one primary side MOSFET compared with two one-phase NFBs. The total switching loss of the two-phase NFB is seven times the switching loss of Q1; for the two parallel one-phase NFBs, the switching loss is eight times the switching loss of Q1.

If only four MOSFETs at the primary side and four SRs for the rectifier stage are used, compared with two paralleled one-phase NFBs, no switching loss could be saved since the current stress of the MOSFETs at primary side will be doubled.

If we assume the following. 1) $\text{Ton} = 10$ ns and $\text{Toff} = 15$ ns. 2) Lagging leg does no achieve ZVS. 3) Leading legs can achieve ZVS and recover 75% of the switching loss, the calculated results are: Two-phase NFB converter switching loss = 5.92 W, two paralleled NFB converters switching loss= 6.64 W. Therefore, 0.72 W loss is saved.

B. Conduction Loss

The conduction loss can be calculated using (32). Table II shows the RMS current comparison between two one-phase

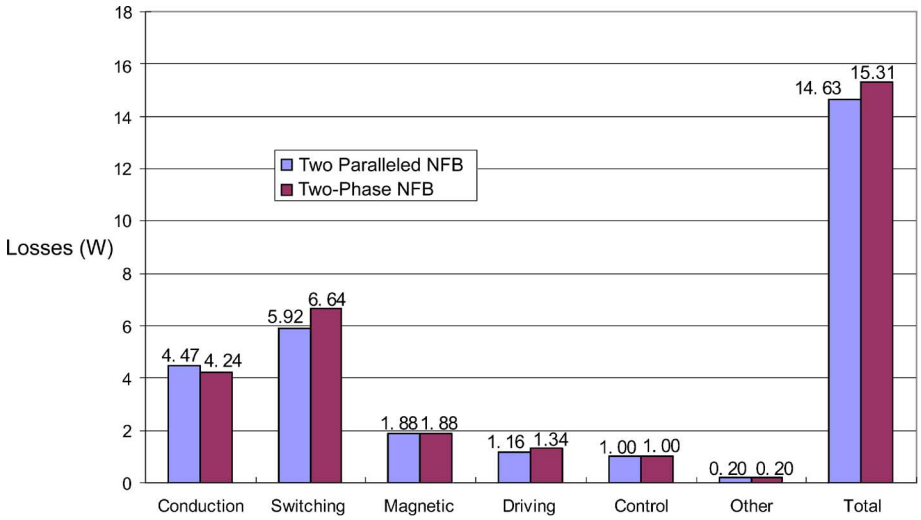

Fig. 25. Losses breakdown comparison between the two-phase NFB converter and two paralleled NFB converters at 1-MHz switching frequency and 1 V/80 A load.

TABLE II
RMS CURRENT COMPARISON BETWEEN TWO NFB CONVERTERS AND TWO-PHASE NFB CONVERTER

Two-Phase NFB	Q1,Q2,Q5,Q6	Q3	Q4	Q7,Q8	SR
I_{RMS}	3.6A	5.1A	7.2A	Not needed	22.4A
Two NFB Converters in Parallel	Q1,Q2,Q5,Q6	Q3	Q4	Q7,Q8	SR
I_{RMS}	3.6A	3.6A	3.6A	3.6A	22.4A

NFBs and the two-phase NFB. Q4's RMS current is doubled compared with Q1. Q3's RMS current is between Q1 and Q4; this benefit is achieved by phase shifting the current in Q2 and Q6 120 ° from each other.

$$P_{\rm con} = I_{\rm RMS} R_{\rm dson} \tag{32}$$

At the primary side, the two-phase NFB will result in more conduction loss since it has a higher RMS current. At the secondary side they will have the same conduction loss. The calculated total MOSFETs conduction losses are Two−phase NFB converter conduction loss $=$ 4.47 W, two paralleled NFB converters conduction loss$=$ 4.24 W. Therefore, there is an increase of 0.23-W conduction loss for the two-phase NFB from the primary side.

C. Gate Loss

The gate loss can be calculated using (33), assuming 50% of the gate loss from the SR can be saved as the self-drive circuit used in this design can recover some of the gate energy. Since the proposed two-phase NFB has fewer MOSFETs, it will have less gate loss. The calculated total MOSFETs gate loss: Two−phase NFB converter gate loss $=$ 1.16 W, two paralleled NFB converters gate loss $=$ 1.34 W. Therefore, 0.18-W gate loss is saved.

$$P_{\rm gate} = Q_g V_{gS} f_s. \tag{33}$$

D. Loss Summary

The loss breakdown comparison between the two-phase NFB converter and two paralleled NFB converters at 1 MHz switching frequency is shown in Fig. 25. It is observed that the total loss is reduced from 15.31 W (for two paralleled NFB converter) to 14.63 W (for two-phase NFB converter). 0.68 W loss is saved since fewer MOSFETs results in less gate loss and phase-shift control reduces the switching loss.

VIII. EXPERIMENTAL RESULTS

To verify the analysis in the previous sections, two prototypes were built on a 12-layer 2-oz copper PCB, one with four output inductors as shown in Fig. 2, the other with three output inductors as shown in Fig. 3. The primary MOSFET is the IRF7821, and four IRF6619s are used as synchronous MOSFETs. The design parameters are: $Vin = 12$ V, $Vo = 1$ V, $Fs = 1$ MHz, $Iout = 80$ A, $N = 3$, Lout is LP02 100-nH SMD inductor (from ICE Components).

Fig. 26 illustrates the leading leg transition of Q5 at 10 A, 1 MHz. It is observed that Vgs rises 16 ns after Vds reduces to zero, and ZVS turn-on is achieved.

Fig. 27 illustrates the lagging leg transition of Q6 at 50 A. From the testing results it is observed that ZVS turn-on is not achieved. The failure of ZVS turn-on occurs because the energy stored in the leakage inductance is limited and the SR's gate capacitor is paralleled with the output capacitors of lagging leg MOSFETs. This equivalently increases the output capacitance of the primary side MOSFETs, and makes it more difficult to fully discharge the output capacitors.

Fig. 28 illustrates the synchronous MOSFETs turn-on and turn-off transition at 80 A load. From the waveform it is observed that during the turn-on transition, the SR will be turned on before it begins to conduct current, thus the SR's body diode does not turn on during the turn-on transition.

Fig. 29 illustrates the gate signal of the synchronous MOSFETs. Each phase is 120° shifted from each other so the ripple current of the output inductor can cancel each other. Therefore,

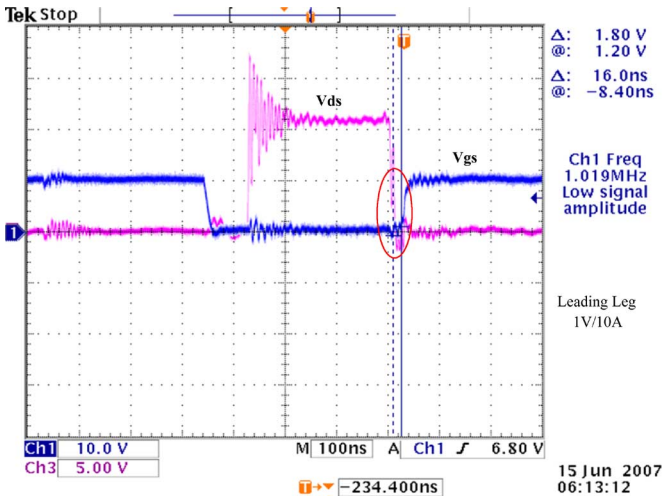

Fig. 26. Zero voltage turn-on of Leading Leg MOSFET Q5 at 10 A.

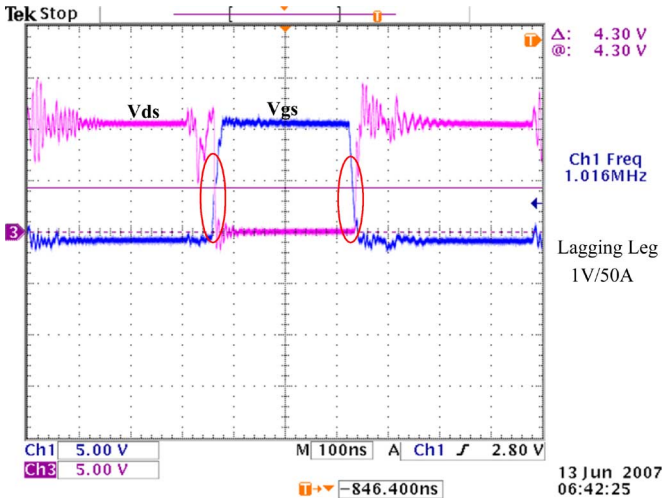

Fig. 27. Lagging leg MOSFET(Q6) switching transition at 50 A, fails to achieve ZVS.

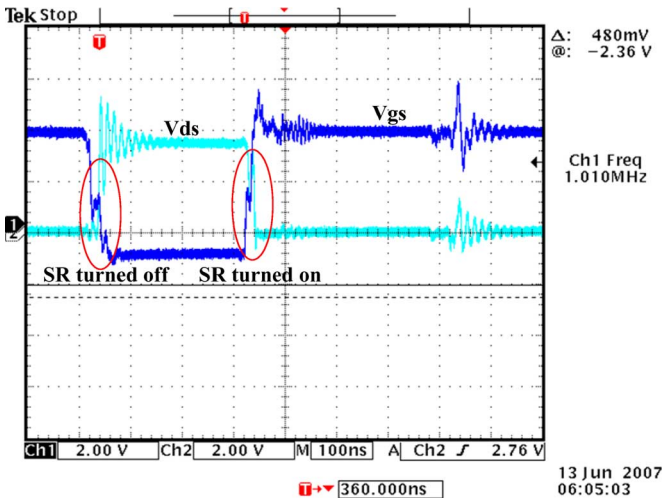

Fig. 28. Synchronous MOSFETs turn-on and turn-off transition at 80-A load.

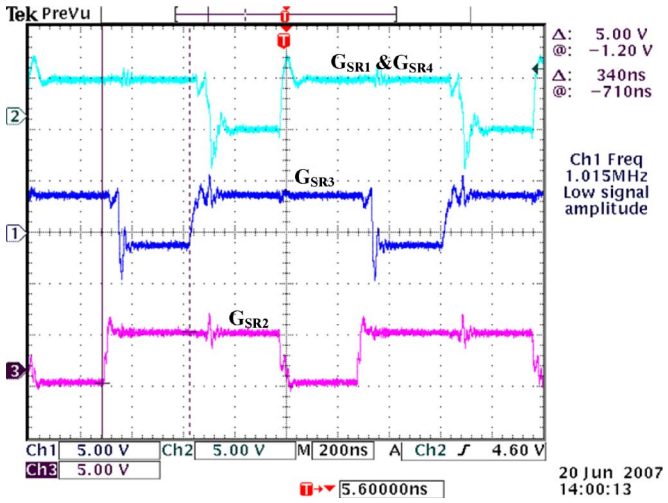

Fig. 29. Gate driving signal of synchronous MOSFETs phase shift 120° from each other.

a small output inductor can be used to improve dynamic performance. In the prototype, SR1 and SR4 are driven by the same driver, this is verified in the analysis in Section II.

Fig. 30 shows the measured efficiency curves of the two-phase NFB converter and two parallel NFB converters operating at 1-MHz switching frequency. At full load (1 V/80 A) the two-phase NFB converter achieves efficiency of 82.3% which is compared with 81.8% efficiency of the two paralleled NFB converters, thus a 0.5% improvement is achieved. At light load (1 V/10 A) a 4% efficiency improvement is achieved.

Another prototype with three inductors was also built and tested. It is observed from experimental results that when the number of inductors is reduced from four to three at full load (1 V/80 A) an efficiency of 82% is achieved. The efficiency is reduced by 0.3% because of the higher conduction loss from the output inductors, but the 82% efficiency is still better than two paralleled NFB converters (81.8%).

The experimental results demonstrate that the two-phase NFB converter is able to achieve better efficiency compared with two paralleled NFB converters, and with a simplified power train circuit and reduced cost.

A six-phase 1 V/80 A 1 MHz Buck was also tested with equivalent power MOSFETs. The six-phase buck is used in the comparison because a one-phase Buck reaches its peak efficiency at around 12-A load. If an 80-A output is required, a six-phase Buck will reach peak efficiency at around 80 A. From the experimental results the six-phase buck reaches a peak efficiency of 79.6% at 70 A, which is 2.7% lower than the peak efficiency of the two-phase NFB converter. Table III compares the number of major parts between the six-phase Buck, two paralleled NFB converters and the two-phase NFB converter. From the comparison it is shown that the two-phase NFB converter has the minimum number of components and the highest efficiency.

IX. Conclusion

Two new two-phase nonisolated full bridge converters are proposed as alternatives for parallel two nonisolated full bridge converters in this paper as shown in Figs. 2 and 3, respectively.

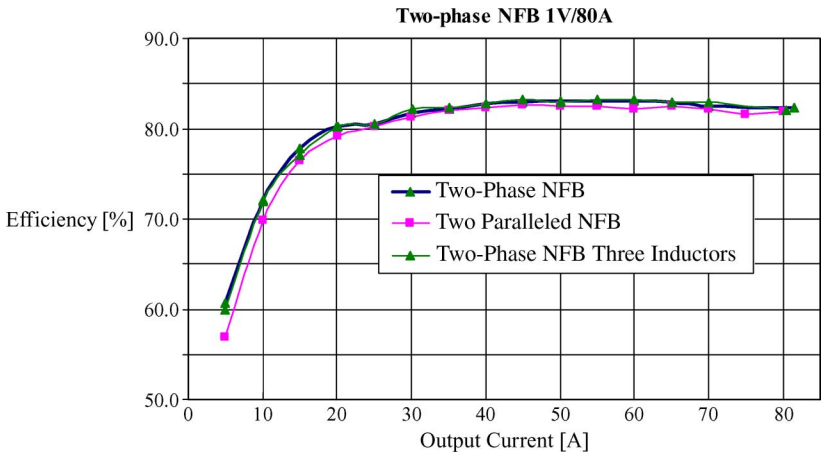

Fig. 30. Measured efficiency comparison between two-phase NFB converter and two paralleled NFB converters operate at 1-MHz switching frequency.

TABLE III
NUMBER OF MAJOR PARTS COMPARISON BETWEEN THE TWO-PHASE NFB CONVERTER, SIX-PHASE BUCK, AND TWO NFB CONVERTERS

	6 phase Buck	Two 1-phase NFBs	2-phase NFB
Total MOSFETs	12	12	10
Control MOSFETs	6	8	6
SR MOSFETs	6	4	4
Magnetics	6	6	6
Inductors	6	4	4
Transformers	0	2	2
Controllers	1	1	1
Drivers	6	4	3
Efficiency	Lowest	Medium	Highest
Cost	High	High	Low

Compared with two paralleled NFB converters, the two-phase NFB converter can handle the same output power. In addition, the number of MOSFETs at the primary side is reduced from eight to six. The power train is simplified and the cost is reduced. Moreover, higher efficiency can be achieved because of significant reduction of switching loss. To further reduce the cost, a further simplified two-phase NFB version is also proposed and tested. From the testing results, the efficiency is reduced slightly due to higher conduction loss, but the cost is further reduced.

The advantages of the new topology are summarized as follows.

1) Components cost is reduced. At the primary side, two MOSFETs are saved. At the secondary side, only three MOSFET drivers are needed to drive four SRs.
2) Better efficiency is achieved since fewer MOSFETs and phase shift control result in less switching loss and gate drive loss. In addition, ZVS turn-on can be achieved for all MOSFETs when phase-shift control is used.
3) Current sharing is simplified due to the sharing leg (Q3, Q4) which couples two power stages with each other.
4) Compared with the single phase topology [11], a smaller output capacitor and inductor can be used to improve dynamic performance, since the two-phase NFB converter can triple the frequency of the output ripple current. In addition, the output inductor current of the two-phase NFB converter has a phase shift 120° from each other, which also reduces the ripple current. And the method proposed in [22] can be used to further improve the dynamic performance.
5) Since SR1 and SR4 operate in parallel, the number of SRs and inductors can be reduced from four to three to further reduce the components cost with limited efficiency reduction.

To demonstrate the advantages of this topology, two VRM modules have been built and tested at 12-V input and 1-V output with an 80-A load and a 1-MHz switching frequency. The experimental results demonstrate that the two-phase NFB converter is able to achieve better efficiency with a simplified power train circuit and a reduced cost compared with two paralleled NFB converters. The two-phase NFB converter is also compared with a six-phase Buck, and the testing result demonstrates that the two-phase NFB converter can achieve better efficiency than the six-phase Buck and with less components.

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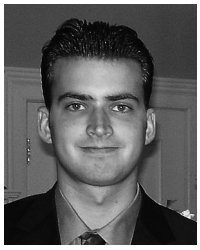

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