A Current Source Gate Driver Achieving Switching Loss Savings and Gate Energy Recovery at 1-MHz

Wilson Eberle, *Member, IEEE*, Zhiliang Zhang, *Student Member, IEEE*, Yan-Fei Liu, *Senior Member, IEEE*, and Paresh C. Sen, *Fellow, IEEE*

***Abstract*—In this paper, a new current source gate drive circuit is proposed for power MOSFETs. The proposed circuit achieves quick turn on and turn off transition times to reduce switching loss and conduction loss in power MOSFETs. In addition, it can recover a portion of the CV^2 gate energy normally dissipated in a conventional driver. The circuit consists of four controlled switches and a small inductor (typically 100 nH or less). The current through the inductor is discontinuous in order to minimize circulating current conduction loss. This also allows the driver to operate effectively over a wide range of duty cycles with constant peak current—a significant advantage for many applications since turn on and turn off times do not vary with the operating point. Experimental results are presented for the proposed driver operating in a boost converter at 1 MHz, 5 V input, 10 V/5 A output. At 5 V gate drive, a 2.9% efficiency improvement is achieved representing a loss savings of 24.8% in comparison to a conventional driver.**

***Index Terms*—Metal oxide semiconductor field effect transistor (MOSFET), root mean square (RMS), zero voltage switching (ZVS).**

I. Introduction

In recent years there has been a trend to increase the switching frequency beyond 1 MHz [1], [2] in low voltage high current dc–dc power supplies. The objectives of this trend are to increase the power density by decreasing the size of passive components and to improve the dynamic performance. Furthermore, it is well understood that as switching frequency increases, both switching loss and gate loss increase. In the past two decades, much work has been done on reducing, or eliminating turn on switching loss through soft switching techniques. However, in general, these techniques require additional components [3]–[5] and require snubber capacitors to reduce turn off loss. Unfortunately, adding snubber capacitors to reduce turn off loss, makes achieving zero voltage switching (ZVS) at turn on more challenging for all line and load conditions. Furthermore, these techniques do not reduce gate loss. Therefore, with some improvements achieved through reduction in turn on switching loss, it is now essential to focus some effort on reducing turn off switching loss and gate loss in order to continue to achieve greater power density and dynamic performance.

A conventional gate drive circuit is illustrated in Fig. 1 to drive a power metal oxide semiconductor field effect transistor (MOSFET), M. Its associated waveforms are given in Fig. 2. With these drivers, all of the power MOSFET gate energy is dissipated. Energy is absorbed from the line source, V_{cc} during the turn on of M and then dumped to ground during turn off. Examining Fig. 2, it is clear that the line current, i_{Vcc} only contains a positive component and therefore, since there is no negative component, there is no energy returned to the line.

For the conventional driver, the gate energy loss due to charging and discharging the gate capacitance of M is given by (1), where Q_g represents the total gate charge, V_{cc} is the driving voltage and f_s is the switching frequency

$$P_g = Q_g V_{cc} f_s. \tag{1}$$

The gate energy is dissipated as RMS loss in: 1) the driver switches S_N and S_P, 2) the external resistance, R_{ext}, and 3) the MOSFET internal gate mesh resistance, R_g, of M. This loss component is well understood and is often called the CV^2 gate loss. In addition to the CV^2 loss, conventional gate drivers exhibit switching loss, shoot-through loss and gate loss in their switches. These losses are often neglected by engineers, providing an underestimate of the total drive loss. It was demonstrated in [6] that the power MOSFET CV^2 RMS loss is approximately only 66.7% (170 mW) of the total gate drive circuit loss. The additional components of the gate drive circuit loss include approximately 17.6% (45 mW) for switching loss and 15.7% for gate loss (40 mW) in the driver switches. As illustrated in Fig. 3, normalized with respect to the CV^2 RMS gate loss, these components are significant. An additional 26% of loss can be attributed to hard switching in the driver switches and 24% to gate loss in the driver switches. Neglecting these components yields an under estimate of gate loss that neglects an additional 50% of the total gate circuit loss.

The problems of the conventional gate driver extend beyond the gate drive circuit loss. There are two other significant problems.

1) Since these drivers operate with voltage source RC type charging and discharging, switching speed is limited. The MOSFET gate current is limited to a value significantly less than the peak driver current during the turn on and turn off times which occur during the plateau and threshold regions of the MOSFET gate-to-source voltage. This effect is clearly illustrated in Fig. 2, where the drive current at turn on and turn off decays significantly. During the

Manuscript received May 11, 2007; revised September 26, 2007. The paper was presented in part at APEC'06. Recommended for publication by Associate Editor Y. C. Liang.

The authors are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6 Canada (e-mail: wilson.eberle@ece.queensu.ca; zhiliang.zhang@queensu.com; yanfei.liu@queensu.ca; senp@post.queensu.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2007.915769

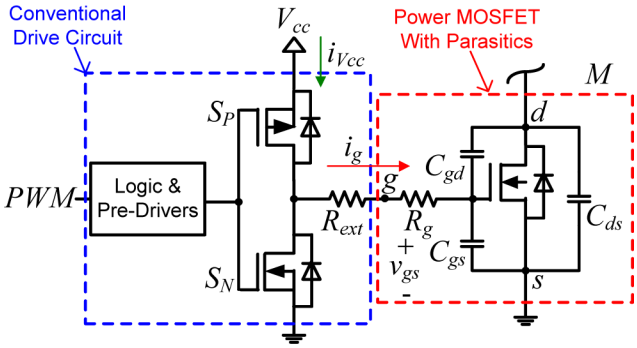


Fig. 1. Conventional gate drive circuit with power MOSFET and its associated parasitics.

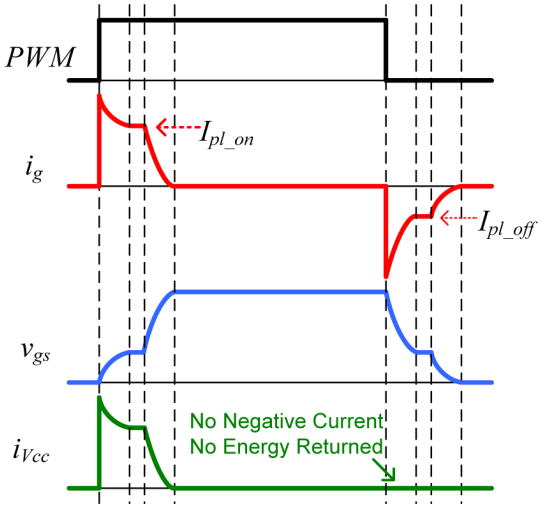


Fig. 2. Power MOSFET gate drive waveforms with conventional gate drive.

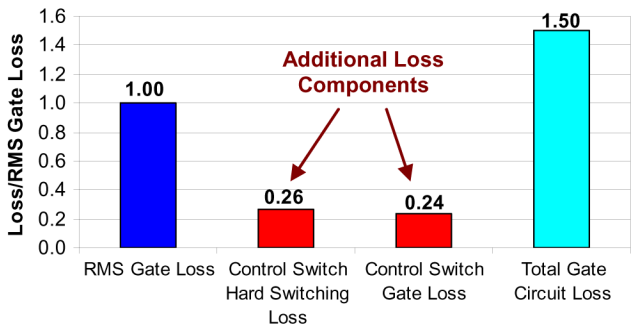


Fig. 3. Conventional gate drive circuit loss normalized with respect the power MOSFET CV^2 gate loss.

turn on switching time from the threshold to the end of the Miller plateau, the gate current decays to I_{pl_on}. During the turn off switching time, the problem is even more severe since the gate current decays to I_{pl_off}. Some conventional drivers attempt to overcome this problem with BJT driver switches operating as current sources in the active region, however, due to the limited gains of the devices, they do not behave as ideal current sources.

2) A second significant problem is that these drivers typically have a large source impedance (e.g., several Ωs), so the gate drive voltage often does not reach the driver supply voltage, V_{cc} when the MOSFET is turned on. This leads to greater conduction loss since the MOSFET $R_{\rm dson}$ decreases with increasing gate voltage. This effect is illustrated in Fig. 4, where it is clear that the MOFET gate voltage never reaches the driver supply voltage of 5 V. Furthermore, the very large source impedance leads to very slow turn on and therefore high turn on switching loss.

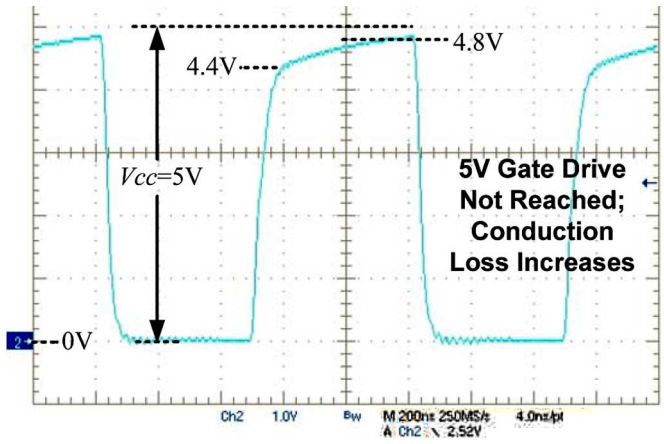


Fig. 4. Typical MOSFET gate voltage waveform illustrating that the gate voltage amplitude does not reach the control voltage of 5 V leading to increased conduction loss; UCC37322 driving IRF6618 at 1 MHz (Y-axis: 1 V/div, X-axis: 200 ns/div).

For these two reasons, conventional gate drivers are not optimized to minimize switching loss or conduction loss.

From a gate energy perspective, in order to recover a portion of the gate energy otherwise lost in conventional drivers, several papers have been published since the early 1990s proposing resonant gate drive techniques. In most of these techniques, the inductance is used to resonate with the gate capacitance for charging, so switching speed is limited. Of the methods previously proposed, all of them suffer from at least one of six problems.

1) High circulating current in the driver switches during the power MOSFET on and off states resulting in excessive conduction loss [7]–[12].
2) Peak driver current dependent on duty cycle, or switching frequency resulting in switching times that vary with the operating point [7]–[12].
3) High transient current in the driver switches during transients due to the DC energy storage in the blocking capacitance [7]–[12].
4) Large inductance [7]–[10], bulky transformer, or coupled inductor [11], [12], [15]–[18], [20].
5) Slow turn on and/or turn off transition times, which increases both conduction and switching losses in the power MOSFET due to charging the power MOSFET gate beginning at zero inductor current [13]–[23].
6) The inability to actively clamp the power MOSFET gate to the line during the on time and/or to ground during the off time, which can lead to undesired false triggering of the power MOSFET gate, i.e., lack of *Cdv/dt* immunity [14]–[21], [23].

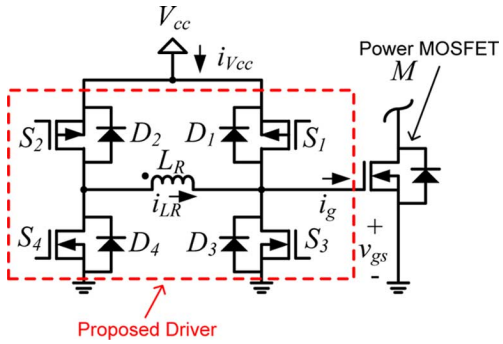


Fig. 5. Proposed current source gate drive circuit.

To solve the problems inherent to conventional drivers, the five problems above, and to reduce switching loss, a new current source gate drive circuit is proposed in the following section. The driver achieves the two main requirements of a good driver cited in the conclusion of [24], namely current source drive during transitions to achieve high speed drive and operate as a low impedance voltage source during the on and off states to minimize false triggering. The proposed driver is suitable for ground referenced drive applications and is best suited for applications in which there is natural limitation of the voltage across the power MOSFET at turn off (e.g., the boost converter) [25].

II. Proposed Current Source Gate Driver

The proposed current source gate driver is illustrated in Fig. 5. It consists of four controlled switches, $S_1 - S_4 (S_1, S_2$ p-channel and S_3, S_4 n-channel) including their body diodes, $D_1 - D_4$, and a small inductance, L_R. The switches are controlled and diodes are used to allow the inductor current to be discontinuous and allow the power MOSFET to turn on or off beginning from a non-zero pre-charge current. Following charging, or discharging of the power MOSFET, the excess inductor stored energy is allowed to return to the supply voltage, V_{cc}, thereby allowing ideally 100% of the power MOSFET gate charge energy to be recovered.

The gating waveforms of the four driver switches, $S_1 - S_4$, along with the inductor current, gate current, power MOSFET gate-to-source voltage and the line current are illustrated in Fig. 6. The key waveforms to note are: 1) the inductor current, labeled i_{LR}, which is discontinuous to minimize conduction loss, 2) the gate current, labeled i_g, which remains approximately constant (in comparison to the conventional voltage source drivers), although slightly increasing during the turn on and turn off transitions, and 3) the line current, i_{Vcc}, which contains negative intervals, indicating that energy is returned to the line. The operation of the circuit is explained in the following paragraphs.

Initially it is assumed that the power MOSFET is in the off state before time t_0. The on states are indicated in Fig. 6 for the driver switches and diodes. Initially, before t_0, only switch S_3 and D_4 are on and the gate of M is clamped to zero volts. The current paths during the intervals of the turn on stage are illustrated in Fig. 7(a)–(e). It is noted that M has been replaced by its equivalent total gate capacitance, C_g.

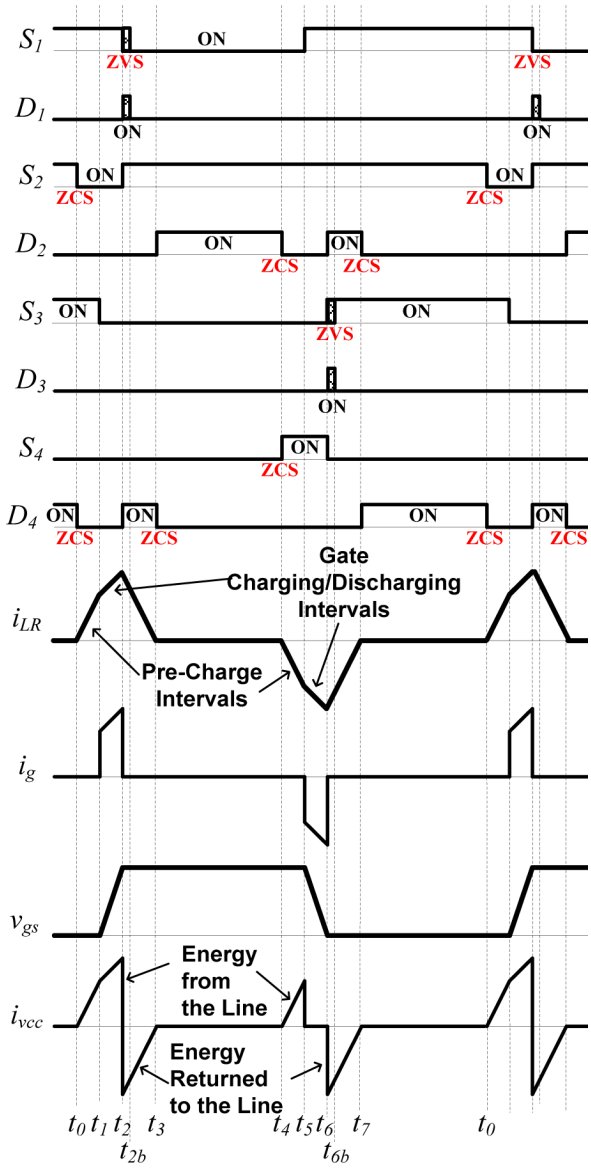


Fig. 6. Waveforms of the proposed current source gate driver.

$t_0 - t_1$: At t_0, S_2 turns on (with ZCS) turning off D_4 by commutation with zero current switching (ZCS) and allowing the inductor current to ramp up as illustrated in Fig. 7(a). The current path during this interval is $S_2 - L_R - S_3$. Since S_3 is in the on state, the gate of M is clamped low. This interval is the inductor current pre-charge interval and it ends at time t_1, which is a pre-determined time set by the user.

$t_1 - t_2$: At t_1, S_3 is turned off, which allows the inductor current to begin to charge the power MOSFET gate as illustrated in Fig. 7(b). The inductor current continues to ramp up from the pre-charged level, but with a reduced slope as the voltage across the gate capacitance increases. The current path during this interval is $S_2 - L_R - C_g$. This interval ends at t_2, when v_{gs} reaches V_{cc}.

$t_2 - t_3$: At t_2, D_1 is driven on and S_2 is turned off, therefore driving D_4 on to allow the inductor current to continue to conduct into the dot through the path $D_4 - L_R - D_1$ as illustrated in Fig. 7(c). This interval continues for a short dura-

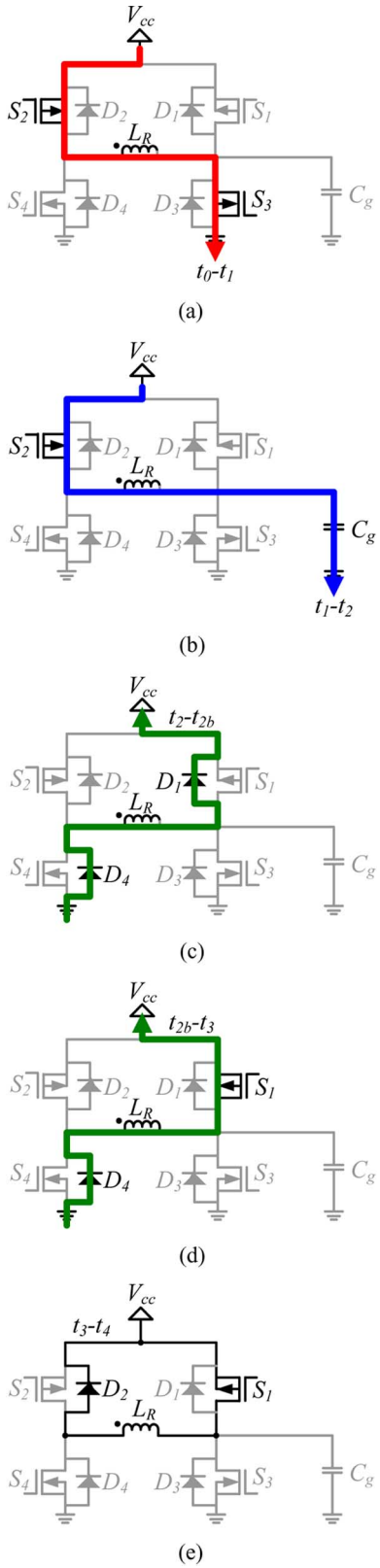


Fig. 7. Turn on operating intervals of the proposed current source gate driver.

tion until t_{2b}, when S_1 is turned on (with ZVS) as illustrated in Fig. 7(d). Most importantly, it is during this interval when the stored energy in the inductor is returned to the line. This can be observed from the negative portion of the i_{Vcc} curve in Fig. 6. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero. During this interval, the gate voltage of M remains clamped to the line voltage, V_{cc}. The interval ends when the inductor current reaches zero at t_3.

$t_3 - t_4$: At t_3, D_4 turns off (with ZCS) and D_2 turns on, which clamps the driver supply voltage across both inductor terminals as illustrated in Fig. 7(e). During this interval, the gate voltage of M remains clamped to V_{cc}. The interval ends at t_4 when the pre-charging interval for the turn off cycle begins as dictated by the PWM signal.

The current paths during the intervals of the turn off stage are illustrated in Fig. 8(a)–(e).

$t_4 - t_5$: At t_4, the turn off inductor pre-charging interval begins as illustrated in Fig. 8(a). S_4 is turned on (with ZCS) therefore turning off D_2 by commutation (with ZCS). Since S_1 was previously on, the inductor current begins to ramp negative out of the dot through the path $S_1 - L_R - S_4$. During this interval, the gate voltage of M remains clamped to V_{cc}. The interval ends at t_5.

$t_5 - t_6$: At t_5, S_1 is turned off, which allows the inductor current to begin to discharge the power MOSFET gate as illustrated in Fig. 8(b). The inductor current continues to ramp negative from the pre-charged level, but with a reduced slope as the voltage across the gate capacitance decreases. The current path during this interval is $C_g - L_R - S_4$, where C_g represents the equivalent gate capacitance of M. This interval ends at t_6, when v_{gs} reaches zero.

$t_6 - t_7$: At t_6, D_3 is driven on and S_4 is turned off, therefore driving D_2 on to allow the inductor current to conduct out of the dot through the path $D_3 - L_R - D_2$ as illustrated in Fig. 8(c). This interval continues for a short duration until t_{6b}, when S_3 is turned on (with ZVS) as illustrated in Fig. 8(d). Most importantly, it is during this interval when the gate discharging energy is returned to V_{cc}. This can be observed from the negative portion of the i_{Vcc} curve in Fig. 6. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down positive towards zero. During this interval, the gate voltage of M remains clamped to ground. The interval ends when the inductor current reaches zero at t_7.

$t_7 - t_0$: At t_7, D_2 turns off (with ZCS) and D_4 turns on, which clamps both inductor terminals to ground as illustrated in Fig. 8(e). During this interval, the gate voltage of M remains clamped to ground. The interval ends at t_0 when the pre-charging interval for the turn on cycle begins and the entire process repeats as dictated by the PWM signal.

There are several benefits of the proposed current source driver.

1) It behaves as a current source, which enables quick switching and reduced switching loss (Section III).
2) The driver inductance is very small (Section IV).
3) The driver has the potential to recover gate energy (Sections V and VI).
4) The peak current is independent of duty cycle and frequency, so it is suitable for different types of control and wide operating conditions (Section VIII).

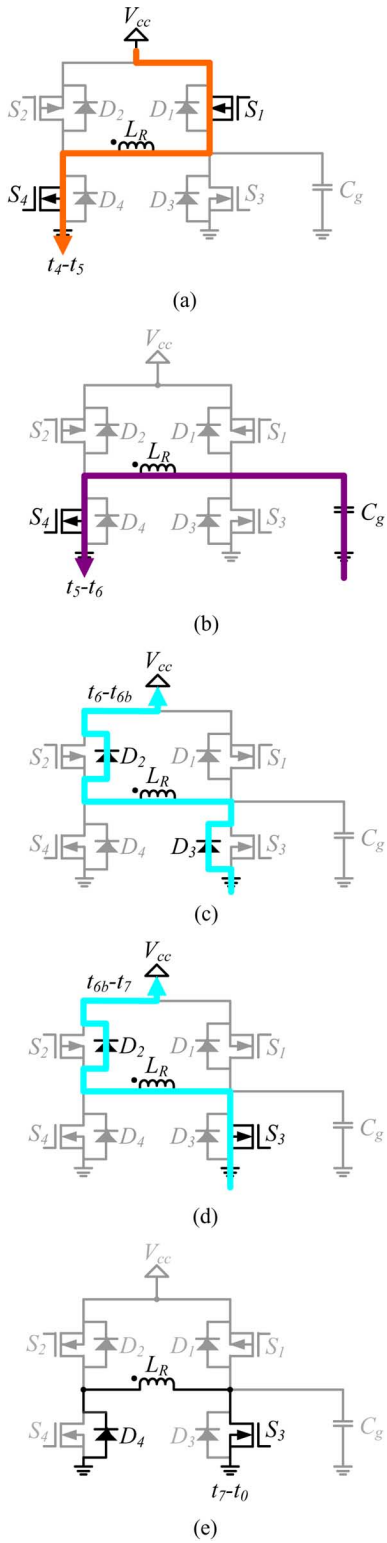


Fig. 8. Turn off operating intervals of the proposed current source gate driver.

5) The inductor current is discontinuous, minimizing circulating current, so conductions losses in the driver are minimized (Section II).
6) The driver switches operate with soft switching (Section II).

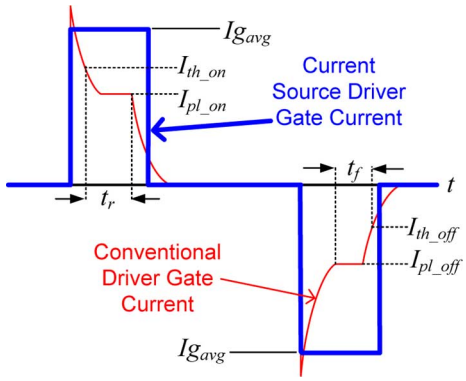


Fig. 9. Comparison between the gate current waveform shapes for the conventional driver and an ideal current source driver.

III. Switching Loss Savings

The potential for gate loss energy recovery was presented in the previous section. This section elaborates on the potential for switching loss energy savings by faster switching with a current source driver. In hard switched converters, the actual potential total switching loss savings can be much more significant than the gate loss savings. This statement can hold true for most soft switching converters, since zero voltage switching converters typically only eliminate turn on loss, or with the addition of snubber capacitors, they are not able to maintain zero voltage switching across varying line and load conditions.

In hard switching converters, neglecting any body diode reverse recovery and drain and common source inductance, the turn on switching loss can be approximated by (2), and the turn off switching loss by (3), where V_{ds} represents the voltage across the switch. In (2), I_{onpk}, represents the peak current through the switch at turn on and t_r represents the rise time. In (3), I_{offpk} represents the peak current through the switch at turn off and t_f represents the fall time. Since both t_r and t_f are both inversely proportional to the average gate current, $Ig_{\rm avg}$, it is clear that switching losses can be reduced by increasing gate current. However, in conventional gate drivers, this is generally not possible since the peak current is already limited by the current handling capability of the driver switches

$$P_{\rm on} = \frac{1}{2} f_s V_{ds} I_{onpk} t_r \tag{2}$$

$$P_{\rm off} = \frac{1}{2} f_s V_{ds} I_{offpk} t_f. \tag{3}$$

In the conventional driver, the gate current decays significantly from its peak value due to the RC type charging and discharging. On the other hand, the proposed current source gate driver behaves like a nearly constant current source and the gate current actually increases slightly during the rise and fall times as illustrated in Fig. 9 where it is clear that the magnitude of $Ig_{\rm avg}$ is greater than $I_{pl\_{\rm on}}$ and $I_{pl\_{\rm off}}$, respectively. The result is that the turn on and turn off times decrease significantly and more importantly, the rise and fall times decrease significantly, which decreases switching loss.

For a conventional gate driver, the turn on switching loss, $P_{\rm on\_conv}$, is given by (4). In (4), $I_{\rm th\_on}$ represents the gate current when the gate voltage is at the threshold and is given by

(5). Also in (4), I_{pl_on} represents the gate current when the gate voltage is at the plateau and is given by (6). Other parameters noted include the power MOSFET total gate charge at the beginning of the plateau, Q_{pl}, the total gate charge at the threshold, $Q_{\rm th}$, the gate-to-drain charge, $Q_{\rm gd}$, the source impedance of the driver, R_P, the sink impedance of the driver, R_N, the MOSFET internal gate resistance, R_g, the MOSFET plateau voltage, V_{pl} and the external gate resistance in the drive circuit, $R_{\rm ext}$

$$P_{\rm on\_conv} = \frac{1}{2} f_s V_{ds} I_{onpk} \left(\frac{Q_{pl} - Q_{\rm th}}{\frac{1}{2}(I_{\rm th\_on} + I_{pl\_on})} + \frac{Q_{\rm gd}}{I_{pl\_on}} \right) \tag{4}$$

$$I_{\rm th\_on} = \frac{V_{cc} - V_{\rm th}}{R_P + R_{\rm ext} + R_g} \tag{5}$$

$$I_{pl\_on} = \frac{V_{cc} - V_{pl}}{R_P + R_{\rm ext} + R_g}. \tag{6}$$

In addition, for a conventional gate driver, the turn off switching loss, $P_{\rm off\_conv}$, is given by (7). In (7), $I_{\rm th\_off}$ represents the gate current when the gate voltage is at the threshold and is given by (8). Also in (7), I_{pl_off} represents the gate current when the gate voltage is at the plateau and is given by (9)

$$P_{\rm off\_conv} = \frac{1}{2} f_s V_{ds} I_{offpk} \left(\frac{Q_{pl} - Q_{\rm th}}{\frac{1}{2}|I_{\rm th\_off} + I_{pl\_off}|} + \frac{Q_{\rm gd}}{|I_{pl\_off}|} \right) \tag{7}$$

$$I_{\rm th\_off} = \frac{V_{\rm th}}{R_N + R_{\rm ext} + R_g} \tag{8}$$

$$I_{pl\_off} = \frac{V_{pl}}{R_N + R_{\rm ext} + R_g}. \tag{9}$$

With an ideal current source driver with constant gate current, the turn on, $P_{\rm on\_csd}$, and turn off $P_{\rm off\_csd}$, switching loss are given by (10) and (11), respectively

$$P_{\rm on\_csd} = \frac{1}{2} f_s V_{ds} I_{onpk} \frac{Q_{pl} - Q_{\rm th} + Q_{\rm gd}}{Ig_{\rm avg}} \tag{10}$$

$$P_{\rm off\_csd} = \frac{1}{2} f_s V_{ds} I_{offpk} \frac{Q_{pl} - Q_{\rm th} + Q_{\rm gd}}{|Ig_{\rm avg}|}. \tag{11}$$

To demonstrate the potential switching loss savings with a current source driver, a boost converter example is used. Circuit parameters are listed in Table I.

Equations (4)(11) are used to calculate the switching loss for the conventional driver and an ideal current source driver. To validate the results, the boost converter illustrated in Fig. 10 was simulated with SIMetrix. Waveforms of the conventional driver are given in Fig. 11 and for the current source driver age given in Fig. 12. The results are summarized and a comparison is given in Table II. $P_{\rm tot\_sw}$ represents the sum of the turn on and turn off switching loss.

The results in Table II demonstrate that a current source driver can reduce switching loss significantly. There is also good agreement between the theoretical calculated results and the simulated results. In the example given, the rise time is reduced from 48 ns to 19 ns and the fall time is reduced from 23 ns to 18 ns. The turn on loss is reduced by 1.05 W (from 2.62 W to 1.01 W) and the turn off loss is reduced by 0.22 W

TABLE I
CIRCUIT PARAMETERS FOR SWITCHING LOSS CALCULATION COMPARISON

Converter Topology	**Boost**
Gate Drive Voltage, V_{cc}	5V
MOSFET Turn On Current, I_{onpk}	10A
MOSFET Turn Off Current, I_{offpk}	12A
External Impedance, R_{ext}	1Ω
MOSFET	**IRF6618**
Q_{gd}	12nC
Q_{th}	8nC
Q_{pl}	15nC
V_{th}	1.64V
V_{pl}	3V
R_g	1Ω
Conventional Driver	**UCC37322**
Source Impedance, R_P	2.5Ω
Sink Impedance, R_N	1.1Ω
Current Source Driver	
Ig_{avg}	1.25A

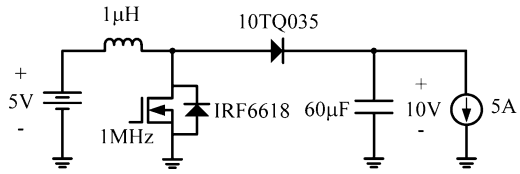


Fig. 10. Boost converter circuit used in simulation.

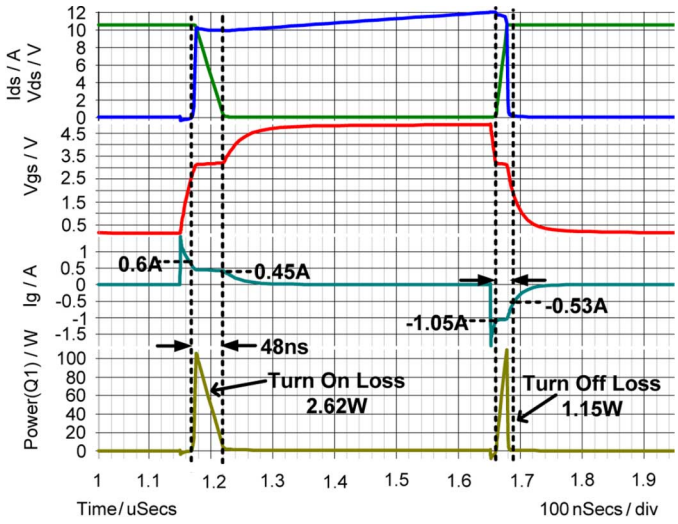


Fig. 11. Boost converter MOSFET switching loss waveforms for the conventional driver; top: drain voltage and current, second: gate-source voltage, third: gate current, bottom: power loss.

(from 1.15 W to 0.96 W). Therefore, the total switching loss is reduced by 1.8 W (from 3.77 W to 1.97 W)—a significant savings.

IV. CURRENT SOURCE DRIVER DESIGN PROCEDURE

The power MOSFET turn on transition time, $T_{\rm on}$, (from 0 V to V_{cc}), or average gate current, $Ig_{\rm avg}$, must be chosen by the designer for the given application. For the designer, there is a tradeoff between speed, which translates into switching loss savings, or reduced body diode conduction, and gate energy recovery. Increased gate current (smaller values of $T_{\rm on}$) results

TABLE II
CIRCUIT PARAMETERS FOR SWITCHING LOSS CALCULATION COMPARISON

	Conventional Driver (Conv) Calculated	Conventional Driver (Conv) Simulated	Current Source Driver (CSD) Calculated	Current Source Driver (CSD) Simulated	Switching Loss Savings with CSD (Conv-CSD) Calculated	Switching Loss Savings with CSD (Conv-CSD) Simulated
I_{th_on}	0.67A	0.60A	-	-	-	-
I_{pl_on}	0.44A	0.45A	-	-	-	-
I_{th_off}	-0.65A	-0.53A	-	-	-	-
I_{pl_off}	-0.97A	-1.05A	-	-	-	-
Ig_{avg}	-	-	+/-1.25A	+/-1.25A	-	-
t_r	40ns	48ns	15ns	19ns	-	-
t_f	25ns	23ns	15ns	18ns	-	-
P_{on}	**1.98W**	**2.62W**	**0.76W**	**1.01W**	**0.83W**	**1.05W**
P_{off}	**1.56W**	**1.15W**	**0.95W**	**0.96W**	**0.46W**	**0.22W**
P_{tot_sw}	**3.54W**	**3.77W**	**1.71W**	**1.97W**	**1.83W**	**1.8W**

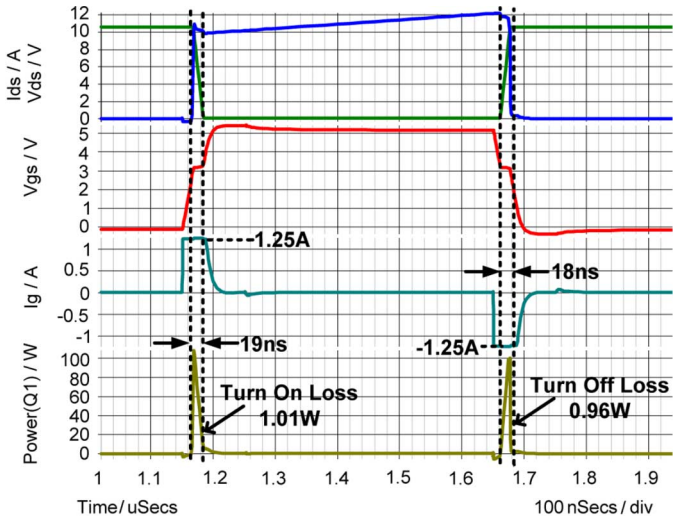


Fig. 12. Boost converter MOSFET switching loss waveforms for an ideal current source driver; top: drain voltage and current, second: gate-source voltage, third: gate current, bottom: power loss.

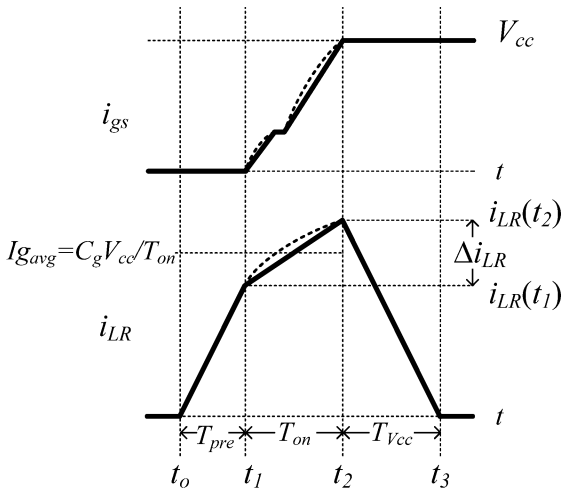


Fig. 13. Detailed inductor current waveform and power MOSFET gate voltage during the turn on interval.

in greater conduction loss in the driver. Typically, $T_{\rm on}$ should be less than 10% of the switching period. After selecting $T_{\rm on}$, the turn on inductor pre-charge time, $T_{\rm pre}$ should be selected. This is illustrated in Fig. 13 from $t_0 - t_1$, of the inductor current waveform during the turn on interval. Typically, $T_{\rm pre}$ should be less than $T_{\rm on}$. Larger values of $T_{\rm pre}$ yield a larger required inductance and add more delay in the control loop. On the other hand, if $T_{\rm pre}$ is too small, the gate energy recovery is limited, or the pre-charge current level is small. The optimized value of $T_{\rm pre}$ is typically half of $T_{\rm on}$.

In order to calculate the required current source inductance, (12)–(14), must be used. Equation (12) is derived assuming that there is no resistive loss in the drive circuit during $T_{\rm pre}$

$$L_R = \frac{V_{cc} T_{\rm pre}}{i_{LR}(t_1)}. \tag{12}$$

Equation (13) is derived using an approximation. The equivalent circuit during $T_{\rm on}$ is an under damped RLC circuit with initial inductor current, which is complex to solve. However, since the power MOSFET gate capacitor voltage increases from zero to V_{cc} during $T_{\rm on}$, then the average capacitor voltage during the interval is $V_{cc}/2$. Using this approximation, the ripple current component, $\Delta i_{\ LR}$, is approximated as

$$\Delta i_{LR} = \frac{V_{cc}}{2} \frac{T_{\rm on}}{L_R}. \tag{13}$$

The current at time t_1 is then approximated by

$$i_{LR}(t_1) = Ig_{\rm avg} - \frac{\Delta i_{LR}}{2}. \tag{14}$$

Using (12)–(14), the required inductance can be calculated using

$$L_R = \frac{V_{cc} T_{\rm on}}{Q_g} \left(\frac{T_{\rm on}}{4} + T_{\rm pre} \right). \tag{15}$$

In summary, the current source driver can be designed as follows.

1) Select $T_{\rm on}$.
2) Set $T_{\rm pre}$ at $T_{\rm on}/2$.
3) Calculate the required driver inductance, L_R, using (15).

V. DRIVER LOSS COMPONENTS

The loss components of the proposed current source gate drive circuit are outlined in the following sub sections.

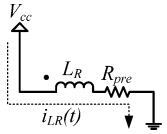


Fig. 14. Equivalent circuit during the turn on pre-charge interval.

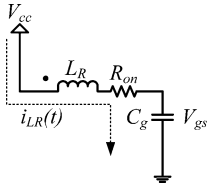


Fig. 15. Equivalent circuit during the turn on interval.

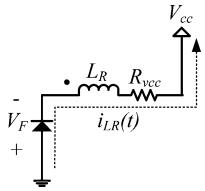


Fig. 16. Equivalent circuit after turn on when the energy stored in the inductor is returned to the line.

A. Conduction Loss

This sub-section will focus on the conduction loss in the driver switches. The power MOSFET being driven is represented by an RC network consisting of its parasitic series gate resistance, R_g, and an equivalent gate capacitance, C_g using total gate charge data from the device datasheet. During the on state, the driver switches can be represented by series resistances $R_1 - R_4$. The inductor copper loss can be represented by an equivalent series ac resistance, R_L.

The conduction loss can be determined by analyzing the losses during the three main states of the turn on interval $(t_0 - t_3)$ and three states of the turn off interval $(t_4 - t_7)$ when the inductor current is non-zero. The detailed inductor current waveform and power MOSFET gate voltage waveform are shown for the turn on interval in Fig. 13. Using a piecewise linear approximation to simplify the analysis, the inductor current waveform can be approximated using the dotted portion during $T_{\rm on}$, if it is assumed that the gate is driven by a constant current source of value $Ig_{\rm avg}$ during $T_{\rm on}$. The analysis of the turn on intervals is explained as follows.

$T_{\rm pre}$: The equivalent circuit during $T_{\rm pre}$ is given in Fig. 14, where R_2, R_L and R_3 have been lumped together as R_{pre} (i.e., $R_{\rm pre} = R_2 + R_L + R_3$). The inductor current, $i_{LR}(t)$, is given by (16). Since the series resistance $R_{\rm pre}$ is quite small, the time constant is large relative to the transition interval, so (16) can be approximated by (17). Using the approximation, the RMS current during this interval is given by (18) and the power consumption, $P_{\rm pre}$, during the interval is given by (19)

$$i_{LR}(t) = \frac{V_{cc}}{R_{\rm pre}}\left(1 - e^{-\frac{R_{\rm pre}}{L_R}t}\right) \tag{16}$$

$$i_{LR}(t) = \frac{V_{cc}}{L_R}t \tag{17}$$

$$i_{\rm pre\_RMS} = i_{LR}(t_1)\sqrt{\frac{T_{\rm pre}f_s}{3}} \tag{18}$$

$$P_{\rm pre} = \frac{1}{3}i_{LR}(t_1)^2 T_{\rm pre} f_s R_{td1}. \tag{19}$$

The pre-charge time interval can be derived as

$$T_{\rm pre} = \frac{L_R}{V_{cc}}i_{LR}(t_1). \tag{20}$$

$T_{\rm on}$: The equivalent circuit during $T_{\rm on}$ is given in Fig. 15. The circuit is a series RLC circuit consisting of R_2, R_L, R_g, L_R and C_g, where R_2, R_L and R_g have been lumped together as R_{on} (i.e., $R_{\rm on} = R_2 + R_L + R_g$). Using the piecewise linear approximation illustrated in Fig. 13, the RMS current during $T_{\rm on}$ is given by (21), shown at the bottom of the page, and the power consumption, $P_{\rm on}$, during the interval is given by (22), shown at the bottom of the page.

T_{Vcc} : The equivalent circuit during T_{Vcc} is given in Fig. 16, where R_L and R_1 have been lumped together as R_{Vcc} (i.e., $R_{Vcc} = R_1 + R_L$) and the diode voltage drop is considered constant at V_F. The inductor current, $i_{LR}(t)$, is given by (23). Since the series resistance R_{Vcc} is quite small, the time constant is large relative to the transition interval, so (25) can be approximated by (24). Using the approximation, the RMS current during this interval is given by (25) and the power consumption, P_{Vcc}, during the interval is given by (26), which simplifies to (27)

$$i_{LR}(t) = i_{LR}(t_2) - \frac{V_{cc} - V_F}{R_{Vcc}}\left(1 - e^{-\frac{R_{Vcc}}{L_R}t}\right) \tag{23}$$

$$i_{LR}(t) = i_{LR}(t_2) - \frac{V_{cc} - V_F}{L_R}t \tag{24}$$

$$i_{vcc\_\rm RMS} = i_{LR}(t_2)\sqrt{\frac{T_{Vcc}f_s}{3}} \tag{25}$$

$$P_{Vcc} = i_{LR}(t_2)^2\frac{T_{Vcc}f_s}{3}R_{Vcc} + f_s V_F\int_{t_2}^{t_3}\left(i_{LR}(t_2) - \frac{V_{cc} - V_F}{L_R}t\right)dt \tag{26}$$

$$i_{\rm on\_RMS} = \sqrt{T_{\rm on}f_s}\sqrt{\left[\frac{i_{LR}(t_2) + i_{LR}(t_1)}{2}\right]^2 + \frac{[i_{LR}(t_2) - i_{LR}(t_1)]^2}{12}} \tag{21}$$

$$P_{\rm on} = T_{\rm on}f_s\left(Ig_{\rm avg}^2 + \frac{\Delta i_{LR}^2}{12}\right)R_{\rm on}. \tag{22}$$

$$P_{Vcc} = \frac{1}{3} i_{LR}(t_2)^2 T_{Vcc} f_s R_{Vcc} + \frac{1}{2} V_F i_{LR}(t_2) T_{Vcc} f_s. \quad (27)$$

The time interval T_{Vcc} can be expressed by (28) and $i_{LR}(t_2)$ can be expressed by (29)

$$T_{Vcc} = \frac{L_R}{V_{cc} + V_F} i_{LR}(t_2) \quad (28)$$

$$i_{LR}(t_2) = I_{\text{avg}} + \frac{\Delta i_{LR}}{2}. \quad (29)$$

To simplify the analysis, it can be assumed that the turn on and turn off states of operation are identical. Therefore, under this assumption, the total conduction loss in the proposed current source gate drive circuit is two times the sum of P_{pre} plus P_{on} plus P_{Vcc} as given by

$$P_{\text{cond}} = 2(P_{\text{pre}} + P_{\text{on}} + P_{vcc}). \quad (30)$$

B. Gate Loss

The gate loss in $S_1 - S_4$ is given by

$$P_{S1-S4\text{gate}} = (Q_{g1} + Q_{g2} + Q_{g3} + Q_{g4}) V_{cc} f_s. \quad (31)$$

C. CV^2 Output Loss

The CV^2 output loss in S_2 and S_4 at turn on, is given by (32) where C_{oss2} and C_{oss4} represent the output capacitance values for S_2 and S_4 obtained from the MOSFET data sheets

$$P_{\text{out}} = 1/2(C_{\text{oss2}} + C_{\text{oss4}}) V_{cc}^2 f_s. \quad (32)$$

D. Turn Off Loss

S_2 and S_4 turn off at the peak inductor current, $i_{LR}(t2)$. The turn off loss in S_2 and S_4 is given by (33) where the fall times, t_{f2} and t_{f4} are obtained from the MOSFET data sheets

$$P_{\text{off}} = \frac{1}{2} V_{cc} i_{LR}(t_2)(t_{f2} + t_{f1}) f_s. \quad (33)$$

E. Core Loss

The core loss can be obtained by standard core loss estimation methods and should be small in comparison to the other loss components. If air core inductors are used, the core loss is zero.

F. Logic Loss

The loss in the logic circuit should be negligible in comparison to the other components, so it can be neglected.

VI. Design Example

A design and loss analysis of the proposed driver was conducted using the design procedure presented in Section IV and the loss analysis presented in Section V. The parameters for the design are given in Table III. A turn on time, T_{on}, of 50 ns, was selected along with a pre-charge time, T_{pre}, of 25 ns. Using these values, the calculated driver inductance is 208 nH. A loss breakdown of the proposed driver is given in Fig. 17 using (16)–(33). The results are compared to the estimated loss in a conventional driver using (1) at 1.5 times the CV^2 loss as explained in Section I, Fig. 3. It is noted that the losses in the conventional driver are 67% greater than those in the proposed current source driver.

The largest loss component in the proposed current source driver is conduction loss and the largest portion of the conduction loss is dissipated in the power MOSFET parasitic gate resistance, R_g. A curve of current source driver loss as a function of R_g are given in Fig. 18 in order to demonstrate the potential benefits of using MOSFETS with lower internal gate resistance.

TABLE III
Current Source Driver Design Parameters

Switching Frequency	1MHz	
Gate Drive Voltage, V_{cc}	5V	
Turn On Time, T_{on}	50ns	
Pre-charge Time, T_{pre}	25ns	
Energy Return Time, T_{Vcc}	50ns	
Driver Inductor, L_R	208nH	
Inductor Ripple Current, ΔI_{LR}	0.6A	
Driver Inductor Resistance, R_L	25mΩ	
MOSFET, *M*	**IRF6618**	
Total Gate Charge, Q_g	45nC	
Internal Gate Resistance, R_g	1Ω	
Diodes, D_2 & D_4	**MBR0520**	
Diode Forward Voltage, V_F	0.385V	
Current Source Driver Switches, S_1-S_4	**NDS351AN (S_3 & S_4)**	**FDN342P (S_1 & S_2)**
Total Gate Charge, Q_g	1.25nC	6nC
On Resistance, R_{dson}	90mΩ	60mΩ
Output Capacitance, C_{oss}	50pF	200pF
Fall Time, t_f	1ns	2ns

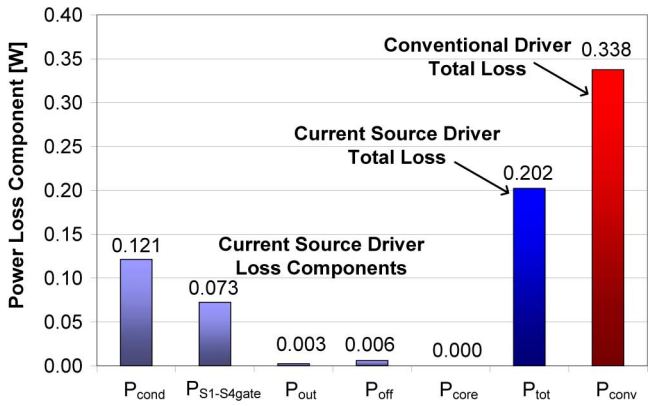


Fig. 17. Proposed current source driver gate drive loss breakdown with comparison of total losses to total loss in a conventional driver circuit.

VII. Logic Implementation

The logic required to produce the gating signals for the four driver switches, $S_1 - S_4$ is very simple. The waveforms used to derive the logic are illustrated in Fig. 19. The logic circuit is illustrated in Fig. 20. The circuit requires only two delay elements

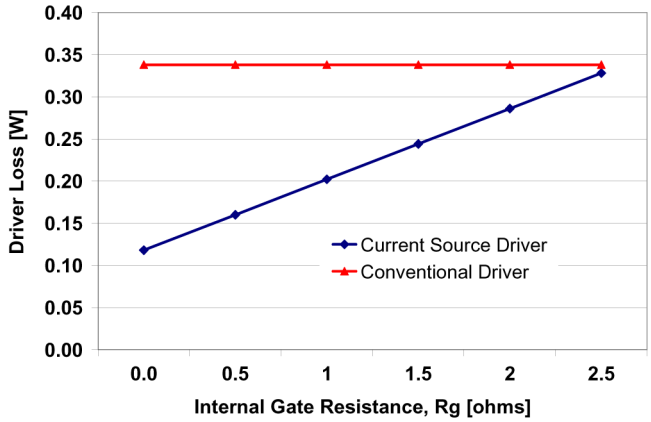


Fig. 18. Current source driver loss as a function of MOSFET gate resistance.

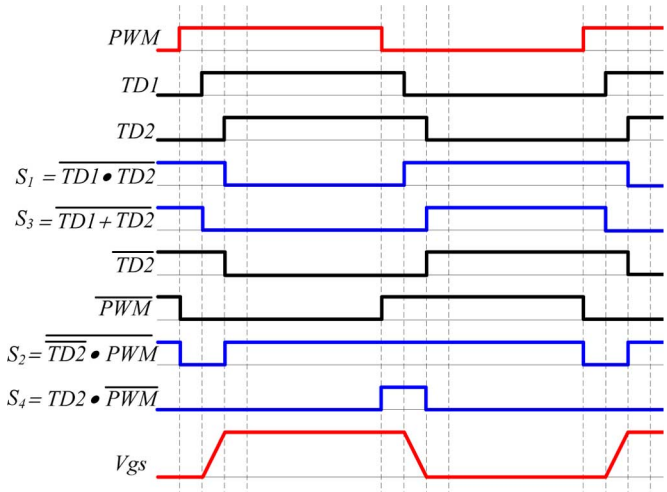


Fig. 19. Logic waveforms.

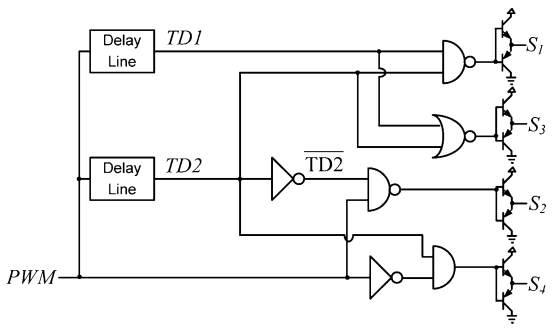


Fig. 20. Logic circuit.

and six logic elements. The delay elements can be implemented using tapped delay line ICs. The output of the logic circuit is the four gate drive signals. Following the logic, BJT pre-drivers are used to drive the four switches.

VIII. Experimental Results

A. Driver and Circuit Parameters

The proposed current source driver was built using discrete components and compared to the Texas Instruments UCC37322 state of the art driver using the boost converter topology operating at 1 MHz. The UCC37322 driver contains parallel bipolar and MOSFET driver switches and can deliver peak gate currents up to 9 A at 14 V drive. The boost converter and its input/output specifications were chosen as a simple, ground referenced drive, single switch, test application in order to demonstrate the capabilities of the proposed current source driver. All specifications for the boost converter are the same as given in Section III, Table I. In addition, an International Rectifier 10TQ035 schottky diode was used in the boost converter. The output capacitance consists of six 10 μF, 16 V, 1206 ceramic capacitors. A six-layer, 1.5 oz. PCB was used for both prototypes. A photo illustrating both prototypes is given in Fig. 21. The boost converter with current source driver is on the left and the boost converter with conventional driver, UCC37322, is on the right. It is noted that the circuit area occupied by the proposed driver is much larger than the conventional driver. However, for practical implementation and wide spread use, complete semiconductor integration of the proposed driver would reduce its size significantly.

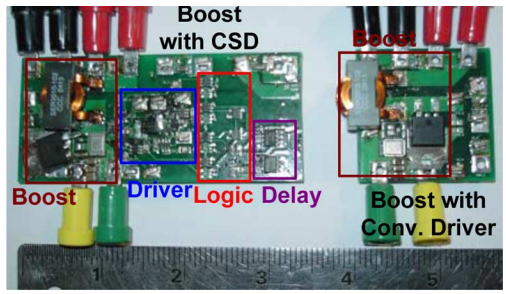


Fig. 21. Photo of the proposed current source driver (CSD) in a boost converter topology (left) and the boost converter with UCC37322 driver (right; UCC37322 driver on other side of board).

The current source driver was designed to deliver 1.25 A average gate charging current to the IRF6618 gate in order to demonstrate the switching loss savings discussed in Section III. In order to do so, a turn on time of approximately 40 ns ($T_{\rm on} = Q_g/Ig_{\rm avg} = 45$ nC/1.25 A $= 36$ ns) was selected with a pre-charge time of 20 ns. Dallas Semiconductor DS1100 tapped delay lines were used to implement the delay times. Fairchild UHS series discrete logic components were used to implement the logic. Fairchild FMBT3646 BJT pair pre-drivers were used to drive the CSD driver switches, $S_1 - S_4$. A 100 nH Coilcraft 1812SMS-R10L air core inductor was used for the driver inductance, L_R. Fairchild NDS351AN n-channel MOSFETs were used for S_3 and S_4. Fairchild FDN342P p-channel MOSFETs were used for S_1 and S_2.

B. Driver Operation

Waveforms for the proposed current source driver are given in Fig. 22. The waveforms are given for one-cycle of operation at 1 MHz. The four driver gate signals are given along with the gate-source voltage of the IRF6618 MOSFET and the driver inductor current. All waveforms agree with the theory. Most notably, the pre-charge intervals and turn on/off intervals are demonstrated by the gating signals and inductor current shape. Note that the S_1 and S_2 switches are p-channel MOSFETs, so

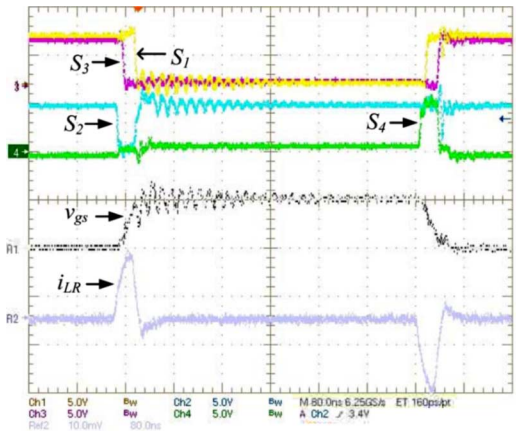


Fig. 22. Current source driver waveforms; top: S_1 and S_3 gate signals (5 V/div, 200 ns/div), second: S_2 and S_4 gate signals (5 V/div), third: IRF6618 gate-source voltage (5 V/div), bottom: inductor current (1 A/div).

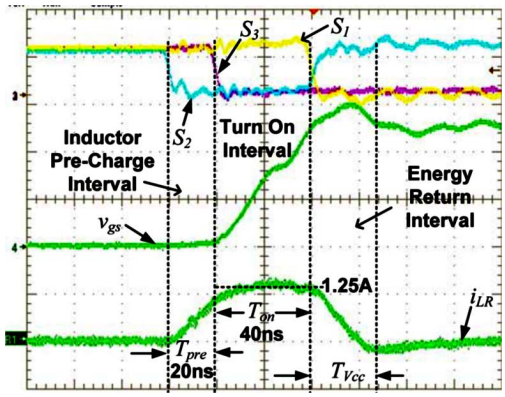


Fig. 23. Detailed turn on waveforms; top: gate signals for S_1, S_2 and S_3 (5 V/div, 20 ns/div), second: IRF6618 gate-source voltage (2 V/div), bottom: CSD inductor current (1 A/div).

they are active low. The inductor current is discontinuous as expected.

Detailed waveforms of the turn on transition are provided in Fig. 23. The three control signals for S_1, S_2 and S_3 are at the top (S_4 not shown remains off for the entire turn on transition). The middle waveform is the IRF6618 gate voltage and the bottom waveform is the driver inductor current. The turn on of S_2 (active low) initiates the turn on inductor pre-charge interval where the inductor current ramps up during the pre-charge time. After the designed 20 ns, S_3 turns off allowing the inductor continue to continue to ramp up at a decreasing rate while at the same time charging the gate of the IRF6618 power MOSFET during $T_{\rm on}$. During this interval the average drive current is approximately 1.25 A and the power MOSFET voltage charges from 0 V to $V_{cc} = 5$ V. After 40 ns, the gate is clamped high when S_1 (active low) turns on. After S_1 turns on, the inductor current ramps back down to zero while the inductor energy is returned to V_{cc}.

Detailed waveforms of the turn off transition are provided in Fig. 24. The three control signals for S_1, S_3 and S_4 are at the top (S_2 not shown remains off for the entire turn on transition). The middle waveform is the IRF6618 gate voltage and the bottom

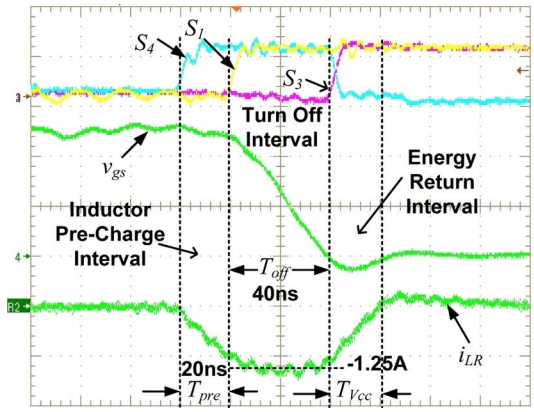


Fig. 24. Detailed turn off waveforms; top: gate signals for S_1, S_3 and S_4 (5 V/div, 20 ns/div), second: IRF6618 gate-source voltage (2 V/div), bottom: CSD inductor current (1 A/div).

waveform is the driver inductor current. The turn on of S_4 initiates the turn off inductor pre-charge interval, allowing the inductor current to ramp negative. After the designed 20 ns, S_1 turns off (active low) allowing the inductor continue to continue to ramp negative at a decreasing rate while at the same time discharging the gate of the IRF6618 power MOSFET. During this interval the average drive current is approximately -1.25 A and the power MOSFET voltage discharges from $V_{cc} = 5$ V to 0 V. After 40 ns, the gate is clamped low when S_3 turns on. After S_3 turns on, the inductor current ramps back down to zero while the inductor energy is returned to V_{cc}.

C. Boost Converter Efficiency and Losses

The efficiency and total loss curves (driver and boost converter powertrain) for the proposed current source driver and UCC37322 are given in Figs. 25 and 26, respectively. The current source driver maintains greater efficiency and lower power loss across the entire load range. Furthermore, the efficiency improvement at full load is 2.9%, representing a total power loss savings of 1.85 W. It is noted that the loss savings of 1.85 W is very close to the 1.8 W predicted and simulated in Section III. The conduction loss savings with the proposed driver is estimated to be 18 mW assuming an $R_{\rm dson}$ of 3 m Ω at 5 V gate drive for the proposed driver and an $R_{\rm dson}$ of 3.3 m Ω at an effective drive voltage of 4.6 V for the UCC37322 driver.

A curve of loss savings with the current source driver with respect to the conventional driver is given in Fig. 27. It is noted that the proposed driver enables the boost converter to operate with 24.8% less loss at full load than the conventional driver. For many applications, this loss savings could potentially lead to significant cost savings in components, heat sinks, or cooling.

D. Driver Losses

The proposed driver was tested at other turn on times of 20 ns, 50 ns, 80 ns, 110 ns, and 140 ns. There is a design tradeoff for the proposed driver between speed and driver loss. Greater switching speed (smaller turn on time) requires greater driver current, which increases conduction loss in the driver. On the other hand, an added benefit is that as turn on time decreases,

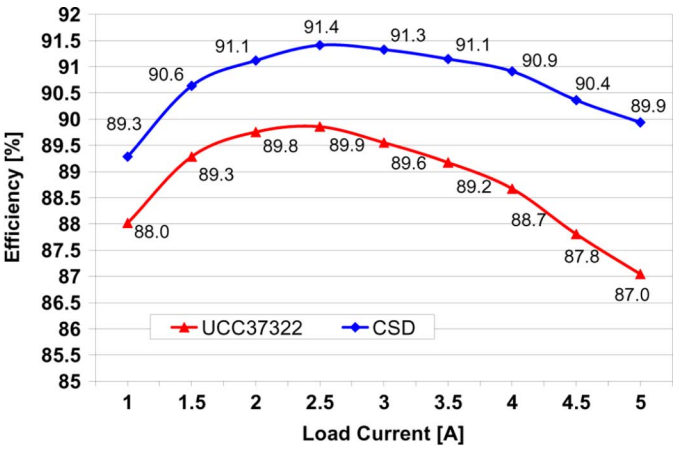


Fig. 25. Efficiency curves as a function of load for the boost converter with proposed current source driver and UCC37322 driver operating at 1 MHz, 5 V input and 10 V output; NOTE: 2.9% efficiency improvement at full load.

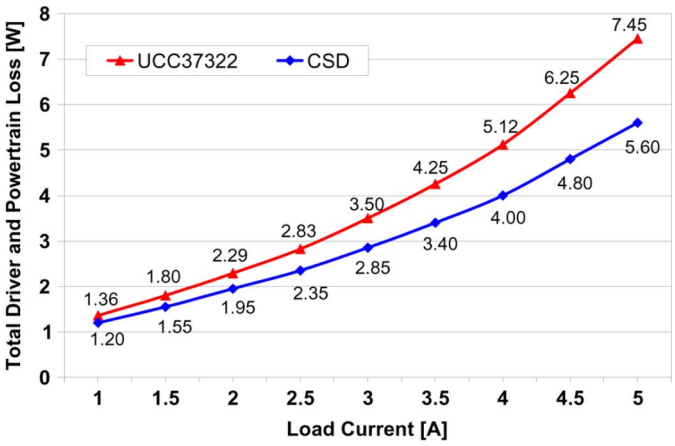


Fig. 26. Total loss curves as a function of load for the boost converter with proposed current source driver and UCC37322 driver operating at 1 MHz, 5 V, input and 10 V output; NOTE: 2.9% efficiency improvement achieved at full load.

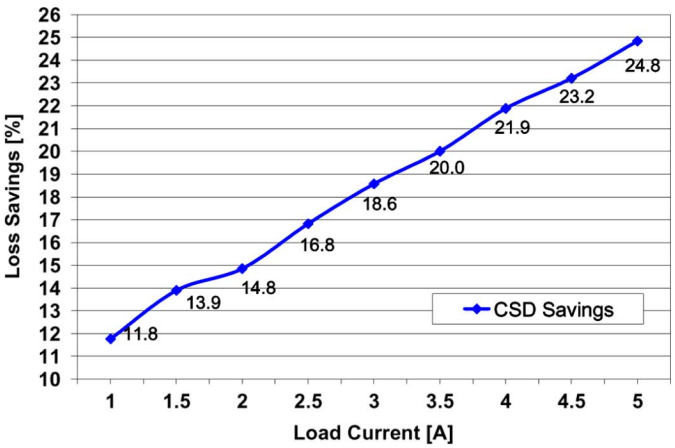


Fig. 27. Loss savings as a function of load current for the boost converter with proposed current source driver with respect to the UCC37322 driver operating at 1 MHz, 5 V input and 10 V output.

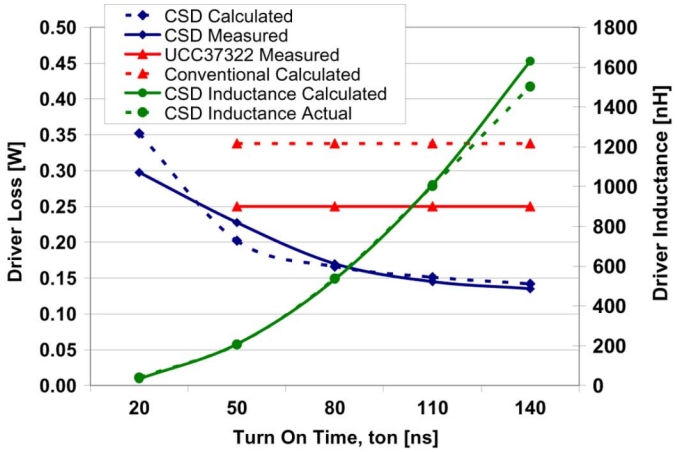


Fig. 28. Curves of driver loss and current source driver inductance as a function of turn on time.

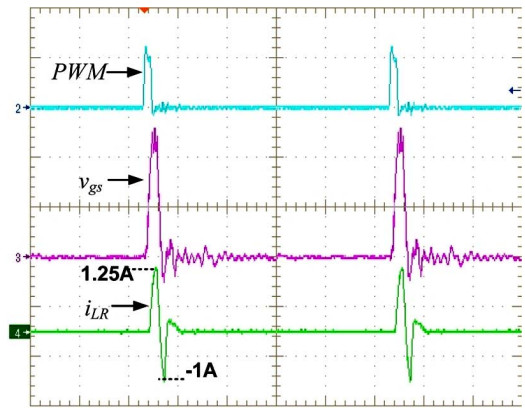


Fig. 29. Current source driver waveforms at 3% duty cycle; top: PWM signal (5 V/div, 200 ns/div), second: IRF6618 gate-source voltage (2 V/div), bottom: driver inductor current (1 A/div).

the required driver inductance also decreases. Curves of the proposed driver loss and required inductance are given as a function of turn on time, $T_{\rm on}$, in Fig. 28. Curves of the actual measured driver loss and actual inductance used are also included. It is noted that the proposed driver operates with lower driving loss than the UCC37322 for all turn on times achievable with the UCC37322 driver. While the driving loss savings is small (50–100 mW for the example given), in other applications at higher switching frequencies, or with multiple switches, the potential for gate energy savings can become a significant.

E. Range of Duty Cycle Operation

The proposed current source driver operates correctly for duty cycles ranging from 0%–100%. Driver waveforms at 3% duty cycle are given in Fig. 29. The top waveform is the PWM signal. The second waveform is the IRF6618 gate-source voltage and the bottom waveform is the driver inductor current. The peak inductor current during turn on is 1.25 A as expected. However, at turn off the peak inductor current is −1 A. The lower peak inductor current at narrow duty cycles is expected since the turn on energy recovery time, T_{Vcc} and the turn off pre-charge time, $T_{\rm pre}$ overlap. This overlap causes the turn off time to be slightly slower than expected. However, if the power MOSFET gate is

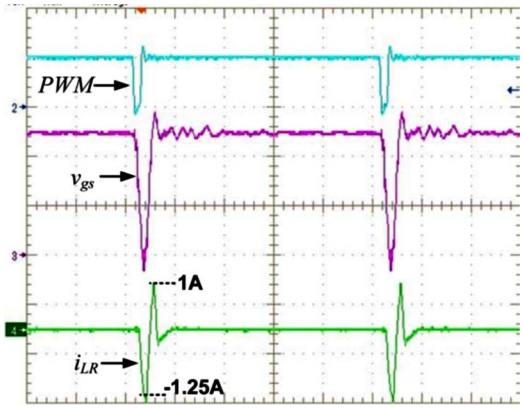


Fig. 30. Current source driver waveforms at 97% duty cycle; top: PWM signal (5 V/div, 200 ns/div), second: IRF6618 gate-source voltage (2 V/div), bottom: driver inductor current (1 A/div).

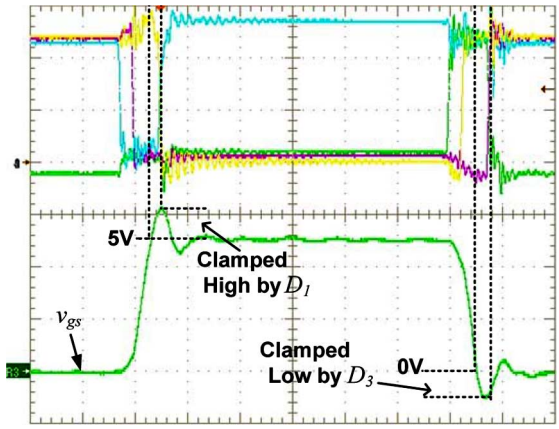


Fig. 31. (Current source driver waveforms illustrating the effect of an undersized inductor; top: gate signals for $S_1 - S_4$ 2 V/div, 80 ns/div), bottom: IRF6618 gate-source voltage (2 V/div.)

not fully discharged by the inductor current after $T_{\rm off}$, it quickly discharges to ground when S_3 turns on. It is also noted that when the PWM input duty cycle is 0%, the power MOSFET gate-source voltage remains clamped at 0 V.

Driver waveforms at 97% duty cycle are given in Fig. 30. The top waveform is the PWM signal. The second waveform is the IRF6618 gate-source voltage and the bottom waveform is the driver inductor current. In contrast to the 3% duty cycle example, the peak inductor current during turn off is -1.25 A as expected and the peak inductor current at turn on is 1 A. At wide duty cycles, the turn off energy recovery time, T_{Vcc} and the turn on pre-charge time, $T_{\rm pre}$ overlap resulting in the turn on time to be slightly slower than expected. However, if the power MOSFET gate is not fully charged by the inductor current after $T_{\rm on}$, it quickly charges to V_{cc} when S_1 turns on.

F. Driver Inductor Tolerance

The most significant benefit of the proposed current source driver is that it operates as a current source to drive the power MOSFET during the turn on and turn off times. However, another significant benefit is that during the remainder of the switching period, the driver behaves like a conventional driver with the power MOSFET gate clamped high, or low by the driver switches. This complementary behavior of the driver switches makes the driver very robust.

One common issue in implementation is inductor tolerance. Inductors typically have tolerances of $\pm 20\%$ or more. In the proposed driver, if the inductor is undersized, the power MOSFET gate will charge and discharge quicker than expected. If the gate voltage reaches the supply rails during the dead time between S_1 and S_3, then the body diodes of S_1 and S_3 clamp the voltage high at turn on and low at turn off. This is illustrated in Fig. 31, where the 100 nH inductance was replaced by a 40 nH inductance. The smaller inductance yields greater inductor current, allowing the gate capacitance to charge/discharge quicker and reach the supply rail before S_1 turns on at turn on and before S_3 turns off at turn off. At turn on, the gate voltage is briefly clamped to approximately 1 V above V_{cc} by D_1. At turn off, the gate voltage is briefly clamped to approximately -1 V by D_3.

The examples in Figs. 29 and 30 demonstrate similar behaviour to when the inductor is above tolerance. In this case, the inductor current is lower than expected when S_1, or S_3 turn on, so the additional gate charge is supplied from the line, or discharged to ground through S_1, or S_3 when they turn on.

IX. Conclusion

A new current source gate drive circuit has been proposed for power MOSFETs. The proposed circuit achieves quick turn on and turn off transition times to reduce switching loss and conduction loss in power MOSFETS. In addition, it can recover a portion of the CV^2 gate energy normally dissipated in a conventional driver. The circuit consists of four controlled switches and a small inductor (100 nH or less, typical). The current through the inductor is discontinuous in order to minimize circulating current conduction loss in the driver. This also allows the driver to operate effectively over a wide range of duty cycles with constant peak current—a significant advantage for many applications since turn on and turn off times do not vary with the operating point. The driver provides superior performance in comparison to conventional drivers and solves the problems of existing resonant gate drivers. Experimental results have been presented for the proposed driver operating in a boost converter at 1 MHz, 5 V input, 10 V/5 A output. At 5 V gate drive, a 2.9% efficiency improvement is achieved representing a loss savings of 24.8% in comparison to a conventional driver.

References

[1] X. Xu, A. Khambadkone, T. M. Leong, and R. Oruganti, "A 1-MHz zero-voltage-switching asymmetrical half-bridge dc/dc converter: Analysis and design," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 105–113, Jan. 2006.

[2] A. M. Abou-Alfotouh, A. Radun, H. R. Chang, and C. Winterhalter, "A 1-MHz hard-switched silicon carbide dc-dc converter," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 880–889, Jul. 2006.

[3] W. Huang and G. Moschopoulos, "A new family of zero-voltage-transition PWM converters with dual active auxiliary circuits," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 370–379, Mar. 2006.

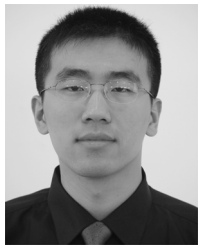
[4] G. Yao, A. Chen, and X. He, "Soft switching circuit for interleaved boost converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 80–86, Jan. 2007.

[5] Y. Jang, M. Jovanovic, and D. Dillman, "Soft-switched PFC boost rectifier with integrated ZVS two-switch forward converter," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1600–1606, Mar. 2004.
[6] T. Lopez, G. Sauerlaender, T. Duerbaum, and T. Tolle, "A detailed analysis of a resonant gate driver for PWM Applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2003, pp. 873–878.
[7] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE Power Electron. Spec. Conf.*, 1991, pp. 527–532.
[8] Z. Yang, S. Ye, and Y. F. Liu, "A new dual channel resonant gate drive circuit for synchronous rectifiers," in *Proc. IEEE Appl. Power Electron. Conf.*, 2006, pp. 756–762.
[9] Z. Yang, S. Ye, and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1311–1320, Jul. 2007.
[10] Z. Yang, S. Ye, and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2006, pp. 52–58.
[11] Y. Ren, M. Xu, and F. C. Lee, "12 V VR efficiency improvement based on two-stage approach and a novel gate driver," in *Proc. IEEE Power Electron. Spec. Conf.*, 2005, pp. 2635–2641.
[12] K. Xu, Y. F. Liu, and P. C. Sen, "A new resonant gate drive circuit with centre-tapped transformer," in *Proc. IEEE Ind. Electron. Conf.*, 2005, pp. 639–644.
[13] R. L. Steigerwald, "Lossless Gate Driver Circuit for a High Frequency Converter," U.S. 5 010 261, Apr. 23, 1991.
[14] H. L. N. Wiegman, "A resonant pulse gate drive for high frequency applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 1992, pp. 738–743.
[15] S. H. Weinberg, "A novel lossless resonant MOSFET driver," in *Proc. IEEE Power Electron. Spec. Conf.*, 1992, pp. 1003–1010.
[16] B. S. Jacobson, "High frequency resonant gate drive for a Power MOSFET," in *Proc. High Freq. Power Conv. Conf.*, 1993, pp. 133–141.
[17] J. Diaz, M. A. Perez, F. J. Linera, and F. Nuno, "A new family of loss-less power MOSFET drivers," in *Proc. Power Electron. Congress (CIEP)*, 1994, pp. 43–48.
[18] J. Diaz, M. A. Perez, F. M. Linera, and F. Aldana, "A new lossless power MOSFET driver based on simple dc/dc converters," in *Proc. IEEE Power Electron. Spec. Conf.*, 1995, pp. 37–43.
[19] Y. Panov and M. M. Jovanovic, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 776–783, Nov. 2001.
[20] K. Yao and F. C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 180–186, Mar. 2002.
[21] I. D. de Vries, "A resonant power MOSFET/IGBT gate driver," in *Proc. IEEE Appl. Power Electron. Conf.*, 2002, pp. 179–185.
[22] L. Faye and Q. Jinrong, "Gate Driver Apparatus Having an Energy Recovering Circuit," U.S. 6 650 169 B2, Nov. 18, 2003.
[23] Y. Chen, F. C. Lee, L. Amoroso, and H. Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 470–477, Mar. 2004.
[24] J. T. Strydom, M. A. de Rooij, and J. D. van Wyk, "A comparison of fundamental gate-driver topologies for high frequency applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, pp. 1045–1052.
[25] L. Balogh, "Design and application guide for high speed MOSFET gate drive circuits," in *Proc. TI-Unitrode Power Supply Design Sem.*, 2000, pp. 1–37.

Wilson Eberle (S'98–M'07) received the B.Sc. and M.Sc. degrees from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2000 and 2003, respectively, where he is currently pursuing the Ph.D. degree.

He has one U.S. and international patents pending and twenty technical papers published at conferences and in IEEE journals. He worked three summers as an engineering co-op student at Ford Motor Company in Windsor, Ontario, Canada from 1997 to 1999. His research interests include high efficiency, high power density, low power dc–dc converters, digital control techniques for dc–dc converters, emi filter design for switching converters, and resonant gate drive techniques for dc-dc converters.

Mr. Eberle received the Ontario Graduate Scholarship and has won awards through the Power Source Manufacturer's Association (PSMA) and Ontario Centres of Excellence (OCE).



Zhiliang Zhang (S'03) received the B.S. and M.Sc. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2002 and 2005, respectively, and is currently pursuing the Ph.D. degree in power electronics with the Queen's Power Group, Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada.

He was a Design Engineering Intern from June to September 2007 with the Burlington Design Center, Linear Technology Corporation, Burlington, VT. His research interests include high-frequency voltage regulators, novel soft-switching topologies and control methods, and resonant gate driver techniques.

Yan-Fei Liu (M'94–SM'97) received the B.S. and M.S. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1984 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

Since August 1999, he has been an Associate Professor with the Department of Electrical and Computer Engineering, Queen's University. Prior to this (February 1994 to July 1999), he was a Technical Advisor with the Advanced Power System Division, Astec (formerly Nortel Networks), where his was responsible for high quality design, new products and technology development. His research interests include digital control technologies for dc–dc switching converter and ac–dc converter with power factor correction, EMI filter design methodologies for switching converters, topologies and controls for high switching frequency, low switching loss converters, modeling and analysis of core loss and copper loss for high frequency planar magnetics, topologies and control for VRM, large signal modeling of switching converters.

Dr. Liu received the "Premiere's Research Excellent Award" (PREA) in 2001, the Golden Apple Teaching Award in 2000, both in Queen's University, and the "1997 Award in Excellence in Technology" from Nortel.

Paresh C. Sen (M'67–SM'74–F'89) was born in Chittagong, Bangladesh. He received the B.Sc. degree (with honors) in physics and the M.Sc. degree in applied physics from the University of Calcutta, India, in 1958 and 1961, respectively, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1965 and 1967, respectively.

Presently, he is an Emeritus Professor of electrical and computer engineering at Queen's University, Kingston, ON. He has written more than 160 research papers in the area of power electronics and drives. He is the author of two internationally acclaimed textbooks: *Principles of Electric Machines and Power Electronics* (New York: Wiley, 1989, 2nd ed., 1997) and *Thyristor DC Drives* (New York: Wiley, 1981). His fields of interest include power electronics, electric drive systems, switching power supplies, power factor correction circuits, modern control techniques for high performance drive systems, and applications of fuzzy logic control in power electronics and drive systems.

Dr. Sen received the IEEE Canada Outstanding Engineering Educator Award in 2006 for his outstanding contributions over four decades as an author, teacher, supervisor, researcher and consultant and the Prize Paper Award from the Industrial Drives Committee for technical excellence at the IEEE Industry Applications Society (IAS) Annual Meeting in 1986. He was an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS (1975–1982) and a Chairman of the Technical Committees on Power Electronics (1979–1980) and Energy Systems (1980–1982) of the IEEE Industrial Electronics Society. He served as an NSERC (Natural Science and Engineering Research Council of Canada) Scientific Liaison Officer evaluating University-Industry coordinated projects (1994–1999).