A New Dual-Channel Resonant Gate Drive Circuit for Low Gate Drive Loss and Low Switching Loss

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***Abstract*—At high-frequency applications, the gate drive loss of the power metal oxide semiconductor field-effect transistor (MOSFET) becomes quite significant. A new dual-channel low side resonant gate drive circuit is proposed in this paper. The proposed drive circuit can provide two symmetrical drive signals for driving two MOSFETs. It charges and discharges the MOSFET gate capacitor with a constant current source. Both gate drive loss and, more importantly, switching loss can be reduced significantly. The proposed resonant gate drive circuit can be used to drive the synchronous MOSFETs in a current doubler or full-wave rectifier configuration. It can also be used to drive the primary MOSFETs in push-pull converters. Analysis, computer simulation, and experimental results show that significant power loss reduction is achieved by the proposed circuit.**

***Index Terms*—Gate drive loss, MOSFET driver, resonant gate drive circuit, switching converters, switching loss.**

I. Introduction

THE development of microprocessor and other integrated circuits submits new challenges to power converter. In order to reduce the passive component size, and also to meet the stringent transient response requirement, the switching frequency of the power converter will move into the megahertz range in the next few years. At high-frequency applications, the effect of the gate drive circuit of MOSFETs on the overall performance of the converter becomes quite significant. As the switching frequency increases, the gate drive loss of the power MOSFET, which is proportional to the switching frequency, increases as well. In addition, as power MOSFET die size is increased to improve the MOSFET on-resistance, the gate-source capacitance of the MOSFET increases proportionally. Therefore, the gate drive loss becomes more significant, especially in low-voltage, high-current applications. High gate capacitance also increases the switching time and thus the switching loss. Fig. 1 shows the widely used conventional gate drive scheme, where Q represents the driven power MOSFET and $R_{\rm DRV}$ represents the gate resistor in the driving path. Unfortunately, this conventional gate drive scheme is a voltage source drive approach, and all the drive energy is dissipated on the resistor in the charge and discharge path [1]–[4].

Lossless gate drive circuits have already attracted much attention in recent years. A resonant gate driver is an efficient alternative to the conventional methods to drive power MOSFETs. Many circuits have been proposed. Most of them are designed for single MOSFET and are based on *L-C* resonant techniques [5]–[12]. DC/DC converters with transformers are used in some other solutions [13]–[16]. A few of drive schemes for synchronous rectifier are also proposed [17], [18]. Unfortunately, these circuits are complicated and they can only reduce the gate drive loss, which limit the potential of loss reduction.

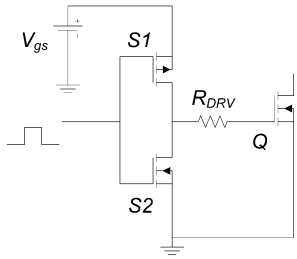

Fig. 1. Conventional gate drive scheme.

This paper presents a new resonant gate drive circuit, which can provide two symmetrical drive signals for driving two MOSFETs. The proposed drive circuit can recover most of the driving energy. It can also reduce the switching loss significantly. The proposed resonant gate drive circuit can be used to drive the synchronous rectifier in a current doubler or full-wave rectifier. It can also be used to drive the primary MOSFETs in push-pull converters. Section II discusses the operation of the proposed resonant gate drive circuit. Gate drive loss comparison between the proposed gate drive circuit and the conventional gate drive circuit is provided in Section III. The advantages of the proposed drive circuit are summarized in Section IV. Some application examples are provided in Section V. Section VI provides the computer simulation results and experimental results. Section VII is the Conclusion.

II. Operating Principle of the Proposed Resonant Gate Drive Circuit

The proposed new resonant gate drive circuit is shown in Fig. 2. The circuit consists of four switches $S1-S4$, which is inherited from dual-channel conventional gate drive circuit, connecting as a bridge configuration, and an inductor $L1$ connecting across the bridge. Capacitors, C_{g_Q1} and C_{g_Q2} represent the input capacitors of the power MOSFETs $Q1$ and $Q2$,, respectively. V_c is the voltage source which is applied to gate-source of MOSFET $Q1$ and $Q2$. A P-channel MOSFET is used for $S1$ and $S2$ and an N-channel MOSFET is used for $S3$ and $S4$ in Fig. 2. It is noted that other implementation methods can also be used to achieve the same objective.

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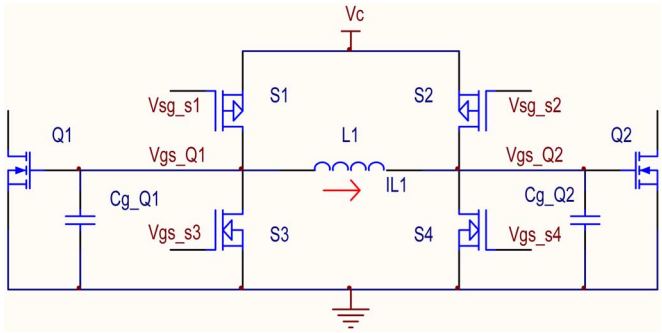

Fig. 2. Proposed resonant gate drive circuit.

The major objectives of the proposed resonant gate drive circuit are 1) to charge and discharge the input capacitors, C_{g_Q1} and C_{g_Q2}, with minimum energy loss, 2) to do this as soon as possible, and 3) to clamp the voltages across C_{g_Q1} and C_{g_Q2} to either source voltage V_c or zero via low-impedance path. With this circuit, the duty cycles of the voltages across C_{g_Q1} and C_{g_Q2} are the same, which is decided by the gate drive signals of $S1-S4$. By applying different gate drive signals to $S1$, $S2$, $S3$, and $S4$, the duty cycle D of $Q1$ and $Q2$ can be smaller than 0.5, equal to 0.5, or bigger than 0.5. The operation is a little different for these three operating conditions. The operation of this circuit under the $D > 0.5$ situation is described in detail as follows by eight operation modes shown in Fig. 3. The red arrows in the figure indicate the reference current direction. The current is positive when the actual current has the same direction as the reference direction, otherwise it is negative. The typical waveforms are shown in Fig. 4.

1) Before t0: $S1, S4$ are on and $S2, S3$ are off. $Q1$ is on and $Q2$ is off. Inductor current I_{L1} increases to maximum value at t0, as shown in Fig. 3(a).

2) From t0 to t1: $S4$ is turned off at t0. Inductor $L1$ resonates with the input capacitor of MOSFET $Q2$, $C_{g\_Q2} \cdot C_{g\_Q2}$ will be charged at this period. The voltage across C_{g_Q2} increases, and it will be clamped to the source voltage V_c by the body diode of $S2$ before t1. $Q2$ is turned on in this time interval. At t1, $S2$ turns on with zero voltage. By controlling the turn-off instant of $S4$ (t0), the turn-on instant of $Q2$ can be controlled, as shown in Fig. 3(b).

3) From t1 to t2: $S1, S2$ are on and $S3, S4$ are off. Both $Q1$ and $Q2$ are on and the inductor current I_{L1} is circulating through $S1$ and $S2$ and remains constant in this interval, as shown in Fig. 3(c).

4) From t2 to t3: $S1$ is turned off at t2 with zero voltage. Inductor $L1$ resonates with the input capacitor of MOSFET $Q1$, $C_{g\_Q1} \cdot C_{g\_Q1}$ will be discharged at this period. The voltage across C_{g_Q1} decreases, and it will be clamped to zero by the body diode of $S3$ before t3. $Q1$ is turned off in this time interval. At t3, $S3$ turns on with zero voltage. By controlling the turn-off instant of $S1$ (t2), the turn-off instant of $Q1$ can be controlled, as shown in Fig. 3(d).

5) From t3 to t4: $S2, S3$ are on and $S1, S4$ are off. $Q1$ is off and $Q2$ is on. The inductor current I_{L1} decreases to zero, and it will increase in the opposite direction. It reaches the negative maximum at t4, as shown in Fig. 3(e).

6) From t4 to t5: $S3$ is turned off at t4. Inductor $L1$ resonates with capacitor $C_{g\_Q1} \cdot C_{g\_Q1}$ will be charged. The voltage across C_{g_Q1} increases, and it will be clamped to the source voltage V_c by the body diode of $S1$ before t5. $Q1$ is turned on in this time interval. At t5, $S1$ turns on with zero voltage. By controlling the turn-off instant of $S3$ (t4), the turn-on instant of $Q1$ can be controlled, as shown in Fig. 3(f).

7) From t5 to t6: $S1, S2$ are on and $S3, S4$ are off. Both $Q1$ and $Q2$ are on, and the inductor current I_{L1} is circulating through $S1$ and $S2$ and remains constant in this interval, as shown in Fig. 3(g).

8) From t6 to t7: $S2$ is turned off at t6 with zero voltage. Inductor $L1$ resonates with capacitor $C_{g\_Q2} \cdot C_{g\_Q2}$ will be discharged at this period. The voltage across C_{g_Q2}decreases and it will be clamped to zero by the body diode of $S4$ before t7. $Q2$ is turned off in this time interval. At t7, $S4$ turns on with zero voltage. By controlling the turn-off instant of $S2$ (t6), the turn-off instant of $Q2$ can be controlled, as shown in Fig. 3(h).

9) From t7 to t8: $S1, S4$ are on and $S2, S3$ are off. $Q1$ is on and $Q2$ is off. The negative inductor current rises through zero and becomes positive. The value of the current I_{L1} will increase to positive maximum at t8. The next cycle will start at t8, as shown in Fig. 3(a).

It is noted that the auxiliary circuit is a typical bridge configuration with pure inductive load, all four switches (S1–S4) can achieve zero voltage switching as discussed in [19].

When the duty cycle D equals 0.5, the operation is similar to that for $D > 0.5$ and the details are not explained here in order to save space. The key difference is that there is no overlap between the drive signal of $S1$ and $S2$, so $S1$ and $S2$ will not conduct simultaneously and there is no current circling through them. The waveforms are shown in Fig. 5.

When the duty cycle D is less than 0.5, the operation is similar to that for $D > 0.5$ and the details are not explained here. The key difference is that current circles though $S3$ and $S4$ instead of $S1$ and $S2$. The waveforms are shown in Fig. 6.

Theoretically, the proposed resonant gate drive circuit can operate in full duty cycle range (from 0 to 1). This can be achieved by controlling the drive signals of switches $S1 - S4$.

It can be noted that one significant difference between the proposed resonant gate drive circuit and the existing resonant gate drive circuits is that the inductor is connected in a bridge configuration. Therefore, the inductor current can be controlled much more tightly as compared with other configurations, as in [9]–[11], [13], and [14]. In addition, because the MOSFET gate voltage is clamped between 0 and V_{cc}, there is no resonance between the inductor and MOSFET input capacitor. Consequently, the proposed resonant gate drive circuit does not have transient issue related to the existing resonant gate drive circuits. During large and sudden duty cycle change, the worst case situation for the proposed circuit is that the auxiliary switches cannot achieve zero voltage switching and the gate energy cannot be recovered.

III. Loss Comparison

This section analyzes the loss of the proposed resonant gate drive circuit. The key parameter impacting the gate drive loss is the peak inductor current I_{Lpeak} which is used to charge and

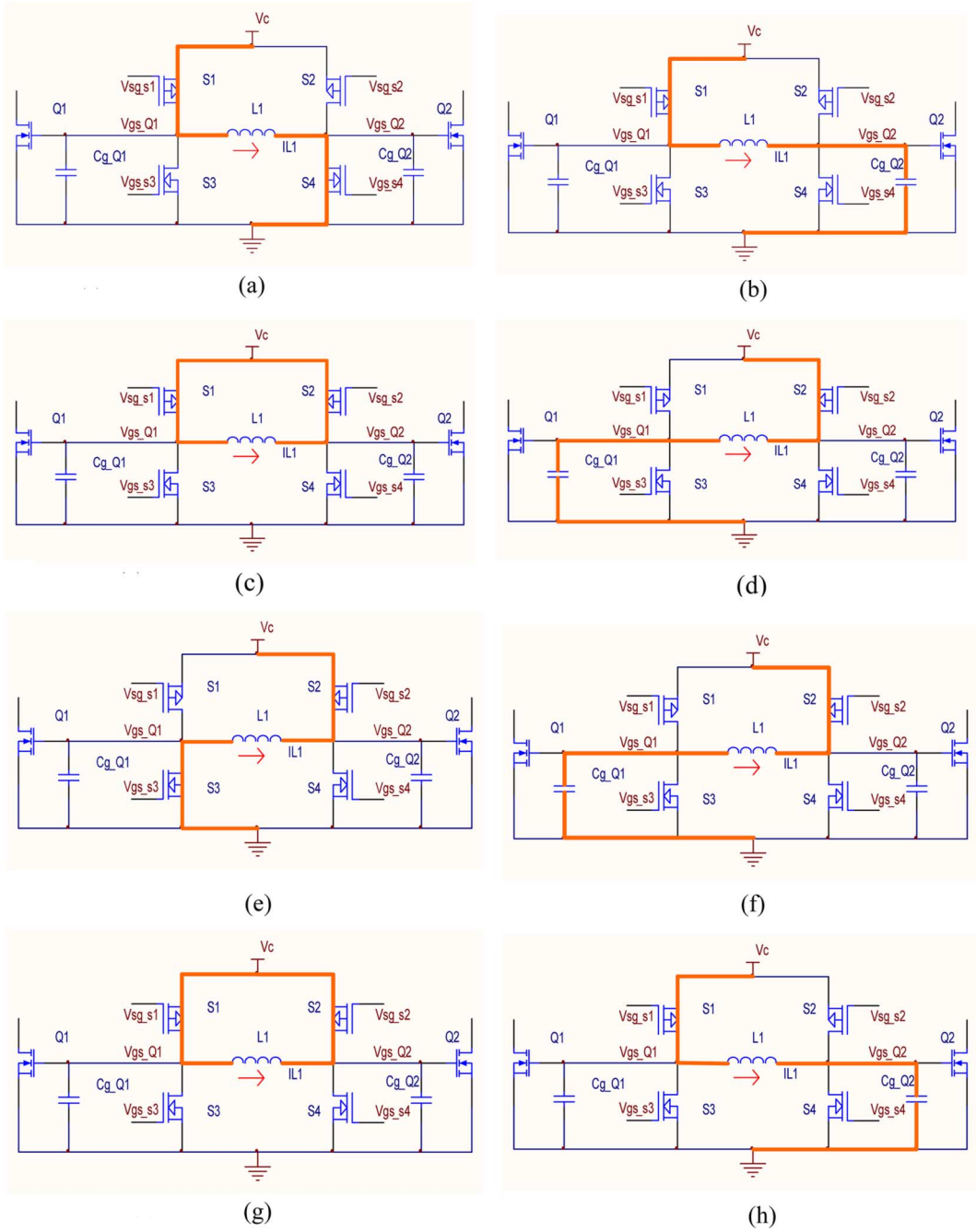

Fig. 3. Equivalent circuits of eight operation modes in dual low side symmetrical drive circuit. (a) Mode 1 ($t < t0$ and $t7 < t < t8$). (b) Mode 2 ($t0 < t < t1$). (c) Mode 3 ($t1 < t < t2$). (d) Mode 4 ($t2 < t < t3$). (e) Mode 5 ($t3 < t < t4$). (f) Mode 6 ($t4 < t < t5$). (g) Mode 7 ($t5 < t < t6$). (h) Mode 8 ($t6 < t < t7$).

discharge the input capacitors of power MOSFETs. Assume the power MOSFET $Q1$ and $Q2$ in Fig. 2 are identical and their desired switching time is $t_{\rm sw}$, the required peak inductor current, which is also the charge and discharge current can be given as follows:

$$I_{L\rm peak} = \frac{Q_g}{t_{\rm sw}} \tag{1}$$

where, Q_g is the total gate charge of each power MOSFET. It is noted that increasing $I_{L\rm peak}$ will reduce the switching time as well as the switching loss.

Fig. 7 redraws the inductor current and the current through $S1 - S4$ when $D > 0.5$, where $D = (t7 - t0)/(t8 - t0)$. The RMS value of the inductor current can be calculated as follows:

$$\begin{aligned} I_{L\rm RMS} &= \sqrt{2 * \frac{2D-1}{2} * {I_{L\rm peak}}^2 + 2(1-D) * \frac{{I_{L\rm peak}}^2}{3}} \\ &= I_{L\rm peak} * \sqrt{\frac{4D-1}{3}}. \end{aligned} \tag{2}$$

At $D = 0.5$, the inductor current becomes triangular and $I_{L\rm RMS}$ equals $I_{L\rm peak}/\sqrt{3}$.

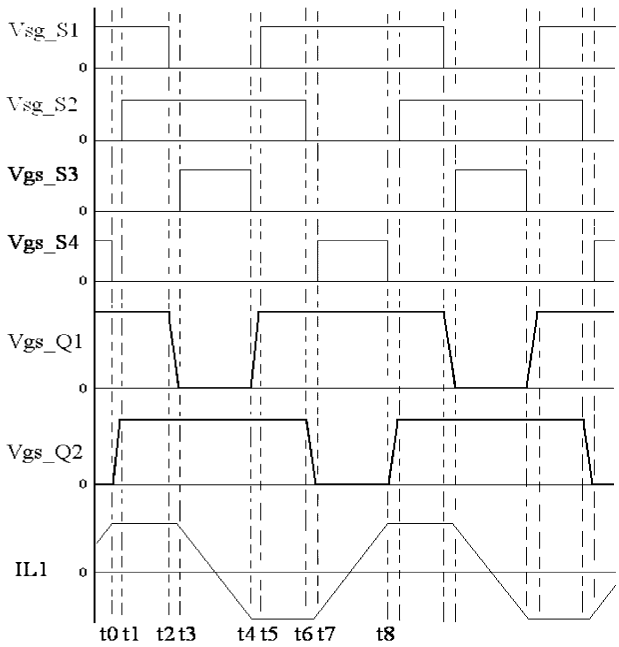

Fig. 4. Typical waveforms of the proposed resonant gate drive circuit with $D > 0.5$.

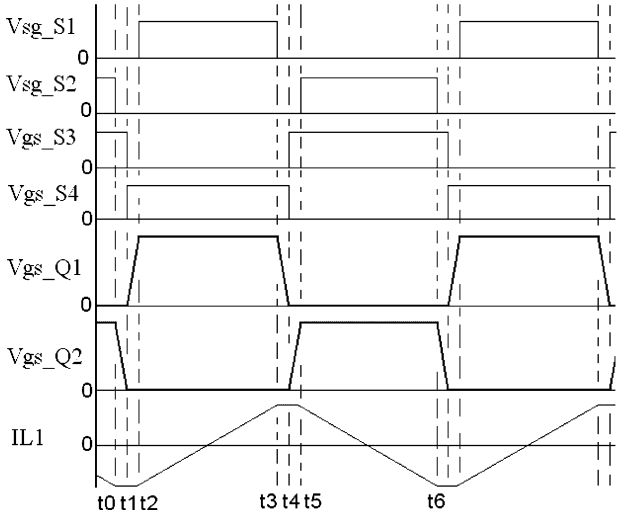

Fig. 5. Typical waveforms of the proposed resonant gate drive circuit with $D = 0.5$.

As time intervals t0–t1, t2–t3, t4–t5, and t6–t7 are much shorter than the on/off time and the operating period of the circuit, they are neglected when evaluating the RMS currents for switches $S1 - S4$ in order to simplify the analysis. The RMS currents through switches $S1$ and $S2$ are the same and are given as follows:

$$\begin{aligned} I_{S1\mathrm{RMS}} &= I_{S2\mathrm{RMS}} \\ &= \sqrt{2 * \frac{2D-1}{2} * I_{L\mathrm{peak}}^2 + (1-D) * \frac{I_{L\mathrm{peak}}^2}{3}} \\ &= I_{L\mathrm{peak}} * \sqrt{\frac{5D-2}{3}}. \end{aligned} \tag{3}$$

At $D = 0.5$, the RMS current flowing through switches $S1$ and $S2$ equals $I_{L\mathrm{peak}}/\sqrt{6}$.

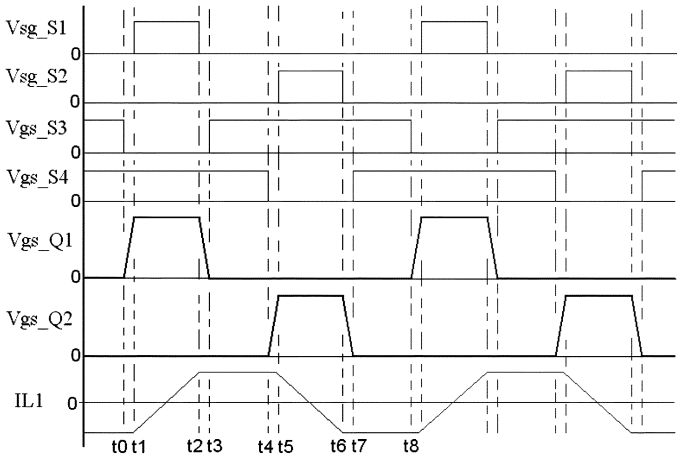

Fig. 6. Typical waveforms of the proposed resonant gate drive circuit with $D < 0.5$.

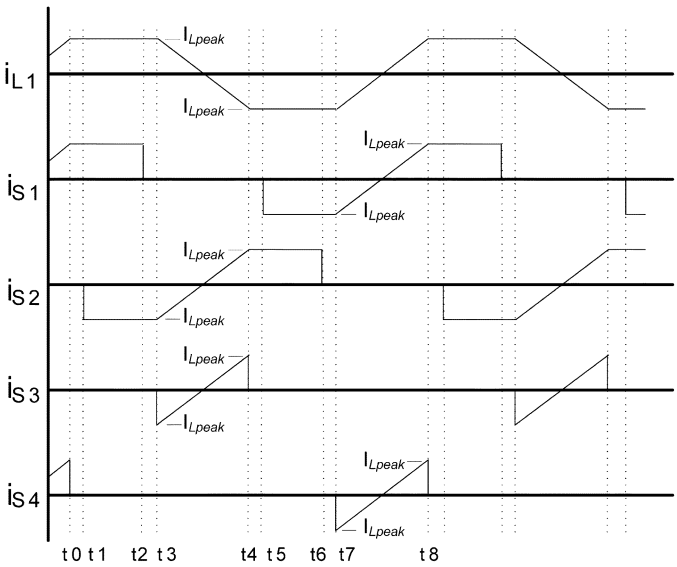

Fig. 7. Current through inductor and switches $S1 - S4$ at $D > 0.5$.

The RMS currents through switches $S3$ and $S4$ are the same and given as follows:

$$I_{S3\mathrm{RMS}} = I_{S4\mathrm{RMS}} = I_{L\mathrm{peak}} * \sqrt{\frac{1-D}{3}}. \tag{4}$$

At $D = 0.5$, the RMS current equals to $I_{L\mathrm{peak}}/\sqrt{6}$.

In the case of duty cycle $D < 0.5$, the RMS value of the inductor current can still be obtained by (2), the RMS currents through $S1$ and $S2$ can be obtained by (4), and the RMS currents through $S3$ and $S4$ can be obtained by (3), except that the duty cycle D needs to be replaced by $1 - D$ in those equations.

The total power loss of the proposed resonant gate drive circuit is the sum of the resistive loss caused by $R_{ds(\mathrm{on})}$ of $S1 - S4$, the gate drive losses of $S1 - S4$, the core loss and the copper loss of the resonant inductor $L1$, and the resistive loss caused by the internal gate resistor of the power MOSFET R_G. There is no switching loss or cross conduction loss as switches $S1 - S4$ operate in ZVS condition.

The copper loss of the inductor winding is given as follows:

$$P_{\mathrm{copper}} = R_{\mathrm{ac}} * {I_{L\mathrm{RMS}}}^2 \tag{5}$$

where $R_{\rm ac}$ is the ac resistance of the inductor winding. The inductor core loss $P_{\rm core}$ depends upon the inductor design. High-frequency core materials such as 3F5 or PC50 should be used to reduce core loss. Air core inductor may be used when the switching frequency goes above 2 MHz. In that case, core loss is eliminated. The total inductor loss is given as follows:

$$P_{\rm ind} = P_{\rm copper} + P_{\rm core}. \tag{6}$$

Both the charge and discharge currents flow through the internal gate mesh resistor R_G of the power MOSFET and cause resistive loss. The charge and discharge current is the peak value of the inductor current. Thus, the total losses caused by the internal resistance of two power MOSFETs during turn-on and turn-off intervals can be calculated as follows:

$$P_{\rm RG} = 2 * 2 * R_G * I_{L\rm peak}^2 * t_{\rm sw} * f_s \tag{7}$$

where $t_{\rm sw}$ is the switching time and f_s is the switching frequency. $P_{\rm RG}$ includes both the charging loss and discharging loss caused by the internal resistance of two power MOSFETs.

The conduction loss caused by $S1$ and $S2$ can be calculated by (8), where $R_{\rm ds1(on)}$ is the on resistor of $S1$ and $S2$

$$P_{\rm top} = 2 * R_{\rm ds1(on)} * {I_{L\rm peak}}^2 * \frac{5D-2}{3}. \tag{8}$$

The conduction loss of $S3$ and $S4$ can be calculated by (9), where $R_{\rm ds3(on)}$ is the on resistor of $S3$ and $S4$.

$$P_{\rm bott} = 2 * R_{\rm ds3(on)} * I_{L\rm peak}^2 * \frac{1-D}{3}. \tag{9}$$

As mentioned before, switches $S3$ and $S4$ are N-channel MOSFETs, whereas switches $S1$ and $S2$ can be either N-channel MOSFET or P-channel MOSFETs depending on design. When same MOSFET is selected for all switches $S1-S4$, the total conduction loss caused by the switches $S1-S4$ is given by (10), where $R_{\rm ds(on)}$ is the on resistor of $S1-S4$

$$P_{\rm cond} = P_{\rm top} + P_{\rm bott} = 2 * R_{\rm ds(on)} * I_{L\rm peak}^2 * \frac{4D-1}{3}. \tag{10}$$

The switching frequency of these $S1-S4$ is the same as the switching frequency f_s of the power MOSFETs. The total gate drive loss of all four switches $(S1-S4)$ is given by (11), where Q_{g_s} is the total gate charge of switch $(S1-S4)$, V_{gs_s} is the drive voltage of the switch $(S1-S4)$, which is usually 5 V

$$P_{\rm Gate} = 4 * Q_{g\_s} * V_{gs\_s} * f_s. \tag{11}$$

Therefore, the total loss of the resonant gate drive circuit can be calculated by adding all above losses together and given as follows:

$$P_{\rm DRV} = P_{\rm cond} + P_{\rm RG} + P_{\rm Gate} + P_{\rm ind}. \tag{12}$$

It is noted that the above loss is for driving two power MOSFETs. The above analysis assumes $D \geq 0.5$. In the case of duty cycle $D < 0.5$, the total loss of the proposed resonant gate drive circuit can be calculated in the same way, except that different expressions for the RMS currents of the inductor and switches need to be used.

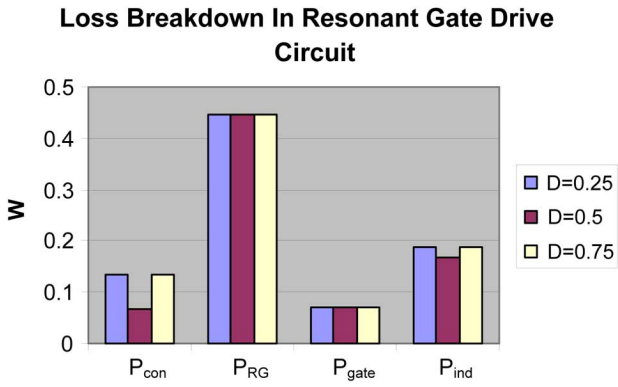

Fig. 8. Loss breakdown in resonant gate drive circuit under different duty cycle.

An example is taken for understanding the gate drive loss under the proposed resonant gate drive circuit. Two IRF6618 are selected as power MOSFET, with total gate charge $Q_g = 93$ nC when $V_{\rm gs} = 12$ V. Its internal gate resistor R_G is 1 Ω. FDN335N is selected for switches S1-S4, with typical $R_{\rm ds(on)} = 0.07\,\Omega$ and total gate charge $Q_{g\_s} = 3.5$ nC. Assume the inductor peak current is 1.2 A. The switching frequency is 1 MHz. DS3316P-2.2 uH is chosen as the resonant inductor. The core loss of the inductor at 1 MHz is 0.147 W and the estimated ac winding resistance is 0.044 Ω. The loss breakdown under different duty cycle D is calculated and shown in Fig. 8.

As indicated from (2)–(12), the RMS currents flowing through the resonant inductor and switches vary with the operation duty cycle, so does the total loss of the proposed drive circuit. However, the loss variation is not significant. It can be observed that the total gate drive loss is 0.75 W at $D = 0.5$, and total gate drive loss is 0.88 W for $D = 0.25$ and $D = 0.75$. This shows that when D changes from 0.25 to 0.75 (a very large variation range for a practical power supply), the power loss changes from 0.75 W to 0.88 W, only 0.13 W. It is quite small.

It is also observed from Fig. 8 that the most significant loss is caused by the internal gate resistor R_G of the power MOSFET. Many presented resonant gate drive circuits claim that most of the driving loss can be recovered, but they did not actually mentioned the loss caused by the internal resistor of the power MOSFET. This is one of the major reasons that their experiment results are usually much worse than the claimed calculation results. Refer to the calculated results in Table I, which will be explained in next section, the loss saving of the proposed circuit is more than 86% if the loss caused by R_G is not considered. The number can be even more impressive by reducing the charge/discharge current. Obviously, this is not realistic as the switching time and the switching loss may become unreasonable.

Another concern should be addressed here is that a tradeoff between the power MOSFET switching loss reduction and the driving loss increase needs to be made. As mentioned before, increasing peak inductor current $I_{L\rm peak}$ will reduce the switching time as well as the switching loss, but large $I_{L\rm peak}$ will slightly increase the driving loss as discussed earlier.

TABLE I
CALCULATED GATE DRIVE LOSS

	Gate charge loss	*Driver chip loss*	*Total Drive loss*
Conventional driver	2.23W	0.3W	2.53W
Resonant gate driver	0.75W	0.04W	0.79W
Loss Saving	1.48W	0.26W	1.74W

IV. ADVANTAGES OF THE NEW RESONANT GATE DRIVE CIRCUIT

This section discusses the advantages of the proposed resonant gate drive circuit.

A. Gate Drive Loss Saving

The same example is taken for comparing the gate drive loss under the proposed resonant gate drive circuit and conventional gate drive scheme. At switching frequency at 1 MHz and $D = 0.5$, the gate drive loss of resonant gate drive circuit is calculated to be 0.75 W by the analysis in Section III.

The gate drive loss under conventional gate drive scheme can be calculated to be 2.23 W by as follows:

$$P_{\mathrm{DRV}} = Q_s * V_{\mathrm{gs}} * f_s. \tag{13}$$

There are lots of driver chips based on conventional gate drive scheme in the market. The loss of the driver chip itself is usually around 300 mW at 1 MHz [1]. Therefore, the total gate drive related loss under conventional drive scheme is 2.53 W (2.23 W + 0.3 W). It is noted that the loss will be dissipated in drive chip, which cannot handle such a high power loss. The compromise is to lower the gate voltage to around 5 V. The penalty is increased conduction loss as $R_{\mathrm{ds(on)}}$ will be increased at $\mathrm{V_{gs}} = 5$ V. In this paper, $V_{\mathrm{gs}} = 12$ V is used for both cases.

In the proposed resonant gate drive circuit, some logic circuits and level shift circuits are needed to generate the drive signals for switches $S1-S4$. The loss of these logic circuits is estimated as 40 mW. Therefore, the total gate drive related loss for proposed resonant gate drive circuit is 0.79 W (0.75 W + 0.04 W). The gate drive loss saving realized by using resonant gate drive circuit is 68.7% (1.74/2.53). Table I summarizes the above calculation result.

B. Switching Loss Reduction

It is noted that most of the switching loss happens at Miller plateau. At the MOSFET turn-on interval, during Miller plateau, the drain current rises from zero to load current level while the drain-source voltage is still high. At MOSFET turn-off interval, during Miller plateau, the drain-source voltage rises from zero to high voltage while the drain current is still at load current level. Therefore, by reducing the Miller plateau interval, the switching loss can be reduced. The Miller voltage is normally around $2-3$ V.

Take the turn-off interval as an example, the theoretical discharge current at Miller plateau is 0.86 A when ($\mathrm{R_G}$ ($\sim 1\ \Omega$, driver resistance ($\sim 1.5\ \Omega$), and optional external resistor (1 Ω) are considered. However, because of the leakage inductance in the discharge loop introduced by PCB track and bonding wire inside MOSFET, the actual discharge current is much smaller. Therefore, the turn-off time is longer and turn-off loss is greater. Similarly, during turn-on interval, the charge current at Miller plateau will be even smaller if $\mathrm{V_{gs}} = 5$ V is used and therefore, longer turn-on time and greater turn loss. This is the problem with conventional gate drive scheme.

With the proposed resonant gate drive circuit, the MOSFET gate is charged and discharged at the peak inductor current during the switching interval (Miller plateau). The current is constant during the switching interval. In addition, the impact of the leakage inductance is removed as it is in series with a much larger inductor. Therefore, the turn-on and turn-off time can be significantly reduced and the switching loss can be reduced. The experimental results provided in Section VI verified this.

C. Body Diode Conduction Time Reduction

It is noted that in order to avoid cross conduction, dead time is introduced for synchronous rectifier MOSFET gate drive signals. During the dead time, the body diode of the SR FET is on and causing loss. With the proposed resonant gate drive circuit, the dead time can be reduced as the SR FET can be turned on and turned off faster as shown in the analysis above. Therefore, the diode conduction loss can be reduced.

D. High Noise Immunity and Alleviation of Dv/Dt Effect

With the new resonant gate drive circuit, the gate of the power MOSFET is connected to either source or ground via low impedance path, rather than through the external gate resistor and driver's on-resistance (a few ohms) in conventional gate drive scheme. Therefore, the noise immunity is significantly improved and it is much less likely the synchronous FET will be turned on by dv/dt effect.

E. Less Impact of Parasitic Inductance

As the gate is charged/discharged by a constant current source, the negative impact by the parasitic inductance in the gate drive loop (such as PCB track, lead inside the MOSFET) can also be significantly reduced.

V. APPLICATIONS

The proposed resonant gate drive circuit can be used in a wide range of switching power converters. It can be used to drive the synchronous rectifier in a current doubler circuit, the primary MOSFET in push–pull converters, as well as the so-called bus converter when the duty cycle is 50%. Fig. 9 shows that the proposed resonant gate drive circuit is used to drive the synchronous

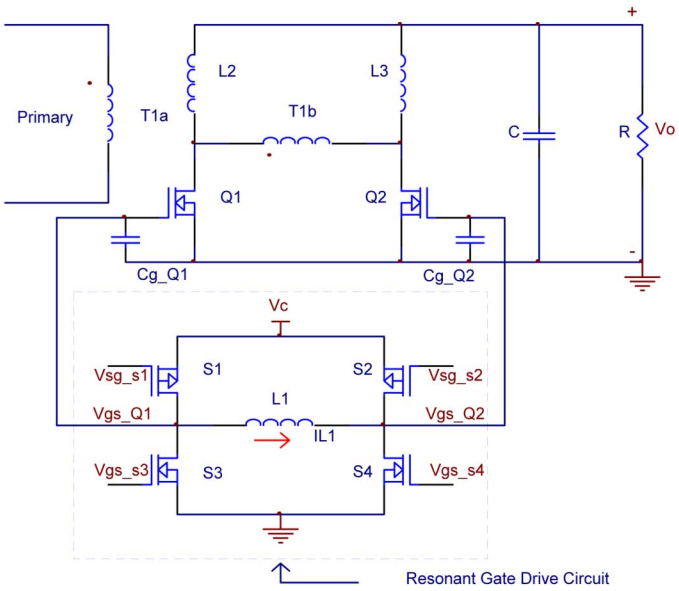

Fig. 9. Current doubler with resonant gate drive circuit.

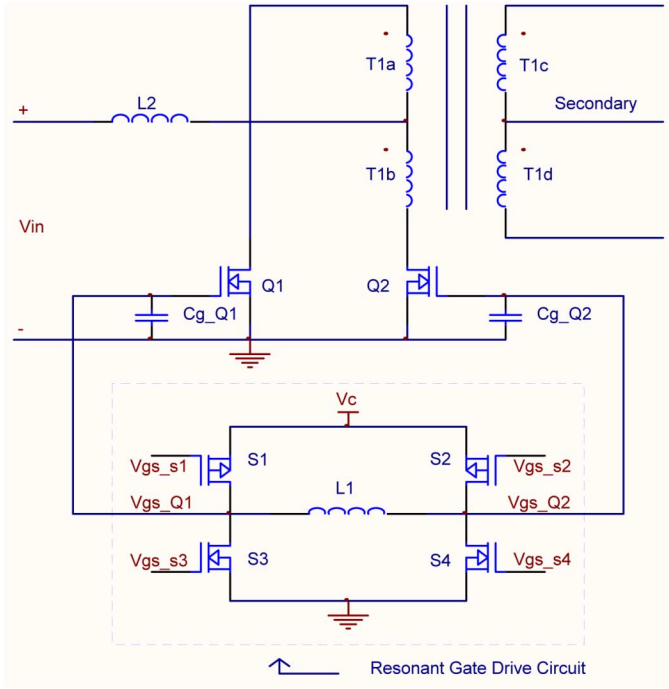

Fig. 10. Current fed push–pull converter with resonant gate drive circuit.

rectifiers in a current doubler circuit. In this application, the duty cycles for $Q1$ and $Q2$ are the same and larger than 50%. With the resonant gate drive circuit, most of gate drive energy can be recovered. In addition, the turn-on and turn-off time of $Q1$ and $Q2$ can also be reduced, which will help reduce their body diode conduction loss.

Figs. 10 and 11 show the current fed push–pull converter and voltage fed push–pull converter with resonant gate drive circuit to drive the primary side MOSFET, $Q1$ and $Q2$. In current fed push–pull converter, the duty cycle for $Q1$ and $Q2$ is same and larger than 50%. In voltage fed push–pull converter, the duty cycle is less than 50%.

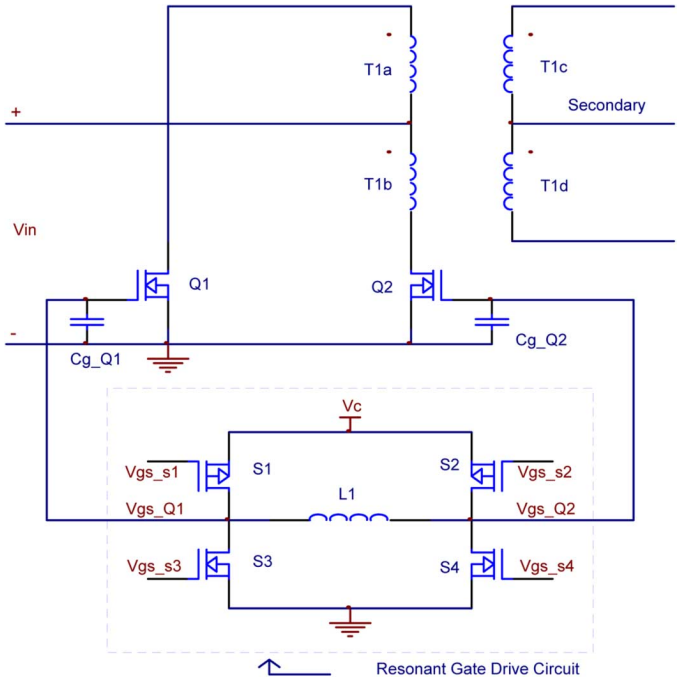

Fig. 11. Voltage fed push–pull converter with resonant gate drive circuit.

VI. Computer Simulation and Experimental Results

The proposed resonant gate drive circuit shown in Fig. 2 was simulated by PSPICE. The operation of the conventional gate drive circuit shown in Fig. 1 was also simulated. The components listed at the end of Section III are used for the simulation. Besides, a 3-Ω resistor is connected from the drain of each power MOSFET to a 12-V source as the load. Simulated gate voltage and charge/discharge current waveforms at duty cycle $D = 0.7$ condition are shown in Fig. 12. It is observed from Fig. 12(a) that the charge current and discharge current is fairly constant during turn-on and turn-off time interval. Hence, the input capacitor of the driven power MOSFET, including both gate-source capacitor $C_{\rm gs}$ and gate-drain capacitor $C_{\rm gd}$ (or Miller capacitor) is charged and discharged very fast and the Miller plateau is not obvious in the simulation waveform. Fig. 12(b) shows the gate charge/discharge current for conventional gate drive circuit. It is observed that although the peak current is 2.5 A, the current used to remove the Miller capacitor $(C_{\rm gd})$ in turn-off transition is quite small, only around 0.5 A. Thus, $C_{\rm gd}$ needs more time to be discharged and The Miller plateau at the turn-off interval is clearly observed.

The longer it takes to charge/discharge the input capacitor of the power MOSFET, the higher the switching loss is generated. The proposed resonant gate drive circuit can charge/discharge the Miller capacitor faster than the conventional gate drive scheme, thus lower switching loss can be expected. By selecting appropriate peak inductor current, which is also the charge/discharge current, the proposed drive circuit can achieve significant gate drive loss saving and switching loss reduction.

Boost converters are used to demonstrate the feasibility and advantages of the proposed resonant gate drive circuit. One Boost converter is driven by conventional drive chip UCC27323 from Texas Instrument and the other is driven by the proposed resonant gate drive circuit. The power train of

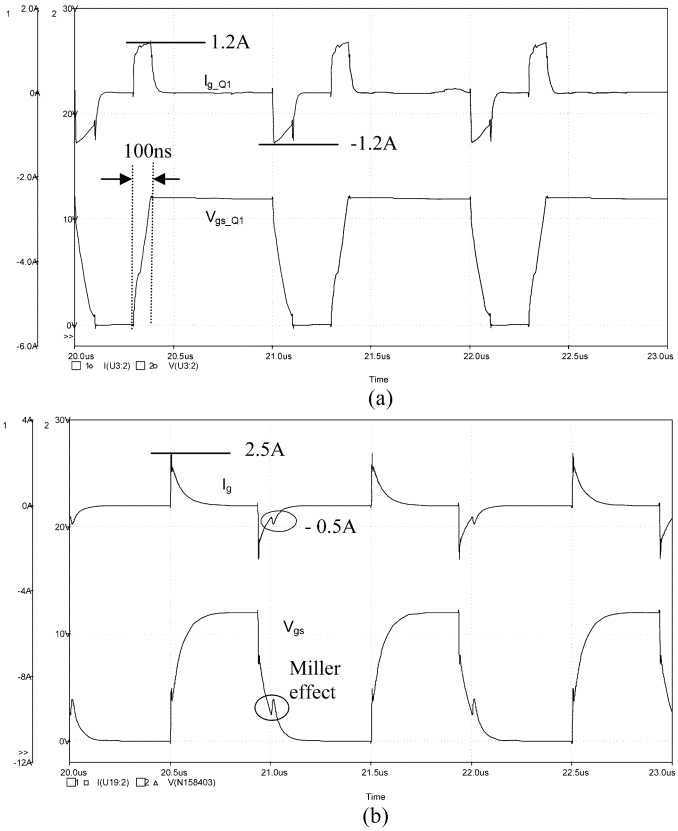

Fig. 12. Simulated key waveforms of the proposed resonant gate drive circuit and conventional gate drive circuit. (a) Gate drive voltage and charge/discharge current of the proposed resonant gate drive circuit. (b) Gate drive voltage and charge/discharge current of the conventional gate drive circuit.

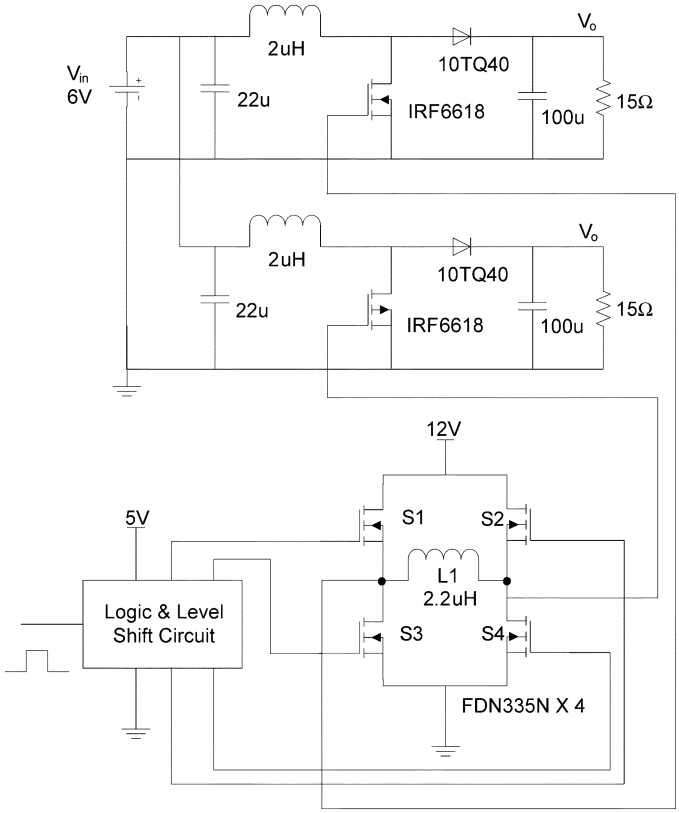

Fig. 13. Circuit diagram of the prototype.

the Boost converters is same. IRF6618 is used as the Boost MOSFET. Schottky diode 10TQ40 is used as the diode. The Boost inductor value is 2 μH. The Boost inductor current ripple is 1.4 A peak to peak. The switching frequency is 1 MHz for both cases. The duty cycle is 50% and the output voltage is regulated at 11.35 V by slightly adjusting the input voltage. The input voltage is around 5.7 V for all the test cases. In the test setup, the gate drive circuit is powered by one power supply (with Vc of 12 V) and the Boost converter is powered by another power supply. Thus, the gate drive loss can be separated from the power circuit loss.

The circuit diagram of the prototype is shown in Fig. 13.

In the prototype, all switches $S1 - S4$ are of N channel MOSFET. Since the driving voltage of the power MOSFETs is 12 V and the driving voltage of the switches $S1 - S4$ is 5 V, level shift circuit is needed for generating the drive signals of high-side switches $S1$ and $S2$, no matter what P channel MOSFET or N channel MOSFET is used. Usually, P channel MOSFET has higher $R_{\rm dson}$ than N channel MOSFET. However, the conduction loss caused by the switches $S1 - S4$ is a small portion of the total loss of the proposed circuit (refer to Fig. 8). Furthermore, two MOSFETs, an N channel MOSFET FDN335N with 0.07 Ω typical $R_{\rm dson}$ and a P channel MOSFET FDN342P with 0.08 $\Omega R_{\rm dson}$ are considered for the loss estimation of the proposed drive circuit. The difference of the conduction loss caused by these two MOSFETs is not significant since the difference of their $R_{\rm dson}$ is small.

Fig. 14 shows the logic circuit for generating the drive signals of switches $S1 - S4$. A simple *RC* network is used to generate the needed delay time. Fig. 15 shows the level shift circuit used in the prototype.

The measured gate drive loss under conventional drive scheme is 2.61 W (2.53 W from calculation) at 1-MHz operation. The gate drive loss for proposed resonant gate drive scheme is only 0.864 W (0.75 W from calculation). The loss reduction is 1.746 W, or 67% of the conventional gate drive loss. The measured gate drive loss is very close to the calculated loss.

Fig. 16 shows measured key waveforms of the resonant gate drive circuit. Fig. 16(a) shows the gate signals for $S1$, $S2$, $S3$, and $S4$. The dead time is easily achieved. Fig. 16(b) shows the gate voltage and the resonant inductor current. It is observed that waveform is very clean and the peak inductor current is used to charge and discharge the gate capacitor. No Miller plateau is observed.

Fig. 17 shows the comparison of gate voltage and gate current of the resonant gate drive circuit and the conventional gate drive circuit. It is observed from Fig. 17(a) that the gate current during switching interval is almost constant. The charging and discharging current is about 1.3 A. The miller plateau is not observed, which shows that the Miller charge is removed very quickly. It is also observed from Fig. 17(b) that for conventional gate drive circuit, the peak current is similar. However, the gate current at Miller plateau is quite small (around 0.3 A) and significant Miller plateau is observed.

The waveforms shown in Fig. 17 also indicate that the switching time is reduced for resonant gate drive circuit. In

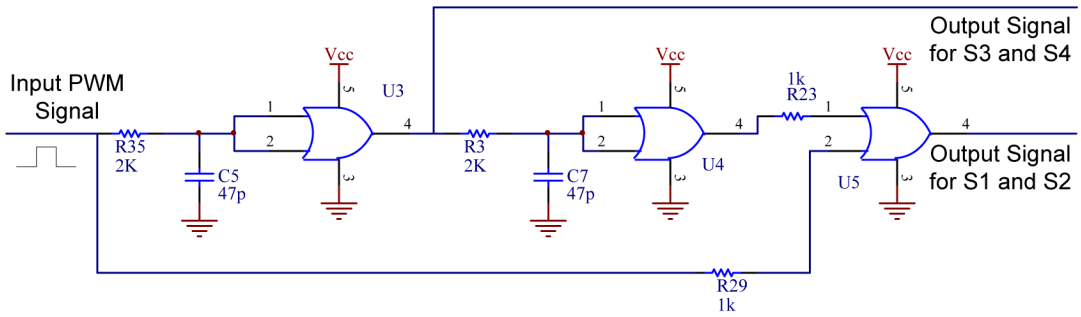

Fig. 14. Logic circuit for generating the drive signals for switches $S1 - S4$.

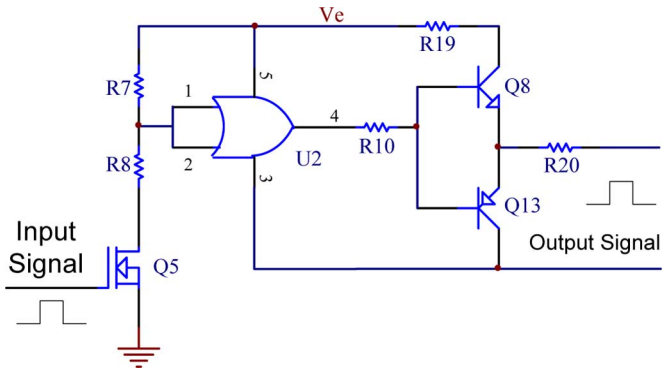

Fig. 15. Level shift circuit designed for two high-side switches S1 and S2.

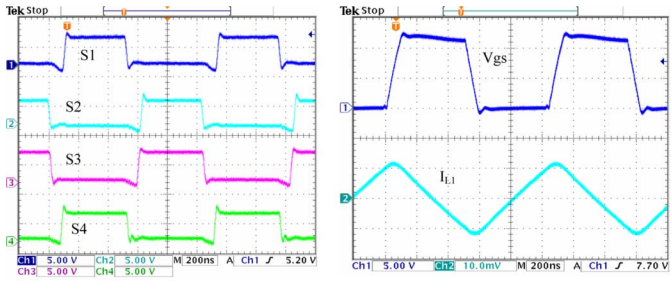

Fig. 16. Measured key waveforms of the proposed resonant gate drive circuit and conventional gate drive circuit, time scale 200 ns/div. (a) Gate drive signals of switches S1-S4 (5 V/div). (b) Resonant inductor current (1 A/div,) and gate drive voltage (5 V/div).

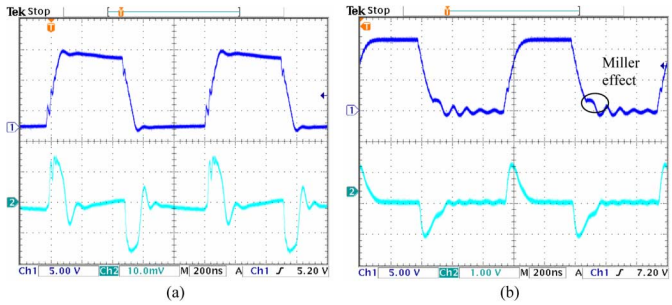

Fig. 17. Measured key waveforms of the proposed resonant gate drive circuit and conventional gate drive circuit, time scale 200 ns/div. (a) Gate voltage (top, 5 V/div) and gate current (1 A/div) for resonant gate driver. (b) Gate voltage (top, 5 V/div) and gate current (bottom, 1 A/div) for conventional gate driver.

order to illustrate this point more clearly, the total power train loss of the Boost converter (excluding gate drive loss) is measured under different load current (0.4 A and 0.8 A) when output voltage is regulated at 11.35 V. For conventional gate drive scheme, the loss is measured under four conditions, with gate resistor of 2.5 Ω and 1 Ω, as well as with load current of 0.4 A and 0.8 A. Table II summarizes the total power train loss measurement (excluding gate drive loss).

The following two points can be concluded from Table II:

A. *External Gate Resistor Impact Switching Loss for Conventional Driver*

For conventional drive, comparing case 1 to case 3, and case 2 to case 4, it can be observed that with a smaller gate resistor, the total loss is smaller. The loss difference is due to the switching loss difference in these cases as all the other conditions are same. This is known to the engineering field.

B. *Resonant Gate Driver Can Reduce Switching Loss*

As can be observed from case 3, with the proposed resonant gate driver, the total loss is 1.92 W, while the total loss with conventional driver is 1.98 W. The difference of the total power loss is the switching loss reduction as all the other conditions are same. Therefore, the switching loss reduction is 0.06 W. In case 4, where the current is doubled, the total loss is also increased. The switching loss reduction with resonant gate driver is 0.18 W (2.5 W–2.32 W). It is noted that the power circuit is same for both cases. When the external gate resistor is 2.5 Ω, the switching loss reduction is even further.

The above observation indicates that the proposed resonant gate drive circuit can reduce the switching loss by reducing the switching time, which is achieved by charging and discharging the gate capacitor at high current level. It is expected that the switching loss reduction will become more significant when the load current is further increased.

VII. Conclusion

A new resonant gate drive circuit is proposed in this paper. The proposed drive circuit can provide two symmetrical drive signals to drive two MOSFETs. It charges and discharges the MOSFET gate capacitor at a high current level and clamp the drive voltage to either source voltage level or zero via a low impedance path. The proposed circuit can recover most of the gate drive energy. More importantly, it can reduce the switching time and thus reduce the switching loss. Operation principle and loss analysis are provided. Simulation and experimental results and key waveforms are provided as well. From measurement, the gate drive loss can be reduced by 67% as compared with

TABLE II
TOTAL POWER TRAIN LOSS COMPARISON, $V_{gs} = 12$ V, $V_o = 11.35$ V, $F_s = 1$ MHz

	Load Current	Conventional Driver		Resonant Driver	Loss Saving
		Rg_ext	P_loss	P_loss	
Case 1	0.4 A	2.5 Ω	2.07 W	1.92 W	0.15 W
Case 2	0.8 A	2.5 Ω	2.78 W	2.32 W	0.46 W
Case 3	0.4 A	1 Ω	1.98 W	1.92 W	0.06 W
Case 4	0.8 A	1 Ω	2.50 W	2.32 W	0.18 W

the conventional gate drive approach. In addition, the switching loss can also be reduced significantly. Computer simulation and experimental prototype verifies the feasibility of the new circuit and the significant advantages of the new resonant gate drive circuit.

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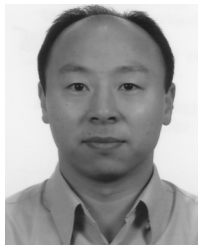

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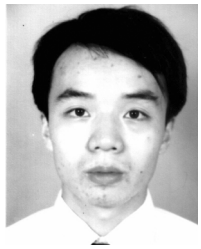

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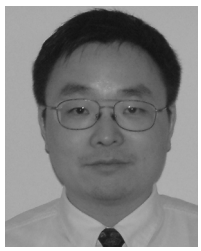

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