Optimal Design of Resonant Gate Driver for Buck Converter Based on a New Analytical Loss Model

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***Abstract*—In this paper, the advantages of a new resonant driver are verified thoroughly by the analytical analysis, simulation and experimental results. A new accurate analytical loss model of the power metal oxide semiconductor field effect transistor driven by a current-source resonant gate driver is developed. Closed-formed analytical equations are derived to investigate the switching characteristics due to the parasitic inductance. The modeling and simulation results prove that compared to a voltage driver, a current-source resonant driver significantly reduces the propagation impact of the common source inductance during the switching transition at high (>1 MHz) switching frequency, which leads to a significant reduction of the switching transition time and the switching loss. Based on the proposed loss model, a general method to optimize the new resonant driver is proposed and employed in the development of a 12 V synchronous buck voltage regulator (VR) prototype at 1 MHz switching frequency. The level-shift circuit and digital implementation of complex programmable logic device (CPLD) are also presented. The analytical modeling matches the simulation results and experimental results well. Through the optimal design, a significant efficiency improvement is achieved. At 1.5 V output, the resonant driver improves the VR efficiency from 82.7% using a conventional driver to 86.6% at 20 A, and from 76.9% using a conventional driver to 83.6% at 30 A. More importantly, compared with other state of the art VR approaches, the new resonant driver is promising from the standpoints of both performance and cost-effectiveness.**

***Index Terms*—Resonant gate driver, switching loss model, voltage regulator (VR).**

I. Introduction

In order to meet the strict transient requirements of future microprocessors [1] and reduce the passive components to achieve high power density on the mother board (MB), the switching frequency of a Voltage Regulator (VR) will move into the megahertz (MHz) range in the next few years [2]–[5].

However, an increase in switching frequency could lead to poor efficiency due to excessive switching loss and gate drive loss, which are proportional to switching frequency, and consequently degrade VRs' overall performance. More importantly, it has been noticed that the parasitic inductance, especially, the common source inductance has a serious propagation effect during the switching transition and thus results in high switching loss in a high (>1 MHz) frequency synchronous buck VR. In order to understand the parasitic effect thoroughly, accurate analytical models considering the common source inductance and the loop inductance are developed and the switching behavior is also analyzed in details in [6]–[9]. It should be noted that the common source inductance can be reduced but could not be eliminated completely. So methods to reduce the significant switching loss, due to the negative effect of the common source inductance, of a high frequency buck VR have become a critical issue.

In the last fifteen years, resonant gate drive circuits have originally been proposed with the objective of recovering gate energy lost in a conventional gate driver [10]–[15]. For the application of radio frequency (RF) power amplifier featuring sinusoidal waveforms commonly, the self-oscillating resonant gate driver using a resonant network provides an efficient method [16], [17]. For low voltage and high current VR applications, the synchronous field effect transistors (FETs) are generally optimized with a low on-resistance and large gate capacitance, especially when several devices are used in parallel. This causes a significant gate loss at high frequency. Therefore, the resonant driver technique becomes critical and effective to improve the efficiency for VR applications [18], [19]. Self-driven scheme proposed in [20], [21] for synchronous FETs can be applied to save gate drive loss by using the leakage inductance of the transformer as a current-source driver.

The resonant drivers in [19] and [22] feature simplicity and low circulating. However, the disadvantage is that the power metal oxide semiconductor field effect transistor (MOSFET) gate is not actively clamped high or low, which results in lower noise immunity. The resonant drivers using a coupled inductor [23] and using a transformer [24] are able to drive two MOSFETs. Nevertheless, the leakage inductance becomes a big concern at high (>1 MHz) frequency. A full-bridge topology drive circuit with one inductor is proposed to drive two ground-sharing MOSFETs in a 1 MHz Boost converter in [25]. An assessment of resonant drive techniques for use in low power dc/dc converters is presented in [26] and the mathematical model is built to estimate the power loss of the drive circuit in [27]. However, these investigations are generally emphasizing gate energy savings by the resonant driver and concentrating on the drive topologies, but ignore the potential switching loss savings that are much more dominant in a high frequency buck VR.

Recently, several new current source resonant gate drivers with continuous current [28]–[31] and with discontinuous current [32] are proposed, which are able to reduce the switching loss significantly by using a constant current to charge and

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discharge the input capacitor of a power MOSFET during the switching transition to achieve fast switching speed. However, there are still several important issues need to be explored. Firstly, the effect of the parasitic inductance on the resonant driver has not been investigated analytically and the switching behavior of a power MOSFET with a current source resonant driver has not been presented in the known literature. Secondly, the potential switching loss saving by a resonant driver considering the parasitic inductance at high (>1 MHz) frequency over a conventional voltage driver is not addressed clearly. Thirdly, a general method for the purpose of optimal design of a resonant driver should be proposed to achieve maximum improvement of the efficiency for a high frequency synchronous buck VR.

The objective of this paper is to solve the above problems and demonstrate the advantages of the new resonant driver for high frequency VR application. At first, the paper develops a new analytical loss model of the power MOSFET driven by a current-source resonant gate driver. Closed-formed analytical equations are derived to investigate switching characteristics due to the parasitic inductance. The comparison between a voltage driver and a resonant driver is presented concentrating on the common source inductance in detail. The modeling and simulation results prove that a current source resonant driver can significantly reduce the propagation impact of the common source inductance on the switching transition, which leads to a significant reduction of the switching transition time and the switching loss. Based on the proposed loss model, a generalized method to optimize the new current-source resonant gate driver is proposed and employed in the development of a 12 V synchronous buck VR prototype at 1 MHz switching frequency. A level-shift circuit for the resonant driver and the implementation of the complex programmable logic device (CPLD) are also presented. A digital method to generate the control signals with the precise dead time for the resonant drive circuit is also introduced. The analytical modeling matches the simulation results and the experimental results well. Through the optimal design, a significant improvement of the efficiency is achieved. At 1.5 V output, a VR with resonant gate driver achieves 86.6% efficiency at 20 A (up 3.9% from a conventional gate driver). At 30 A load current, the efficiency is 83.6% (up 6.7% from a conventional driver). Compared with other state of the art VR approaches, the new resonant driver is promising from the standpoints of both performance and cost-effectiveness.

In this paper, the analytical model is derived in details in Section II. The analytical modeling and simulation results are presented in Section III. The resonant gate driver under investigation is introduced in Section IV. The proposed optimization method based on the analytical loss model is presented in Section V. Experimental results and efficiency comparison to other stat of the art VR approaches are presented in Section VI. Finally, the conclusion is given in Section VII.

II. Proposed MOSFET Loss Model With Current Source Resonant Driver

The MOSFET switching loss models can be classified into 1) a physical-based model using physical parameters of the device, 2) a behavior model provided by device vendor supplies, and 3) an analytical model (also called a mathematical model). The physical-based model and the behavior model are

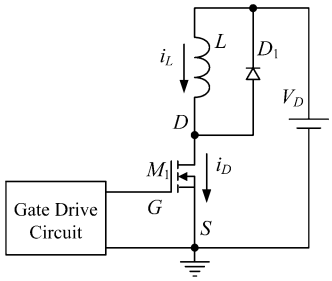

Fig. 1. Circuit with a clamped inductive load.

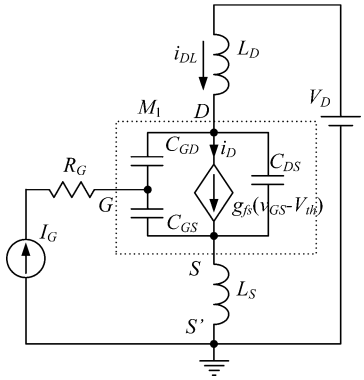

Fig. 2. Equivalent circuit of MOSFET switching transition.

convenient using simulation software, but simulation can not be used for the purpose of design and optimization directly. It should be stressed that the piecewise loss model by linearizing the switching waveforms is no longer valid due to the parasitic inductance at high frequency. Therefore, we need a new analytical loss model to predict the optimal design solution for a resonant driver.

A. Circuit and Basic Assumption

Fig. 1 shows a basic converter circuit including a MOSFET in series with a diode D_1, with dc input voltage V_D and an inductive load. The simplified equivalent circuit for the switching transition is shown in Fig. 2, where MOSFET M_1 is represented with a typical capacitance model, the clamped inductive load is replaced by a constant current source and the current source gate driver is simplified as a current source (I_G) since the charge and discharge current is kept constant during the switching transition. L_D is the switching loop inductance including the packaging inductance and any unclamped portion of the load inductance. L_S is the common source inductance, which is shared by the main current path and the gate diver loop. The critical MOSFET parameters are as follows: 1) the gate-to-source capacitance $C_{\rm GS}$, the gate-to-drain capacitance $C_{\rm GD}$, the drain-to-source capacitance $C_{\rm DS}$; 2) the gate equivalent series resistance (ESR) R_G (external and internal); 3) the threshold voltage $V_{\rm th}$; and 4) transconductance g_{fs}.

For purpose of transient analysis, we make the following simplifying assumptions:

1) $i_D = g_{fs}(v_{\rm GS} - V_{\rm th})$ and MOSFET is ACTIVE, provided $v_{\rm GS} > V_{\rm th}$ and $v_{\rm DS} > i_D R_{\rm DS(on)}$;
2) for $v_{\rm GS} < V_{\rm th}$, $i_D = 0$, and MOSET is OFF;
3) when $g_{fs}(v_{\rm GS} - V_{\rm th}) > v_{\rm DS}/R_{\rm DS(on)}$, the MOSFET is fully ON.

B. Analytical Modeling of Main Switching Transition

During the main switching transition period, the MOSFET enters its active state and the linear transfer characteristics is assumed as given in (1), [33], where $i_D(t)$ is the instantaneous switching current of the MOSFET and $v_{\rm GS}(t)$ is the instantaneous gate-to-source voltage of the MOSFET

$$i_D(t) = g_{fs}(v_{\rm GS}(t) - V_{\rm th}). \tag{1}$$

According the equivalent circuit in Fig. 2, the circuit equations take the form

$$I_G = C_{\rm GD}\frac{dv_{\rm GD}}{dt} + C_{\rm GS}\frac{dv_{\rm GS}}{dt} \tag{2}$$

and

$$v_{\rm GD} = v_{\rm GS} - v_{\rm DS}. \tag{3}$$

So

$$I_G = (C_{\rm GS} + C_{\rm GD})\frac{dv_{\rm GS}}{dt} - C_{\rm GD}\frac{dv_{\rm DS}}{dt}. \tag{4}$$

From (4), $dv_{\rm DS}/dt$ is solved as

$$\frac{dv_{\rm DS}}{dt} = \frac{C_{\rm GS} + C_{\rm GD}}{C_{\rm GD}} \cdot \frac{dv_{\rm GS}}{dt} - \frac{I_G}{C_{\rm GD}}. \tag{5}$$

So $d^2v_{\rm DS}/dt^2$ and $d^3v_{\rm DS}/dt^3$ are, respectively

$$\frac{d^2v_{\rm DS}}{dt^2} = \frac{C_{\rm GS} + C_{\rm GD}}{C_{\rm GD}} \cdot \frac{d^2v_{\rm GS}}{dt^2} \tag{6}$$

$$\frac{d^3v_{\rm DS}}{dt^3} = \frac{C_{\rm GS} + C_{\rm GD}}{C_{\rm GD}} \cdot \frac{d^3v_{\rm GS}}{dt^3}. \tag{7}$$

During the switching interval, the change of the switching loop current $i_{\rm DL}$ induces a voltage across the parasitic inductance. The drain-to-source voltage $v_{\rm DS}$ is given as

$$\begin{aligned} v_{\rm DS} &= V_D - L_D\frac{di_{\rm DL}}{dt} - L_s\frac{d(i_{\rm DL} + I_G)}{dt} \\ &= V_D - (L_D + L_s)\frac{di_{\rm DL}}{dt} \end{aligned} \tag{8}$$

And

$$\begin{aligned} i_{\rm DL} = {} & C_{\rm GS}\frac{dv_{\rm GS}}{dt} + C_{\rm DS}\frac{dv_{\rm DS}}{dt} \\ & + g_{fs}(v_{\rm GS} - V_{\rm th}) - I_G. \end{aligned} \tag{9}$$

Substituting (9) to (8) yields

$$\begin{aligned} v_{\rm DS} = V_D - (L_D + L_s)\Bigg(& C_{\rm GS}\frac{d^2v_{\rm GS}}{dt^2} \\ & + C_{\rm DS}\frac{d^2v_{\rm DS}}{dt^2} + g_{fs}\frac{dv_{\rm GS}}{dt}\Bigg). \end{aligned} \tag{10}$$

Substituting (6)–(10) yields

$$\begin{aligned} v_{\rm DS} = V_D - (L_D + L_s)\Bigg(& \frac{C_{\rm GS}C_{\rm GD} + C_{\rm DS}C_{\rm GD} + C_{\rm DS}C_{\rm GS}}{C_{\rm GD}} \\ & \cdot \frac{d^2v_{\rm GS}}{dt^2} + g_{fs}\frac{dv_{\rm GS}}{dt}\Bigg). \end{aligned} \tag{11}$$

Differentiating (11) yields

$$\begin{aligned} \frac{dv_{\rm DS}}{dt} = -(L_D + L_s)\Bigg(& \frac{C_{\rm GS}C_{\rm GD} + C_{\rm DS}C_{\rm GD} + C_{\rm DS}C_{\rm GS}}{C_{\rm GD}} \\ & \cdot \frac{d^3v_{\rm GS}}{dt^3} + g_{fs}\frac{d^2v_{\rm GS}}{dt^2}\Bigg). \end{aligned} \tag{12}$$

Substituting (5) into (12), (13) is derived as

$$A\frac{d^3v_{\rm GS}(t)}{dt^3} + B\frac{d^2v_{\rm GS}(t)}{dt^2} + C\frac{dv_{\rm GS}(t)}{dt} = I_G \tag{13}$$

where parameters A, B and C are represented in terms of the device parameters ($C_{\rm GS}, C_{\rm GD}, C_{\rm DS}, g_{fs}$ and R_G) and the equivalent circuit parameters (L_D and L_S) as $A = (L_D + L_s)(C_{\rm GS}C_{\rm GD} + C_{\rm DS}C_{\rm GD} + C_{\rm DS}C_{\rm GS}), B = g_{fs}(L_D + L_s)C_{\rm GD}$ and $C = C_{\rm GS} + C_{\rm GD}$.

For turn-on transition, the initial condition for (13) is $v_{\rm GS}(0) = V_{\rm th}$. Then (13) solves to give either sinusoidal or exponential solutions, depending on the relative magnitudes of B^2 and AC.

When $B^2 - 4AC < 0$, sinusoidal solution occurs and $v_{\rm GS}(t)$ takes the form

$$\begin{aligned} v_{\rm GS}(t) = {} & \frac{B}{C^2} \cdot I_G \cdot \exp\left(-\frac{t}{T_2}\right) \cdot \mathrm{Cos}(\omega_1 t) \\ & + \left(\frac{B^2}{2C^2 \cdot \sqrt{4AC - B^2}} - \frac{\sqrt{4AC - B^2}}{2C^2}\right) \\ & \cdot I_G \cdot \exp\left(-\frac{t}{T_1}\right) \cdot \mathrm{Sin}(\omega_1 t) \\ & + \frac{I_G \cdot t}{C} - \frac{B}{C^2} \cdot I_G + V_{\rm th} \end{aligned} \tag{14}$$

where

$$T_1 = \frac{2A}{B}, \quad \omega_1 = \frac{\sqrt{4AC - B^2}}{2A}.$$

When $B^2 - 4AC > 0$, exponential solution occurs. Then $v_{\rm GS}(t)$ takes the form

$$\begin{aligned} v_{\rm GS}(t) = {} & -\frac{(\sqrt{B^2 - 4AC} + B) \cdot I_G \cdot A \cdot \exp\left(-\frac{t}{T_2}\right)}{(\sqrt{B^2 - 4AC} - B) \cdot C \cdot \sqrt{B^2 - 4AC}} \\ & + \frac{(\sqrt{B^2 - 4AC} - B) \cdot I_G \cdot A \cdot \exp\left(-\frac{t}{T_3}\right)}{(\sqrt{B^2 - 4AC} + B) \cdot C \cdot \sqrt{B^2 - 4AC}} \\ & + \frac{I_G \cdot t}{C} - \frac{B \cdot I_G}{C^2} + V_{\rm th} \end{aligned} \tag{15}$$

where

$$T_2 = \frac{2A}{B - \sqrt{B^2 - 4AC}}, \quad T_3 = \frac{2A}{B + \sqrt{B^2 - 4AC}}.$$

Then, by substituting $v_{\rm GS}(t)$ to (1) and (11), $i_D(t)$ and $v_{\rm DS}(t)$ of the MOSFET can be calculated, respectively. The turn-off transition is similar to the turn-on transition except for the initial condition becomes $v_{\rm GS}(0) = V_{\rm th} + (I_L/g_{fs})$.

TABLE I
CIRCUIT SPECIFICATIONS AND DEVICE PARAMETERS IN ANALYTICAL MODELING

V_D=12V, I_L=20A, f_s=1MHz						
C_{GS} (pF)	C_{GD} (pF)	C_{DS} (pF)	V_{th} (V)	g_{fs} (S)	R_G: current driven (Ω)	R_G: voltage driven (Ω) (external and internal)
1600	200	500	1.8	60	1	1.5 ohm

TABLE II
EFFICIENCY COMPARISON BETWEEN THE RESONANT DRIVER AND DIFFERENT STATE OF THE ART VR APPROACHES

Input voltage: 12V and switching frequency: 1MHz			
VR Topologies	Conversion Efficiency	Output current/ Phase	Output voltage
Tapped-inductor (TI) buck converter [34]	84%	12.5A	1.5V
Toshiba synchronous buck Multi Chip Module (TB7001FL) [37]	85%	20A	1.5V
Proposed resonant driver (Figure 21)	87%	12.5A	1.5V
	86.6%	20A	1.5V
Soft-switching phase-shift buck (PSB) converter [35]	82%	17.5A	1.3V
Self-driven soft-switching buck-derived multiphase converter [36]	84.7%	25A	1.3V
Proposed resonant driver (Figure 21)	86%	17.5A	1.3V
	84.3%	25A	1.3V

III. ANALYTICAL MODELING AND SIMULATION RESULTS

The modeling results in Section II are presented in this section. The turn-on and turn-off transients are divided into several intervals, during which the gate-to-source voltage $v_{\rm GS}(t)$, the drain current $i_D(t)$ and the drain voltage $v_{\rm DS}(t)$ can be calculated analytically with corresponding boundary conditions and constraints. Once the instantaneous waveforms of $v_{\rm GS}(t), i_D(t)$ and $v_{\rm DS}(t)$ are solved, the switching transition time and the switching loss can be easily obtained.

In the experimental prototype, MOSFET Si7860 from Vishay is used and the circuit specifications and the device parameters are listed in Table I. The estimated value of the parasitic inductances are $L_S = 1$ nH and $L_D = 2$ nH by Maxwell simulation software. In this case, since B^2 is more than $4AC$ depending on the above parameters, the exponential solution occurs as (15).

Fig. 3 shows the switching loss comparison between the above model using Mathcad software and the simulation results based on Si7860AD SPICE model provided by Vishay. It is noted that the modeling results are in good agreement with the simulation results.

For comparison, Fig. 4 shows the simulation waveforms of the switching transition between of the resonant driver and the conventional driver with the same parasitic inductance of L_s =1 nH and L_D =2 nH. It is observed that the turn-on transition time of the resonant driver is reduced to 2.3 ns [see Fig. 4(a)] compared to 12.2 ns [see Fig. 4(c)] of the voltage driver (a reduction of 81%) and similarly, the turn-off transition time of the resonant driver is reduced to 5 ns [see Fig. 4(b)] compared to 13.4 ns [see Fig. 4(d)] of the voltage driver (a reduction of 62%). Accordingly, from calculation, the turn-on loss is reduced from 0.65 W to 0.1 W (a reduction of 84.6%) and the turn-off loss is reduced 2.1 W to 1.16 W (a reduction of 44.8%), which is a significant reduction. So the total switching loss saving is 1.49 W (a reduction of 54.2%).

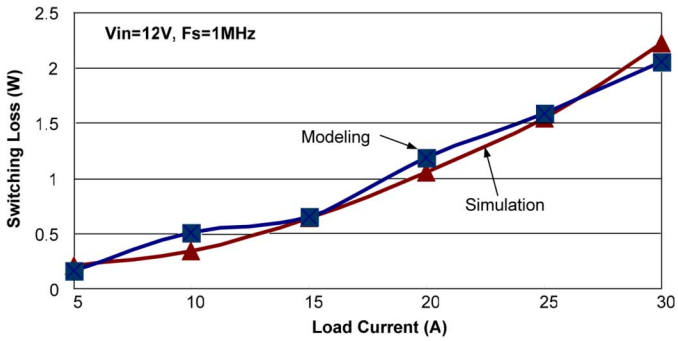

Fig. 3. Switching loss comparison between modeling and simulation.

It is noted that the common source inductance has a significant negative impact on the switching transition of the conventional driver. Fig. 5 shows the gate charge current during the turn-on transition and turn-off transition of the conventional driver respectively when the common source inductance is not zero.

It is observed from Fig. 5(a) that during turn-on transition, before the actual gate-to-source voltage $v_{\rm GS}$ reaches the miller plateau voltage, the drain current i_d still remain zero and the gate charging current is about 3 A. However, as soon as i_d starts to rise, the induced voltage $v_{Ls}(v_{Ls} = L_s \cdot di_d/dt)$ over the common source inductance L_s occurs due to the rise of the drain current, which is against the gate drive voltage $v_{GS'}$. Since $v_{\rm GS} = v_{GS'} - L_s \cdot di_d/dt$, the actual gate-to-source voltage $v_{\rm GS}$ is reduced significantly. As a result, the gate charging current i_G is reduced to as low as 10 mA, which increases the turn-on transition time and the turn-on loss dramatically.

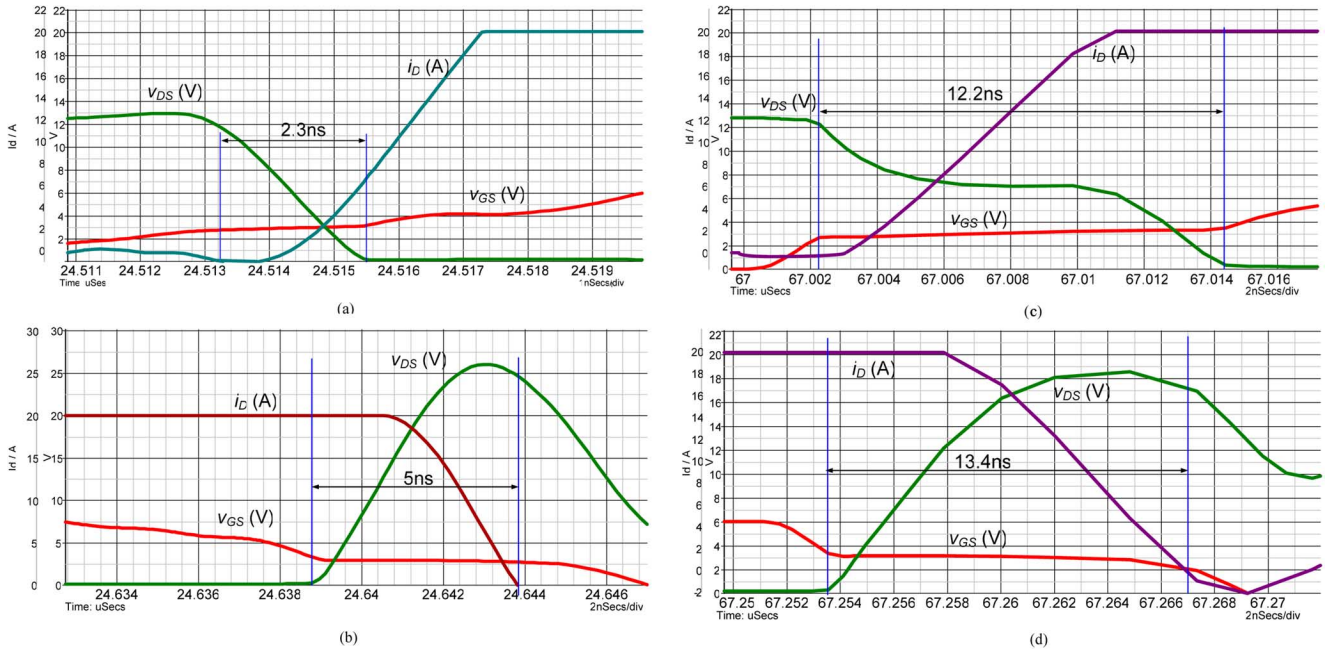

Fig. 4. Simulation comparison between the resonant driver and the conventional driver: the gate-to-source voltage $v_{\rm GS}$, the drain-to-source voltage $v_{\rm DS}$, the drain current i_D ($V_{\rm in}$ = 12 V, I_o = 20 A, f_s = 1 MHz, L_s = 1 nH, L_D = 2 nH, R_G = 1.5 Ω): (a) turn-on transition: resonant driver, (b) turn-off transition: resonant driver, (c) turn-on transition: conventional driver, and (d) turn-off transition: conventional driver.

It is observed from Fig. 5(b) that during turn-off transition, before the actual gate-to-source voltage $v_{\rm GS}$ declines to the miller plateau voltage, the drain current i_d still remains as the load current and the gate discharging current is around 3 A. But, as soon as the drain current begins to decrease, the induced voltage v_{Ls} over L_s occurs, which is also against the gate drive voltage. This also results in the reduction of the gate discharging current to as low as 15 mA and thus increases the turn-off transition time and the turn-off loss significantly.

As a conclusion, for both of the turn-on transition and the turn-off transition, the voltage v_{Ls} induced over common source inductance is always against the gate drive voltage $v_{\rm GS'}$, and thus decreases the actual gate-to-source voltage $v_{\rm GS}$ and the gate charge current i_G, which consequently slows down the turn-on speed and the turn-off speed of the MOSFET and increases the switching transition time and the switching loss dramatically.

However, as for a current source resonant driver, the great advantage is that the common source inductance is absorbed by the resonant inductor to ensure the constant drive current during the switching transition. Therefore, the propagation impact of the common source inductance on the switching transition is eliminated, which leads to a significant reduction of the switching time and the switching loss.

Fig. 6 gives the comparison of the turn-on and turn-off loss as a function of the common source inductance on the basis of the above analytical loss model. With today's MOSFET packaging and compact PCB layout, the parasitic inductance is usually less than 2 nH and the parasitic values can be extracted by Maxwell simulation software. It is observed that with the resonant driver, the common source inductance L_s does not increase the switching loss of the MOSFET. Therefore, the resonant driver significantly reduces the switching loss compared to a conventional voltage source driver due to the common source inductance.

IV. A Current Source Resonant Gate Driver

Fig. 7 shows the resonant driver under investigation, which is proposed in [28]. In next section, this resonant driver is optimized for a buck converter operating at 1 MHz switching frequency and 12 V input.

Fig. 8 shows the key waveforms. C_{g1} and C_{g2} are the gate-source capacitors of the control FET Q_1 and the synchronous FET Q_2 respectively, and they are not external capacitors. In Fig. 8, the gate-to-source signals of Q_1 and Q_2 have a small crossover level, which is less than the threshold voltage of the devices, to minimize the dead time and reduce the conduction loss and reverse recovery of the body diode. It should also be pointed that an additional margin should be set for this crossover level according to the threshold voltage at high temperature, which reduces with temperature increasing.

The advantages of this drive circuit are highlighted as follows: 1) fast switching of the power MOSFET, which reduces the switching time and the switching loss significantly; 2) gate energy recovery; 3) reduced dead time; 4) zero-voltage-switching (ZVS) of the drive switches ($S_1 - S_4$); and 5) high Cdv/dt immunity.

More importantly, it should be pointed that the resonant driver is a most cost-effective approach to increase the efficiency at high frequency significantly based on today's multiphase buck VRs compared to other buck derived topologies in the known literature. The comparison among different state of the art VR approaches will be discussed concentrating on the experimental efficiency results in Section VII. The proposed loss model will be used to optimize the design in the following section.

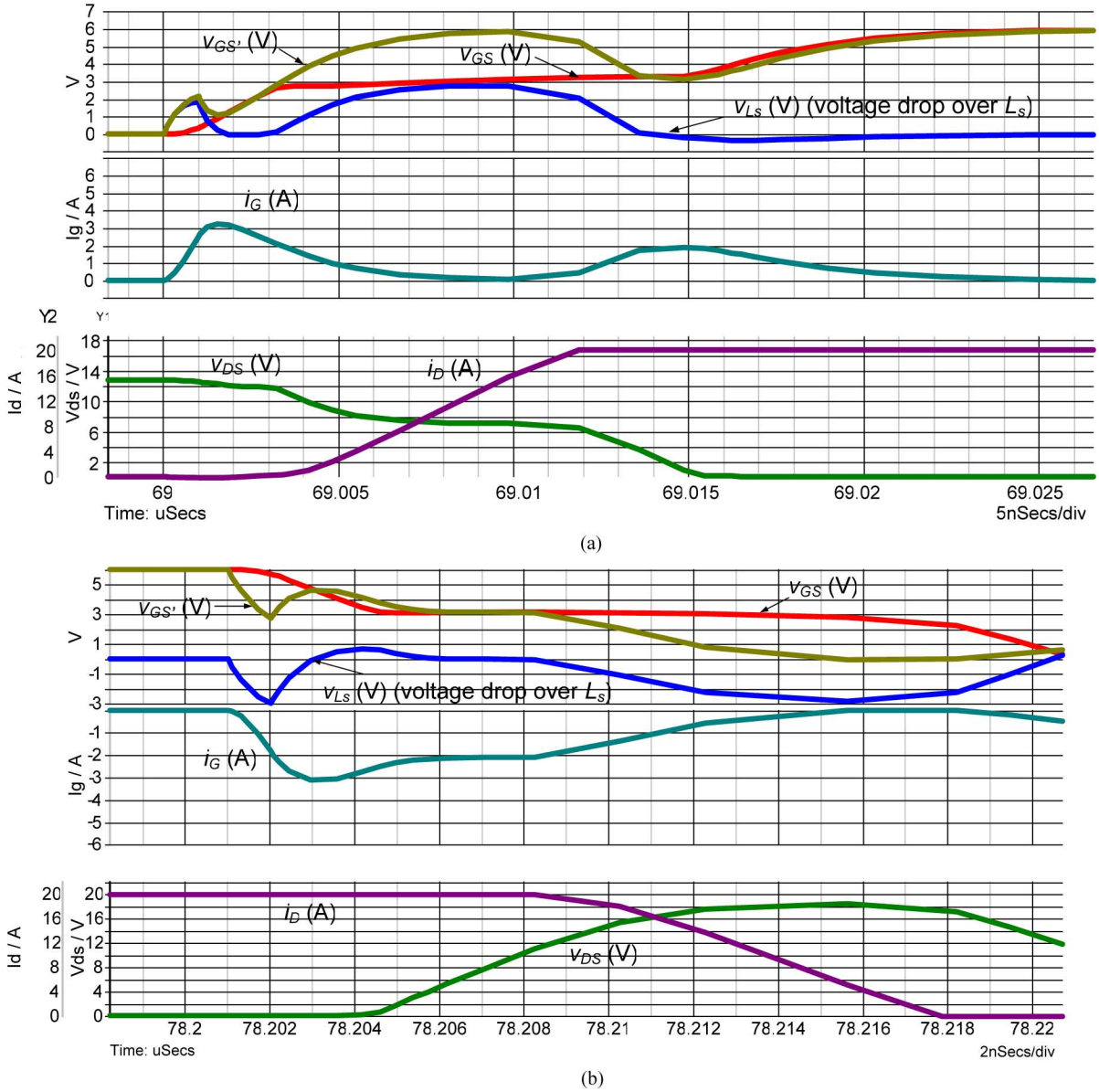

Fig. 5. Simulation of delay effect of the common source inductance on the conventional driver ($V_{\rm in}$ = 12 V, I_o = 20 A, f_s = 1 MHz, L_s = 1 nH, L_D = 2 nH): (a) turn-on transition: conventional driver and (b) turn-off transition: conventional driver.

V. Proposed Optimization Method

In order to achieve design optimization, the loss analysis of the resonant gate driver is given. The total power loss of the proposed resonant driver includes: 1) the resistive loss and the gate drive loss of switches $S_1 - S_4$; 2) the loss of the resonant inductor; and 3) the resistive loss caused by the internal gate mesh resistance of the power MOSFETs. The detail loss analysis was presented in [28].

As seen from the principle of operation in Fig. 8, the peak current I_{Lr_pk} of the resonant inductor L_r is regarded as the current source magnitude I_G. So the higher I_{Lr_pk} is, the shorter of switching transition is, thus more switching loss can be saved. On the other hand, higher I_{Lr_pk} will result in a larger RMS value of the inductor circulating current i_{Lr} since the waveform of i_{Lr} is triangular, which increases the resistive circulating loss in the drive circuit and decreases the gate energy recovery efficiency. Therefore it is critical to decide I_{Lr_pk} (i.e., I_G) properly so that the maximum loss saving can be achieved.

The general method proposed here is to find the optimal solution on the basis of the object function that adds the switching loss and the resonant drive circuit loss together. The object function should be a U-shape curve as function of the drive current I_G, and the optimization solution is simply located at the lowest point of the curve. It is noted that the analytical loss model proposed in Section II is used to calculate the switching loss since the piecewise loss model is no longer valid due to the parasitic inductance at high frequency. The demonstration of the optimization methodology is employed to the new resonant gate driver. The specifications are: $V_{\rm in}$ = 12 V; V_o = 1.5 V; I_o = 30 A; V_c = 8 V; f_s = 1 MHz; Q_1:Si7860DP; Q_2:Si7336ADP.

First, the switching loss of the control FET as function of drive current I_G is given in

$$P_{Q1} = \int_0^{t_{\rm sw(on)\_Q1}} v_{\rm ds(on)\_Q1} \cdot i_{d(\rm on)\_Q1} dt \cdot f_s + \int_0^{t_{\rm sw(off)\_Q1}} v_{\rm ds(off)\_Q1} \cdot i_{d(\rm off)\_Q1} dt \cdot f_s \quad (16)$$

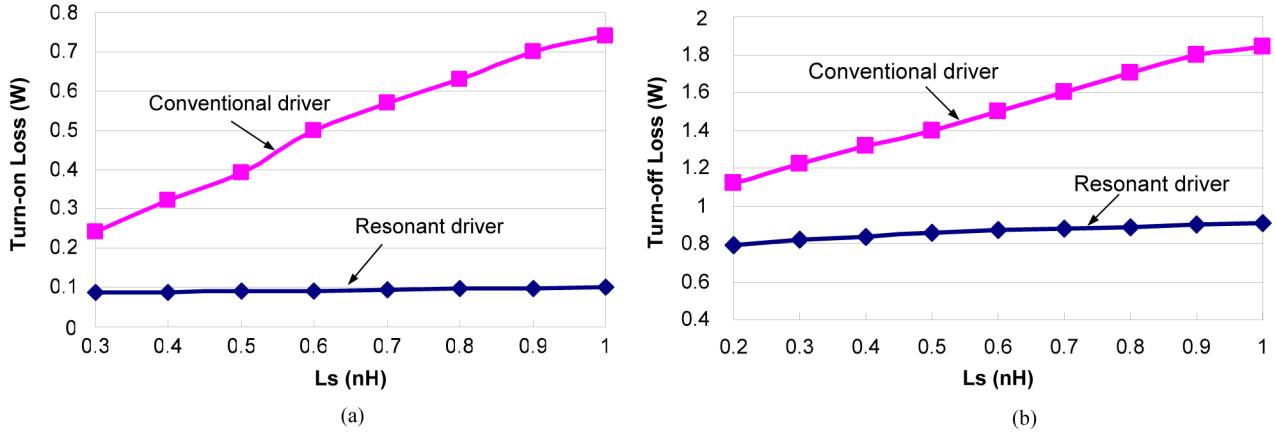

Fig. 6. Switching loss comparison as function with different common source inductances ($V_{\text{in}} = 12$ V, $I_o = 20$ A, $f_s = 1$ MHz, $L_D = 2$ nH): (a) turn-on loss and (b) turn-off loss.

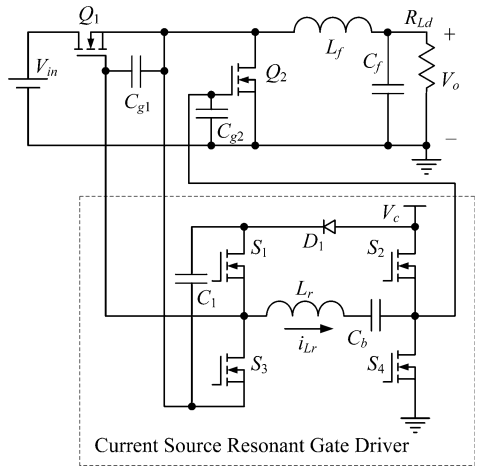

Fig. 7. Synchronous buck converter with the proposed current source resonant gate driver.

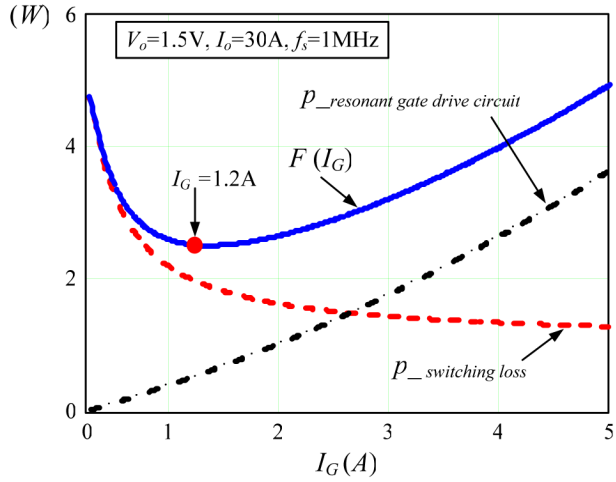

Fig. 9. Objective function $F(I_G)$ as function of current I_G.

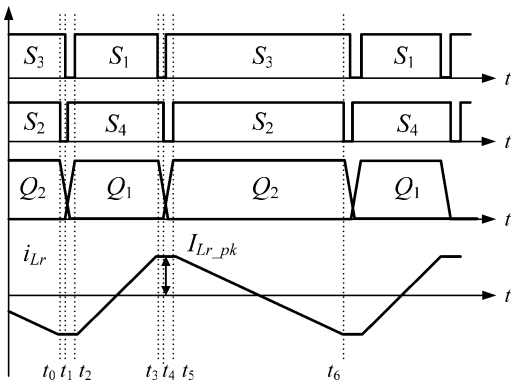

Fig. 8. Key waveforms.

where $v_{\text{ds(on)}\_Q1}$ and $v_{\text{ds(off)}\_Q1}$ are the drain-to-source voltages during turn-on interval and turn-off interval respectively; $i_{\text{(on)}\_Q1}$ and $i_{d\text{(off)}\_Q1}$ are the drain currents at turn-on interval and turn-off interval respectively; $t_{\text{sw(on)}\_Q1}$ is the turn-on switching transition time and $t_{\text{sw(off)}\_Q1}$ is the turn-off switching transition time. In Fig. 9, the switching loss $P_{\text{switching}}$ as function of driven current I_G is given, illustrating that the switching loss reduces when I_G increases.

Secondly, the total loss of the resonant gate drive circuit as function of drive current I_G is calculated [28]. In Fig. 9, the loss of the total gate drive circuit $P_{\text{circuit}}(I_G)$ as function of drive current I_G is given, illustrating that the resonant drive circuit loss increases when I_G increases.

Thirdly, in order to find the optimized gate drive current, the objective function is established by adding the switching loss and the resonant driver circuit loss together as

$$F(I_G) = P_{\text{circuit}}(I_G) + P_{\text{switching}}(I_G). \tag{17}$$

In Fig. 9, the objective function $F(I_G)$ with the drive current I_G is given, which is a U-shaped curve. Therefore, the optimization solution can be found at the lowest point of the curve, and accordingly, the gate drive current I_G is chosen as 1.2 A.

Finally, from the selected gate drive current, the calculated resonant inductor value from (18) is 1.5 μH

$$L_r = \frac{(V_{\text{in}} + 2V_c) \cdot D \cdot (1 - D)}{2 \cdot I_G \cdot f_s} \tag{18}$$

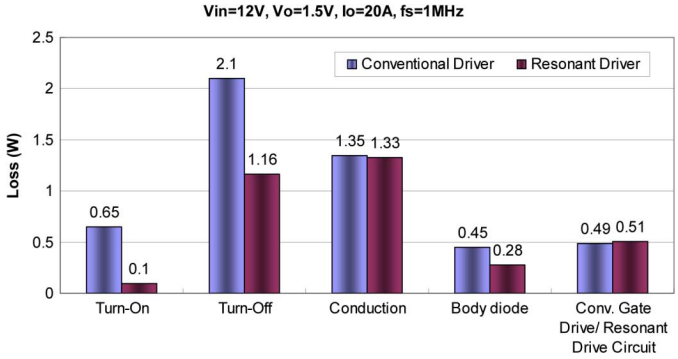

Fig. 10. Loss breakdown between the resonant gate driver and the conventional gate driver ($V_{\rm in} = 12$ V, $V_o = 1.5$ V and $I_o = 20$ A).

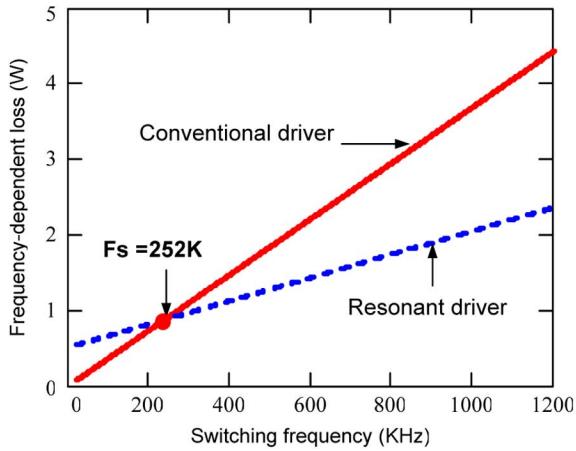

Fig. 11. Loss comparison between resonant driver and conventional driver with different switching frequencies ($V_{\rm in} = 12$ V, $V_o = 1.5$ V and $I_o = 20$ A).

where $V_{\rm in} = 12$ V, $f_s = 1$ MHz, $V_o = 1.5$ V, $V_c = 8$ V and $I_G = 1.2$ A.

Fig. 10 illustrates the loss breakdown comparison based on the analytical loss model between the above optimized resonant driver and the conventional diver. At $V_o = 1.5$ V and $I_o = 20$ A, the turn-on loss is reduced by 0.55 W and the turn-off loss is reduced by 0.94 W. The total loss reduction is 1.66 W, which is 5.5% (1.66 W/1.5 V/20 A) of the output power.

Fig. 11 shows the loss comparison between the resonant driver and the conventional driver as function of the switching frequency based on the above circuit parameters. It is interesting to observe that as long as the switching frequency is above 252 KHz, the loss of the resonant driver is always lower than that of the conventional driver, which means that the resonant driver can always achieve loss saving over the conventional driver. The higher switching frequency, the more loss saving we have. However, when the switching frequency is lower than 252 KHz, the loss of the resonant driver is higher than that of the conventional driver. The reason is that though the frequency-dependent loss is reduced, it is offset by the circulating loss of the resonant driver circuit itself, which means the resonant drive can not achieve the loss saving when the switching frequency is below 252 KHz.

VI. Hardware Implementation

A. Bootstrap and Level-Shift Circuit

From the viewpoint of a standard gate driver for a synchronous buck converter, the control PWM signal is the input of the driver and two complimentary gate drive signals with minimum dead time are the output of the driver. Therefore, all the control signals for the four switches $(S_1 - S_4)$ in the resonant drive circuit should be implemented internally based on the input PWM signal. As seen from Fig. 7, since the switches $S_1 - S_3$ (N-channel) have the floating source and do not share the same ground with switch S_4, the bootstrap gate drive technique need to be used in the control circuit. It should be noted that if switches S_1 and S_3 are P-channel MOSFETs with a little bit higher $R_{\rm ds(on)}$, only one set of level shift circuit is required for the whole drive circuit. In the paper, N channel MOSFET is used.

Fig. 12 gives the complete schematic of the level-shift drive circuit. It should be pointed out that in order to maintain high efficiency and minimize power dissipation; the level shifters should not draw any current during the on-time of the control switch.

As indicated in Fig. 12, the input PWM signal are fed to the CPLD and is translated to ON and OFF commands as two short pulses at the rising and the falling edges with certain delay time. Through the pulse filter, these two pulses drive the level shift transistor pair which interfaces with the level-shifted circuitry. This operation leads to lower power dissipation because of the short duration of the current in the level shifter. Then these two level-shifted signals are fed to a SR latch to generate the level-shifted PWM gate signal. Finally, the level-shifted PWM signal goes to the bipolar totem-pole circuit to drive the switches $(S_1 - S_3)$ in the resonant drive circuit. In addition to the drive signal level-shifter, the bootstrap circuit including a bootstrap diode and bootstrap capacitor to provide the supply voltage for the level-shift circuit.

B. CPLD Implementation

The four control signals should be generated based on the PWM signal and the delayed circuit should be used to give the proper delay time between two complimentary signals, i.e., S_1 and S_3, S_2, and S_4 as seen from Fig. 8. As the switching time of the main power MOSFETs is less than 10 ns, it is important to adjust the dead time precisely. Usually, RC delay circuit is popular to achieve the delay function due to its simplicity, but the drawback of RC delay is difficult to adjust the time accurately and conveniently due to the tolerance of the resister and the capacitor. Delay line such as Maxim Ds1100 is another option to achieve the delay, but it is difficult to do the component replacement and modification once the PCB is completed. We present a simple digital method to achieve the programmable delay function and generate the desired the control signals by using the CPLD MAX II from Altera. Owing to the programmable capability of CPLD, the delay time of the control signals can be adjusted precisely and conveniently.

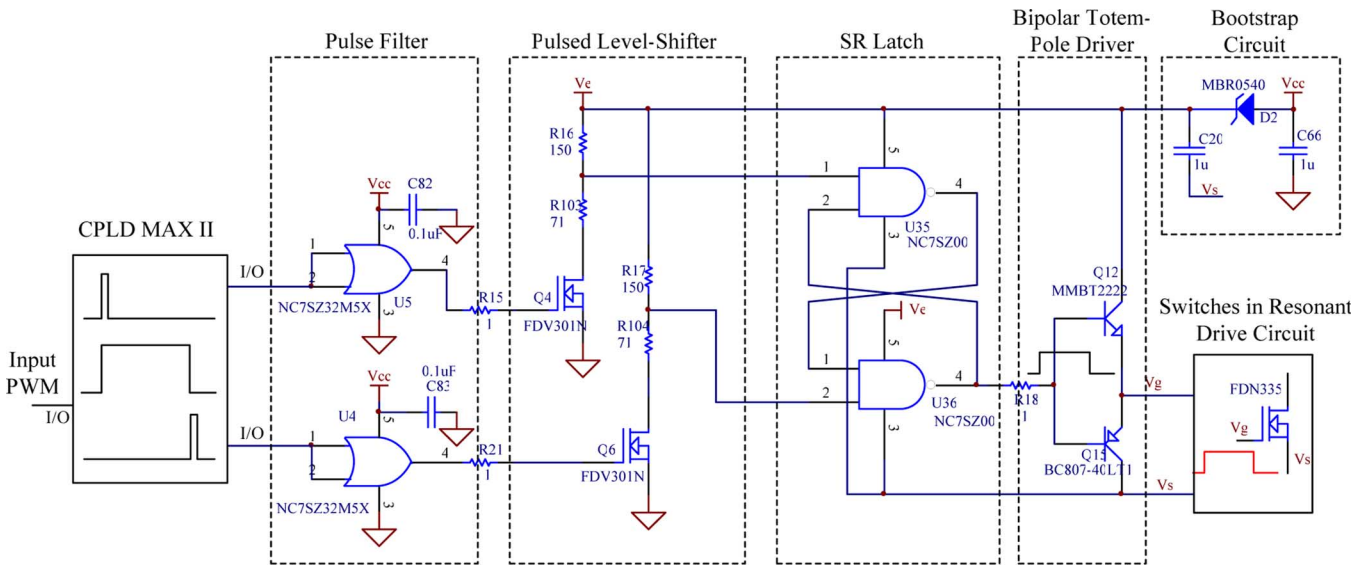

Fig. 12. Schematic of the level-shift drive circuit.

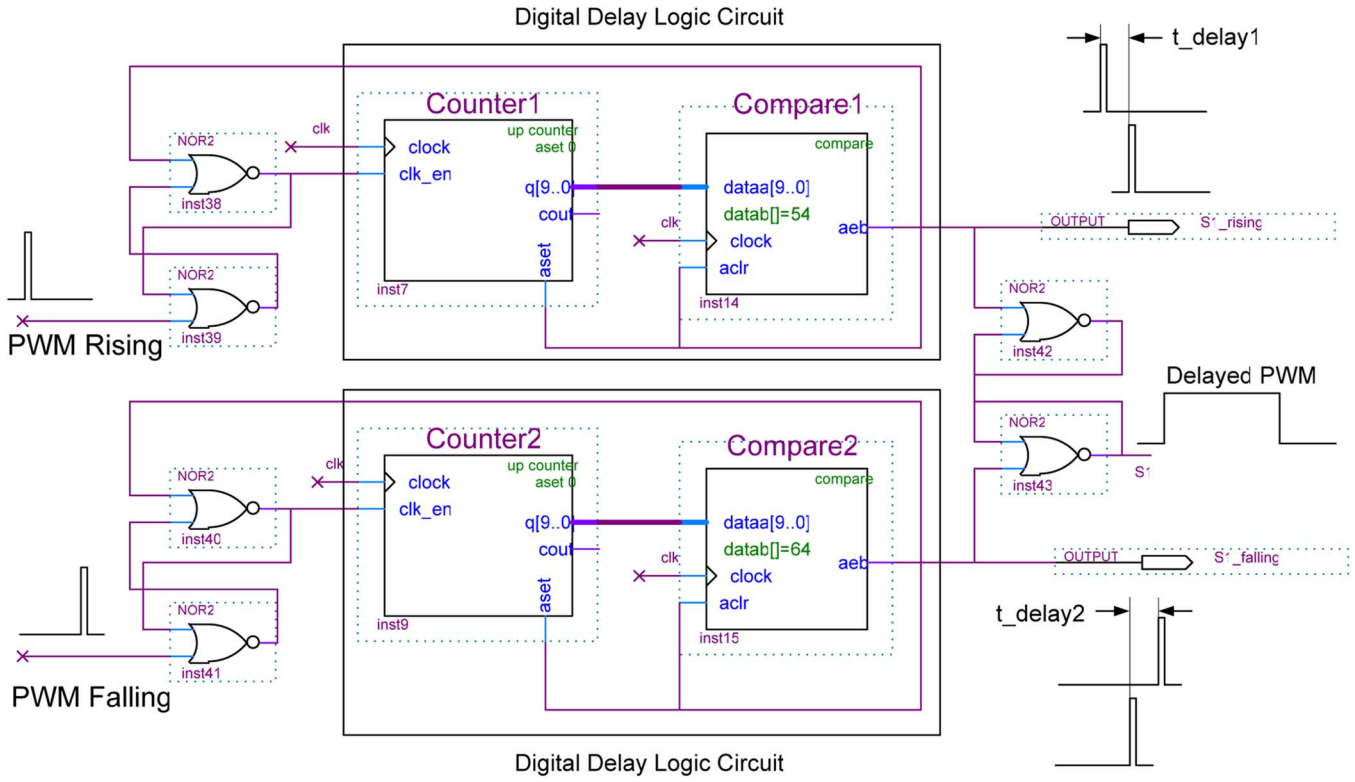

Fig. 13. Schematic of the delay circuit for one channel in Quartus II software.

Fig. 13 shows the schematic of the digital circuit in Quartus II software. The basic idea is presented as follows. First, the rising edge of the input PWM signal is used to enable one counter chain. Then, later on, the falling edge of the input PWM signal is used to enable the other counter chain. When the first chain times out, a single pulse is generated to set an SR latch and reset that chain meanwhile. When the second chain times out, a single pulse is generated to set an SR latch and reset that chain. Then, the output of the latch will be the delayed version of the input PWM signal if the two counter chains have the same delay. On the other hand, by setting the different delay time of the two counters, the output of the latch will be the PWM signal with the desired width and delay time. In our implementation, the delayed rising/falling pulses are directly sent to the level-shift circuit because the SR latch has been included in the level-shift circuit as shown in Fig. 12.

The asynchronous counter clock based on a ring oscillator is used here as shown in Fig. 14. The PWM rising edge is used to

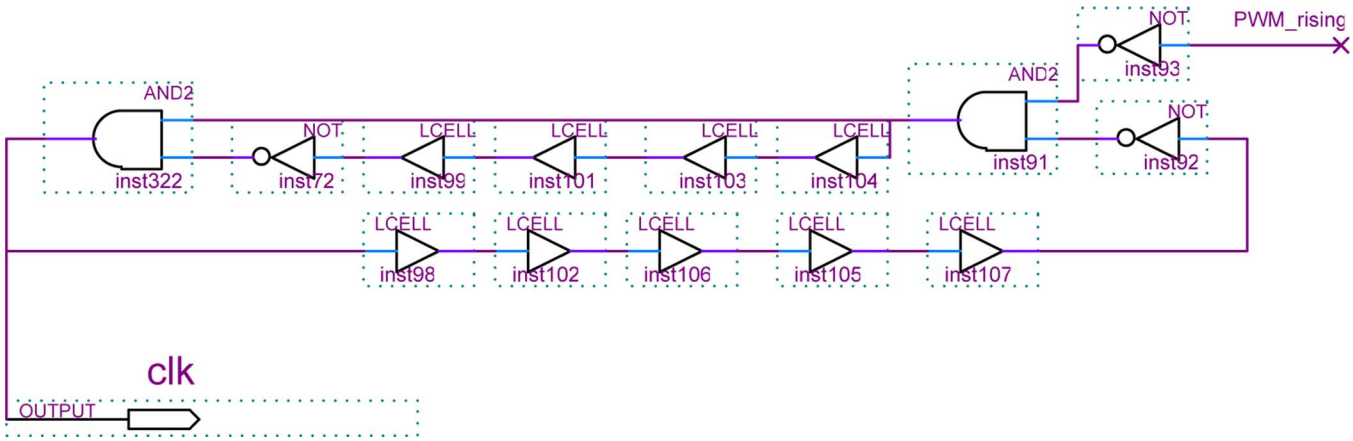

Fig. 14. Schematic of asynchronous counter.

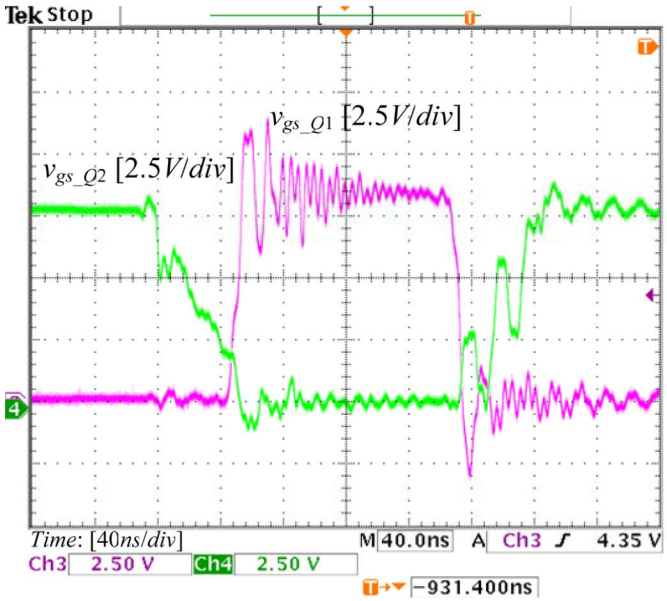

Fig. 15. Waveforms of the gate signals $v_{\mathrm{gs\_}Q1}$ (control FET) and $v_{\mathrm{gs\_}Q2}$ (synchronous FET).

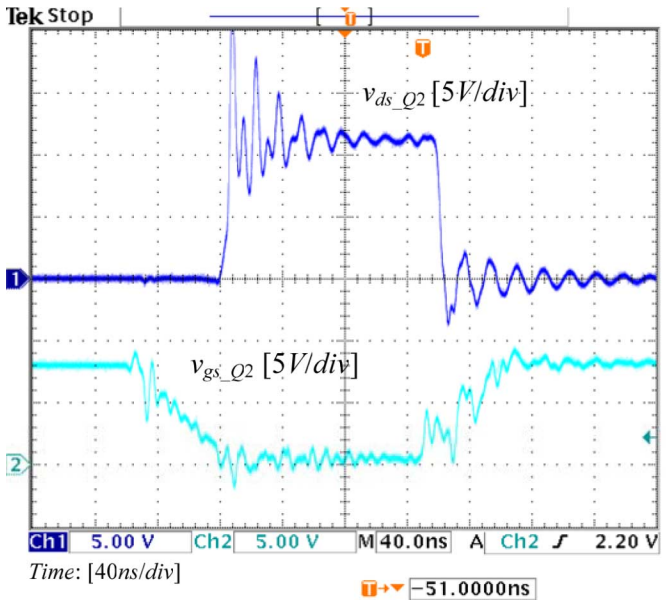

Fig. 16. Waveforms of the drain-source voltage $v_{\mathrm{ds\_}Q2}$ and the gate signal $v_{\mathrm{gs\_}Q2}$ (synchronous FET).

trigger the asynchronous counter to generate the counter clock signal. The clock signal in the experimental hardware is set to 3 ns, which equals the resolution of the dead time.

VII. Experimental Verification and Discussion

A 1 MHz synchronous buck converter with the new resonant driver was built to verify the modeling results and demonstrate the advantages of the proposed resonant driver. The specifications are as follows: input voltage $V_{\mathrm{in}} = 12$ V; output voltage $V_o = 1.5$ V; output current $I_o = 30$ A; switching frequency $f_s = 1$ MHz; resonant driver voltage $V_c = 8$ V. The PCB uses six-layer 2 oz copper. The components used in the circuit are listed as follows.

Control FET Q_1: Si7860DP (30 V N-channel, $R_{\mathrm{DS(on)}} =$ 11 mΩat $V_{\mathrm{GS}} = 4.5$ V, Vishay).

Synchronous FET Q_2: Si7336ADP (30 V N-channel, $R_{\mathrm{DS(on)}} = 4$ mΩ at $V_{\mathrm{GS}} = 4.5$ V, Vishay).

Drive switches $S_1 - S_4$: FDN335N (20 V N-channel, $R_{\mathrm{DS(on)}} = 70$ mΩat $V_{\mathrm{GS}} = 4.5$ V, Fairchild).

Output filter inductance: $L_f = 330$ nH ($R = 1.3$ mΩ, IHLP-5050CE-01, Vishay).

Resonant inductor: $L_r = 1.5$ μH.

Fig. 15 shows the gate drive signal $v_{\mathrm{gs\_}Q1}$ of the control FET Q_1 and $v_{\mathrm{gs\_}Q2}$ of the synchronous FET Q_2. The crossover level of these two gate signals is less than the threshold voltage of the switches so that the dead time can be minimized significantly and the shoot-through can also be avoided. It is observed that $v_{\mathrm{gs\_}Q1}$ is smooth and the miller plateau is less than 5 ns due to the constant charging current. Moreover, the rise time and fall time of vgs_$Q1$ is less than 15 ns, which indicates the gate charging time is significantly reduced compare to a conventional driver.

Fig. 16 shows the drain-source voltage $v_{\mathrm{ds\_}Q2}$ and the gate signal $v_{\mathrm{gs\_}Q2}$ of the synchronous FET. It can bee seen from $v_{\mathrm{ds\_}Q2}$ that the body diode conduction time is small, which reduces the conduction loss and the reverse recovery loss of the body diode significantly.

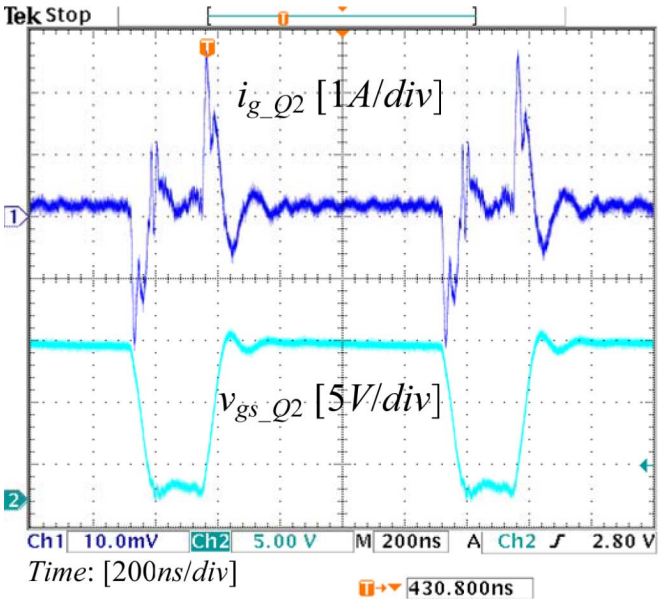

Fig. 17. Waveforms of the gate drive current i_g and the gate signal v_{gs_Q2} (synchronous FET).

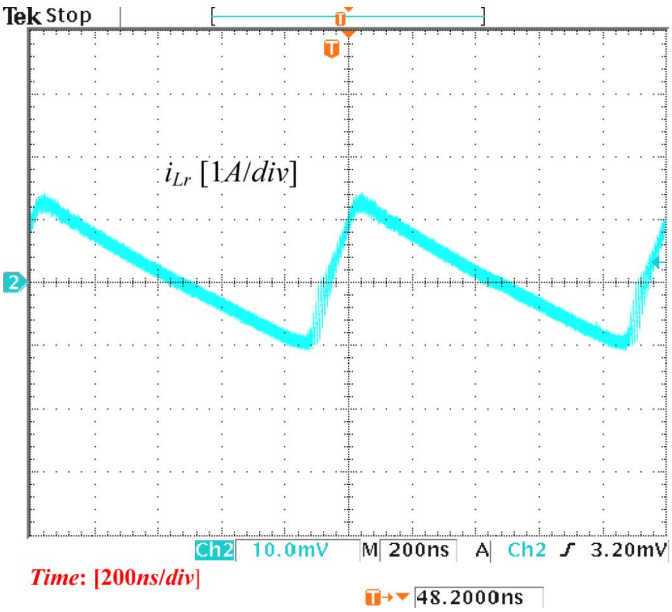

Fig. 18. Waveform of the resonant inductor current i_{Lr}.

Fig. 17 shows the gate drive current i_g and the gate signal v_{gs_Q2} of the synchronous FET. It is noted that the gate drive current keeps constant during the switching interval disregarding the current oscillations. Because the extra wire length is used to allow the insertion of a current probe to measure the current waveforms, this introduces higher stray inductances, which causes the parasitic oscillations of the current waveform at high frequency.

Fig. 18 shows the resonant inductor current i_{Lr} and its peak current value is 1.2 A, which is the optimized value of the drive current.

In order to illustrate efficiency improvement by the resonant driver, a benchmark of a synchronous buck converter with the conventional gate driver was built. A Predictive Gate Drive UCC

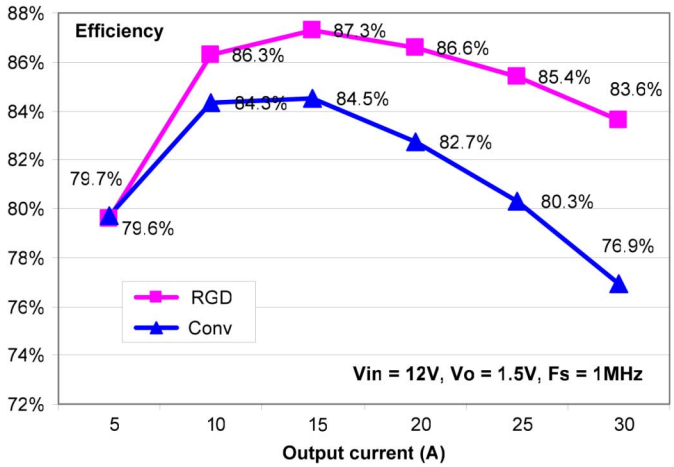

Fig. 19. Efficiency comparison at 1.5 V/30 A condition: top, resonant gate driver (RGD); bottom: conventional driver (Conv.).

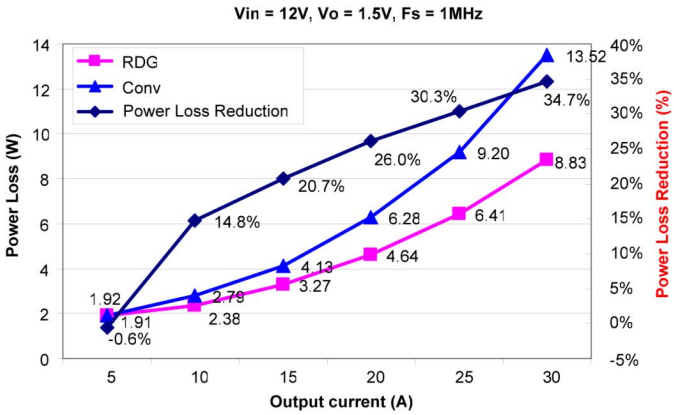

Fig. 20. Power loss comparison at 1.5 V/30 A condition. Top: Resonant gate driver (RGD), bottom: Conventional driver (Conv).

27222 from Texas Instruments was used as the conventional voltage driver.

Fig. 19 shows the measured efficiency comparison for the resonant gate driver and the conventional gate driver at 1.5 V output. It is observed that at 20 A, the efficiency is improved from 82.7% to 86.6% (an improvement of 3.9%) and at 30 A, the efficiency is improved from 76.9% to 83.6% (an improvement of 6.7%).

Fig. 20 shows the converter power loss comparison for the resonant gate driver and the conventional driver. It shows that at 20 A, the total loss is reduced from 6.28 W to 4.64 W, a reduction of 26%. At 30 A output current, the total loss is reduced from 13.52 W to 8.83 W, a reduction of 34.7%.

Another interesting observation from Fig. 20 is that for same power loss of 6.4 W, the buck converter with the conventional gate drive can only provide 20 A output current, while the buck converter with the resonant gate driver can provide 25 A (an improvement of 25%). In other words, if the total VR output current is 100 A, we need five phases buck converters if the conventional gate driver is used, while we only need to use 4 phases if he resonant gate driver is used. This will be a significant cost saving. Similarly, if the power loss is limited at 8.8 W, the buck converter with the conventional driver can only provide about 24 A while with the resonant gate driver the converter will be

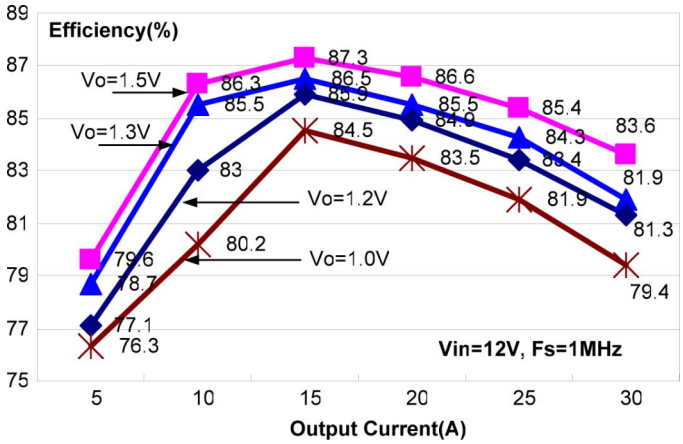

Fig. 21. Efficiency with different output voltages and currents with the resonant driver.

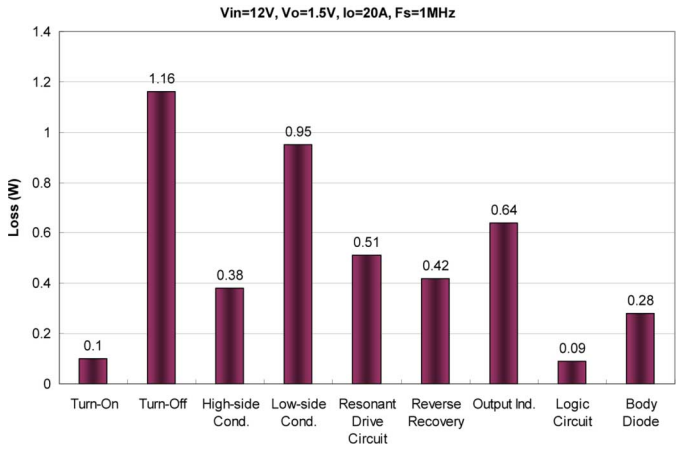

Fig. 22. Loss breakdown.

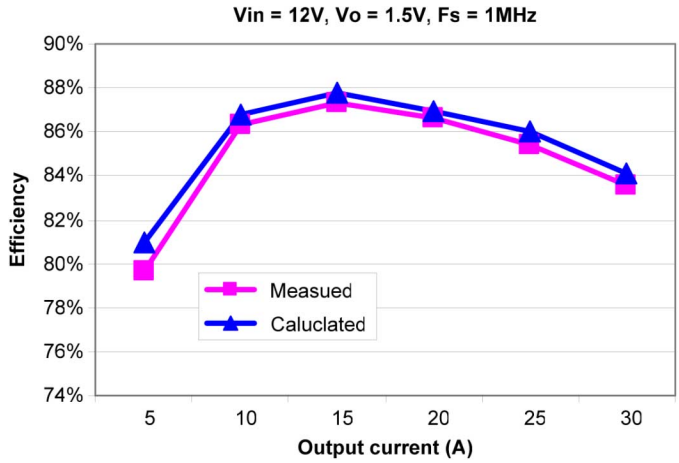

Fig. 23. Loss model verification with experimental results.

able to provide 30 A (an improvement of 25%). In other words, if the total load current is 150 A, we will need six (150/24 = 6.25) phases for the conventional gate driver while we only need five (150/30 = 5) phases for the resonant gate driver.

Fig. 21 shows the measured efficiency for the resonant gate driver at different output voltages and load currents. It is observed that at 1.0 V/20 A, the efficiency is 83.5% and it is even higher than 82.7% (see Fig. 19) of the conventional driver at 1.5 V/20 A, which means that we can reduce the output voltage from 1.5 V to 1.0 V by the resonant gate driver without penalizing the efficiency. This is important because that the VR output voltage keeps reducing and will be less than 1 V in the near future.

The efficiency comparison of different approaches of 12 V VRs at the switching frequency of 1 MHz is listed in Table II. Compared to the tapped-inductor (TI) buck converter in [34], the resonant driver improves the efficiency from 84% to 87% (an improvement of 3%). Compared to the soft-switching phase-shift buck (PSB) converter in [35], the resonant driver improves the efficiency from 82% to 86% (an improvement of 4%). The resonant driver achieves almost the same efficiency as the self-driven soft-switching buck-derived multiphase converter in [36]. But in terms of power density and cost, the resonant driver approach has significant advantages over the self-driven soft-switching buck converter which requires an additional bulk transformer that occupies plenty of space on the mother board. Furthermore, it should be emphasized that the resonant driver does not change the multiphase buck architecture of today's VRs featuring lower cost and simple control while improving the efficiency in a cost-effective manner. However, other buck derived approaches requiring additional magnetic components not only reduce the power density significantly, but also increase the cost and the complexity of the circuits and control scheme. In particular, it should also be mentioned that an efficiency improvement of 1.6% at 1.5 V/20 A is also achieved over the Toshiba synchronous buck multi chip module using semiconductor integration approach to minimize the parasitic inductances [37].

Fig. 22 gives the total loss breakdown of the buck VR with the resonant driver. Fig. 23 shows the measured efficiency and the analytical efficiency based on the loss model. It can be seen that the modeling results matches the experimental result well.

VIII. Conclusion

In this paper, an accurate analytical loss model of a power MOSFET with a current-source resonant driver is developed and the impact of the parasitic inductance is investigated. The advantages of a new resonant driver are verified thoroughly by the analytical analysis, simulation and experimental results. Compared to a voltage driver, the resonant driver uses a constant current source to drive the MOSFET gate and therefore, absorbs the parasitic common source inductance. As a result, the switching transition time can be greatly reduced, which leads to a significant reduction of the switching loss. Based on the proposed loss model, a general method to optimize the new resonant gate driver is proposed. A 12 V synchronous buck converter with the resonant driver operating at 1 MHz was built to verify the analysis and prove the significant loss saving. The level-shift circuit of the resonant driver and the CPLD implementation are also presented. The analytical results of the loss model match the simulation results and the experimental results well and the loss model can be used to optimize a resonant driver at high frequency.

The resonant gate driver achieves a significant efficiency improvement over the conventional driver, improving from 76.9% to 83.6% for 12 V input, 1 MHz, and 1.5 V/30 A output. More importantly, compared to other state of the art VR approaches, the resonant driver approach is promising from the standpoints of both performance and cost-effectiveness.

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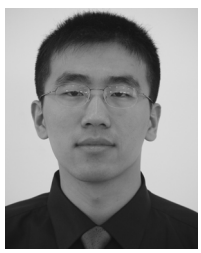

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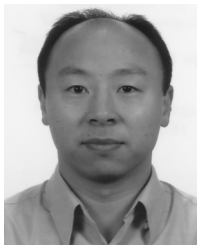

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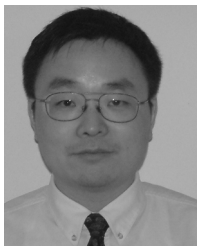

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