A 1-MHz High-Efficiency 12-V Buck Voltage Regulator With a New Current-Source Gate Driver

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***Abstract*—This paper proposes a new current-source gate drive circuit for a synchronous buck converter. The proposed driver can drive two MOSFETs independently with different drive currents for optimal design. For the control MOSFET, the optimal design involves a tradeoff between switching loss reduction and drive circuit loss; while for the synchronous-rectifier MOSFET, the optimal design involves a tradeoff between body diode conduction loss and drive circuit loss. Furthermore, the new drive circuit can achieve: 1) significant switching loss reduction; 2) gate energy recovery and high gate drive voltage to reduce $R_{\mathrm{DS(ON)}}$ conduction losses; 3) reduced conduction loss and reverse recovery loss of the body diode; and 4) zero-voltage switching of all the drive switches. The improved driver using integrated inductors is presented with multiphase buck voltage regulators (VRs) to reduce the number of magnetic cores and the core loss. The experimental results prove that a significant efficiency improvement has been achieved. At 1.5-V output, the new driver improves the efficiency from 84% using a conventional driver to 87.3% at 20 A, and at 30 A, from 79.4% to 82.8%. Overall, the new driver approach is attractive from the standpoints of both performance and cost-effectiveness.**

***Index Terms*—Current–source gate driver, microprocessor, power MOSFET, resonant gate driver, voltage regulator (VR).**

I. Introduction

In RECENT years, megahertz-voltage regulators (VRs) show significant advantages over the conventional hundreds of kilohertz VRs in terms of cost, power density, and dynamic response [1]–[3]. Due to its simplicity and low component count, the multiphase synchronous buck converter is used nearly exclusively for 12-V-input VRs to power microprocessors. However, for a 12-V input voltage, the buck VR suffers significantly from the problem of extremely low duty cycle, which results in high turn-off current, and thus, high turn-off loss at the switching frequency of 1 MHz. Furthermore, it has been recognized that with a conventional voltage driver, the parasitic inductance, especially the common-source inductance, has a serious propagation effect during the switching transition, and thus, further increases the switching loss, especially turn-off loss [4].

Different approaches have been proposed to improve the efficiency of 12-V VRs, such as the tapped-inductor (TI) buck converter in [5], the soft-switching phase-shift buck (PSB) converter in [6], self-driven soft-switching buck-derived multiphase converter in [7] and [8], and the two-stage approach in [9] and [10]. These advanced topologies demonstrate significant efficiency improvements over the conventional buck VR. However, the major concern regarding these techniques is that they require an additional transformer that occupies additional space on the motherboard, which brings up the manufacturing cost and additional magnetic design efforts. The multichip module developed by Toshiba and International Rectifier (IR) uses packing integration to minimize the parasitic inductances in the buck converter to achieve high efficiency [11]–[13]. The concern with this technology is the high cost of the semiconductor technology, and that the common-source inductance still exits in the package.

Another attractive approach is the resonant gate drive technique, which was originally proposed with the objective of recovering gate energy lost in a conventional gate driver. It is interesting to note that a significant efficiency improvement has been reported recently in a cost-effective manner [14], [15].

In Section II, resonant gate drive techniques for power MOSFETs are reviewed. To solve the existing problems, a new current–source gate drive circuit is presented in Section III. An improved version of the new circuit with magnetic integration is presented in Section IV. The experimental results are reported in Section V. Finally, the conclusions and discussion are given in Section VI.

II. Review of Resonant Gate Drive Techniques

The resonant gate drive technique was originally used to recover gate drive loss for resonant power converters operating above 1 MHz (typically, 5–10 MHz) [16]–[18].

For the same reason, a self-oscillating resonant gate drive with a resonant network was used in RF power amplifiers (>30 MHz) featuring sinusoidal waveforms [19], [20]. The self-oscillating resonant gate driver (soft gating driver) is also applied to a high-frequency (>30 MHz) dc–dc converter to achieve high gate loss recovery in [21].

Different resonant drive circuit topologies have been proposed to reduce the gate loss in recent years. However, all of

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them suffer from at least one of the following driver specific problems:

1) only suitable for low-side and ground-referenced drives [18]–[27];
2) the leakage inductance with a bulky transformer or coupled inductance [24], [26], [28]–[30];
3) slow turn-on or turn-off transition times, which increase both conduction and switching losses in the power MOSFET due to the gate drive current beginning at zero current [18], [23]–[26];
4) the inability to actively clamp the power MOSFET gate to the drive voltage during the ON time and/or to ground during the OFF time, which can lead to undesired false triggering of the power MOSFET gate, i.e., lack of *Cdv/dt* immunity [18], [23]–[28].

The self-driven scheme specially proposed for synchronous-rectifier (SR) MOSFETs in [3], [7], and [31] can drive the synchronous MOSFET with high gate drive voltage (e.g., 12 V) to obtain lower $R_{\mathrm{DS(ON)}}$ without excessive gate drive loss using the leakage inductance of the transformer. An assessment of resonant drive techniques for use in low-power dc–dc converters is presented in [32], and a mathematical model is built to estimate the power loss of the drive circuit in [33]. However, these investigations emphasize gate energy savings with the resonant drive and concentrate on the drive topologies. Therefore, they ignore the potential switching loss savings that is much more dominant in megahertz-switching-frequency power converters.

Dual-channel low-side and dual-channel low-side–high-side resonant gate drivers have been proposed in [34]–[36], respectively. The discontinuous current resonant gate driver has also been proposed in [37] and [38]. The key to these drivers' operation is the control of the driver switches to generate either continuous or discontinuous inductor current waveforms, enabling the peak portion of the inductor current to be used to charge/discharge the power MOSFET gate as a near-constant current source. Based on an accurate analytical loss model, a significant reduction of the switching transition time and the switching loss was verified for a 1-MHz buck VR theoretically and experimentally in [14] and [15]. These gate drivers using high-level constant gate currents are also known as current–source drivers (CSDs).

In particular, the CSD, as shown in Fig. 1, for a buck VR presented in [14] and [34], significantly reduces the switching loss since the impact of the parasitic inductances, especially common-source inductance, can be reduced significantly. This gate drive circuit features simplicity, low cost, and efficiency improvement. However, by carefully investigating the equivalent circuits of operation in [34], it is noted that driver circuit in Fig. 1 has several drawbacks.

1) In a buck VR, high drive current is required for the control MOSFET to ensure fast switching speed to reduce switching loss, while low drive current is required for the synchronous MOSFET to achieve gate energy recovery. Therefore, it is beneficial to have different gate drive currents for optimal design. However, this drive circuit can provide only identical drive currents for the two MOSFETs in a buck converter.

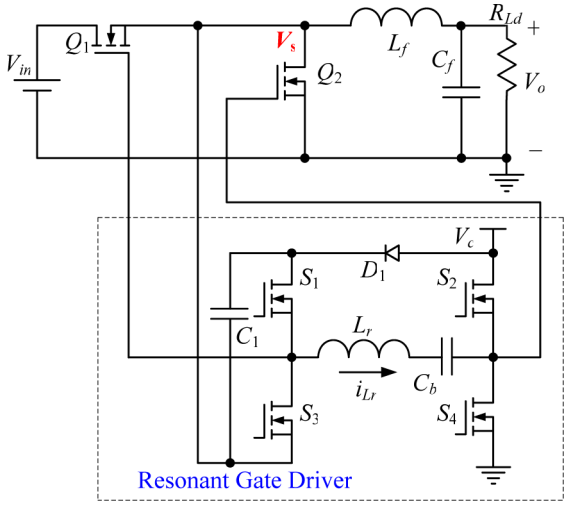


Fig. 1. Buck VR with the resonant gate drive circuit.

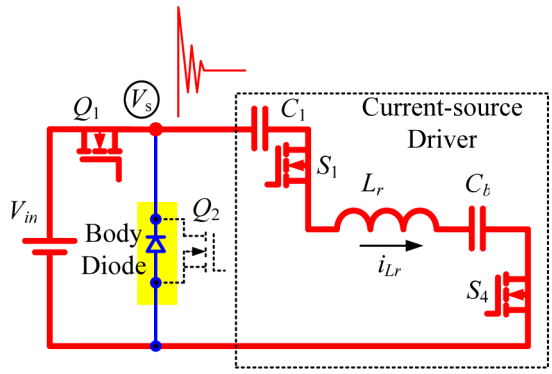


Fig. 2. Equivalent circuit during switching transition.

2) Due to the reverse recovery of the body diode, the switching node has severe oscillation, as shown in Fig. 2. This switching node is actually in series with the level-shift capacitor of the drive circuit, which makes the circuit sensitive to the reverse recovery noise in practical applications.
3) The resonant inductor current flows through the control MOSFET and synchronous MOSFET, which causes additional conduction loss.
4) To enhance light load efficiency, the switching frequency can be reduced or the diode emulation can be used to turn off the synchronous MOSFET to allow discontinuous conduction mode by detecting when the inductor current reaches zero. However, it is difficult to achieve these advanced features using this drive topology.

In order to solve the earlier problems and improve the driver's performance, a new current-source gate driver is introduced in the next section.

III. Proposed Current-Source Gate Driver

One objective of the proposed CSD is to achieve independent drive control for the control and synchronous MOSFETs to achieve optimal performance. For the control MOSFET, the optimal design involves a tradeoff between switching loss and drive circuit loss, while for the SR MOSFET, the optimal design

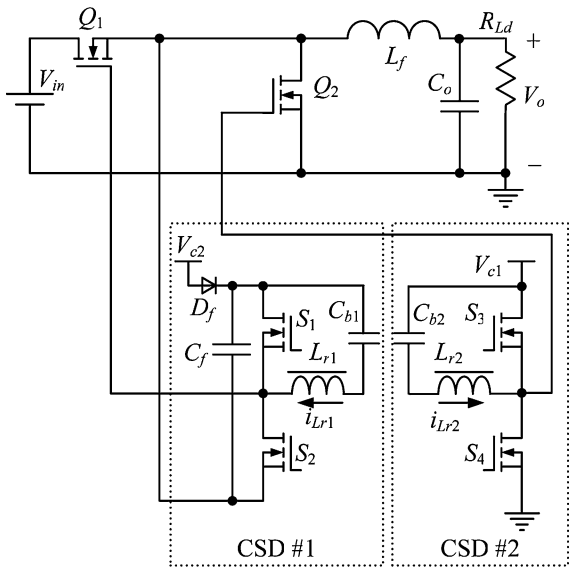


Fig. 3. Buck VR with proposed CSD.

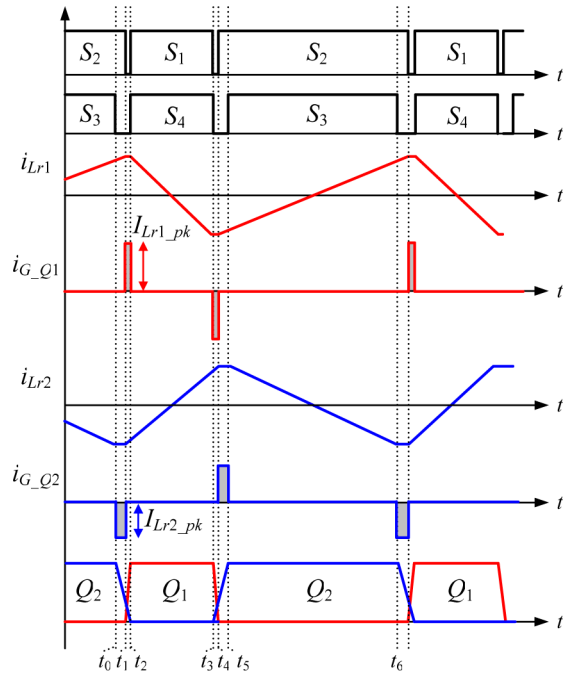


Fig. 4. Key waveforms of the new drive circuit.

involves a tradeoff between body diode conduction loss and drive circuit loss. Moreover, the drive currents should not go through the main power MOSFETs.

All the earlier features can be achieved by the proposed new drive circuit, as shown in the dotted area in Fig. 3, where Q_1 is the control MOSFET and Q_2 is the synchronous MOSFET in a buck converter. Fig. 4 gives the key waveforms.

A. Principle of Operation

In Fig. 3, there are two sets of the drive circuits (CSD #1 and CSD #2), and each of them has the structure of the half-bridge topology, consisting of drive MOSFETs S_1, S_2, S_3, and S_4, respectively.

It is noted that the drive MOSFETs (S_1–S_4) are similar to those in a conventional driver IC, which means S_1–S_1 can also be easily implemented in a driver IC with standard CMOS technology to achieve low profile and high power density with low-footprint packages, such as the small-outline IC (SOIC) package or quad-flat no-lead (QFN) package, which are pin-to-pin compatible with the conventional driver IC. The new current–source gate driver circuit is analyzed with discrete components, and the timing is tuned using a digital complex programmable logic device (CPLD). If the drive circuit is integrated into an IC chip, the circuit timing can also be optimized.

As illustrated in Fig. 4, S_1 and S_2 are switched out of phase with complimentary control to drive Q_1, while S_3 and S_4 are switched out of phase with complimentary control to drive Q_2. With complimentary control, all the drive switches can achieve zero-voltage switching (ZVS). Driver #1 can also be regarded as a level-shift version of driver #2. V_{c1} and V_{c2} are the drive voltages, and they could use the same or independent drive voltages if desired. The diode D_f provides the path to charge C_f to the voltage of the drive voltage V_{c2}. C_{b1} and C_{b2} are the blocking capacitors.

There are six switching modes in a switching period and the equivalent circuits are given in Fig. 5 accordingly. D_1–D_4 are the body diodes and C_1–C_4 are the intrinsic drain-to-source capacitors of S_1–S_4, respectively. C_{gs1} and C_{gs2} are intrinsic gate-to-source capacitors of Q_1 and Q_2, respectively. The switching transitions of charging and discharging C_{gs1} and C_{gs2} are during the interval in $[t_0, t_2]$ and $[t_3, t_5]$. The peak currents i_{G_Q1} and i_{G_Q2} during $[t_0, t_2]$ and $[t_3, t_5]$ are constant during switching transition, which ensures fast charging and discharging of the MOSFET Q_1 gate capacitor including the miller capacitor.

1) *Mode 1* $[t_0, t_1]$ [Fig. 5 (a)]: Prior to t_0, S_2 and S_3 conduct and the inductor current i_{Lr1} increases in the positive direction, while i_{Lr2} increases in the negative direction. Q_2 is ON. At t_0, S_3 turns off. i_{Lr2} charges C_3 and discharges C_4 plus C_{gs2} simultaneously. Due to C_3 and C_4, S_3 achieves zero-voltage turn off. The voltage of C_3 rises linearly and the voltage of C_4 decays linearly.
2) *Mode 2* $[t_1, t_2]$ [Fig. 5 (b)]: At t_1, v_{c3} rises to V_{c1} and v_{c4} decays to zero. The body diode D_4 conducts and S_4 turns on with zero-voltage condition. The gate-to-source voltage of Q_2 is clamped to ground through S_4. At t_1, S_2 turns off. i_{Lr1} charges C_2 plus the input capacitor C_{gs1} and discharges C_1 simultaneously. Due to C_1 and C_2, S_2 is zero-voltage turn off. The voltage of C_2 rises linearly and the voltage of C_1 decays linearly.
3) *Mode 3* $[t_2, t_3]$ [Fig. 5 (c)]: At t_2, v_{c2} rises to V_{c2} and v_{c1} decays to zero. The body diode D_1 conducts and S_1 turns on under zero-voltage condition. The gate-to-source voltage of Q_1 is clamped to V_{c2} through S_1. i_{Lr1} and i_{Lr2} decrease.
4) *Mode 4* $[t_3, t_4]$ [Fig. 5 (d)]: Before t_3, i_{Lr1} and i_{Lr2} changed polarity. At t_3, S_4 and S_1 turns off. i_{Lr2} charges C_4 plus C_{gs2} and discharges C_3. Due to C_3 and C_4, S_4 achieves zero-voltage turn off. The voltage of C_4 rises linearly and the voltage of C_3 decays linearly. i_{Lr1} charges

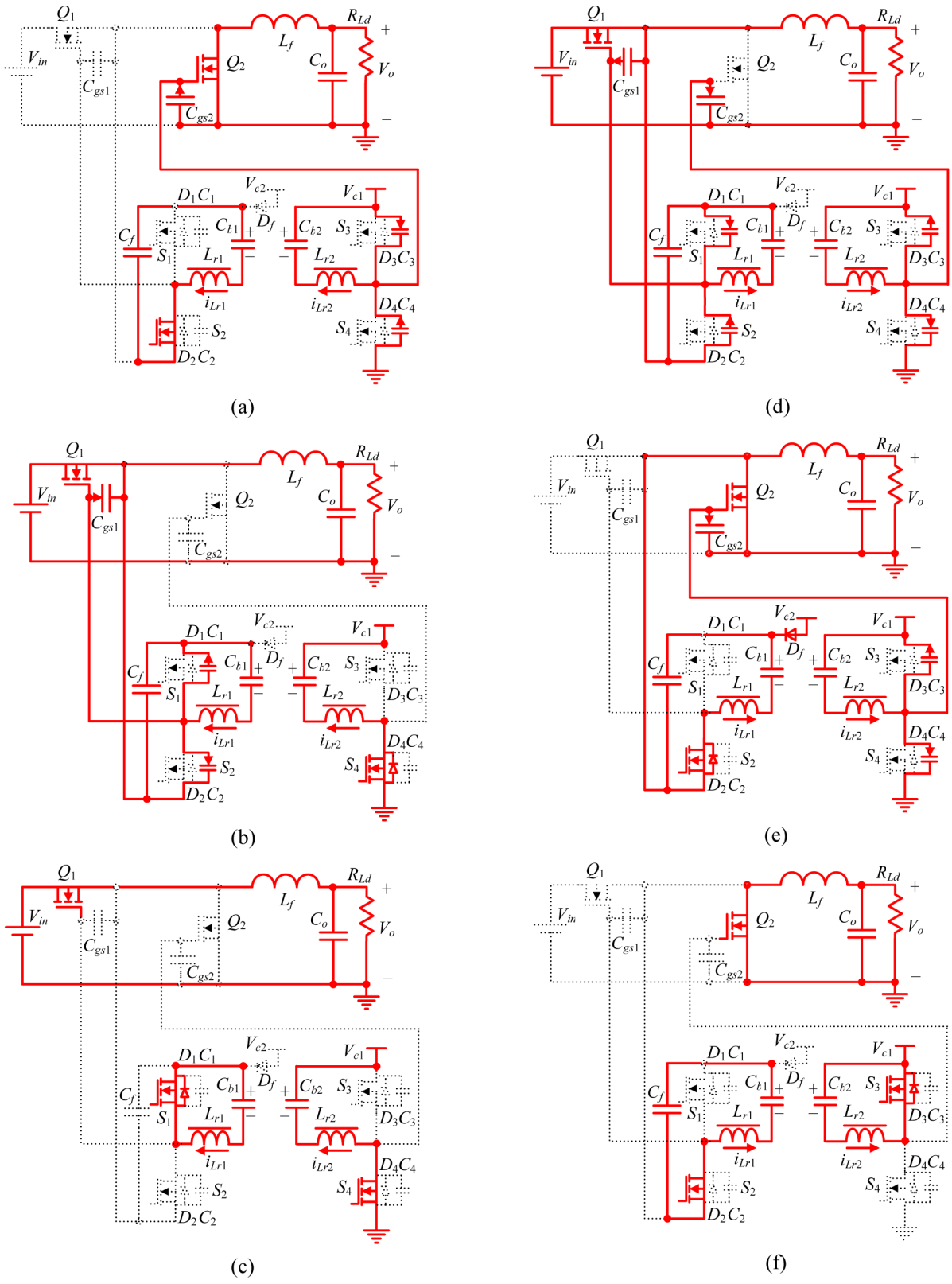


Fig. 5. Equivalent circuits of operation. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$. (c) $[t_2, t_3]$. (d) $[t_3, t_4]$. (e) $[t_4, t_5]$. (f) $[t_5, t_6]$.

C_1 and discharges C_2 plus $C_{\rm gs1}$ simultaneously. Due to C_1 and C_2, S_1 achieves zero-voltage turn off.

5) *Mode 5* $[t_4, t_5]$ [Fig. 5(e)]: At t_4, v_{c1} rises to V_{c2} and v_{c2} decays to zero. The body diode D_2 conducts and S_2 turns on with zero voltage. The gate-to-source voltage of Q_1 is clamped to zero through S_2.
6) *Mode 6* $[t_5, t_6]$ [Fig. 5 (f)]: At t_5, v_{c4} rises to V_{c1} and v_{c3} decays to zero. The body diode D_3 conducts and S_3 turns on with zero voltage. The gate-to-source voltage of Q_2 is clamped to V_{c1} through S_3.

B. Advantages of the Proposed Current-Source Gate Driver

The advantages of the new drive circuit are highlighted as follows.

1) Significant Reduction of the Switching Transition Time and Switching Loss: During the switching transition $[t_1, t_2]$ and $[t_3, t_4]$ (see Fig. 4), the proposed CSD uses the peak portion of the resonant inductor current to drive the control MOSFET and absorbs the common-source inductance. This significantly reduces the propagation impact of the parasitics during the switching transition, which leads to a reduction of the switching transition time and the switching loss.

2) Gate Energy Recovery: CSDs, using an inductor as a current source, store energy in the inductance, which can be recovered to the driver supply voltage rail. In the proposed driver, the inductor returns its stored energy to the line during intervals $[t_0, t_2]$ for the SR MOSFET Q_2. Energy is also returned to the driver supply during the corresponding time intervals for the control MOSFET Q_1. Owing to gate energy recovery, high gate drive voltage can be used to further reduce $R_{\rm DS(ON)}$ conduction losses.

3) Reduced SR Body Diode Conduction: Quick switching is also beneficial to minimize the dead time between the control and SR MOSFETs. As the gate-source voltage rises from the plateau voltage to $V_{\rm cc}$, the $R_{\rm DS(ON)}$ of the SR is decreasing. Quick switching enables a fast transition to the minimum value of $R_{\rm DS(ON)}$ at $v_{\rm gs} = V_{\rm cc}$. This results in conduction loss savings and reverse recovery loss in the body diode of the SR MOSFET.

4) ZVS of the Drive Switches: Through the mode analysis, it is noted that all of the drive switches are able to achieve ZVS, which is beneficial for high frequency (i.e., $>$1 MHz).

5) High Noise Immunity: With the new drive circuit, the gate terminals of the buck MOSFETs (Q_1 and Q_2) are clamped to either the drive voltage source via a low-impedance path (S_1 and S_3 with fairly small $R_{\rm DS(ON)}$) or their source terminals (S_2 and S_4). This offers high noise immunity and leads to the alleviation of *dv/dt* effect to prevent *Cdv/dt* induced turn-on of the SR MOSFET.

C. Drive Circuit Loss Analysis

The two CSDs have similar driver losses, except that each operates with different peak inductor currents. With CSD #1, the drive loss includes: 1) the resistive loss and gate drive loss of drive switches S_1–S_2; 2) the loss of the resonant inductor L_{r1}; and 3) the resistive loss caused by the internal gate mesh resistance of the power MOSFETs.

Using volt·seconds balance across the resonant inductor, the dc voltage $v_{\rm cb1}$ across the blocking capacitor C_{b1} is given by

$$v_{\rm Cb1} = (1 - D)V_{c2} \tag{1}$$

where D is the duty cycle of S_1 and V_{c2} is the drive voltage.

The blocking capacitor value is found using

$$C_{b1} = \frac{I_{\rm Lr1\_pk}}{4kV_{c1}f_s} \tag{2}$$

where k is the percent ripple on C_{b1} and f_s is the switching frequency. For example, for $V_{c1} = 7$ V, $I_{\rm Lr1\_pk} = 1.5$ A, $k = 5\%$, and $f_s = 1$ MHz, then $C_{b1} = 1.0$ μF should be used.

The relationship of the inductor value L_{r1} and the peak inductor current $I_{\rm Lr1\_pk}$ is given by

$$L_{r1} = \frac{V_{c1}D(1 - D)}{2I_{\rm Lr1\_pk}f_s}. \tag{3}$$

By choosing the proper peak inductor current (i.e., drive current for the power MOSFET), the resonant inductor value can be obtained using (3).

As observed from the principle of operation in Fig. 4, the peak current $I_{\rm Lr1\_pk}$ of the resonant inductor L_{r1} is the actual gate drive current for the power MOSFET and can be regarded as a constant current source. Therefore, the higher the $I_{\rm Lr1\_pk}$ is, the shorter the switching transition time is, and thus, more switching loss can be reduced. On the other hand, higher $I_{\rm Lr1\_pk}$ results in a larger rms value of the inductor circulating current $i_{\rm Lr1}$, which increases the circulating current conduction loss in the drive circuit, and therefore, decreases the gate energy recovery. Therefore, it is critical to decide $I_{\rm Lr1\_pk}$ properly so that the maximum loss savings can be achieved. The optimal design to choose $I_{\rm Lr1\_pk}$ is given in Section III-D.

The inductor current waveform in Fig. 4 can be regarded as a triangular waveform since the charging/discharging time $[t_0, t_2]$ and $[t_3, t_5]$ are small and can be neglected. Therefore, the rms value of the inductor current $I_{\rm Lr1\_rms}$ is $I_{\rm Lr1\_pk}/\sqrt{3}$.

The rms current flowing through S_1 is given by

$$I_{s1\_\rm rms} = I_{\rm Lr1\_pk}\sqrt{\frac{D}{3}}. \tag{4}$$

The rms current flowing through S_2 is given by

$$I_{s2\_\rm rms} = I_{\rm Lr1\_pk}\sqrt{\frac{1 - D}{3}}. \tag{5}$$

Assuming that the same MOSFETs are used for S_1 and S_2, the conduction loss in S_1 and S_2 is expressed as

$$P_{\rm cond} = I^2_{s1\_\rm rms}R_{\rm ds(ON)} + I^2_{s2\_\rm rms}R_{\rm ds(ON)}. \tag{6}$$

Substituting (4) and (5) into (6) yields

$$P_{\rm cond} = \frac{1}{3}I^2_{\rm Lr1\_pk}R_{\rm ds(ON)}. \tag{7}$$

The copper loss in the inductor is expressed as

$$P_{\rm copper} = R_{\rm ac}I^2_{\rm Lr1\_rms} \tag{8}$$

where $R_{\rm ac}$ is the ac resistance of the inductor winding and $I_{\rm Lr1\_rms}$ is the rms value of the inductor current.

The loss $P_{\rm core}$ can be calculated using

$$P_{\rm core} = K_1 f^x B^y V_e \tag{9}$$

where K_1 is a constant for core material, f is the frequency, B is the peak flux density, x is the frequency exponent, y is the flux density exponent, and V_e is the effective core volume [39]. These parameters are unique to each core material, which is usually provided by the inductor suppliers. In our case, since the inductor used in the experiment is the DO1608C series from Coilcraft, $P_{\rm core}$ can be estimated as 0.08 W through the Web-based inductor core calculator.

The total inductor loss is given by

$$P_{\rm ind} = P_{\rm copper} + P_{\rm core}. \tag{10}$$

Both the charge and discharge currents flow through the internal gate mesh resistance R_G of the power MOSFET, and therefore, cause resistive loss.

The total loss dissipated in the internal resistance of Q_1 during turn-on ($t_{\rm ON1}$) and turn-off ($t_{\rm OFF1}$) is expressed as

$$P_{\rm RG} = R_{G1} I^2_{\rm Lr\_pk1} (t_{\rm ON1} + t_{\rm OFF1}) f_s \tag{11}$$

where R_{G1} is the internal gate resistors of Q_1.

The gate loss in S_1 and S_2 is given by

$$P_{\rm gate} = 2 Q_{g\_s} V_{\rm gs\_s} f_s \tag{12}$$

where Q_{g_s} is the total gate charge of a drive switch and $V_{\rm gs\_s}$ is the drive voltage, which is typically 5 V.

Therefore, the total loss in CSD #1 is given by

$$P_{\rm Drive} = P_{\rm cond} + P_{\rm ind} + P_{\rm RG} + P_{\rm gate}. \tag{13}$$

D. Optimal Design

One advantage of this new drive circuit is that it can drive the control and synchronous MOSFET independently with different gate currents to achieve an optimized design.

For the control MOSFET Q_1, optimal design involves a tradeoff between the switching loss and the drive circuit loss. Following the optimal design procedure using the analytical loss model in [14], the gate drive current can be decided. The sum of the switching loss and drive circuit loss can be plotted as $P_{Q1\_\rm Optimal}$, and the optimal gate current I_{G_Q1} can be determined from the graph (at the minimum point of $P_{Q1\_\rm Optimal}$). For the given application and parameters in Section V, the curves are given in Fig. 6, where the optimal gate current is 1.5 A and the resonant inductor value is 1.0 μH using (3). In this example, $P_{\rm switching} = 2.3$ W and $P_{\rm Drive} = 0.5$ W.

The synchronous MOSFET Q_2 operates with ZVS since its output capacitance is discharged to zero voltage before it turns on. Therefore, for the synchronous MOSFET, optimal design involves a tradeoff between the body diode conduction loss and gate drive loss.

The body diode conduction loss can be estimated as

$$P_{\rm body\_Q2} = V_{\rm body\_Q2} I_o f_s t_{\rm body} \tag{14}$$

where $t_{\rm body}$ is the body diode conduction time, which can be estimated using (15). Equation (15) assumes that the body diode conducts during the interval when the gate voltage is between the threshold and until the gate voltage is large enough so that the $R_{\rm DS(ON)}$ of the synchronous MOSFET is less than about 20 mΩ, which means that the voltage drop across the channel is less than the body diode drop. The values for Q_{g_Q2} ($V_{20\ \rm m\Omega}$) and $Q_{g\_Q2}(V_{\rm th\_Q2})$ can be estimated using the MOSFET manufacturer datasheets

$$t_{\rm body} = 2\left[\frac{Q_{gQ2}(V_{20\ \rm m\Omega}) - Q_{gQ2}(V_{\rm thQ2})}{I_{gQ2}}\right]. \tag{15}$$

Using $P_{\rm Drive}$ given in (13) and $P_{\rm body\_Q2}$ given in (14), the sum of the two loss components can be plotted as $P_{Q2\_\rm Optimal}$ and the optimal gate current I_{G_Q2} can be determined from the graph (at the minimum point of $P_{Q2\_\rm Optimal}$). For the given application and parameters in the Section V, the curves are given in Fig. 7, where the optimal gate current is 1.1 A and the resonant inductor value is 1.2 μH by using (3). In this example, $P_{\rm Drive} = 0.33$ W, $P_{\rm body\_Q2} = 0.58$ W, and $t_{\rm body} = 27$ ns.

Fig. 8 illustrates the loss breakdown comparison between the new CSD with the optimal design and the conventional diver. At $V_o = 1.5$ V, $I_o = 20$ A, and $f_s = 1$ MHz, the most significant loss reduction is the switching loss. The turn-on loss is reduced by 0.5 W and the turn-off loss is reduced by 0.7 W. The conduction loss and the body diode loss are also reduced by 0.05 and 0.2 W, respectively. The total loss reduction is 1.45 W.

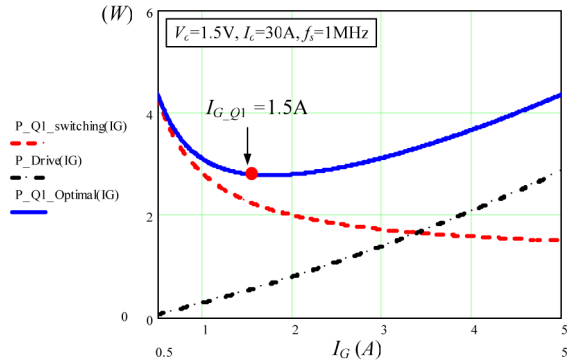


Fig. 6. Optimization curves for the control MOSFET Q_1: power loss versus gate current.

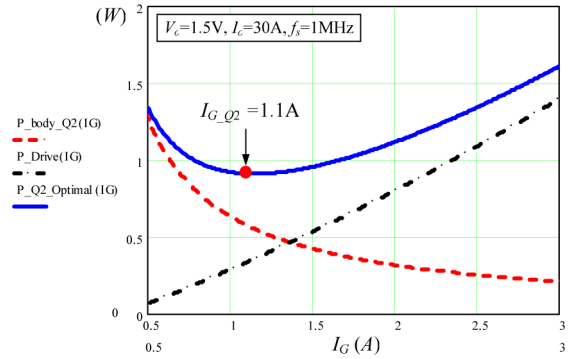


Fig. 7. Optimization curves for the synchronous MOSFET Q_2: power loss versus gate current.

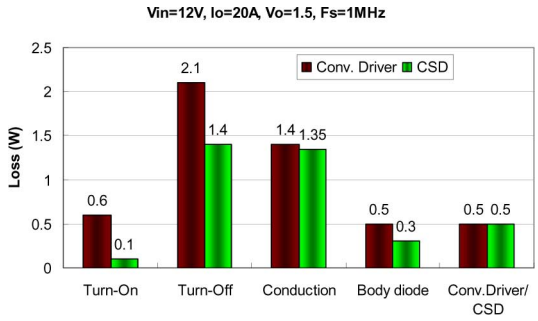


Fig. 8. Loss breakdown between the current-source gate driver and conventional gate driver.

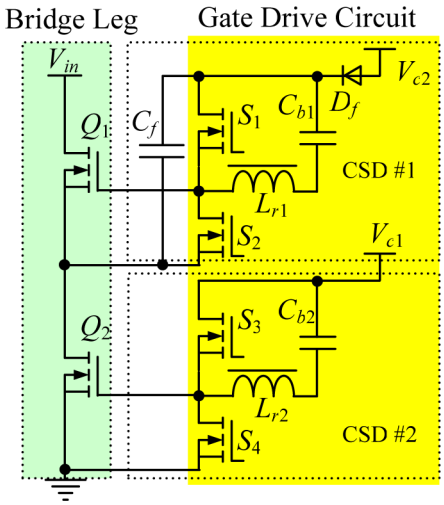


Fig. 9. Bridge leg with the new current-source driver.

E. Application Extension

Half-bridge (HB) converter and full-bridge (FB) converters can achieve ZVS using complimentary control and phase-shift control, respectively. However, turn-off loss still exits and can be high due to the parasitics of the main power MOSFETs. Turn-off loss therefore becomes a concern at megahertz switching frequencies.

It is noted that the proposed gate drive circuit can also be extended to drive two MOSFETs in one leg of the HB or FB topologies to achieve switching loss reduction and gate energy savings at high switching frequencies (>1 MHz), as shown in Fig. 9.

IV. New Current-Source Gate Driver With Integrated Magnetics

It can be observed from the waveforms of two inductor currents i_{Lr1} and i_{Lr2} in Fig. 4 that i_{Lr1} is nearly a mirror image about the time axis of i_{Lr2}. This provides good ripple cancellation effect of the magnetic flux enabling potential inductors integration.

Fig. 10 shows the proposed current-source gate driver with integrated magnetics. It is noted that the reference voltages of the two drivers do not need to be the same.

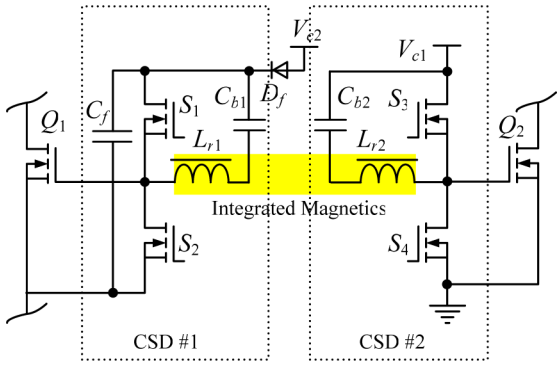


Fig. 10. Proposed current-source driver with integrated inductor.

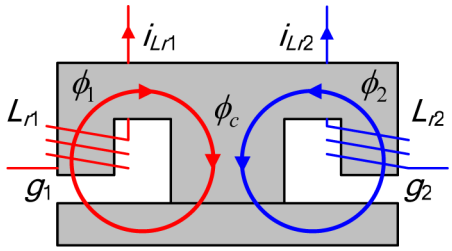


Fig. 11. Integrated inductor structure.

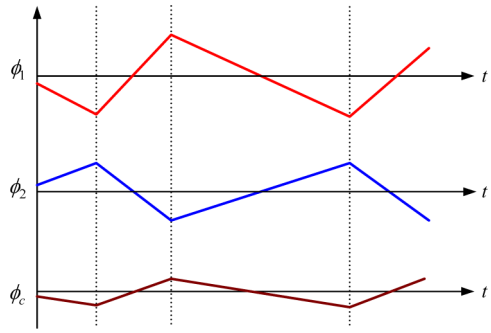
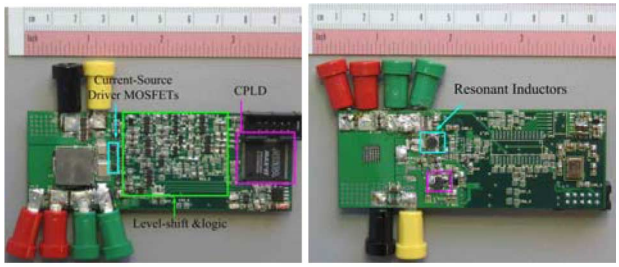


Fig. 12. Flux ripple cancellation effect.

Fig. 11 illustrates an integrated inductor structure for CSD. The two resonant inductors (L_{r1} and L_{r2}) are built on the two outer legs of one E–I core with different air gaps, g_1 and g_2, respectively. The fluxes Φ_1 and Φ_2 in the two outer legs generated by the two windings flow through the center leg, which is a low-reluctance magnetic path with no air gap. Though L_{r1} and L_{r2} are built on the same E–I core, there is no interaction between the two flux loops of Φ_1 and Φ_2, and there is no coupling effect between L_{r1} and L_{r2}. Therefore, the principle of operation of the driver circuits with the integrated inductors do not change; however, the core number is reduced from two to one.

Another benefit of using integrated inductors is that the flux Φ_{c} ($\Phi_{\mathrm{c}} = \Phi_1 + \Phi_2$) in the center leg has smaller ripple due to the flux ripple cancellation effect of the current i_{Lr1} and i_{Lr2}, as shown in Fig. 12. The smaller flux ripple helps to reduce the core losses in the center leg.



(a) Top (b) Bottom

Fig. 13. Prototype photograph of the synchronous buck VR with the proposed current-source gate driver. (a) Top. (b) Bottom.

V. Experimental Results and Discussion

In order to verify the advantages of the new current-source gate drive circuit, a synchronous buck converter with the proposed driver was built. The specifications are as follows: input voltage $V_{\rm in}$ = 12 V; output voltage $V_o = 1.5$ V; output current $I_o = 30$ A; switching frequency $f_s = 1$ MHz; gate driver voltage $V_{c1} = V_{c2} = 8$ V. The PCB uses six-layer 2-oz copper. The components used in the circuit are listed as follows.

1) Control FET Q_1: Si7860DP (30-V N-channel, $R_{\rm DS(ON)} = 11$ mΩ at $V_{\rm GS} = 4.5$ V).
2) Synchronous FET Q_2: Si7336ADP (30-V N-channel, $R_{\rm DS(ON)} = 4$ mΩ at $V_{\rm GS} = 4.5$ V).
3) Drive MOSFETs S_1–S_4: FDN335N (20-V N-channel, $R_{\rm DS(ON)} = 70$ mΩ at $V_{\rm GS} = 4.5$ V).
4) Output filter inductance: $L_f = 330$ nH ($R_{\rm dc} = 1.3$ mΩ, IHLP-5050CE-01, Vishay).
5) Resonant inductors: $L_{r1} = 1$ μH ($I_{\rm pk1} = 1.5$ A) and $L_{r2} = 1.2$ μH ($I_{\rm pk2} = 1.1$ A).

A photograph of the synchronous buck VR prototype with the new CSD is provided in Fig. 13. The driver was built using discrete components and an Altera Max II EPM240 CPLD was used to generate the driver gating signals, as shown in Fig. 13(a). The bootstrap and level-shift circuit in [14] were used for the nonground referenced switches. Surface mount (SMT) power inductors (DO1608C series) from Coilcraft are used for the resonant inductors, as shown in Fig. 13(b).

Waveforms of the gate drive signals $v_{\rm gs\_Q1}$ (control MOSFET) and $v_{\rm gs\_Q2}$ (synchronous MOSFET) are provided in Fig. 14. The zoomed waveforms are shown in Fig. 15. It is observed that the dead time between two gate signals is minimized to reduce the body diode conduction. It is noted that additional fixed dead time can be set to account for the threshold voltage variation at high temperature. Moreover, with full integration of the drive circuit into a drive IC, adaptive control or predictive control using logic monitoring circuitry can be used.

It is also observed that $v_{\rm gs\_Q1}$ is smooth and no miller plateau is observed since the miller charge is removed quickly due to the constant charging/discharging current. It is also noted that due to the gate energy recovery, 8-V drive voltage is used to reduce the $R_{\rm DS(ON)}$ by 25% compared to 5-V drive voltage. This translates into a reduction of the conduction loss by 25%.

Waveforms of the resonant inductor currents $i_{\rm Lr1}$ and $i_{\rm Lr2}$ are illustrated in Fig. 16 for the prototype with discrete inductors. It

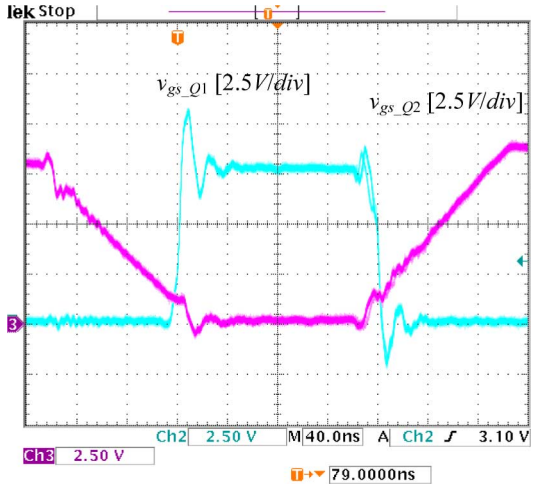


Fig. 14. Gate signals $v_{\rm gs\_Q1}$ (control FET) and $v_{\rm gs\_Q2}$ (synchronous FET).

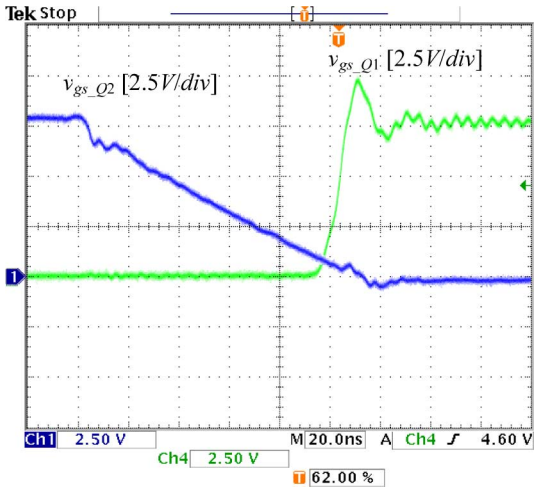


Fig. 15. Zoomed gate signals $v_{\rm gs\_Q1}$ (control FET) and $v_{\rm gs\_Q2}$ (synchronous FET).

is observed that for the control MOSFET, the optimal value of drive current $i_{\rm Lr1}$ is 1.5 A, while for the synchronous MOSFET, the optimal value of drive current $i_{\rm Lr2}$ is 1.1 A.

Waveforms of the resonant inductor currents $i_{\rm Lr1}$ and $i_{\rm Lr2}$ are illustrated in Fig. 17 for the prototype with integrated inductors. It is observed that the mirror relationship between $i_{\rm Lr1}$ and $i_{\rm Lr2}$ leads to the feasibility of inductor integration and lower core loss due to the magnetic flux cancellation effect. In addition, the integrated inductor does not change the operation of the drive circuits.

A benchmark synchronous buck converter with a UCC27222 conventional gate driver was built. The same parameters are used as the current-source gate driver. Fig. 18 illustrates the measured efficiency comparison for the current-source gate driver and the conventional gate driver at 1.5-V output. It is observed that at 20 A, the efficiency is improved from 84% to 87.3% (an improvement of 3.3%), and at 30 A, the efficiency is improved from 79.4% to 82.8% (an improvement of 3.4%). The CSD with

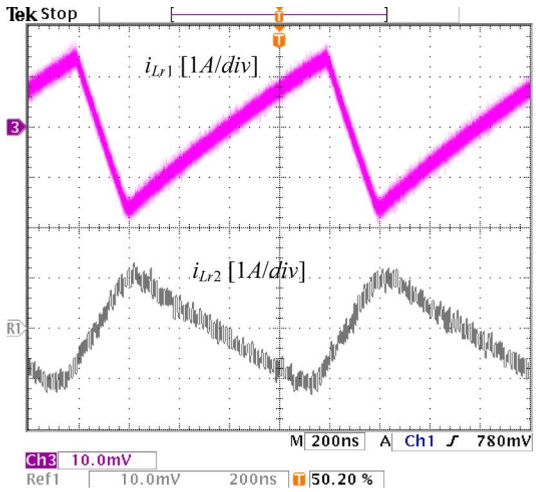


Fig. 16. Waveforms of resonant inductor currents (discrete resonant inductors).

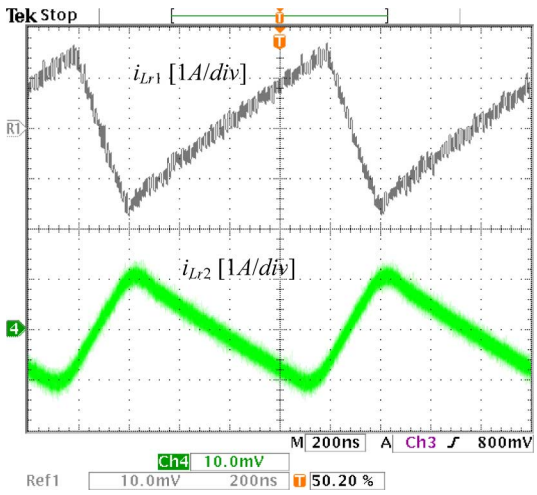


Fig. 17. Waveforms of resonant inductor currents (with magnetic integration).

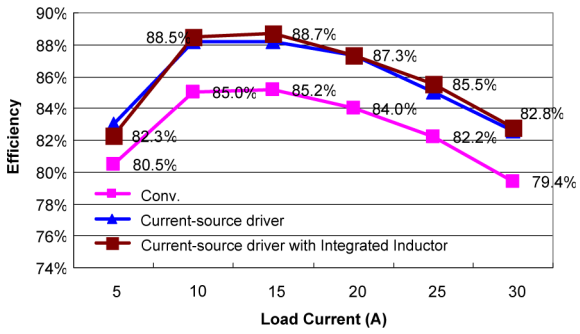


Fig. 18. Efficiency comparison at 1.5 V/30 A/1 MHz.

one integrated inductor achieves similar efficiency to the driver with two discrete inductors.

Fig. 19 shows the converter power loss comparison for the resonant gate driver and the conventional driver. It is noted that at a 30-A load, the proposed current-source gate driver saves approximately 2.2 W (a reduction of 23%) compared

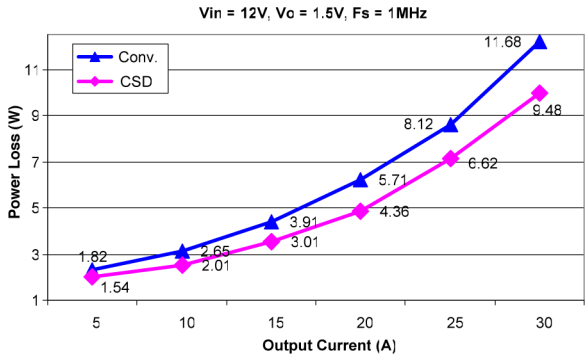


Fig. 19. Power loss comparison at 1.5-V/ 30-A condition. (Top) Conventional driver (Conv). (Bottom) CSD.

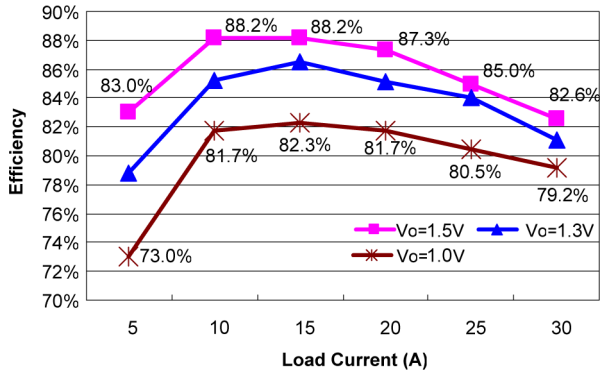


Fig. 20. Efficiency at different output voltages.

to the conventional driver. This loss savings is significant for multiphase VRs. For example, for a five-phase VR, the total loss savings would be 11 W.

Another interesting observation is that if the power loss per phase is limited to 9.5 W, the buck converter with conventional gate drive can only provide 26-A output current, while the buck converter with the current-source gate driver can provide 30 A (an improvement of 15%). In other words, if the total output current is 120 A, we need five phases (120 A/26 A per phase) for the conventional gate driver and only four phases (120 A/30 A per phase) for the current source driver. This yields a significant potential cost savings and space savings enabling high power density.

Fig. 20 shows the measured efficiency for the CSD at different output voltages as a function of load current. It is observed that at 1.0 V/30 A, the efficiency is 79.2%, which is almost the same as 79.4% of the conventional driver at 1.5 V/30 A (see Fig. 18). Therefore, the output voltage can be reduced from 1.5 to 1.0 V using the CSD without an efficiency penalty. This is important since the VR output voltage is reducing to approach sub-1-V in the near future.

VI. Conclusion

In this paper, a new current-source MOSFET gate drive circuit was proposed for a synchronous buck converter. The proposed gate driver is able to drive the control and the synchronous

MOSFET independently with different drive currents, enabling optimal design.

The new drive circuit maintains the following advantages: 1) significant switching loss reduction; 2) gate energy recovery; 3) reduced conduction loss and reverse recovery loss of the body diode; and 4) ZVS for the driver switches. The improved CSD using integrated inductors was also presented to reduce the magnetic core count and the core loss due to magnetic flux cancellation.

The new drive circuit can also be used to drive the two MOSFETs in one leg of an HB converter or an FB converter to further reduce the turn-off loss at megahertz switching frequencies.

Experimental results demonstrate the advantages of the new drive circuit. A significant efficiency improvement has been achieved. At 1.5-V output, the new driver improves the efficiency from 84% using a conventional driver to 87.3% (an improvement of 3.3%) at 20 A, and at 30 A, from 79.4% to 82.8% (an improvement of 3.4%).

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