A New ZVS Non-Isolated Full-Bridge Voltage Regulator Module with Gate Energy Recovery

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***Abstract*- In this paper, a novel self-driven zero-voltage-switching (ZVS) non-isolated full bridge (FB) converter is presented for 12V input VRM application. Existing multiphase buck controller and buck driver can be directly used in the proposed converter. The advantages of the proposed converter are: 1) duty cycle extension; 2) significant switching losses reduction due to ZVS of all the control MOSFETs; 3) reduced reverse recovery loss and lower voltage rating synchronous rectifier (SR) MOSFET with lower $R_{DS(on)}$; 4) high drive voltage to reduce $R_{DS(on)}$ and the conduction losses of SRs due to gate energy recovery capability; 5) reduced body diode conduction and no external drive IC chips with dead time control needed for SRs due to the inherent current source gate drive circuit structure. The experimental results verify the principle of operation and significant efficiency improvement. At 12V input, 1.3V output and 1MHz switching frequency, the proposed VRM improves the efficiency from 80.7% using the buck converter to 83.6% at 50A, and from 77.9% using the buck converter to 80.5% at 60A.**

***Index term*: voltage regulator module (VRM), zero-voltage-switching (ZVS), full-bridge (FB), self-driven, synchronous rectifier (SR)**

I. INTRODUCTION

In high current and low voltage applications, the output voltage of a Voltage Regulator Module (VRM) keeps reducing while the output currents are increasing consistently due to the high power consumption of microprocessors. In order to achieve high power density, high switching frequency (> 1MHz) operation of VRMs is strongly desired [1]- [2].

In order to extend the extremely low duty cycle, the tapped inductor buck converter is proposed in [2], however, the leakage inductance due to the nonideal coupling of the coupled inductor causes high voltage spikes over the main power MOSFET. Non-isolated half-bridge (NHB) converters with extended duty cycle are proposed in [3]-[5], which reduce the current stresses of the power MOSFETs and improve efficiency. A family of buck-type dc-dc converters including forward, push-pull, half-bridge topologies, which take advantages of autotransformers, are proposed in [6]. Similarly, an autotransformer version converter with input current shaper for VRM applications is proposed in [7]. Unfortunately, in the above mentioned topologies, the control power MOSFETs are still under hard-switching condition, which results in high switching losses at high frequencies (>1MHz).

A phase-shift buck (PSB) converter featuring zero-voltage-switching (ZVS) and reduced SR MOSFET conduction loss is proposed in [8]. This topology is able to form an autotransformer structure during the power transfer stages, which can significantly reduce the current stresses of the transformer windings. However, because more active MOSFETs are used in the PSB converter and all control MOSFETs have floating grounds, the gate drive signals become complex and external level-shift drive circuits must be used. In order to recover the gate drive losses of the SR MOSFETs, an improved self-driven 12V VRM topology is proposed based on the PSB converter in [9], which achieves high efficiency and is attractive in VRM applications. Though a simple level-shift drive scheme is used, the drive path of the control MOSFETs goes though the synchronous MOSFETs, which increases the parasitic inductance, especially the common source inductance. This may result in high turn off losses. Additionally, the drain-to-source voltage oscillation of the SR MOSFETs, due to the reverse recovery of the body diode, may cause high voltage spikes over the control MOSFETs.

A non-isolated full-bridge (NFB) topology with direct energy transfer capability is proposed in [10]. Due to direct energy transfer capability, the current stresses of the transformer windings and the power MOSFETs are reduced. In this NFB topology, traditional phase-shift control is applied and auxiliary transformer windings are used to drive the SR MOSFETs. The disadvantage of using the drive transformer self-driven scheme is that the leakage inductance causes the propagation delay of the SR drive signals, which results in a high conduction loss of the body diode.

The objective of this paper is to present a new ZVS self-driven non-isolated full-bridge (FB) converter, which can use existing multiphase buck controller and buck driver directly. The proposed topology achieves duty cycle extension and features ZVS, self-driven capability with SR gate energy recovery and reduced voltage stress over the SR MOSFETs. Owing to the duty cycle extension, lower output inductors can be used and the reverse recovery losses of the body diodes can also be reduced. All these advanced features improve the efficiency significantly to achieve high switching frequency and fast dynamic response.

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II. PROPOSED ZVS SELF-DRIVEN NON-ISOLATED FB VRM

A. Derivation of Proposed ZVS Non-Isolated FB VRM

Fig. 1 illustrates the derivation of the proposed ZVS self-driven converter. Fig. 1(a) shows the conventional isolated FB converter with current doubler rectifier for high current applications. V_{in} is the input voltage, Q_1-Q_4 are the control MOSFETs, T_r is the power transformer (n is the turns ratio), L_k is the leakage of the transformer and Q_5-Q_6 are the SR MOSFETs, L_1 and L_2 are the output filter inductors and C_o is the output filter capacitor.

The derivation of the proposed converter includes the following steps:

1) In order to achieve fast switching and gate energy recovery, the dual low side current source MOSFET driver, proposed in [11], is used to drive SR Q_5 and Q_6, as shown in Fig. 1 (b). In the current source driver, S_1-S_4 are the gate drive switches, L_r is the resonant inductor and V_c is the drive voltage. According to the operation given in [11], in order to achieve the desired drive waveforms for Q_5 and Q_6, the asymmetrical control is applied to drive S_1-S_4.

2) It should be observed that for 12V input VRM applications, there is no requirement for isolation. Therefore, it is possible to have the primary side of the transformer share the same ground of the secondary side as indicated in Fig. 1 (b).

3) It is interesting to notice that the dual low side current source gate drive circuit is also a full-bridge structure. Though phase-shift control is generally used for the conventional FB converter, the asymmetrical control featuring ZVS capability can also be applied to two bridge legs of the FB converter respectively, while the voltage applied to the primary side of the transformer is still symmetrical. The other benefit of the asymmetrical control is that existing buck drivers can be directly used to drive the upper and lower MOSFETs in one bridge leg. Therefore, the drive switch pair (S_1&S_2 and S_3&S_4) can merge with the control MOSFETs (Q_1&Q_2 and Q_3&Q_4) of the primary side respectively as indicated in Fig. 1 (c). At the same time, the resonant inductor L_r can merge with the leakage inductance L_k. The primary side of the transformer shares the same ground as the secondary side, which can provide the gate drive currents a path for the SRs Q_5 and Q_6. Therefore, by connecting the bridge leg midpoints of A and B to the gate terminals of Q_5 and Q_6, as shown in Fig. 1(d), the proposed FB VRM can be derived. Thus V_{in} becomes the SR gate drive voltage.

Since the MOSFETs in the current source driver emerge with the main power MOSFETs in the proposed circuit, there is no additional control required for the SR MOSFETs. In addition, the resonant inductor is eliminated, which helps to shrink the size of the converter and increase the power density. Meanwhile, owing to the gate energy recovery of the current source gate driver, high gate drive voltage can be applied to the SR MOSFETs Q_5 and Q_6 to reduce the conduction losses further.

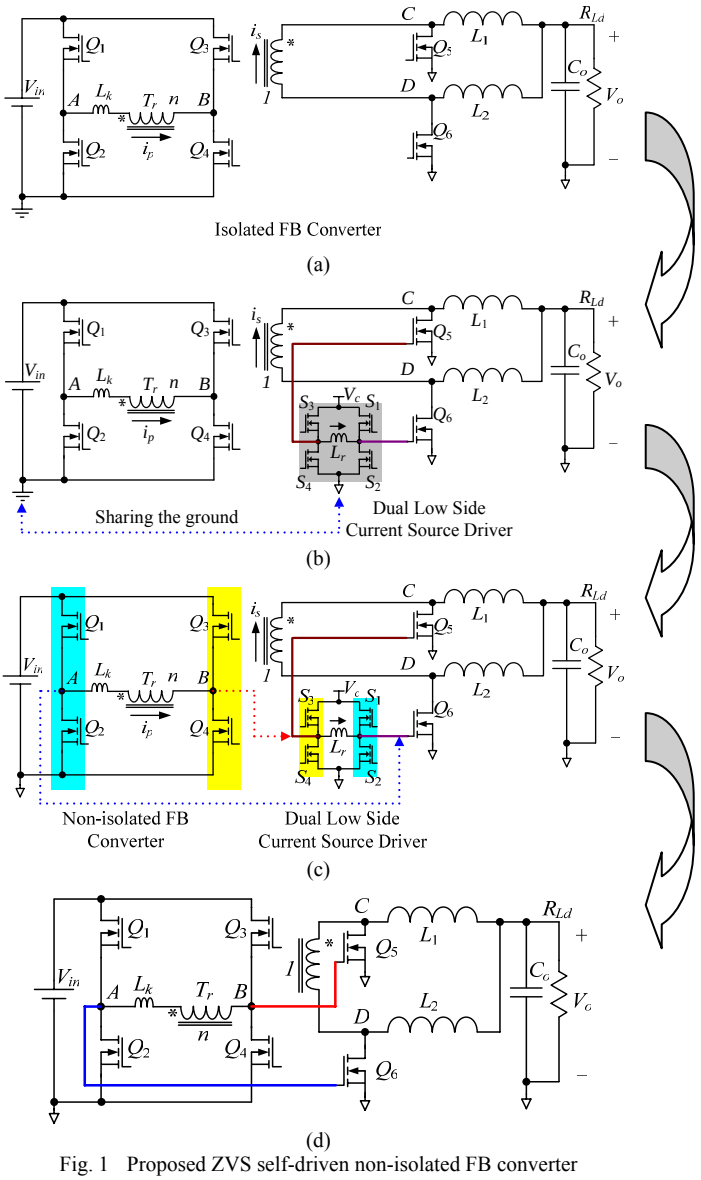


Fig. 1 Proposed ZVS self-driven non-isolated FB converter

B. Principle of Operation

The key waveforms of the proposed topology are shown in Fig. 2. The purpose of the asymmetrical control, for each leg, is that Q_1 and Q_2, and Q_3 and Q_4 are controlled complementarily with the dead time set to achieve ZVS. It is noted that the primary voltage v_{AB} is still a symmetrical waveform. In this case, Q_1 and Q_3 are the upper control MOSFETs; Q_2 and Q_4 are the lower control MOSFETs.

There are twelve switching modes in a switching period. The equivalent circuits in half of a switching cycle are shown in Fig. 3 accordingly. D_1-D_4 are the body diodes and C_1-C_4 are the intrinsic output capacitors of Q_1-Q_4 respectively, assuming C_1=C_2=C_3=C_4=C_{oss}. C_{gs_Q5} and C_{gs_Q6} are the input capacitors of SRs Q_5 and Q_6 respectively, assuming C_{gs_Q5}=C_{gs_Q6}=C_{gs}. The output inductors are large enough to be regarded as current sources. The inductor currents i_{L1}=i_{L2}=I_o/2, where I_o is the total output current.

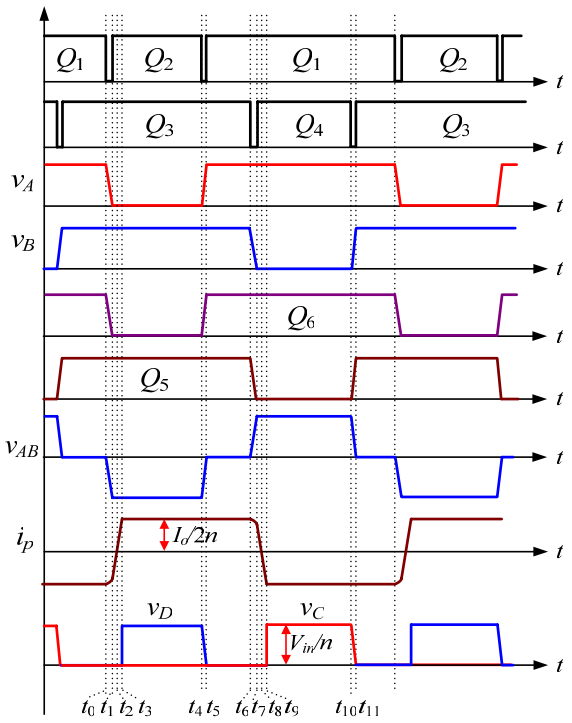


Fig. 2 Key waveforms of the proposed topology

1) Mode 1 [t_0, t_1] [Fig. 3 (a)]: Prior to t_0, Q_1 and Q_3 are on, the voltage over the primary side and the secondary side of the transformer is zero. The gate drive voltages of the SR Q_5 and Q_6 are all clamped high to the input voltage. At t_0, Q_1 turns off, the primary current i_p charges C_1 and discharges C_2 and C_{gs_Q6} at the same time. As C_1 and C_2 and C_{gs_Q6} limit the slew rate of the voltage of C_1, Q_1 is under zero-voltage turn-off condition. It should be noted that the gate drive energy of the SR capacitance C_{gs_Q6} is returned to the input voltage source so that the high gate drive losses of SRs can be reduced significantly. During this stage, the energy to discharge C_2 and C_{gs_Q6} is provided by the leakage inductance of the transformer.

At t_1, $v_{C1}=V_{in}$ and $v_{C2}=0$, D_2 conducts, which provide a zero-voltage turn-on condition for Q_2. The interval of [t_0, t_1] and the value of i_p at t_1 are

$$t_{1,0} = \frac{1}{\omega_r} \cdot \sin^{-1}\left(\frac{2nV_{in}}{Z_r \cdot I_o}\right) \tag{1}$$

$$I_p(t_1) = \frac{I_o}{2n} \cdot \sqrt{1-\left(\frac{2nV_{in}}{Z_r \cdot I_o}\right)^2} \tag{2}$$

where $Z_r = \sqrt{L_k/(2C_{oss}+C_{gs})}$ and $\omega_r = 1/\sqrt{L_k(2C_{oss}+C_{gs})}$.

2) Mode 2 [t_1, t_3] [[Fig. 3 (b)]: During this stage, i_p decreases and is not enough to power the load. i_{L1} freewheels through the body diode of Q_5 and i_{L2} freewheels through Q_6. At t_2, i_p increases inversely but is still not large enough to power the load.

3) Mode 3 [t_3, t_4] [[Fig. 3 (c)]: At t_3, i_p rises to the reflected load current causing D_3 to turn off. During this stage, the voltage over the transformer is the input voltage and the energy

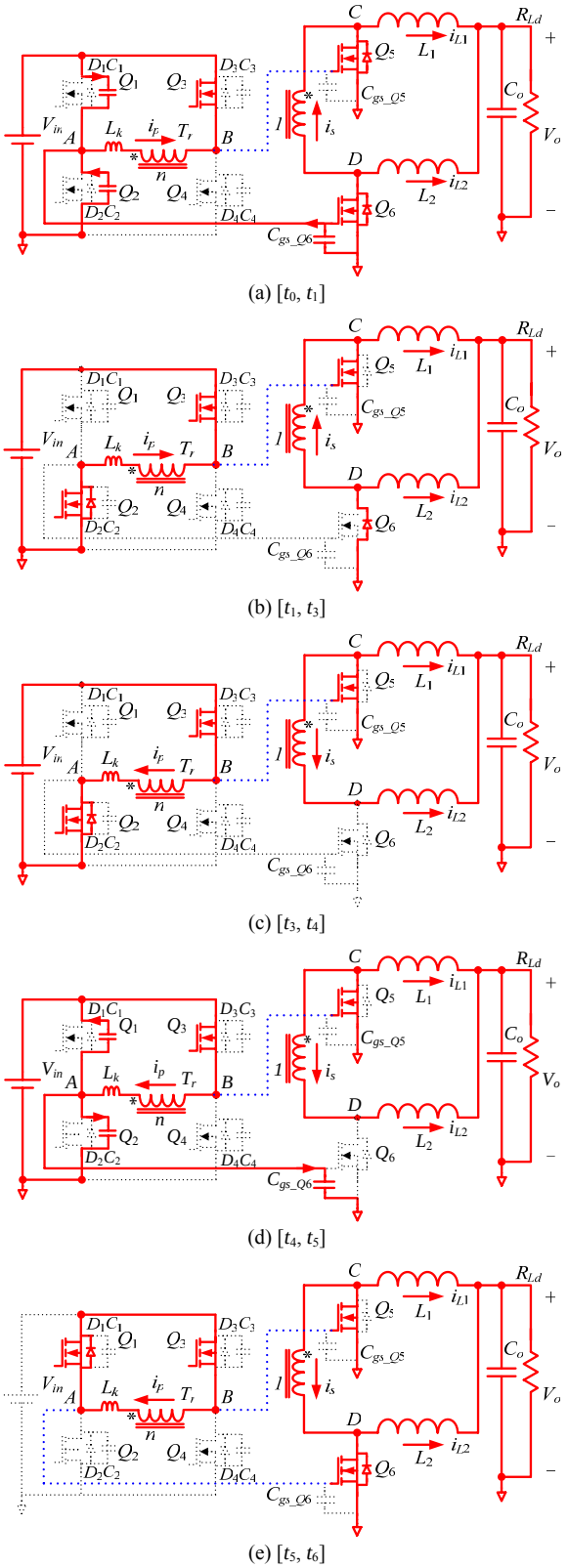


Fig. 3 Equivalent circuits of operation

transfers from the primary side of the transformer to the load.

4) Mode 4 [t_4, t_5] [[Fig. 3 (d)]: At t_4, Q_2 turns off, the primary current i_p charges C_2 and C_{gs_Q6} and discharges C_1. As C_1 and C_2 and C_{gs_Q6} limit the slew rate of the voltage of C_2, Q_2

is under zero-voltage turn-off condition. During this stage, the energy to discharge C_1 is provided by the leakage inductance and L_1. L_1 is large enough to be regarded as a constant current source so that the primary current i_p keeps the value $I_{p2}=I_{L1}/n$, where I_{L1} is the dc current of L_1. The voltage C_2 rises linearly and the voltage of C_2 decays linearly.

5) Mode 5 [t_5, t_6] [[Fig. 3 (e)]: At t_5, D_1 conducts, which provides a zero-voltage turn-on condition for Q_1. The voltage over the primary side is zero. The gate drive voltages of the SRs Q_5 and Q_6 are all clamped high to the input voltage again. At t_6, the other half of switching cycle starts and the principle of operation is similar except for polarity changes.

III. Duty Cycle Loss, ZVS Condition and Loss Analysis

A. Duty Cycle Loss

As shown in Fig. 2, during [t_0, t_3] and [t_6, t_9], the leakage inductance of the transformer limits the rise (or decay) slope of i_p. Finite time is required for i_p to make the transition from the positive direction to the negative direction (or vice versa). During this transition time, v_{AB} is $+V_{in}$ or $-V_{in}$, i_p is lower than the reflected load current and all the SR MOSFET diodes conduct. This makes the secondary rectified voltage v_A and v_B zero, thus v_{AB} loses the voltage in [t_0, t_3] and [t_6, t_9] respectively.

The duty cycle loss D_{loss} during [t_0, t_3] and [t_6, t_9] is

$$D_{loss} = \frac{I_o}{n \cdot T_s} \cdot \frac{L_k}{V_{in}} \tag{3}$$

where I_o is the output current, L_k is the leakage inductance and n is the transformer turns ratio. It is noted that the leakage inductance of the transformer should be minimized to reduce the duty cycle loss.

B. Condition of ZVS

From the principle of operation in Section II, it is noted that the energy to realize the upper control MOSFETs (Q_1 and Q_3) is provided by the output inductor so that they can achieve ZVS in a wide load range. For the lower control MOSFETs (Q_2 and Q_4), the energy to realize ZVS is provided by the leakage inductance of the transformer, so (4) should be satisfied

$$\frac{1}{2} \cdot L_k \cdot (\frac{I_o}{2 \cdot n})^2 \geq C_{oss} \cdot V_{in}^{\ 2} + \frac{1}{2} \cdot C_{gs\_Q5} \cdot V_{in}^{\ 2} \tag{4}$$

where C_{oss} are the output capacitances of Q_2 and Q_4 and C_{gs_Q5} is the gate capacitance of Q_5. It is noted that the larger leakage inductance, the easier to achieve ZVS. However, the larger leakage inductance results in higher duty cycle loss. Therefore a design tradeoff should be made between the ZVS range and the duty cycle loss.

C. Loss Analysis

(a) Switching Losses

Due to ZVS, there is no turn on losses for the control MOSFETs. The total turn off losses are

$$P_{turn\_off} = \frac{2}{n} \cdot V_{in} \cdot I_{off} \cdot t_{sw\_off} \cdot f_s \tag{5}$$

where I_{off} is the turn off current, t_{sw_off} is the turn off transition time and f_s is the switching frequency.

(b) Conduction Losses of Control MOSFETs

The RMS current flowing through Q_1 and Q_3 is

$$I_{RMS1} = \frac{1}{2} \cdot I_o \cdot \sqrt{1-D} \tag{6}$$

where D is the duty cycle.

The RMS current flowing through Q_2 and Q_4 is

$$I_{RMS2} = \frac{1}{2} \cdot I_o \cdot \sqrt{D} \tag{7}$$

From (6) and (7), the total conduction loss of Q_1-Q_4 is

$$P_{cond\_controlFET} = \frac{I_o^{\ 2}}{2n^2} R_{DS\_controlFET} \tag{8}$$

where $R_{DS\_controlFET}$ is the on-resistance of Q_1-Q_4 , assuming Q_1-Q_4 are the same.

(b) Gate Drive Losses of Control MOSFETs

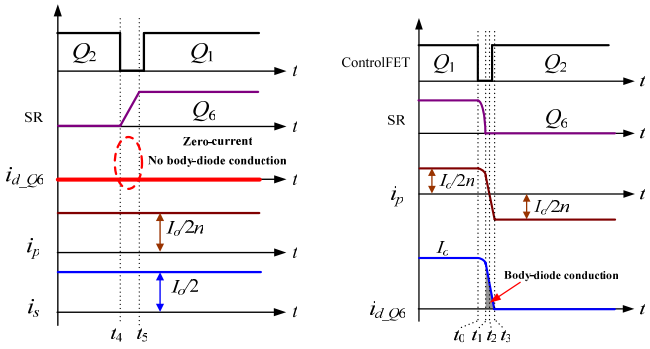
The gate drive losses of Q_1-Q_4 is

$$P_{controlFET} = 4 \cdot Q_g \cdot V_{gs} \cdot f_s \tag{9}$$

where Q_g is the total gate charge of Q_1-Q_4, assuming Q_1-Q_4 are the same. V_{gs} is the gate drive voltage and is usually 5V. It should be pointed that the gate drive losses can be reduced since the Q_{gd} charge is eliminated due to the zero-voltage turn-on condition of the control MOSFETs. For example, for Vishay Si7368DP with Q_{gd}=4.5nC and Q_g=17nC at V_{gs}=5V, the gate drive losses can be reduced by 26% for the primary power MOSFETs.

(c) Body Diode Loss and Reverse Recovery Loss of Synchronous Rectifier

Fig. 4 gives the key waveforms of the turn on transition and the turn off transition of the SR MOSFET Q_6. For the turn on transition [t_4, t_5] of SR Q_6 [see Fig. 4 (a)], the equivalent circuit is shown in Fig. 3 (d). The primary current i_p is the reflected current from the load and charges C_2 and C_{gs_Q6} linearly until v_{gs_Q6} reaches the input voltage at t_5 causing SR Q_6 to turn on. Then the primary side of the transformer is clamped at zero-state and i_p equals $I_o/2n$. Though SR Q_6 turns on before t_6, the drain current of Q_6 remains zero during the zero-state. Therefore, there is no body-diode conduction for the turn on transition of SR Q_6, as shown in Fig. 4 (a).



(a) Turn on transition (b) Turn off transition

Fig. 4 waveforms of turn on transition and turn off transition of SR Q_6

For the turn off transition [t_0, t_1] of SR Q_6 [see Fig. 4 (b)], the equivalent circuit is shown in Fig. 3 (a). At t_0, Q_1 turns off and the leakage inductance L_k starts to resonate with the

capacitance C_2 and C_{gs_Q6} until v_{gs_Q6} reaches zero at t_1, which means SR Q_6 turns off. The current through Q_6 then transfers to the body diode D_6 until i_p changes its polarity and reaches the load current of $I_o/2n$ at t_3. Therefore, from t_1 to t_3 as shown in the shaded area, the body diode conducts see Fig. 4 (b).

From (2), at t_1, the current of the body diode $I_{d\_Q6}(t_1)$ is

$$I_{d\_Q6}(t_1) = \frac{I_o}{2}\left(1+\sqrt{1-\left(\frac{2nV_{in}}{Z_r \cdot I_o}\right)^2}\right) \tag{10}$$

At t_3, i_{d_Q6} reaches zero, so the conduction time of the body diode is

$$t_{13} = \frac{L_k \cdot I_o}{2nV_{in}}\left(1+\sqrt{1-\left(\frac{2nV_{in}}{Z_r \cdot I_o}\right)^2}\right) \tag{11}$$

From (10) and (11), the total conduction losses of the body diodes of the two SRs are

$$P_{body\_diode} = \frac{L_k \cdot {I_o}^2 \cdot V_F \cdot f_s}{4nV_{in}}\left(1+\sqrt{1-\left(\frac{2nV_{in}}{Z_r \cdot I_o}\right)^2}\right)^2 \tag{12}$$

where V_F is the forward voltage drop of the body diode and f_s is the switching frequency. It is noted that the conduction loss of the body diode is proportional to the leakage inductance of the transformer. The larger leakage inductance results in a longer time required [t_1, t_3], as shown in Fig. 4(b), for the primary current to change its polarity, thus resulting in a higher body diode conduction loss.

The reverse recovery loss of the body diode is $P_{rr}=Q_{rr}\cdot V_s \cdot f_s$, where $V_s = V_{in}/n$, which is the peak voltage of the switching node. For the buck converter, the switching node voltage V_s is 12V. For the proposed non-isolated FB converter with n=3, V_s is 4V. Therefore, the reverse recovery loss can be reduced by 67%.

(d) Losses of the SR MOSFETs Gate Driver

As discussed in section II, the gate driver for the SR MOSFETs is actually a current source driver, which can achieve gate energy recovery. The efficiency of the gate energy recovery depends on the gate mesh resistance R_g.

Using the parameters in the experimental prototype in Section V, a curve of the self-driven gate circuit loss as a function of R_g is given in Fig. 5 to demonstrate the potential benefits of using MOSFETs with lower R_g.

D. Loss Comparison

Based on the loss analysis using the parameters of the prototype in Section V, Fig. 6 gives the loss breakdown of the buck converter and the proposed converter. The self-driven ZVS FB converter reduces the switching losses significantly, especially the turn off losses (9W, 12% of the output power) in the buck converter. Other frequency dependent losses including body diode conduction, reverse recovery and gate drive loss are all reduced significantly. In additional, the output inductor conduction losses are also reduced since lower value inductors are used owing to the duty cycle extension. However, the SR conduction losses are increased due to the circulating currents in a FB structure converter and an additional transformer winding loss has to be taken into account. But the overall loss reduction is 4.2W a reduction of 5.4% of the total output power (4.2W/1.3V/60).

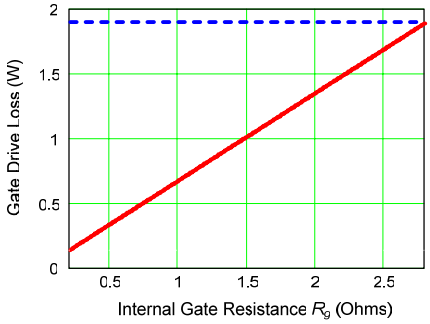


Fig. 5 SR MOSFET gate loss as function of internal mesh resistance R_g

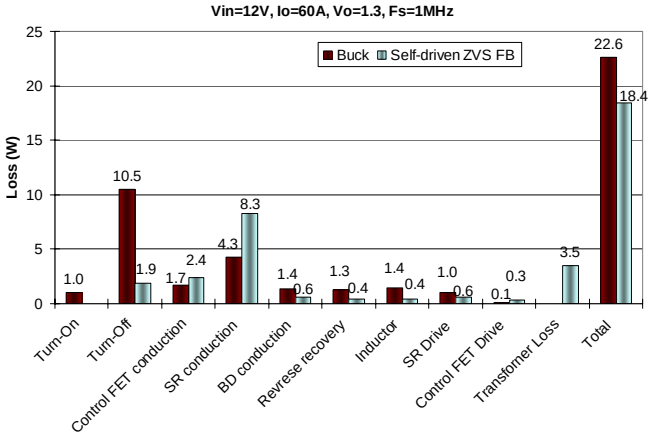


Fig. 6 Loss breakdown comparison

IV. Advantages of Proposed ZVS Self-Driven FB VRM

The advantages of the proposed converter are highlighted as follows:

A. Duty Cycle Extension

The voltage gain of the proposed converter is (13).

$$V_o = \frac{V_{in}}{n}\cdot D \tag{13}$$

As an example, in order to achieve V_{in}=12V, and V_o=1.3V, n=3, the required duty cycle is D=0.33. However, for the same output voltage and input voltage, the duty cycle of a buck converter is only 0.11. Therefore, the duty cycle is extended by three times.

B. ZVS of the Control MOSFETs with Low Voltage Stress

For the proposed converter, owing to the asymmetrical control used to achieve ZVS, there are no turn on losses. The turn off losses are

$$P_{Q1} = \frac{1}{n}\cdot\frac{1}{2}\cdot V_{in}\cdot I_{(off)\_Q1}\cdot t_{sw(off)\_Q1}\cdot f_s \tag{14}$$

In a practical design, for instance, for V_{in}=12V, V_o=1.3V, n=3, switching frequency 1MHz, output inductance L_f=300nH

and total output current I_o=60A, for two phase buck converters, the turn off current of each control MOSFETs is 35A and the total turn off current is 70A. However, for the proposed converter, the turn off current of the control MOSFETs is only 10A and the total turn off current is 40A (a reduction of 43%). This results in a significant reduction of turn off losses due to the duty cycle extension.

For a 12V input buck converter, 30V MOSFETs are generally used for the control MOSFETs. In the proposed converter, the voltage stress of the control MOSFETs is the input voltage (12V, usually), so a 20V MOSFETs with lower $R_{DS(on)}$ can be used to reduce the conduction losses.

C. *Gate Energy Recovery of SR MOSFETs and Reduced Body Diode Conduction*

One of the most important advantages of the new topology is the self-driven capability so that no driver ICs are needed. It is inherent adaptive drive control for SR MOSFETs so that no additional dead time control circuit is needed anymore.

With the self-driven control, the dead time is minimized inherently to reduce the body diode conduction loss in the proposed topology. For the turn on transition, there is no body diode conduction. For the turn off transition, the body diode conduction is minimized. More importantly, the self-driven circuit actually forms a current source drive using the leakage inductance of the transformer to ensure fast turn on and turn off transition of the SRs and recovery of the gate energy. This is very beneficial at high switching frequency operation (>1MHz) and allows for high drive voltages (input voltage, usually 12V) for SR MOSFETs with lower $R_{DS(on)}$ to reduce the conduction losses further. Compared to 5V drive voltage for the SR MOSFETs, the $R_{DS(on)}$ value with 12V drive voltage is reduced by 20%. This translates into a 20% reduction of the SR conduction loss.

D. *Reduced Conduction Losses and Reverse Recovery Losses of SR MOSFETs*

Similar to the control MOSFETs, 30V rated MOSFETs are generally used as SRs in 12V input buck converters due to the parasitics. However, due to duty cycle extension of the new topology, the voltage stresses of the SR MOSFETs (including the ringing) are reduced to less than 10V when n=3. Thus lower voltage rating MOSFETs with lower $R_{DS(on)}$ can be chosen to reduce the conduction further. New low-voltage devices, with extremely low $R_{DS(on)}$ (sub 1 mΩ), will be in production in the near future. This provides the new topology with potential to achieve an even greater efficiency improvement. For example, if the 7V lateral power MOSFETs using CSP concept with 0.9 mΩ at V_{GS}=6V is chosen as SR MOSFETs [12], the SR conduction losses can be further reduced from 8.1W to 4.3W. This is a significant loss reduction of 4.9% of the output power (3.8W/1.3V/60A).

The reverse recovery loss of the body diode is $P_{rr}=Q_{rr}\cdot V_s\cdot f_s$, where $V_s= V_{in}/n$, is the peak voltage of the switching node. Therefore, for n=3, since V_s is reduced from 12V to 4V, the reverse recovery losses are also significantly reduced by as much as 67%.

E. *Design Compatibility with Existing VRM Technology*

Another important aspect mentioned is that since the control MOSFETs are located in the legs of the FB structure, low cost commercial drive ICs of high side and low side drivers for the conventional buck converter can be directly used to drive these control MOSFETs without additional auxiliary circuitry. The SR MOSFET can be driven directly without extra driver nor auxiliary windings. Exiting VRM controller and existing Buck converter driver can be used. In addition, the design procedure of the proposed topology is very straightforward and similar to a traditional FB converter, which is familiar to most design engineers. Therefore, less design efforts are required by the proposed topology.

V. Experimental Verification And Discussion

A 1MHz self-driven ZVS FB VRM was built to verify the operation of principle and demonstrate the advantages. Fig. 7 shows a photograph of the prototype. The specifications are as follows: input voltage V_{in}=12V; output voltage V_o=1.3V; output current up to 60A; switching frequency f_s=1MHz, transformer turns ratio n=3:1. The PCB uses six-layers of 2 oz copper. The components used in the circuit are listed as follows: Control MOSFET Q_1- Q_4: Si7368DP; Synchronous MOSFET Q_5 and Q_6: IRF6691; Power transformer: RM50 (core materials 3F5); Output filter inductors: L_1= L_2=190nH.

Fig. 8 shows the gate drive signal v_{GS}, the voltage across the drain and source v_{DS} of the upper control MOSFET Q_1, which indicates that ZVS has been achieved for Q_1. Similarly, Fig. 9 demonstrates ZVS achievement of Q_2.

Fig. 10 shows the gate drive signal v_{GS} and the drain-to-source voltage v_{DS} of the SR MOSFET Q_6. It is noted that the gate drive voltage is 12V, which means the $R_{DS(on)}$ of SRs is only 1.6 mΩ compared to 2.2 mΩ with 5V gate drive voltage (a reduction of 20%). This reduces the conduction losses by 2.2 W (30% of the output power). Moreover, there is no body diode conduction time for the turn on transition of Q_6 since the gate voltage has been applied before v_{DS} reaches zero. It is also noted that the peak rectified voltages v_C and v_D (i.e. drain-to-source voltage of the SR MOSFET) is only 5V, which means a significant reduction of the reverse recovery losses.

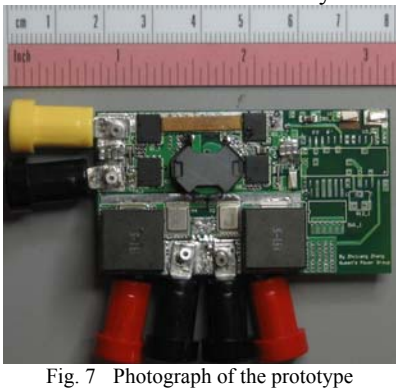


Fig. 7 Photograph of the prototype

Fig. 11 gives the measured efficiency comparison between the proposed topology and the conventional buck converter at 1.3V output. It is observed that at 50A, the efficiency is improved from 80.7% to 83.6% (an improvement of 2.9%) and at 60A, the efficiency is improved from 77.9% to 80.5% (an improvement of 2.6%). The efficiency improvement is due to the significant reduction of the frequency dependent losses. It is noted that only two SR MOSFETs are used for the current doubler rectifier and the efficiency can be further improved using more SR MOSFETs paralleled and low rating SR MOSFETs to reduce the conduction losses.

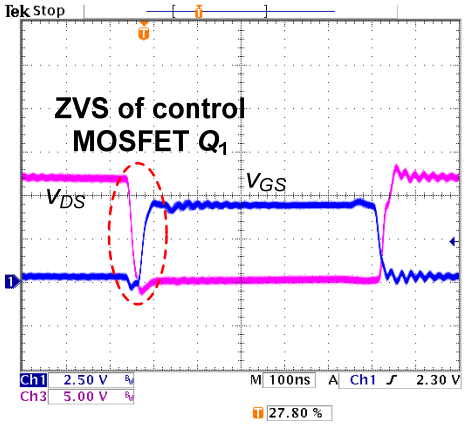


Fig. 8 v_{DS} and v_{gs} of upper control MOSFET Q_1@I_o=60A

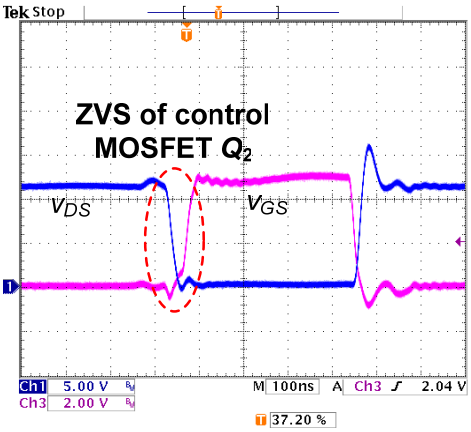


Fig. 9 v_{DS} and v_{GS} of lower control MOSFET Q_2@I_o=60A

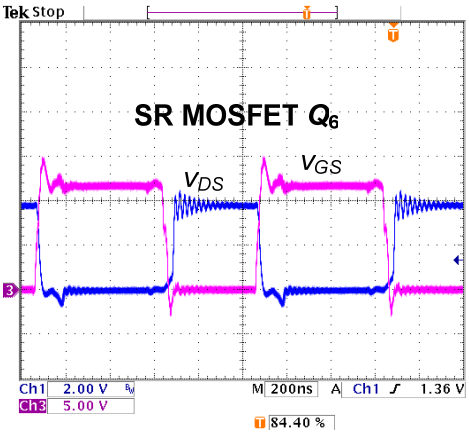


Fig. 10 Gate drive signal and drain-to-source voltage of Q_6@I_o=60A

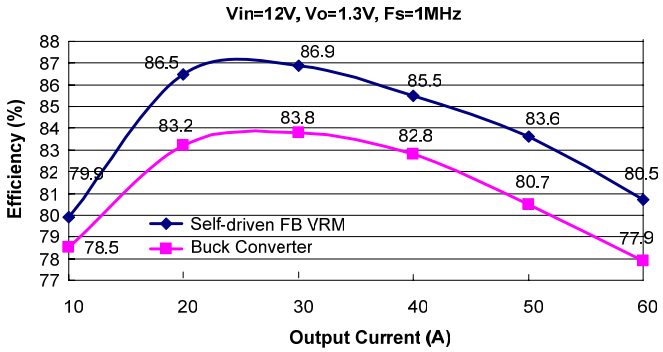


Fig. 11 Efficiency comparison with different load currents:

VI. Conclusion

A novel self-driven ZVS non-isolated FB converter is presented for 12V input VRM applications in this paper. Existing multiphase buck controller and buck driver can be directly used in the proposed converter. A 12V input prototype of the proposed converter with a switching frequency of 1 MHz was built to verify the operation and demonstrates the significant loss savings. The proposed power converter achieves a significant efficiency improvement over the conventional buck converter. At 12V input and 1.3V output voltage, the proposed converter improves the efficiency from 80.7% using the buck converter to 83.6% at 50A, and from 77.9% using the buck converter to 80.5% at 60A.

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