A High Efficiency Current Source Driver with Negative Gate Voltage for Buck Voltage Regulators

Jizhen Fu(*Student Member IEEE*)*, Zhiliang Zhang(*Member IEEE*) **,
Wilson Eberle*** (*Member IEEE*), Yan-Fei Liu (*Senior Member IEEE*)*
and P.C. Sen* (*Fellow IEEE*)

* Queen' Power Group, Department of Electrical and Computer Engineering
Queen's University, Kingston, Ontario, Canada, K7L 3N6
** Aero-Power Sci-tech Center, College of Automation Engineering
Nanjing University of Aeronautics and Astronautics, Nanjing, P. R. China
***School of Engineering, The University of British Columbia, BC, Canada, V1V 1V7
jizhen.fu@queensu.ca, zlzhang@nuaa.edu.cn, wilson.eberle@ubc.ca, yanfei.liu@queensu.ca, senp@post.queensu.ca

***Abstract* -- In this paper a novel current source driver (CSD) for power MOSFETs is proposed. The proposed CSD alleviates the gate current diversion problem of the CSDs in previous work by clamping the gate voltage to a negative value. Therefore, the proposed driver is able to turn off the MOSFET much faster with a higher effective gate current. The idea presented in this paper can also be extended to other CSDs to improve the efficiency further at high output currents. The experimental results verify the benefits of the proposed CSD. For buck converter with 12V input at 1MHz, the proposed driver improves the efficiency from 80.5% using the previous CSD to 82.5% (an improvement of 2%) at 1.2V/30A, and at 1.3V/30A output, from 82.5% to 83.9% (an improvement of 1.4%).**

***Index Terms*—Voltage Regulators (VRs), Buck Converter, Current Source Driver (CSD), Current Diversion Problem, Negative Gate Voltage.**

I. INTRODUCTION

The next generation Voltage Regulators (VRs) feature low output voltage, high output current and high power density [1]. In order to meet the requirements of the future microprocessors, it is necessary to increase the switching frequency as high as possible (>1MHz) within the practical constraints, in order to reduce the size of passive components and achieve better dynamic performance [2].

However, as the switching frequency increases, the efficiency of a buck converter using the conventional voltage source driver suffers from two frequency-dependent losses: 1) switching loss; 2) gate loss [3][4]. In addition to frequency dependent loss, the impact of parasitic inductance introduced by the PCB track and the bonded wire inside the MOSFET package becomes even worse at higher frequency, which significantly introduces extra switching loss [5]-[7].

One way to solve the aforementioned problems is resonant gate drives (RGDs)[8][9], which can recover part of the gate drive energy to the source. Some RGDs can drive two MOSFETs with transformer or coupled inductor [10][11]. Nevertheless, the design of the transformer is really challenging. Most importantly, RGDs only emphasize on gate energy loss, but they can not reduce the switching loss which dominant loss for high frequency operations. Therefore, the efficiency improvement potentials for RGDs are limited. Several Current Source Driver (CSD) circuits are proposed to reduce the switching loss are reported in [12]-[15] to solve the problems of RGDs.

In Section Ⅱ, the current diversion problem of the previous current source drivers is analyzed. Section Ⅲ reports the topology and the operation principle of the proposed CSD, which alleviates the current diversion problem by creating a negative voltage during turn off transition. Section Ⅳ summarizes advantages of the proposed CSD in this paper. In section Ⅴ, the experimental results are presented to verify the features of the CSD proposed. Finally, the conclusion is drawn in section Ⅵ.

II. LIMITATIONS OF PREVIOUS CURRENT SOURCE DRIVERS

The topology of the CSD in [15] is given in Figure 1, and it has the following features:

1. Minimized circulating current and thus minimal conduction loss.
2. Independent of the duty cycle, suitable for narrow duty cycle operation.
3. Smaller inductor value, easier for integrated circuit.
4. Soft switching of driver MOSFETs

However, the CSDs proposed in the previous work have the common problem of gate current diversion during switching transition due to the conduction of the body diode of the gate drive MOSFET. Since the turn off loss dominates the switching loss [16], the turn off transition is analyzed in details in this paper. During the turn off transition, the CSD in Figure.1 can be simplified as the circuit in Figure 2.The gate-to-source voltage V_{gs} in Figure 2 is given below,

$$V_{gs} = -i_g R_g + V_{Cgs} - L_s \frac{di_{ds}}{dt} \quad (1)$$

where V_{Cgs} represents the voltage across the gate-to-source capacitance of the MOSFET Q, i_g is the effective discharge current, R_g represents the gate resistance, L_s is the parasitic inductance including the PCB track and the bonded wire inside the MOSFET package, and i_{ds} represents the drain-to-source current.

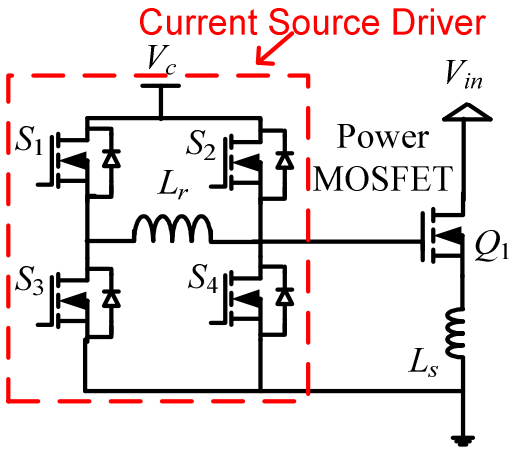

Fig. 1. Topology of Current Source Driver in [15]

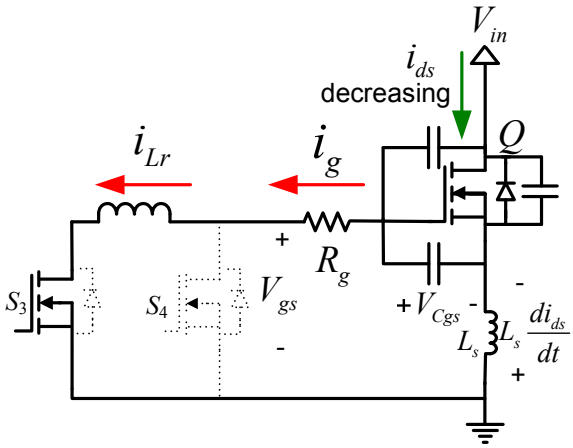

Fig. 2 Simplified Discharging Circuit of Previous Current Source Driver in [15]

The higher the drain current falling rate di_{ds}/dt is, the faster the turn off transition is achieved. According to the relationship in Equation (1), V_{gs} decreases when (di_{ds}/dt) increases. However, when V_{gs} goes below -0.7V, the body diode of S_4 (D_4) in Figure 2 will conduct, clamping V_{gs} at -0.7V. Thus the falling rate of drain current, di_{ds}/dt, is limited. As shown in the equivalent circuit in Figure 3, after D4 is on, part of the inductor current i_{Lr} is diverted through D_4. Therefore, the effective discharge current i_g derived in Equation (2) is reduced, which increases the turn-off transition time and thus weakens the effectiveness of current source driver.

$$i_g = i_{Lr} - i_{D4} \quad (2)$$

where i_g stands for the effective discharge current, i_{Lr} is the current flowing in the inductor, and i_{D4} is the current diverted in the body diode D_4. It should be noted that, due to the effect of L_s, the gate current diversion problem becomes even worse at high load current condition.

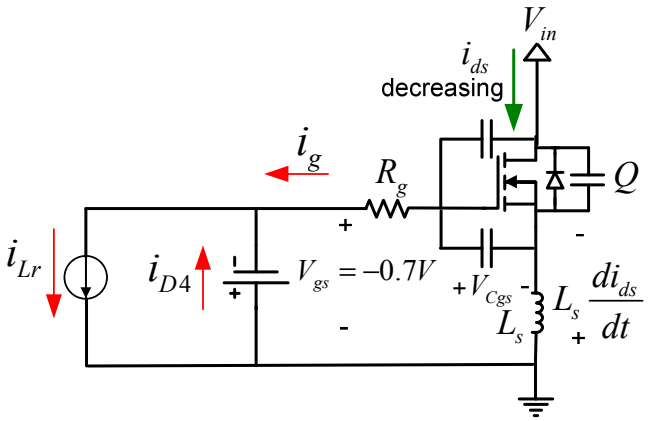

Fig. 3 Equivalent Circuit of Previous Current Source Driver in [15] after D4 is on

To validate the analysis about the limitation of CSD in [15], computer simulation is conducted with SwitcherCAD. Waveforms of the inductor current i_{Lr}, effective discharge current i_g and current diverted in the body diode D_4, i_{D4}, are shown in Figure 4. It's observed from Figure 4 that although the peak current source driver current is 3.3A, the actual discharge current is only 1.5A, which significantly reduces the turn-off speed.

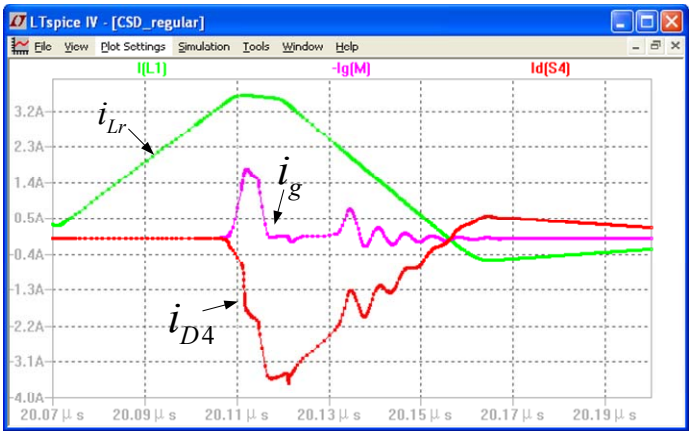

Fig. 4 Simulation Waveforms of Discharging Current of Current Source Driver in Fig.1.[15]

III. Proposed Current Source Driver Circuit With Negative Gate Voltage

A. Proposed Current Source Driver

In order to alleviate the gate current diversion problem

mentioned above and reduce the switching loss, a new CSD with a negative gate voltage during turn off is proposed as given in Figure 5. It is noted that as compared with the CSD in Figure 1, S_4 is replaced by S_4 and S_5, which are palced in series with source terminals connected together as one bi-direction node switch to block the conduction of body diodes. Another key feature of the proposed CSD is to use diodes D_{s1}-D_{s5} as an anti-diode path of the S_4 &S_5 branch to create a negative gate voltage during turn-off transition, which can noticeably increase the effective discharge current.

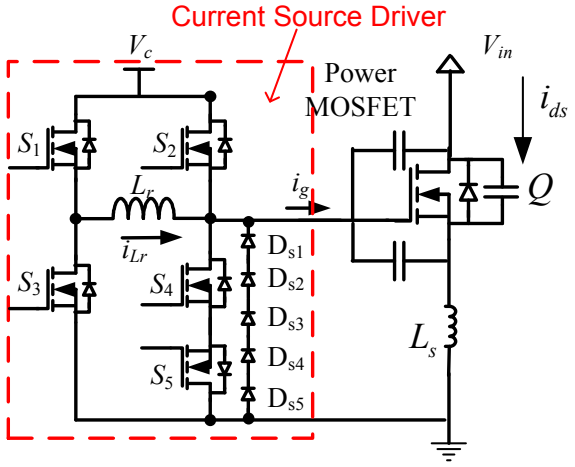

Fig.5. Proposed Current Source Driver with Parasitic Common Source Inductor

The waveforms of the five switches driving signals, v_{gs1}-v_{gs5}, along with the inductor current i_{Lr}, power MOSFET gate-to-source voltage v_{gs}, as well as the drain-to-source current i_{ds} are illustrated in Figure 6. It's worth mentioning that the gate signals of S_4 and S_5 are exactly the same all through the switching cycles. The switches and diodes are controlled to charge and discharge the power MOSFET with a nearly constant current during intervals (t_1, t_2) and (t_5, t_6).

B. *Detailed Turn-On Operation*

The operation principle of the turn on transition is illustrated as follows. Prior to t_0, the power MOSFET is assumed to be in the OFF state.

1. Turn on Precharge (t_0, t_1): At t_0, S_1 is turned on, and the inductor current i_{Lr} rises almost linearly in the positive direction through the current path shown in Fig. 7(a). The pre-charge state ends at t_1, which is usually set by the designer.

2. Turn on switching interval (t_1, t_2): After S_4 &S_5 is turned off at t_1, the inductor current i_{Lr} begins to charge the power MOSFET through the current path given in Fig. 7(b). The interval ends at t_2 when v_{gs} equals to V_c. As indicted in Fig. 4, the inductor current increases due to the resonance of the inductor L_r and the input capacitance of the power MOSFET C_{gs}. During this interval, the gate current still remains at a high level, therefore the power MOSFET is charged with a constant current.The interval ends at t_2 when the switching transition ends.

3. Energy Recovery (t_2, t_3): At t_2, S_1 is turned off and S_2 is turned on (with ZVS). The body diode of the S_3, D_3, is driven on, and the CSD circuit goes into the energy recovery interval. The inductor current decreases sharply to zero through the path shown in Fig. 7(c). The interval ends at t_3 when the inductor current becomes zero. It is worth mentioning that the gate voltage of power MOSFET is clamped to V_c through a low impedance path, which prevents the circuit being false triggered by Cdv/dt effect.

After t_3, the inductor current remains zero and D_3 is turned off. The power MOSFET remains at on state as given in Fig. 7 (d).

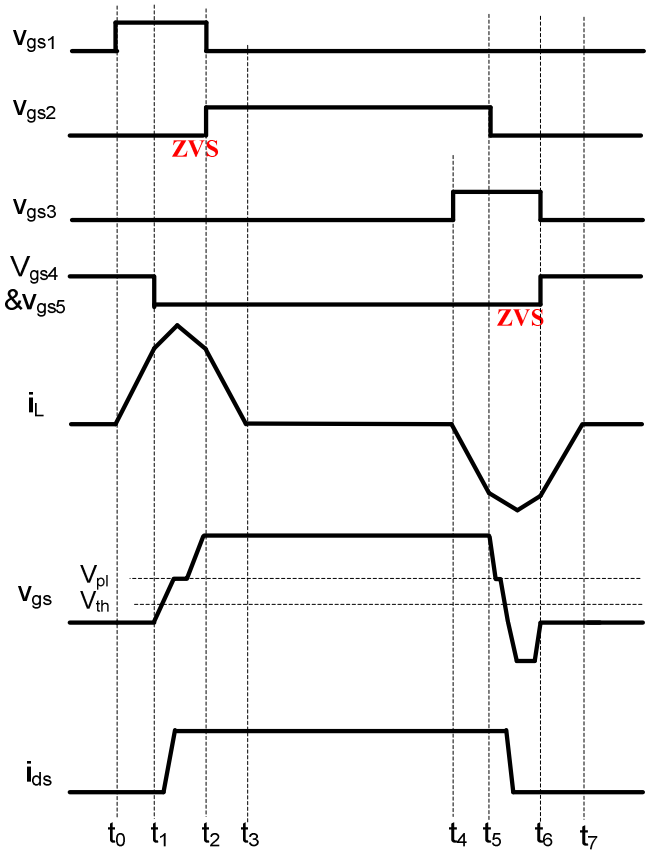

Fig.6. Waveforms of Proposed Current Source Driver

C. *Detailed Turn-OFF Operation*

The operation principle of the turn off transition is illustrated as follows. Prior to t_4, the power MOSFET is assumed to be in the ON state.

1. Turn off precharge (t_4, t_5): At t_4, S_3 is turned on, and the inductor current i_{Lr} rises almost linearly in the negative direction through the current path shown in Fig. 7 (e). The pre-charge state ends at t_5, which is set by the designer, and S_2 is turned off with ZVS at t_5.

2. Turn off switching transition (t_5, t_6): After S_2 is turned off at t_5, the inductor current i_{Lr} begins to discharge the

power MOSFET through the current path given in Fig. 7(f_1). The gate-to-source capacitance of the MOSFET V_{Cgs} and the drain current i_{ds} both decrease in this interval. According to Equation (1), due to the effect of L_s, D_{s1}-D_{s5} are driven on, clamping V_{gs} at -3.5V. Then the equivalent circuit of this interval is shown in Fig. 7(f2). Comparing with the CSD in Fig.1, there is a higher voltage of 2.8V applied to the portion of $L_s i_{ds}/dt$ in Equation (1), which means turn off speed is about four times of CSD in Fig. 1.The power MOSFET can be considered to be discharged with a constant effective discharge current defined by Equation (2). The interval ends at t_6 when the voltage across the gate-to-source capacitance is lower than V_{th} at t_6.

3. Energy Recovery (t_6, t_7): At t_6, S_3 is turned off and S_4& S_5 are turned on with ZVS. The body diode of S_1, D_3, is forced on by i_{Lr}, and the CSD circuit turns into the mode of energy recovery through the path shown in Fig. 7(g). During this interval, the energy stored in L_r is recovered to V_c. The interval ends at t_7 when the inductor current becomes zero.

After t_7, the inductor current remains zero and the D_1 is turned off. The power MOSFET is at the off stat in Fig. 7(h)

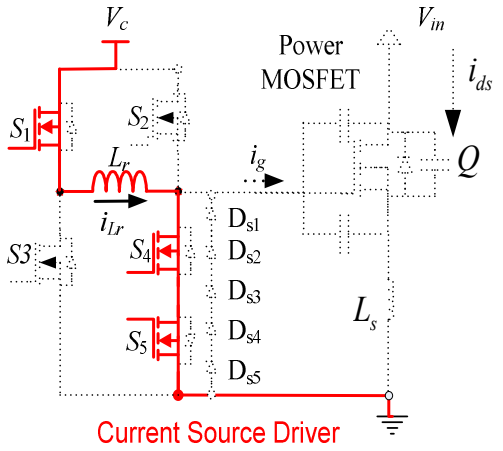

Fig. 7 (a) :(t_0, t_1)

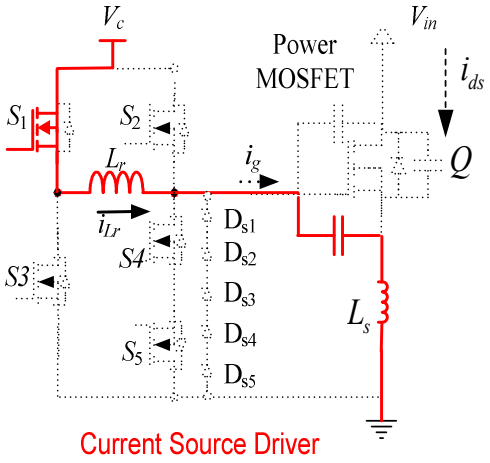

Fig. 7 (b) :(t1, t2)

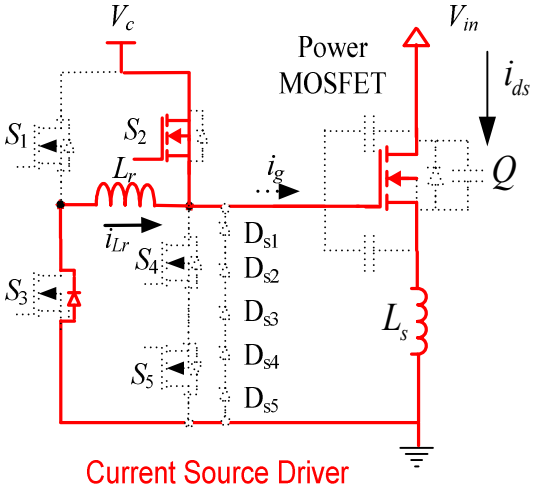

Fig. 7 (c) :(t2, t3)

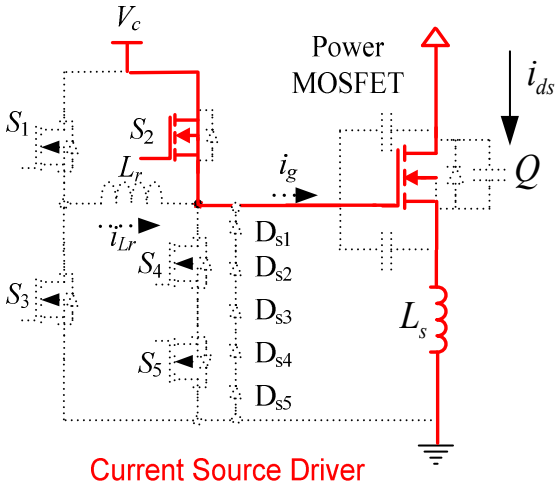

Fig. 7 (d) :(t3, t4)

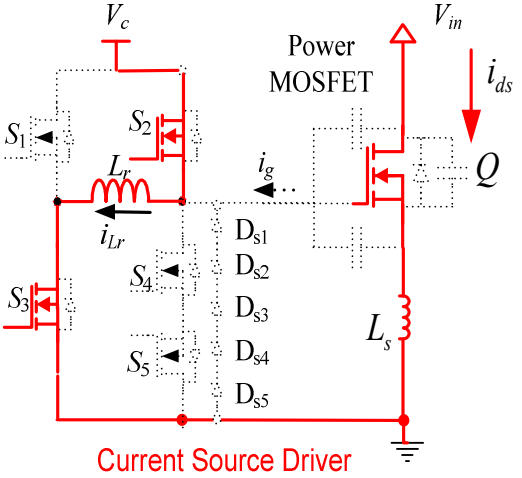

Fig. 7 (e) :(t4, t5)

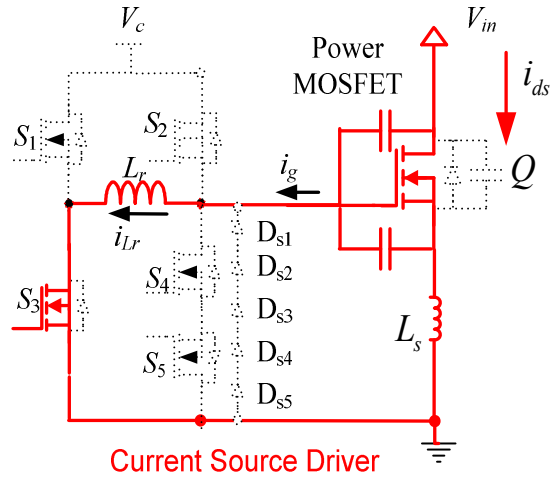

Fig. 7 (f1)

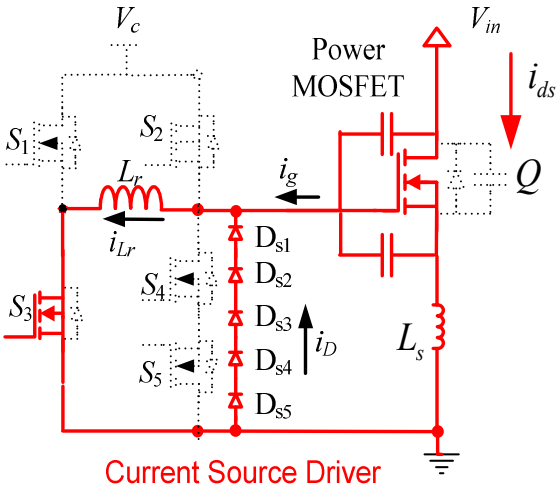

Fig. 7 (f2)

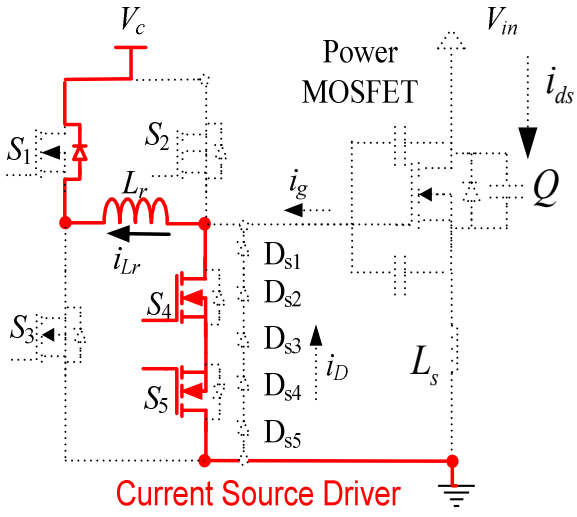

Fig. 7(g): (t6, t7)

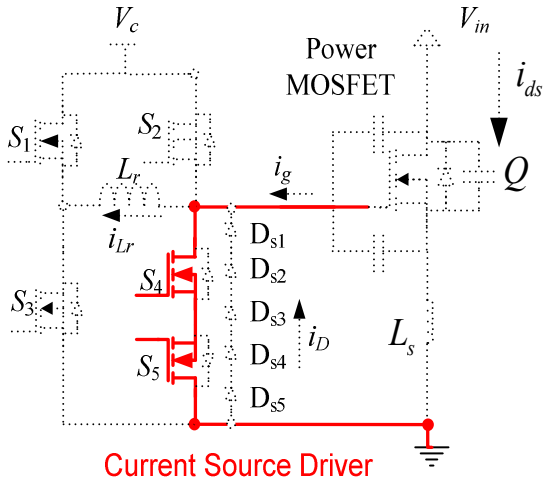

Fig. 7 (h): (t7, t8)

IV. ADVANTAGES

The proposed CSD circuit in this paper has the following advantages:

A. Significantly reduced switching time and the turn-off loss.

During turn-off transition, the gate discharge current is not diverted to diode until the gate voltage reaches a much lower voltage (<-3V). In Fig.1, V_{gs} =-0.7V because of the conduction of D_4, and V_{Cgs} is obtained by Equation (3) using a piecewise linear approximation [17]. And according to the datasheet of power MOSEFT Si7386DP used in the experiment, V_{pl}= 3.5V, V_{th}=2V, R_g=1.7Ω and assume i_g=1A, then $L_s di_{ds}/dt$=1.75V according to Equation (1); while using the proposed CSD, V_{gs} =-3.5V, then $L_s di_{ds}/dt$ =4.55V. Therefore, the turn-off time of proposed CSD is about one third of the original CSD in [15], which means faster turn-off transition.

$$V_{Cgs} = \frac{V_{pl} + V_{th}}{2} \tag{3}$$

where V_{Cgs} is the voltage across the gate-to-source capacitance of the MOSFET Q, V_{pl} means the Miller plateau voltage of Q, and V_{th} is the gate threshold voltage of Q.

B. Less impact of parasitic inductance

Whether in conventional drivers or CSDs in the previous work, the parasitic inductance significantly decelerates the switching speed and hereby reduces the efficiency [16]. The proposed circuit can well alleviate the impact of parasitic inductor with V_{gs} clamped to a negative voltage, which can reduce the turn-off time and hereby improve the efficiency.

C. Smaller Current Source Inductor

The CSD in this paper works in discontinuous mode, which allows the current source inductor to be very small.

D. *High Stability and Noise Immunity*

The MOSFET is either actively clamped to Vcc during on or to zero during off, which will minimize the possibility for MOSFET to be false triggered by Cdv/dt effect and increase the stability of the circuit.

V. EXPERIMENTAL VERIFICATION AND DISCUSSION

A prototype for a synchronous buck converter shown in Figure 8 was built to verify the advantages of the proposed CSD circuit. The control FET of the buck converter is driven by proposed CSD while the SR is driven by the conventional voltage source driver for the purpose of simplicity. The design parameters are given in Table 1, and the photo of the prototype is shown in Figure 9.

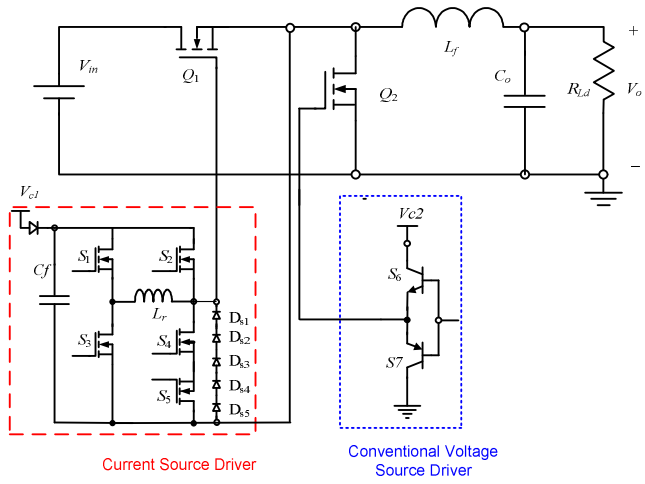

Fig. 8 Buck Converter with proposed Current Source Driver

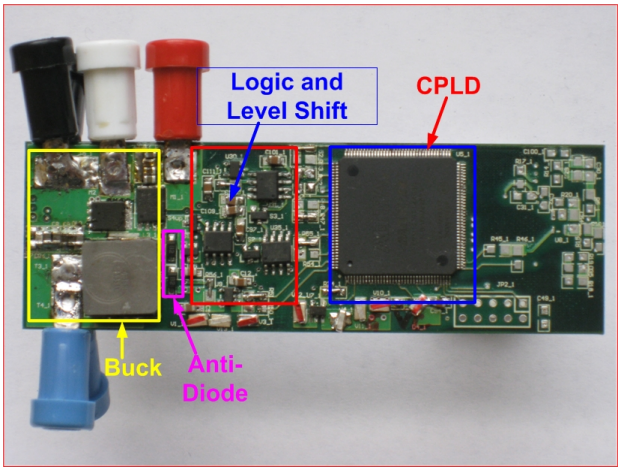

Fig9. Photo of prototype with proposed Current Source Driver Circuit

Figure 10 shows switch gate signals, v_{gs1}-v_{gs5} and four corresponding modes for turn-on and turn-off transition respectively.

TABLE I
DESIGN PARAMETERS

Switching Frequency, f_s	1MHz
Input Voltage, V_{in}	12V
Output Voltage, V_o	1.2-1.3V
SR Gate Drive Voltage, V_{c2}	6.5V
SR, Q_2	IRF6691
CSD Voltage, V_{c1}	5V
Control FET, Q_1	Si7386DP
Output Inductor, L_f(330nH)	Vishay IHLP5050CE
Driver Switches, $S_1 - S_5$	FDN335N
Driver Inductor, L_r(23nH)	Coilcraft B10T_L_(43nH)
Diodes, $D_{s1} - D_{s5}$	MBR0520

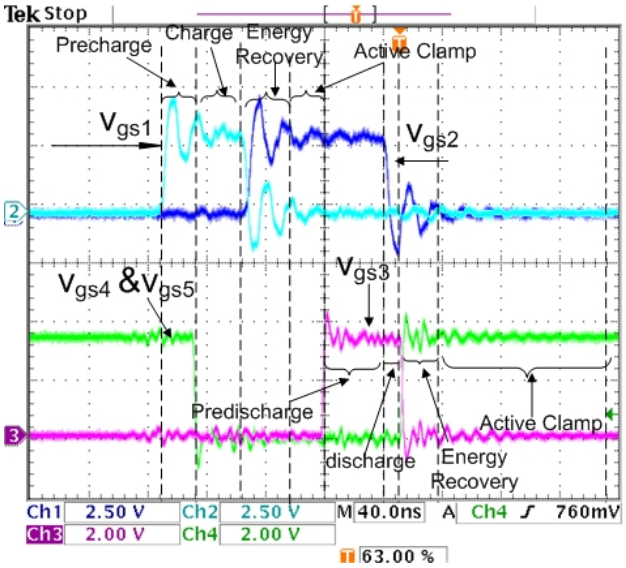

Fig.10 Driver Switch Gate Signals (V_{gs1}-V_{gs5})

Figure 11 illustrates that driver inductor current i_{Lr} and the gate-to-source voltage V_{gs_Q1} of control FET. It can be observed that V_{gs_Q1} is clamped to about -3.5V, Q1 is charged and discharged with nearly constant current. Most importantly there is no Miller Plateau observed in V_{gs_Q1}.It also noted that the effective charge current, i_g, is hard to measure without disturbing the circuit operation. Therefore, the waveform of i_g is not provided in this paper.

It can be observed in Figure 12 that the dead time between V_{gs_Q1} and V_{gs_Q2} is adjusted carefully to be minimal, with a view to avoiding the shoot-through and minimizing the switching loss.

Figure 13 summarizes the efficiencies of the proposed CSD in 1.2V and 1.3V output. Figure 14 shows efficiency comparison among proposed CSD circuit, CSD in proposed in [15] and conventional voltage source driver at 1.2V output, while Figure 15 illustrates the efficiency comparison at 1.3V output. It is noted that, compared to conventional voltage source driver, the proposed CSD increases the efficiency from 73.1% to 82.5% by 9.4% at 1.2V/30A output (a loss

reduction of 5.62W) and from 77.5% to 83.9% by 6.4% at 1.3V/30A output (a loss reduction of 3.84W). Even compared with CSD in [15] , the proposed circuit improves the efficiency from 80.5%to 82.5% at 1.2V/30A output (a loss reduction of 1.2W) and 81.9% to 83.9% at 1.2V/30A output (a loss reduction of 1.24W). It's observed that the proposed CSD achieves higher efficiency improvement at high load current. This is because the proposed CSD significantly alleviates the gate current diversion problem at high current load.

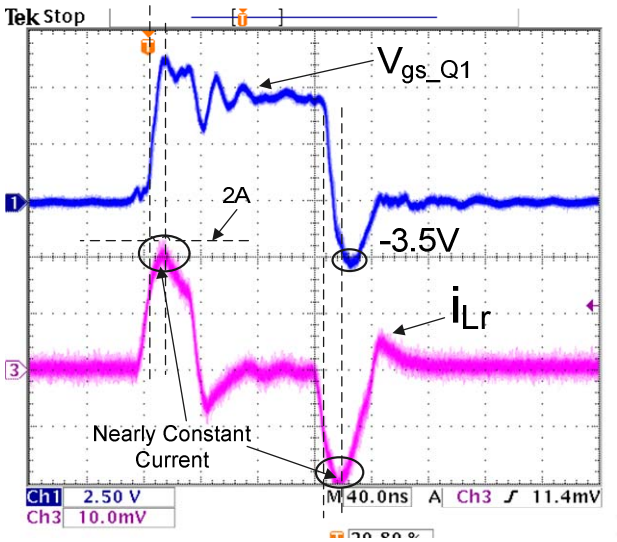

Fig. 11 V_{gs_Q1} and current source inductor current I_{Lr}

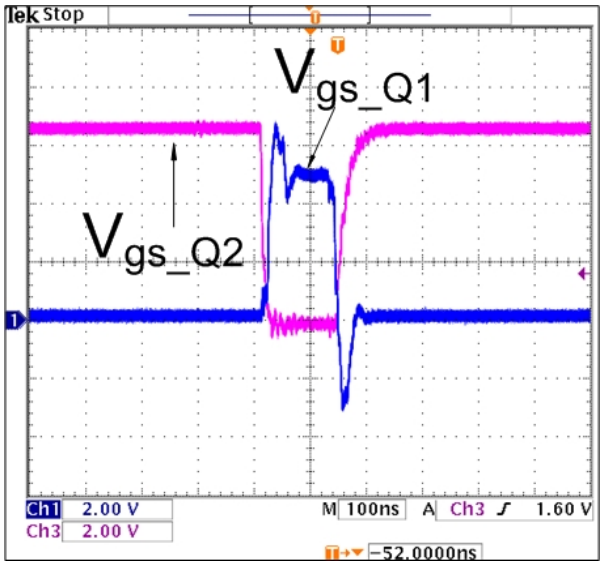

Fig. 12 V_{gs_Q1}&V_{gs_Q2}

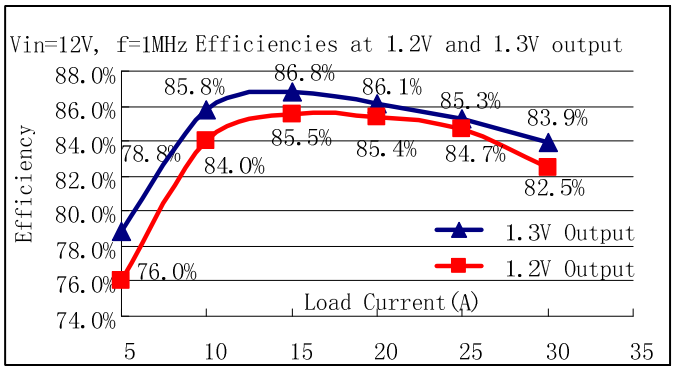

Fig.13 Efficiencies at 1.2V and 1.3V output

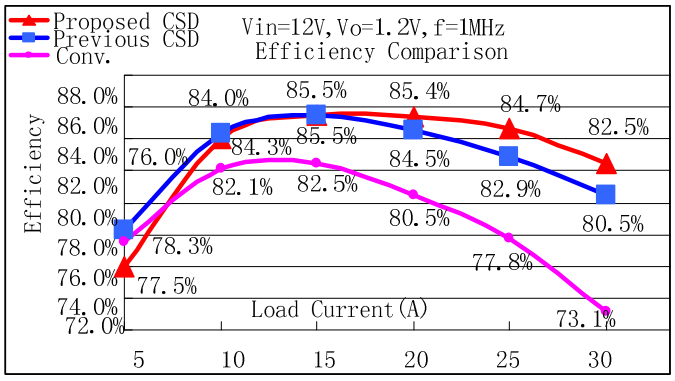

Fig.14 Efficiency Comparison (at 1.2V output): Top: Proposed Current Source Driver; Middle: Previous Current Source Driver in [15]; Bottom: Conventional Driver

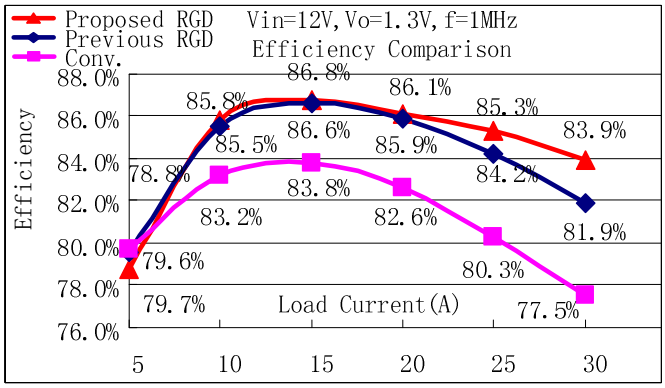

Fig. 15. Efficiency Comparison (at 1.3V output): Top: Proposed Current Source Driver; Middle: Previous Current Source Driver in [15]; Bottom: Conventional Driver

VI. CONCLUSION

In this paper, a new current source driver which can achieve faster switching speed is proposed. The proposed CSD significantly alleviates the problem of gate current diversion by a negative gate voltage. The experimental results demonstrate the great efficiency improvement over the conventional voltage source driver. Compared with the conventional voltage source driver, the proposed CSD

achieves a loss reduction of 5.62W at 1.2V/30A output and 3.84W at 1.3V/30A output. The comparison between the proposed CSD and the driver in [15] demonstrates the circuit proposed in this paper is a better alternative for next generation VRs. More importantly, the basic idea presented in this paper can be also extended to other CSD drivers to enhance the current-source driver performance.

ACKNOWLEDGMENT

The authors gratefully thank IEEE Power Electronics Society (PELS) for their generous travel grant award.

REFERENCES

[1] Ed Standford "Power Technology Road Map for Microprocessor Voltage Regulators" APEC2004 Presentation.

[2] Y.Han, O.Leitermann, D.A.Jackson, J.M.Rivas and D.J.Perreault, "Resistance compression networks for radio-frequency power conversion," IEEE Trans. Power Electron., Vol. 22, No. 1, Mar. 2007, pp. 41 - 53.

[3] R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics", 2nd. Edition, Kluwer Academic Publishers, 2001.

[4] T. Lopez, G. Sauerlaender, T. Duerbaum and T. Tolle, "A detailed analysis of a resonant gate driver for PWM applications," in Proc. IEEE APEC, 2003, pp. 873-878.

[5] D.A.Grant and J. Gowar, "Power MOSFET Theory and Applications". New York: Wiley,1989

[6] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical Loss Model of Power MOSFET," IEEE Trans. Power Electronics, Vol. 21, No.2, Mar. 2006, pp. 310-319.

[7] Y.Xiao, H.Shah, R.Natarajan, E.J.Gutmann, "Analytical Modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics," in Proc.IEEE APEC, 2004, Vol.1, pp 516-521.

[8] D. Maksimovic, "A MOS gate drive with resonant transitions," in Proc. IEEE PESC, 1991, pp. 527-532.

[9] Y. Chen, F.C. Lee, L. Amoros and H. Wu, "A resonant MOSFET gate driver with efficient energy recovery," IEEE Trans. Power Electron., Vol. 19, No.2, pp.470-477, Mar. 2004.

[10] K. Yao and F.C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," IEEE Trans. Power Electron., Vol. 17, No. 2, pp.180-186, Mar. 2002.

[11] Y. Ren, M. Xu, Y. Meng and F.C. Lee, "12V VR efficiency improvement based on two-stage approach and a novel gate driver," in Proc. IEEE PESC, 2005, pp. 2635-2641.

[12] Z. Yang, S. Ye and Y. F. Liu, "A new dual channel resonant gate drive circuit for synchronous rectifiers," in Proc. IEEE Applied Power Electronics Conf., 2006, pp. 756-762.

[13] Z. Zhang, W. Eberle, Z. Yang, Y.F. Liu and P.C. Sen, "Optimal design of current source gate driver for a buck voltage regulator based on a new analytical loss model," in Proc. IEEE PESC, 2007, pp. 1556-1562.

[14] Z. Yang, S. Ye and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," IEEE Trans. Power Electronics, Vol. 22, No.4, Jul. 2007, pp. 1311-1320.

[15] W. Eberle, Z. Zhang, Y. Liu and P. C. Sen, "A high efficiency synchronous buck VRM with current source gate driver," in Proc. IEEE PESC, 2007, pp. 21-27.

[16] Z. Zhang, W. Eberle, P. Liu, Y.F. Liu, P.C. Sen, " A 1-MHz high-efficiency 12-V buck voltage regulator with a new current-source gate driver", IEEE Transactions on Power Electronics, Vol. 23, No. 6, Nov. 2008, pp. 2817-2827.

[17] W. Eberle, Z. Zhang, Y.F. Liu, P.C. Sen, " A Practical switching loss model for buck voltage regulators", IEEE Transactions on Power Electronics, Vol. 24, No. 3, Mar. 2009, pp. 700-7.