A New Discontinuous Current Source Driver for High Frequency Power MOSFETs

Zhiliang Zhang* (*Member*, *IEEE*), Jizhen Fu** (*Student Member*, *IEEE*), Yan-Fei Liu** (*Senior Member, IEEE*) and P. C. Sen** (*Fellow*, *IEEE*)
*Aero-Power Sci-tech Center, College of Automation Engineering
Nanjing University of Aeronautics and Astronautics, Nanjing, P. R. China
**Queen's Power Group, Department of Electrical and Computer Engineering
Queen's University, Kingston, Ontario, Canada, K7L 3N6
zlzhang@nuaa.edu.cn, jizhen.fu@queensu.ca, yanfei.liu@queensu.ca and senp@post.queensu.ca

***Abstract* -- This paper proposes a new Current Source Driver (CSD) with discontinuous inductor current. Compared to other CSDs proposed in the previous work, the most important advantage of the proposed CSD is the small inductance (typically, 20nH at 1MHz switching frequency). This translates into the footprint reduction of as much as 90%. Other features of the proposed CSD includes: 1) fast switching speed and reduced switching loss; 2) discontinuous inductor current with low circulating loss; 3) gate energy recovery; 4) wide range of duty cycle and switching frequency. The experimental results verified the functionality of the proposed CSD. At 1.3V output, the new CSD improves the efficiency from 80.7% using a conventional driver to 85.7% at 25A output, and at 30A output, from 77.9% to 84.4%.**

***Index Terms*— current-source driver (CSD), power MOSFET, buck converter, voltage regulator (VR), voltage regulator module (VRM), resonant gate driver**

I. INTRODUCTION

Resonant gate driver technique was originally used to recover high gate drive loss in high frequency (typically, 5MHz-10MHz) resonant converters [1]-[2]. Self-oscillating resonant gate driver (soft gating driver) with a resonant network was used in radio frequency power amplifiers (>30MHz) featuring sinusoidal waveforms [3]-[4].

Recently, resonant gate driver technique has been used in high current and low voltage application such as Voltage Regulators (VRs). For a conventional voltage source driver, all the gate drive energy is dissipated through resistances in series with the gate and this drive loss is often called CV^2 loss. In VR applications, synchronous rectifier (SR) technique is widely used to reduce the high conduction loss of freewheeling diodes. However, SR MOSFETs normally have high gate drive loss due to the large total gate charge. At the same time, the gate driver loss is proportional to the switching frequency. Therefore, the gate driver loss becomes a penalty when the switching frequency is beyond 1MHz since the switching frequency of VRs has been moved into MHz range. The excessive gate loss not only decreases the overall efficiency but also makes the driver chips hotspots in the whole power supply system.

Different resonant driver topologies have been proposed to reduce the gate drive loss [5]-[9]. The effects of internal parasitic inductance and the parasitic output capacitance of the driver switches were analyzed focusing on their impact on the SR driver losses in different non-isolated resonant driver topologies [10]-[12]. Unfortunately, all the above investigations are generally concentrating on gate energy savings with the different resonant drivers, but ignore the potential switching loss savings that are much more dominant in MHz switching power converters.

Compared to resonant gate drivers, Current Source Drivers (CSDs) are proposed to reduce the dominant switching loss at high switching frequency (>1MHz). Since the basic idea of the CSDs is to achieve the switching loss reduction other than the gate energy recovery for the control MOSFETs, the design criteria turns to be different. The dual channel low side CSD was proposed for the interleaving boost converters in [13]. The advantage of this CSD is that only one inductor is required to drive two power MOSFETs. A continuous current dual channel CSD using bootstrap technique was proposed in [14] to achieve the switching loss reduction and SR gate energy recovery in a buck converter and its improved version was presented in [15]. However, the disadvantage of the continuous CSDs is the gate drive currents vary with the duty cycle and the switching frequency, and furthermore, the inductance value is high (typically, 1μH at the switching frequency of 1MHz). In addition, the switching frequency variation will impact on the inductance value of the continuous CSDs. A discontinuous CSD was proposed to reduce the inductor size and circulating current loss, which can also achieve significant switching loss in [16]-[18]. The key to this CSD is the control of the driver switches to generate discontinuous inductor current waveforms enabling the peak portion of the inductor current to be used to charge/discharge the power MOSFET gate as a near constant current source. Based on an accurate analytical loss model, a significant reduction of the switching transition time and the switching loss was verified for a 1MHz buck converter theoretically and experimentally in [19].

The objective of this paper is to present a new CSD with discontinuous inductor current. Compared to other CSDs proposed in previous work, the most important advantage of the proposed CSD is the small inductance (typically, 20nH at 1MHz switching frequency). This translates into a footprint

reduction of 90%. Other features of the proposed CSD includes: 1) fast switching speed and reduced switching loss; 2) discontinuous inductor current with low circulating loss; 3) wide range of duty cycle and switching frequency; 4) high noise immunity.

II. Proposed CSD and Its Principle of Operation

The proposed CSD is illustrated in Fig. 1. It consists of four drive switches, S_1-S_4, a small inductor L_r and a series capacitor C_s. V_D is the gate drive voltage. In the analysis, it is assumed that the same MOSFETs (n-channel) are used for S_1-S_4. S_1-S_4 are controlled to allow the inductor current to be discontinuous and the power MOSFET can be turned on or off with a non-zero pre-charge current. During charging, or discharging of the power MOSFET, the excess stored energy in the inductor is allowed to return to the series capacitor C_s and drive voltage source.

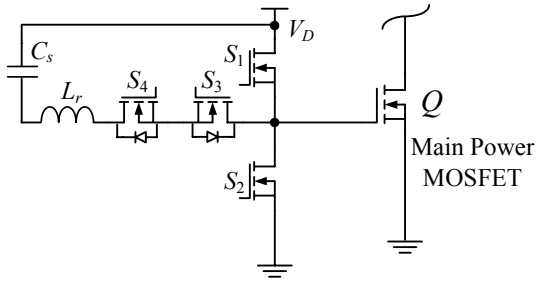


Fig. 1 The proposed discontinuous CSD

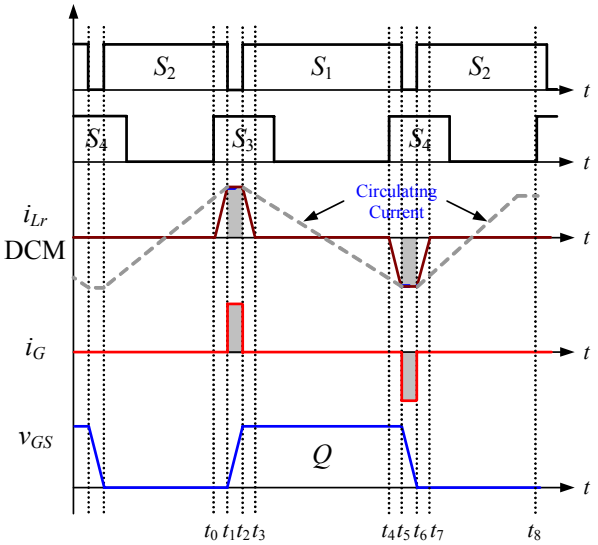


Fig. 2 Key waveforms of the proposed CSD

Fig. 2 illustrates the control gating signals, inductor current i_{Lr}, gate current i_G and power MOSFET gate-to-source voltage v_{GS}. The key waveforms to note are: 1) S_1 and S_2 are switched out of phase with complimentary control to drive Q; 2) the inductor current i_{Lr} is discontinuous to minimize conduction loss compared to the continuous circulating current as shown in dotted line; 3) the gate drive current i_G is relatively constant during turn on and turn off transition, which achieves fast switching speed of the power MOSFET.

A. Principle of Operation

There are eight switching modes in one switching period. The operation of the circuit is explained in the following paragraphs. The equivalent circuits of turn on transition are illustrated in Fig. 3 (a)-(d). D_1-D_4 are the body diodes of S_1-S_4. C_1-C_2 are the intrinsic drain-to-source capacitors of S_1 and S_2. C_{gs} is the intrinsic gate-to-source capacitor of the main power MOSFET Q. The switching transitions of charging and discharging C_{gs} are during the intervals of [t_1, t_2] and [t_5, t_6] respectively as shown in Fig. 2. The peak current i_G during [t_1, t_2] and [t_5, t_6] are nearly constant during the switching transition, which ensures fast charging and discharging the gate capacitance of Q including the miller capacitor. Initially, it is assumed that the power MOSFET is in the off state before time t_0.

1) Mode 1 [t_0, t_1] [Fig. 3 (a)]: Prior to t_0, S_2 is on and the gate of Q is clamped to ground. At t_0, S_3 turns on (with ZCS) allowing the inductor current i_{Lr} to ramp up through D_4. The current path during this interval is C_s-L_r-S_3-D_4-S_2. This interval is the inductor current pre-charge interval and it ends at time t_1, which is a pre-determined time set by the user. Since S_2 is in the on state, the gate of Q is always clamped low.

2) Mode 2 [t_1, t_2] [Fig. 3 (b)]: At t_1, S_2 is turned off, which allows the inductor current to begin to charge the gate capacitor C_{gs}. i_{Lr} charges C_2 plus the input capacitor C_{gs} and discharges C_1 simultaneously. Due to C_1 and C_2, S_2 is zero-voltage turn off. The inductor current continues to ramp up from the pre-charged level.

3) Mode 3 [t_2, t_3] [Fig. 3 (c)]: At t_2, v_{c2} rises to V_D and v_{c1} decays to zero. The body diode D_1 conducts and S_1 turns on under zero-voltage condition. The inductor current continues to conduct through the path C_s-L_r-S_3-D_4-S_1. This interval continues for a short duration until t_3. During this interval, the gate of Q is clamped to the drive voltage V_D. This interval ends when the inductor current reaches zero at t_3. It is noted that it is during this interval when the stored energy in the inductor is returned to C_s. Also during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero.

4) Mode 4 [t_3, t_4] [Fig. 3 (d)]: At t_3, D_4 turns off (with ZCS) and the inductor current is zero. During this interval, the gate of Q remains clamped high. This interval ends at t_4 when the pre-charged interval for the turn off cycle begins as dictated by the PWM control signals.

The equivalent circuits of turn off intervals are illustrated in Fig. 4 (a)-(d).

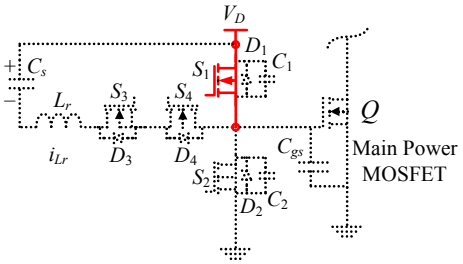
5) Mode 5 [t_4, t_5] [Fig. 4 (a)]: At t_4, S_4 turns on (with ZCS). Since S_1 was previously on, the inductor current i_{Lr} begins to ramp negative through the path C_s-S_1-S_4-D_3-L_r. The energy charge the inductor is provided by C_s. During this interval, the gate of Q remains clamped to V_D. This interval

ends at t_5.

6) Mode 6 [t_5, t_6] [Fig. 4 (b)]: At t_5, S_1 is turned off, which allows the inductor current to begin to discharge the gate capacitor C_{gs}. i_{Lr} discharges C_2 plus the input capacitor C_{gs} and charges C_1 simultaneously. Due to C_1 and C_2, S_1 is zero-voltage turn off. The inductor current continues to ramp negative from the pre-charged level.

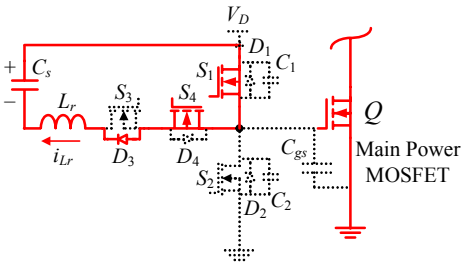
7) Mode 7 [t_6, t_7] [Fig. 4 (c)]: At t_6, v_{c1} rises to V_D and v_{c2} decays to zero. The body diode D_2 conducts and S_2 turns on under zero-voltage condition. The inductor current continues to conduct through the path C_s-L_r-D_3-S_4-S_2. This interval continues for a short duration until t_7. During this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero. It is noted that it is during this interval when the stored energy in the inductor is returned to the drive voltage source. During this interval, the gate of Q is clamped low. This interval ends when the inductor current reaches zero at t_7.

8) Mode 8 [t_7, t_8] [Fig. 4 (d)]: At t_7, D_3 turns off (with ZCS) and the inductor current is zero. During this interval, the gate of Q_1 remains clamped low. This interval ends at t_8 when the pre-charged interval for the turn on cycle begins and the entire process repeats as dictated by the PWM control signal.

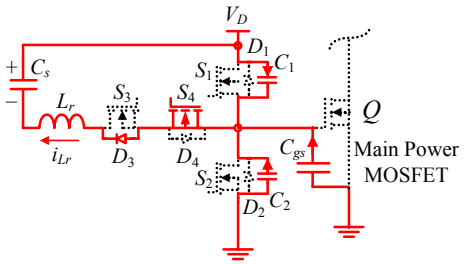


(d) [t_3, t_4]

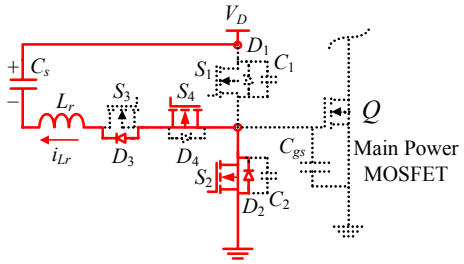
Fig. 3 Equivalent circuits: turn on intervals



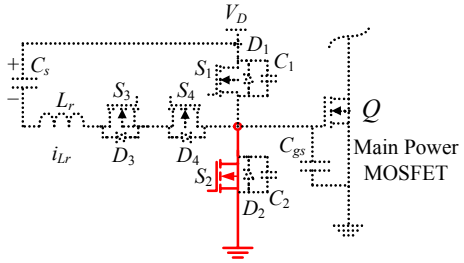
(a) [t_4, t_5]



(b) [t_5, t_6]

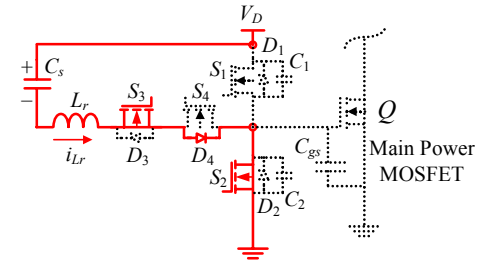


(c) [t_6, t_7]

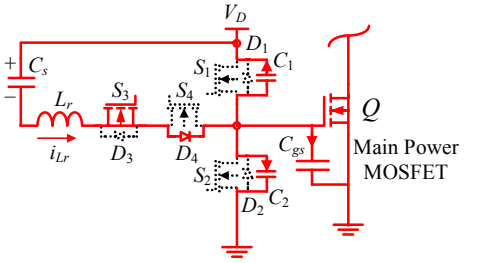


(d) [t_7, t_8]

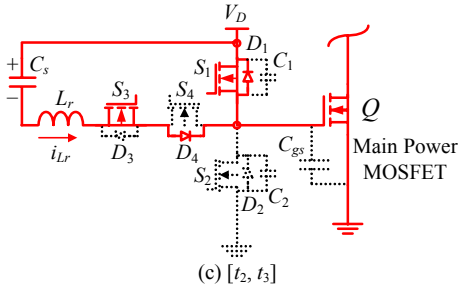
Fig. 4 Equivalent circuits: turn off intervals



(a) [t_0, t_1]



(b) [t_1, t_2]



(c) [t_2, t_3]

B. *Gate Drive Current of The Power MOSFET*

The pre-charge current to turn on and turn off the power

MOSFET is decided by the voltage to charge the current-source inductor and the pre-charge time. For the turn on current, the voltage to charge the inductor is (V_D-V_{Cs}) and the pre-charge time from t_0 to t_1 (t_{10}). For the turn off current, the voltage to charge the inductor is V_{Cs} and the pre-charge time from t_4 to t_5 (t_{54}).

From the volt-second balance condition across the inductor, (1) should be satisfied

$$(V_D - V_{Cs}) \cdot t_{10} = V_{Cs} \cdot t_{32} \quad (1)$$

where V_D is the drive voltage and V_{Cs} is the DC voltage across the capacitor.

From (1), assuming t_{10}=t_{32}, the DC voltage across the series capacitor is

$$V_{Cs} = \frac{V_D}{2} \quad (2)$$

The pre-charge current to turn on the power MOSFT is

$$I_{G\_on} = \frac{V_D - V_{Cs}}{L_r} \cdot t_{10} \quad (3)$$

From (2) and (3), the turn on current is

$$I_{G\_on} = \frac{V_D}{2L_r} t_{10} \quad (4)$$

From (2), the pre-charge current to turn off the power MOSFET is

$$I_{G\_off} = \frac{V_{Cs}}{L_r} \cdot t_{54} = \frac{V_D}{2L_r} \cdot t_{54} \quad (5)$$

From (4) and (5), by changing pre-charge time t_{10} and t_{54}, the turn-on gate current and turn-off gate current can be decided. It is also noted that compared to the discontinuous CSD in [16], since the actual voltage over the inductor is reduced by half as V_D/2, for the same pre-charge time and gate drive current, the proposed CSD can further reduce the inductance value by half.

C. Benefits of The Proposed CSD

The advantages of the new CSD are highlighted as follows:

1) Small current source inductance

One of the most important advantages of the proposed CSD is the small inductance. Compared to the continuous CSDs proposed in [13] and [14], which have the inductance value around 1μH at the switching frequency of 1MHz, the inductance of the proposed circuit is only about 20nH. This is a significant reduction of the inductance value. For example, if Coilcraft Surface Mount (SMT) DS3316 [20] is chosen as 1μH inductor, while Coilcraft SMT 1812SMS [20] is chosen as 22nH inductor, the footprint reduction is as much as 90%. This yields a significant space saving on the Mother Board.

2) Significant reduction of the switching transition time and switching loss

The key idea of the proposed CSD is to control the four drive switches to create a constant current source to drive the main power MOSFETs. During the switching transition [t_1, t_2] and [t_5, t_6] (see Fig. 2), the proposed CSD uses the pre-charge inductor current to drive the control MOSFET and absorbs the prarasitic inductance. This reduces the propagation impact of the parasitics during the switching transition, which leads to a reduction of the switching transition time and switching loss. At the same time, the discontinuous current does not increase the circulating loss compared to other continuous CSDs.

3) Gate energy recovery

The stored energy in the inductor is returned to the series capacitor C_s during [t_2, t_3] and is retuned to the drive voltage source during [t_6, t_7] (see Fig. 2). One benefit of the gate energy recovery capability is that high gate drive voltage can be used to further reduce $R_{DS(on)}$ conduction loss.

4) Wide range of duty cycle and switching frequency

In a high frequency buck converter, the duty cycle is required to response fast during a transient event. At the same time, in order to improve the efficiency in a wide load range, the switching frequency of a buck converter may need to vary according to the load condition. The proposed CSD operates correctly for duty cycles ranging from 0%-100%. The gate drive current (current-source inductor current) only depends on the pre-charge time and is independent of duty cycle and switching frequency, so it is suitable for different types of control and wide operating conditions.

5) High noise immunity

With the new CSD, the gate terminal of the power MOSFETs are clamped to either the drive voltage source via a low impedance path (S_1 fairly small $R_{DS(on)}$) or the source terminal via S_2. This offers high noise immunity and leads to the alleviation of dv/dt effect.

D. Proposed High Side CSD and Hybrid Gate Drive Scheme

Fig. 5 illustrates the proposed high side CSD for non-ground referenced power MOSFET. It uses a bootstrap circuit consisting of a diode D_f and a bootstrap capacitor C_f. This CSD can be used to the control MOSFET in a buck converter to achieve fast switching and reduced switching loss.

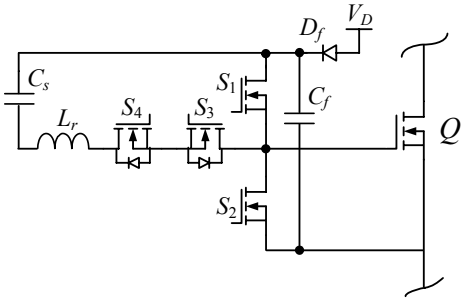


Fig. 5 Proposed high side CSD

Fig. 6 illustrates another version of the high side CSD using C_{s1} and C_{s2} in series as the bootstrap capacitor, where C_{s1} and C_{s2} also serve as the bootstrap capacitors.

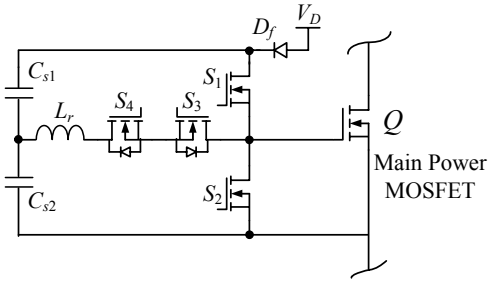


Fig. 6 Proposed high side CSD using series capacitors

Fig. 7 shows the loss breakdown of buck converter with the conventional voltage source driver. Carefully investigating the switching behavior of the MOSFETs in a synchronous buck converter, we can observe that the switching loss of the control MOSFET is dominant among the total loss breakdown as shown in Fig. 7.

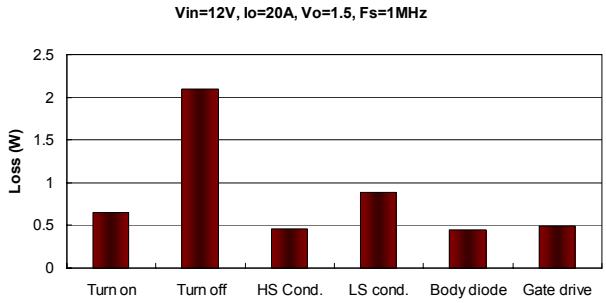


Fig. 7 Loss breakdown of the buck converter with the conventional voltage source driver (L_s=1nH, L_D=2nH, control MOSFET: Si7860DP and SR: Si7336ADP)

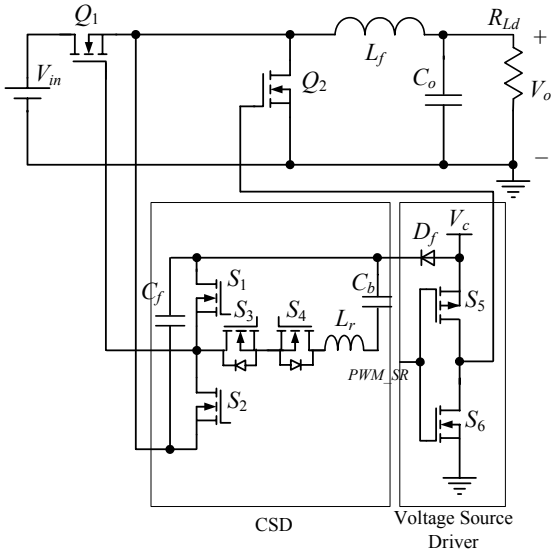


Fig. 8 Buck converter with proposed discontinuous CSD

For the control MOSFET, the common source inductance results in high switching loss, especially, turn-off loss, which makes the fast turn-off transition more desirable. However, on the other hand, for the SR, it almost has much lower switching loss since its output capacitor has been discharged to zero before it turns on, which can be regarded to achieve Zero-voltage-switching (ZVS). Moreover, due to the ZVS condition, no miller charge is present and the gate charge is saved by around 30%. Also, the common-source inductance could help to improve the *dv*/*dt* immunity of the SR MOSFET. So the conclusion is that control MOSFET and the SR MOSFET have different switching behavior as far as the parasitics are concerned.

Therefore, a new hybrid gate drive scheme is proposed for a buck converter as shown in Fig. 8. For the control MOSFET Q_1, the proposed high side CSD is used to achieve the switching loss reduction. For the SR Q_2, the conventional voltage source driver is used for low cost and simplicity. PWM_SR is the signal fed into the voltage source driver.

III. Loss Analysis and Design Procedure

Based on the principle of operation, the loss analysis is presented in this section. This provides design guideline for the proposed CSD.

A. Loss Analysis

1) Conduction Loss

Fig. 9 illustrates the power MOSFET gate voltage and gate drive current waveforms during the turn on interval. The current paths are also listed under the waveforms.

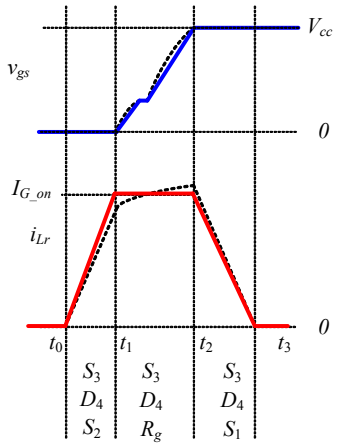


Fig. 9 Detailed inductor current and power MOSFET gate voltage waveforms during the turn on interval

Interval [t_0, t_1] [see Fig. 3 (a)]: The inductor current path is S_3-D_4-S_2.

The RMS current is

$$I_{RMS\_t10} = I_{G\_on} \cdot \sqrt{\frac{t_{10} \cdot f_s}{3}} \tag{6}$$

where I_{G_on} is the pre-charge turn on current from (3).

The average value is

$$I_{Aver\_t10} = \frac{I_{G\_on}}{2} \cdot t_{10} \cdot f_s \tag{7}$$

The total conduction loss is

$$P_{t10} = 2I^2_{RMS\_t10} \cdot R_{DS(on)} + I_{Aver\_t10} \cdot V_F \tag{8}$$

From (6), (7) and (8), P_{t10} becomes

$$P_{t10} = \frac{2}{3} I^2{}_{G\_on} t_{10} f_s R_{DS(on)} + \frac{1}{2} I_{G\_on} V_F t_{10} f_s \quad (9)$$

where $R_{DS(on)}$ is the on-resistance of S_1-S_4, assuming S_1-S_4 are same and V_F is the diode forward voltage.

Interval [t_1, t_2] [see Fig. 3 (b)]: the inductor current path is S_3-R_g-D_4 to charge gate capacitor C_{gs}

The RMS current is

$$I_{RMS\_t21} = I_{G\_on} \sqrt{t_{21} f_s} \quad (10)$$

The average value is

$$I_{Aver\_t21} = I_{G\_on} t_{21} f_s \quad (11)$$

The total conduction loss is

$$P_{t21} = I^2{}_{RMS\_t21} \cdot R_{DS(on)} + I^2{}_{RMS\_t21} \cdot R_g + I_{Aver\_t21} \cdot V_F \quad (12)$$

From (10), (11) and (12), (13) is obtained

$$P_{t21} = I^2{}_{RMS\_t21} \cdot R_{DS(on)} + I^2{}_{RMS\_t21} \cdot R_g + I_{Aver\_t21} \cdot V_F \quad (13)$$

where $R_{DS(on)}$ is the on- resistance of S_1-S_4, assuming S_1-S_4 are same, R_g is the gate mesh resistance and V_F is the diode forward voltage.

Interval [t_2, t_3] [see Fig. 3 (c)]: The inductor current path is S_3-D_4-S_1.

The RMS current is

$$I_{RMS\_t32} = I_{G\_on} \cdot \sqrt{\frac{t_{32} \cdot f_s}{3}} \quad (14)$$

The average value is

$$I_{Aver\_t32} = \frac{I_{G\_on}}{2} \cdot t_{32} \cdot f_s \quad (15)$$

The total conduction loss is

$$P_{t32} = 2I^2{}_{RMS\_t32} \cdot R_{DS(on)} + I_{Aver\_t32} \cdot V_F \quad (16)$$

From (14), (15) and (16), (17) is obtained

$$P_{t32} = \frac{2}{3} I_{G\_on}{}^2 t_{23} f_s R_{DS(on)} + \frac{1}{2} I_{G\_on} V_F t_{23} f_s \quad (17)$$

To simplify the analysis, it can be assumed that the turn on and turn off states of operation are identical. Therefore, under this assumption, the total conduction loss in the proposed CSD is two times the sum of P_{t10} plus P_{t21} plus P_{t32} as given by (18).

$$P_{cond} = P_{t10} + P_{t21} + P_{t32} \quad (18)$$

2) Current-Source Inductor Loss

The copper loss of the inductor winding is

$$P_{copper} = R_{ac} \cdot I^2{}_{Lr\_RMS} \quad (19)$$

where R_{ac} is the AC resistance of the inductor winding and I_{Lr_RMS} is the RMS value of the inductor current.

Core loss of the inductor should be also included. The core loss can be obtained by standard core loss estimation methods and should be small in comparison to the other loss components. If air core inductors are used, the core loss is zero.

3) Gate Drive Loss

The gate drive loss of S_1-S_4 is

$$P_{gate} = 4 \cdot Q_{g\_s} \cdot V_{gs\_s} \cdot f_s \quad (20)$$

where Q_{g_s} is the total gate charge of a drive switch and V_{gs_s} is the drive voltage, which is typically 5V.

B. *Design Example*

1) Optimal Design for Buck Converter

For the given application, in order to achieve fast switching speed, the gate drive current (pre-charge current) should be chosen by the designer properly. The design tradeoff is between switching speed, which translates into reduced switching loss, and gate drive loss. Higher gate charge current leads to lower switching loss, but results in greater conduction loss in the CSD. It is important to achieve the optimal design with proper gate drive current.

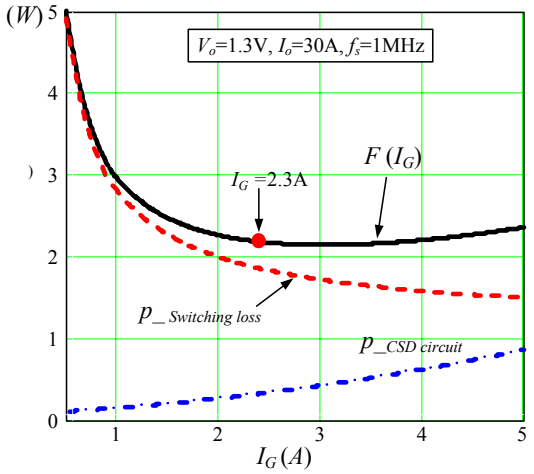


Fig. 10 Loss breakdown of the proposed CSD and total loss comparison with the conventional driver

The optimal design is applied to the buck converter with the hybrid drive scheme in Fig. 8. Using the switching loss model with the CSD and optimal method proposed in [18], Fig. 10 illustrates the switching loss $p\_{switching\ loss}$, the CSD circuit loss $p\_{\ CSD\ circuit}$ and the objective function $F(I_G)$ as function of the gate drive current I_G respectively. The specifications of the buck converter are: V_{in}=12V; V_o=1.3V; I_o=30A; V_c=5V; f_s=1MHz; control MOSFET Q_1: Si7386DP; Q_2: IRF6691 and L_f=330nH.

In Fig. 10, it is observed that $F(I_G)$ is a U-shaped curve, and therefore, the optimization solution can be found at the lowest point of the curve. In this case, the gate drive current I_G is chosen as 2.3A. It is noted that the bottom of the U-shape is flat. In other words, when I_G changes from 2A to 3A, the power loss does not change much.

Once the gate charge current is chosen, we could decide the pre-charge time. In order to minimize the delay in the control loop, the pre charge time t_{10} should be small. For 1MHz switching frequency, the pre-charge time t_{10} is

typically 15ns (2% of the switching period).

From (4), (21) is obtained to calculate the required inductor value

$$L_r = \frac{t_{10}}{2}\frac{V_D}{I_G} \tag{21}$$

For t_{10}=15ns, V_D=5V and I_G=2.3A, the inductor value can be chosen as 18nH.

Table I CSD design parameters

Circuit Parameters	
Switching Frequency, f_s	1MHz
Gate Drive Voltage, V_D	5V
MOSFET	**IRF6691 (Two paralleled)**
Total Gate Charge@V_{gs}=5V	58nC
Internal Gate Resistance, R_g	1Ω
Driver Switches S_1-S_2	**FDN335**
Diode Forward Voltage, V_F	0.7V
On Resistance $R_{DS(on)}$	70mΩ
Total Gate Charge@V_{gs}=5V:	3.5nC
Driver Inductor L_r	**1812SMS-22**
Inductor Value L_r	22nH
Driver Inductor Resistance	4.2mΩ

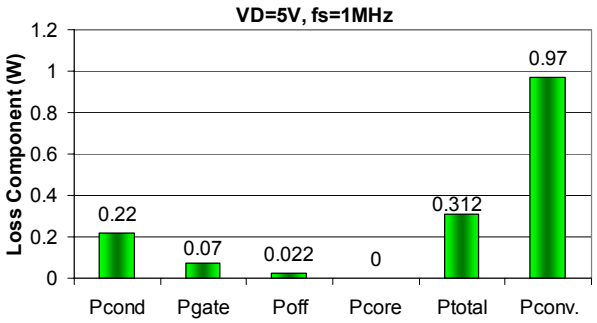


Fig. 11 Loss breakdown of the proposed CSD and total loss comparison with the conventional source driver

2) Gate Energy Recovery for SRs

The loss analysis of the CSD circuit in Section III is also used to verify the gate energy recovery of the CSD. Fig. 11 shows the loss breakdown of the proposed CSD with the parameters in Table I. It is noted that compared to the voltage source driver, the total gate drive loss is reduced by 67.8% with the proposed CSD.

IV. Experimental Results and Discussion

The specifications of the buck converter prototype are as follows: input voltage V_{in}=12V; output voltage V_o=1.0V-1.5V; output current I_o=30A; switching frequency f_s=1MHz; gate driver voltage V_c=5V. The PCB is six-layer with 4 oz copper. The components used in the circuit are listed as follows: Q_1: Si7386DP; Q_2: IRF6691; output filter inductance: L_f=330nH (IHLP-5050CE-01, Vishay); current source inductor: L_r=22nH (SMT 1812SMS-22N, Coilcraft); drive switches S_1-S_4: FDN335.

Fig. 12 shows the inductor current i_{Lr} and gate drive signals v_{GS_Q1} (control MOSFET). Its peak current value is 2.2A, which is the optimized value of the CSD drive current. The inductor current is discontinuous as expected. During the pre-charge time, the current ramps up linearly. After the pre-charge time, the inductor current continues to ramp up while charging the gate capacitance of the Si7386DP power MOSFET during the turn on interval. During this interval the average drive current is approximately 2A and the power MOSFET voltage charges from 0V to V_D=5V. After the power MOSFET turns on, the inductor current ramps back down to zero while the inductor energy is returned to drive voltage source.

Fig. 13 shows the gate drive signals v_{GS_Q1} (control MOSFET) and v_{GS_Q2} (SR). It is observed that v_{GS_Q1} is smooth since the miller charge is removed fast by the constant inductor drive current. Moreover, the total rise time and fall time of v_{GS_Q1} is less than 15ns, which means fast switching speed. The dead time between two drive voltages is fixed to avoid shoot-through and is minimized to reduce the SR body diode conduction loss.

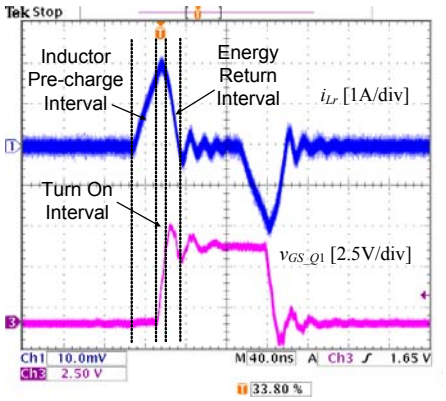


Fig. 12 Inductor current and the gate-to-source voltage at 1MHz

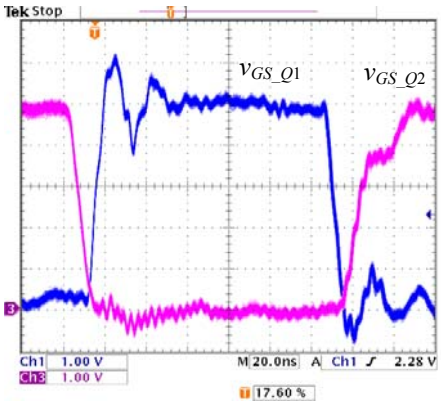


Fig. 13 Gate signals v_{GS_Q1} (control MOSFET) and v_{GS_Q2} (SR)

The Predictive Gate Drive UCC 27222 from Texas Instruments was used as the conventional voltage driver. Fig. 14 shows the measured efficiency comparison between the

hybrid gate driver and the conventional gate driver at 1.3 V output. It is observed that at 25A, the efficiency is improved from 80.7% to 85.7% (an improvement of 5%) and at 30A, the efficiency is improved from 77.9% to 84.4% (an improvement of 6.5%).

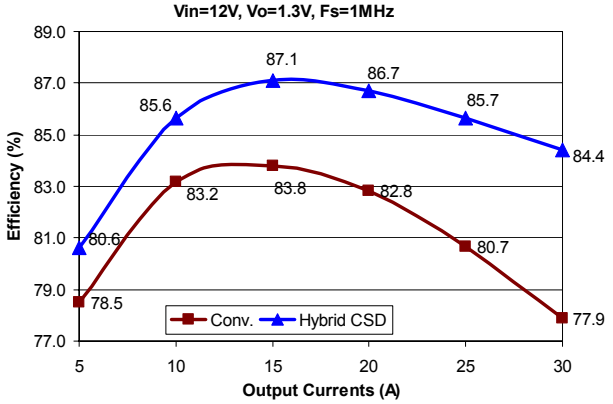


Fig. 14 Efficiency comparison: top: hybrid CSD; bottom: conventional voltage driver (Conv.)

Fig. 15 shows the measured efficiency for the CSD at different load currents and V_o=1.3V when the switching frequency changes. It is observed that at the load current of 30A, when the switching frequency changes from 1MHz to 500kHz, the efficiency is improved from 83.9% to 87% due to the reduction of frequency-dependent losses. The peak efficiency achieves 90.4% at 1.3V, 15A and 750kHz.

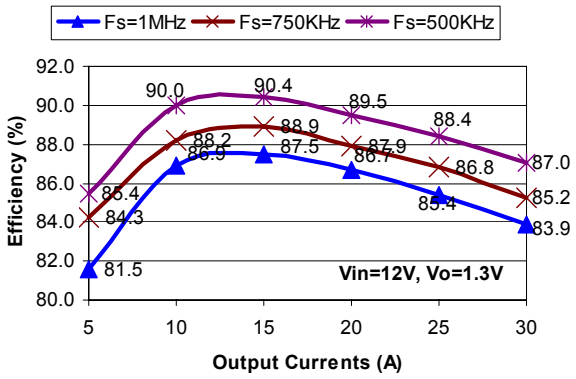


Fig. 15 Efficiency with different currents and switching frequencies

V. Conclusions

In this paper, a new discontinuous CSD is proposed. Compared to other CSDs proposed in previous work, the most important advantage of the new CSD is the small inductance (typically, 20nH at 1MHz switching frequency). This translates into a footprint reduction of as much as 90%. Other features of the proposed discontinuous CSD are: 1) fast switching speed and reduced switching loss; 2) discontinuous inductor current with low circulating loss; 3) wide range of duty cycle and switching frequency and 4) high noise immunity.

A hybrid gate drive scheme for a synchronous buck converter is also proposed to take advantage of the new CSD in a buck converter. The key idea of the hybrid gate driver scheme is to reduce the dominant switching loss with the CSD. The efficiency improvement was verified by the experimental results.

References

[1] W. A. Tabisz and F. C. Lee, "Zero-voltage-switching multiresonant technique- a novel approach to improve performance of high-frequency quasi-resonant converters," *IEEE Trans. Power Electron.*, Vol. 4, No. 4, Oct. 1989, pp. 450-458.

[2] D. Maksimovic and S. Cuk, "Constant-frequency control of qusi-resonant converters," *IEEE Trans. Power Electron.*, Vol. 6, No. 1, Jan. 1991, pp. 141-150.

[3] J. M. Rivas, R. S. Wahby, J. S. Shafran and D. J. Perreault, "New architectures for radio-frequency DC–DC power conversion," *IEEE Trans. Power Electron.*, Vol. 21, No. 2, pp.380-393, Mar. 2006.

[4] Y. Han, O. Leitermann, D.A. Jackson, J.M. Rivas and D.J. Perreault, "Resistance compression networks for radio-frequency power conversion," *IEEE Trans. Power Electron.*, Vol. 22, No. 1, pp.41-53, Mar. 2007.

[5] J. R. Warren, K. A. Rosowski and D. J. Perreault, "Transistor selection and design of a VHF DC-DC power converter," *IEEE Trans. Power Electron.*, Vol. 23, No. 1, pp.27 – 37, Jan. 2008.

[6] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE PESC*, 1991, pp. 527-532.

[7] H. L. N. Wiegman, "A resonant pulse gate drive for high frequency applications," in *Proc. IEEE APEC*, 1992, pp. 738-743.

[8] S. H. Weinberg, "A novel lossless resonant MOSFET driver," in *Proc. IEEE PESC*, 1992, pp. 1003-1010.

[9] L. Huber, K. Hsu, M. M. Jovanovic, D. J. Solley, G. Gurov and R. M. Porter, "1.8-MHz, 48-V resonant VRM: analysis, design, and performance evaluation," *IEEE Trans. Power Electron*., Vol. 21, No. 1, pp.79-88, Jan. 2006.

[10] P. Dwane, D. O' Sullivan and M. G. Egan, "An assessment of resonant gate drive techniques for use in modern low power dc-dc converters," in *Proc. IEEE Applied Power Electronics Conference (APEC)*, 2005, vol. 3, pp. 1572-1580.

[11] T. Lopez, G. Sauerlaender, T. Duerbaum and T. Tolle, "A detailed analysis of a resonant gate driver for PWM applications," in *Proc. IEEE APEC*, 2003, pp. 873-878.

[12] G. Spiazzi; P. Mattavelli and L. Rossetto, "Effects of parasitic components in high-frequency resonant drivers for synchronous rectification MOSFETs," *IEEE Trans. Power Electron.*, Vol. 23, No. 4, July 2008, pp. 2082–2092.

[13] Z. Yang, S. Ye, and Y. F. Liu, "New dual channel resonant gate drive circuit for low gate drive loss and low switching Loss", *IEEE Trans. Power Electron.*, Vol. 23, No. 3, May 2008, pp. 1574-1583.

[14] Z. Yang, S. Ye and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," *IEEE Trans. Power Electron.*, Vol. 22, No. 4, pp.1311-1320, July 2007.

[15] Z. Zhang, W. Eberle, Y. F. Liu and P. C. Sen, "A new current source gate driver for a buck voltage regulator," in *Proc. IEEE APEC*, 2008, pp. 1433-1439.

[16] W. Eberle, Z. Zhang, Y. F. Liu and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, Mar. 2008, pp. 678 -691.

[17] S. Pan and P. K. Jain, "A new pulse resonant MOSFET gate driver with efficient energy recovery," in *Proc. IEEE PESC*, 2006, pp. 1-5.

[18] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen "A high efficiency synchronous buck VRM with current source gate driver," in *Proc. IEEE PESC*, 2007, pp. 21-27.

[19] Z. Zhang, W. Eberle, Z. Yang, Y. F. Liu and P. C. Sen, "Optimal design of resonant gate driver for buck converter based on a new analytical loss model," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, Mar. 2008, pp. 653 -666.

[20] Datasheet of DS3316, http://www.coilcraft.com/pdfs/ds3316p.pdf

[21] Datasheet of 1812SMS, http://www.coilcraft.com/pdfs/midi.pdf