A Non-Isolated ZVS Self-Driven Current Tripler Topology for Low Voltage and High Current Applications

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***Abstract* -- A new non-isolated ZVS self-driven current tripler topology for high current and low voltage applications is proposed in this paper. The most important advantage of the proposed topology is reduced current stress and conduction losses of the synchronous rectifier (SR) MOSFETs and transformer windings, which is beneficial for high current applications. Other features of the proposed topology are: 1) duty-cycle extension; 2) ZVS of all the control MOSFETs; 3) reduced voltage stress over the SRs and reduced reverse recovery loss; 4) gate energy recovery of SRs and no external drive IC with the dead time control needed. A 12V input, 1.0V/50A output, 1MHz prototype was built to verify the advantages of the proposed converter.**

***Index Terms*— zero-voltage-switching (ZVS), high current and low voltage, full-bridge (FB), self-driven, synchronous rectifier (SR), voltage regulator module (VRM)**

I. INTRODUCTION

In high performance computer and communication power systems, the output voltage of the Voltage Regulator Modules (VRMs) keep reducing while output currents are increasing. As an example, for Dual-Core Intel Xeon Processor 7000/7100 series processor, Intel VRM/EVRD 11.0 is required to support a maximum continuous load current of 130A and a maximum load current of 150A peak [1]. This high demanding current causes a serious challenge to rectifier circuits. Furthermore, in order to meet the strict dynamic requirement and achieve high power density, switching frequency of VRMs has been increased to MHz range in recent years [2]-[5].

Among different high frequency DC-DC converters [6]-[9], presently multiphase buck converters are very popular for 12V VRMs in high current and low voltage applications due to the simplicity and low cost. However, the buck converter suffers from an extremely low duty cycle, which increases the switching losses and the reverse recovery losses of the body diode significantly. Moreover, the parasitic inductance increases the switching loss even higher [10]. Another important frequency dependent loss are the gate driver loss, especially synchronous rectifier (SR) MOSFETs with high total gate charge since more SRs are paralleled to reduce the conduction losses at high current applications. Resonant gate driver technique has very strong potential to achieve gate energy recovery [11]-[12]. However, external circuitry has to be required by this technique.

In order to extend the low duty cycle of the buck converter, several non-isolated topologies with the transformers were proposed for 12V input voltage applications such as the non-isolated half-bridge converter (NFB) [13]-[15], non-isolated full-bridge converter (NFB) [16] and ZVS phase shift buck (PSB) converter [17] etc. A non-isolated ZVS self-driven converter was proposed in [18]. The driving loss and synchronous rectifier body diode loss are both reduced by using self-driven technique for the SRs. Among these topologies, current doubler rectifier topology is used as a most efficient way to achieve low winding losses for low voltage and high current applications.

In order to reduce the current stress of the transformer windings with the current doubler rectifier, a new rectification topology for high current isolated converters was proposed in [19]. The advantage of this rectification topology is to use an additional inductor to share the load currents other than two inductors in the current doubler structure. However, the concern of the rectification topology is that the current stress of the SRs is not reduced, and consequently the high current conduction losses of SRs are not reduced. An isolated current tripler topology was proposed in [20]. This current tripler rectification topology reduces current stress of both transformer windings and SRs significantly. However, the above two rectification topologies are only suitable to isolated application such as 48V input, and additionally, the SR need additional drivers and high SR gate drive losses still exist at high frequency (>1MHz).

In this paper, a new self-driven ZVS current tripler topology for non-isolated applications is proposed. The most important advantage of the proposed converter is the reduced current stress and conduction losses of the SRs and transformer windings. It can also achieve: 1) duty cycle extension; 2) ZVS of all the control MOSFETs; 3) reduced reverse recovery loss and lower voltage rating SRs with lower $R_{DS(on)}$; 4) reduced body diode conduction and gate

energy recovery of the SRs. Existing multiphase buck controllers and buck drivers can be directly used in the proposed topology. Section II presents the proposed non-isolated rectifier converter and its principle of operation. Section III presents the analysis of duty cycle loss, ZVS condition and loss analysis. Section IV demonstrates the advantages of the proposed converter. Section V contains the experimental results and discussion. Section VI provides a conclusion.

II. Proposed Non-Isolated ZVS Self-Driven Current Tripler Topology and Principle of Operation

A. Proposed Non-Isolated ZVS Self-Driven Current Tripler Topology

Fig. 1 illustrates the proposed non-isolated ZVS self-driven current tripler converter. In Fig. 1, V_{in} is the input voltage source, Q_1-Q_6 are the control MOSFETs, S_1-S_3 are the SR MOSFETs, L_1, L_2 and L_3 are the output filter inductors and C_o is the output filter capacitor. In this configuration, three transformers T_1, T_2 and T_3 (turn ratio n) are organized with a delta (△) connection. The midpoints (a, b, c) of each bridge leg are connected to the gate terminals of S_1-S_3 to drive the SRs respectively.

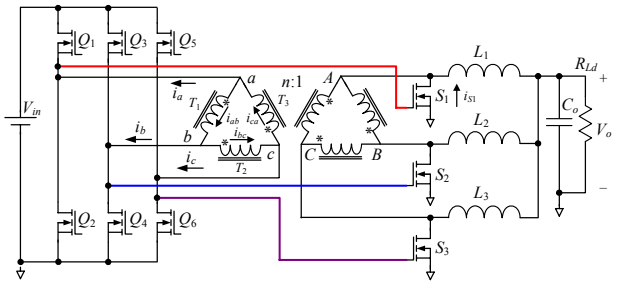


Fig. 1 Proposed non-isolated ZVS self-driven FB converters with current tripler rectifier topology

Fig. 2 illustrates the key waveforms. As shown in Fig. 2, the control MOSFETs in each leg are with complimentarily control. Q_2, Q_4 and Q_6 in each leg are with interleaving control of 120 degrees phase shifting. Therefore, the voltages applied to the primary-sides of each transformer are phase shifted with 120 degrees. In turn, the magnetic field in each core is also 120 degrees phase shifted, which allows for a magnetic flux cancellation effect. So the three transformers can be integrated into one magnetic core similar to an AC three-phase transformer. The connection points (A, B and C see Fig. 1) of the secondary sides of the transformers are applied to the output inductors to form a multiphase rectification structure. Compared to current doubler rectifier, the freewheeling load currents are shared by two SRs rather than one SR. Therefore, the RMS currents of the SRs and transformer windings are significantly reduced. This leads to a significant reduction of the conduction losses of the SRs and transformer windings. This is beneficial since the high conduction losses are the dominant losses in low voltage and high current applications.

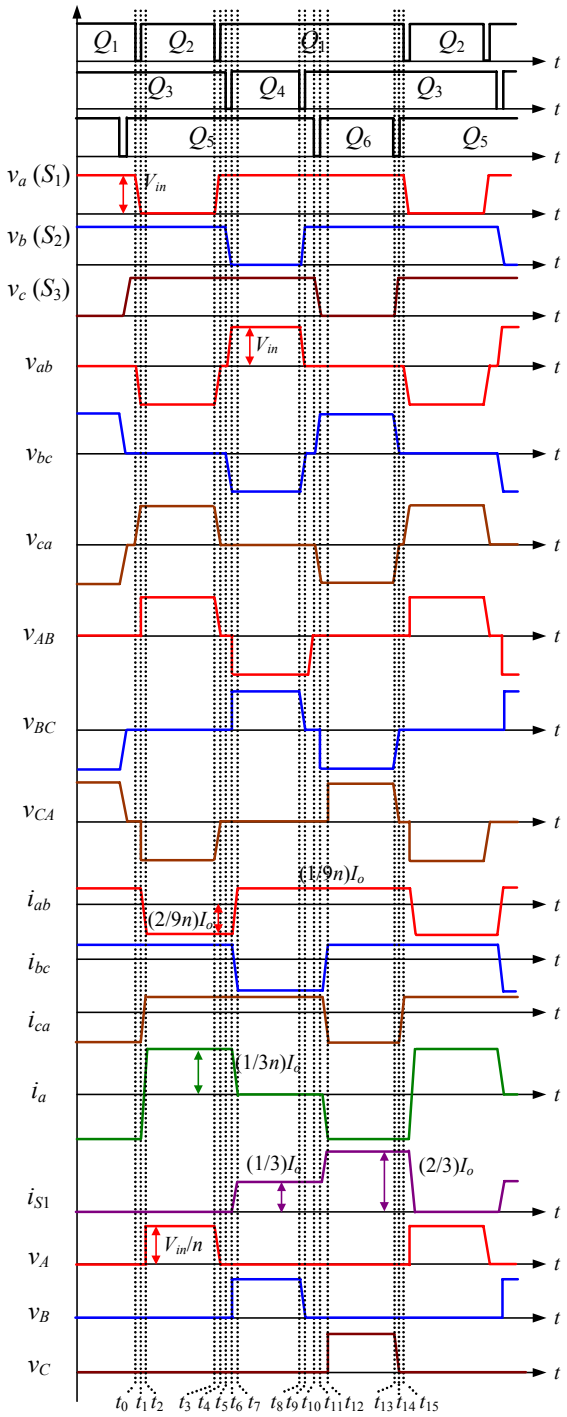


Fig. 2 Key waveforms of proposed non-isolated current tripler converter

B. Principle of Operation

There are fifteen switching modes in one switching period. Accordingly, the equivalent circuits in one third of one switching cycle are shown in Fig. 3. D_1-D_6 are the body

diodes and C_1-C_6 are the intrinsic output capacitors of Q_1-Q_6 respectively, assuming C_1=C_2=C_3=C_4=C_5=C_6=C_{oss}. D_{s1}-D_{S3} are the body diodes and C_{gs_S1}-C_{gs_S3} are the input capacitors of SR S_1-S_3 respectively, assuming C_{gs_S1}=C_{gs_S2}=C_{gs_S3}=C_{gs}. The output inductors are large enough to be regarded as current sources. The inductor currents i_{L1}=i_{L2}= i_{L3}=I_o/3, where I_o is the total output current.

1) Mode 1 [t_0, t_1] [Fig. 3 (a)]: Prior to t_0, Q_1, Q_3 and Q_5 are on, the voltages over the primary sides and the secondary sides of the transformers T_1, T_2 and T_3 are all zero, v_{ab}=v_{bc}=v_{ca}=0. The gate drive voltages of the SR S_1, S_2 and S_3 are all clamped high to the input voltage V_{in}. At t_0, Q_1 turns off, the primary current i_a charges C_1 and discharges C_2 and C_{gs_S1} at the same time. As C_1, C_2 and C_{gs_S1} limit the rising slew rate of the voltage of C_1, Q_1 is under zero-voltage turn-off condition.

During this stage, the energy to discharge C_2 and C_{gs_S1} is provided by the leakage inductance of the transformer. i_a decreases resonantly as

$$i_a(t) = \frac{I_o}{3n} \cdot \cos \omega_r (t - t_0) \tag{1}$$

$$v_{c2} = v_{gs\_S1} = V_{in} - Z_r \cdot \frac{I_o}{3n} \cdot \sin \omega_r (t - t_0) \tag{2}$$

where $\omega_r = 1/\sqrt{L_k(2C_{oss} + C_{gs})}$ and $Z_r = \sqrt{L_k/(2C_{oss} + C_{gs})}$.

2) Mode 2 [t_1, t_2] [Fig. 3 (b)]:

At t_1, v_{C1}=V_{in} and v_{C2}=0, D_2 conducts, which provides zero-voltage turn-on condition for Q_2. It should be noted that due to ZVS, C_{gs_S1} is discharged with i_a, which means the gate drive energy of the SR is returned to the input voltage source so that the high gate drive losses of SRs can be reduced significantly.

The interval of [t_0, t_1] and the value of i_a at t_1 are

$$t_{1,0} = \frac{1}{\omega_r} \cdot \sin^{-1}\left(\frac{3nV_{in}}{Z_r \cdot I_o}\right) \tag{3}$$

$$I_a(t_1) = \frac{I_o}{3n} \cdot \sqrt{1 - \left(\frac{3nV_{in}}{Z_r \cdot I_o}\right)^2} \tag{4}$$

During this stage, i_a decreases and is not enough to power the load. i_{L1} freewheels through the body diode D_{s1} of S_1. i_{L2} freewheels through S_2 and i_{L3} freewheels through S_3 respectively. Then i_a increases inversely but is still not large enough to power the load.

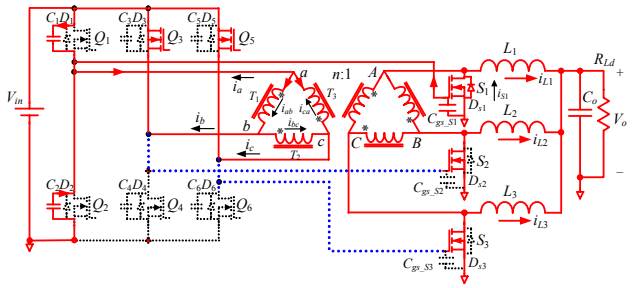
3) Mode 3 [t_2, t_3] [Fig. 3 (c)]: At t_2, i_a rises to the reflected load current causing D_{S1} to turn off. During this stage, the voltage over the transformer is the input voltage, v_{ab}=-V_{in}, v_{ca}=V_{in}. The energy transfers from the primary side of the transformer to the load. The voltage over the primary side of T_2 is zero, v_{bc}=0. i_{L2} freewheels through S_2 and i_{L3} freewheels through S_3 respectively.

4) Mode 4 [t_3, t_4] [Fig. 3 (d)]: At t_3, Q_2 turns off, the primary current i_a charges C_2 and C_{gs_S1} and discharges C_1. As C_1 and C_2 and C_{gs_S1} limit the rising slew rate of the voltage of C_2, Q_2 is under zero-voltage turn-off condition. During this stage, the energy to discharge C_1 is provided by the leakage inductance and L_1. L_1 is large enough to be regarded as a constant current source so that the primary current i_p keeps the value I_{a2}=I_{L1}/n, where I_{L1} is the dc current of L_1. The voltage C_2 rises linearly and the voltage of C_2 decays linearly.

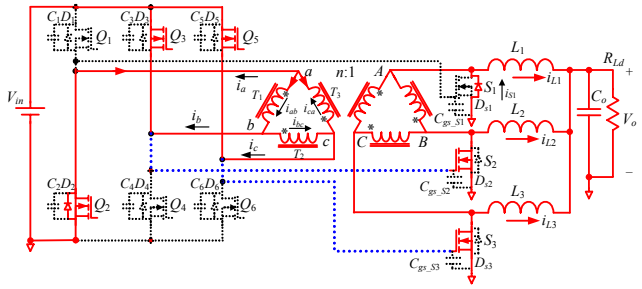
The interval of [t_3, t_4] is

$$t_{4,3} = \frac{3nV_{in}(2C_{oss} + C_{gs})}{I_o} \tag{5}$$

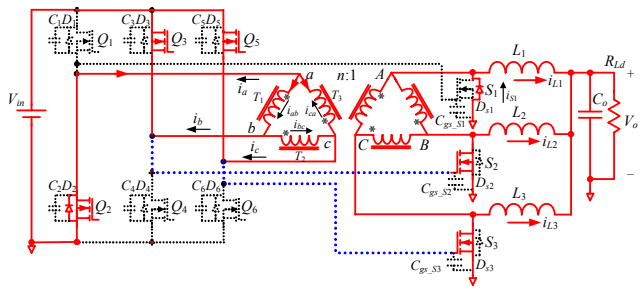
5) Mode 5 [t_4, t_5] [Fig. 3 (e)]: At t_4, D_1 conducts, which provides zero-voltage turn-on condition for Q_1. The voltages over the primary sides of T_1, T_2 and T_3 are zero, v_{ab}=v_{bc}=v_{ca}=0. The gate drive voltages of the SR S_1, S_2 and S_3 are all clamped high to the input voltage again. i_{L1}, i_{L2} and i_{L3} freewheel through S_1, S_2 and S_3 respectively. At t_5, Q_3 turns off and the other two third of the switching cycle starts. The principle of operation is similar to Mode 1-Mode 5 except for polarity changes.



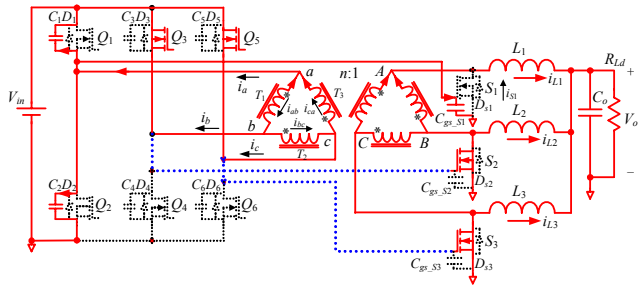
(a) [t_0, t_1]



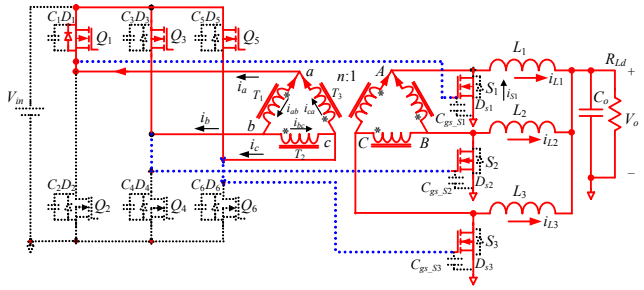
(b) [t_1, t_2]



(c) [t_2, t_3]



(d) [t_3, t_4]



(e) [t_4, t_5]

Fig. 3 Equivalent circuits of operation

III. Duty Cycle Loss, ZVS Condition and Loss Analysis

A. Duty Cycle Loss

As shown in Fig. 2, during [t_1, t_2] and [t_6, t_7], the leakage inductance of the transformer limits the rise (or decay) slope of i_a. Transition time is required for i_a to travel from the positive direction to the negative direction (or vice versa). During this transition time, the primary voltage of the transformer v_{AB} is $+V_{in}$ or $-V_{in}$, i_p is lower than the reflected load current and all the SR diodes conduct. This makes the secondary rectified voltage v_A and v_B zero, thus v_{AB} loses the voltage in [t_1, t_2] and [t_6, t_7] respectively.

The duty cycle loss D_{loss} during [t_1, t_2] and [t_6, t_7] is

$$D_{loss} = \frac{2I_o}{3n \cdot T_s} \cdot \frac{L_k}{V_{in}} \tag{6}$$

where I_o is the output current, L_k is the leakage inductance and n is the transformer turns ratio. It is noted that the leakage inductance of the transformer should be minimized to reduce the duty cycle loss.

B. Condition of ZVS

From Fig. 3 (d), for the upper control MOSFETs (Q_1, Q_3 and Q_5), the energy to achieve ZVS is provided by the output inductors, so (7) should be satisfied

$$\frac{1}{2} \cdot L_f \cdot (\frac{I_o}{3 \cdot n})^2 \geq \frac{1}{2} \cdot C_1 \cdot {V_{in}}^2 + \frac{1}{2} \cdot (C_2 + C_{gs\_S1}) \cdot {V_{in}}^2 = C_{oss} \cdot {V_{in}}^2 + \frac{1}{2} \cdot C_{gs\_S1} \cdot {V_{in}}^2 \tag{7}$$

where L_f is the output filter inductance, C_1=C_2=C_{oss} (output capacitances of Q_1 and Q_2) and C_{gs_S1} is the gate capacitance of S_1. Since L_f is usually large enough to provide the energy, Q_1 and Q_3 can achieve ZVS in a wide load range.

From Fig. 3 (a), for the lower control MOSFETs (Q_2, Q_4 and Q_6), the energy to realize ZVS is provided by the leakage inductance of the transformer, so (8) should be satisfied

$$\frac{1}{2} \cdot L_k \cdot (\frac{I_o}{3 \cdot n})^2 \geq \frac{1}{2} \cdot C_1 \cdot {V_{in}}^2 + \frac{1}{2} \cdot (C_2 + C_{gs\_S1}) \cdot {V_{in}}^2 = C_{oss} \cdot {V_{in}}^2 + \frac{1}{2} \cdot C_{gs\_S1} \cdot {V_{in}}^2 \tag{8}$$

where L_k is the leakage inductance of the transformer. It is noted that the larger leakage inductance, the easier to achieve ZVS. We can take advantage of the energy of the leakage inductance of the transformer, which is very similar to the ZVS condition of the lagging leg of the traditional full-bridge converter [21].

However, the larger leakage inductance results in higher duty cycle loss. The leakage inductance L_k can be chosen based on (8) depending on ZVS range.

$$L_k \geq \frac{2C_{oss} \cdot {V_{in}}^2 + C_{gs\_Q5} \cdot {V_{in}}^2}{(\frac{I_{o\_ZVS}}{3n})^2} \tag{9}$$

As an example, for V_{in}=12V, V_o=1.3V, n=3, C_{oss}= 0.65nF and C_{gs_Q5}=6.6nF, in order to achieve ZVS at I_{o_ZVS}=40A, from (9), the leakage inductance can be calculated as 50nH.

C. Loss Analysis

SR conduction loss comparison and transformer loss comparison

From the waveform of i_{S1} in Fig. 2, the RMS current of SR S_1 with current tripler is

$$I_{S1\_RMS} = \sqrt{\frac{1}{3} \cdot \left(\frac{I_o}{3}\right)^2 + \frac{1}{3} \cdot \left(\frac{2I_o}{3}\right)^2} = \frac{\sqrt{15}}{9} I_o \approx 0.43 I_o \tag{10}$$

The RMS current of SR MOSFET S_1 of the current doubler is

$$I_{S1\_RMS} = \sqrt{\frac{1}{2}} \cdot I_o \approx 0.71 I_o \tag{11}$$

For example, V_{in}=12V, V_o=1.0V and total load current 120A, in order to do the fair comparison, each phase is assumed to proved 20A. So we can use three ZVS self-driven FB VR converters to parallel and each of them provides

I_o=40A. If the three-phase non-isolated ZVS self-driven FB converter with current tripler in Fig. 1 are used, we need two converters to parallel and each of them provides I_o=60A. According to (10) and (11), Fig. 4 shows the SR RMS current comparison between the conventional current doubler and the proposed self-driven converter. It can be seen that at the load current of 60A, the RMS current of each SR is reduced from 28.4A to 25.8A.

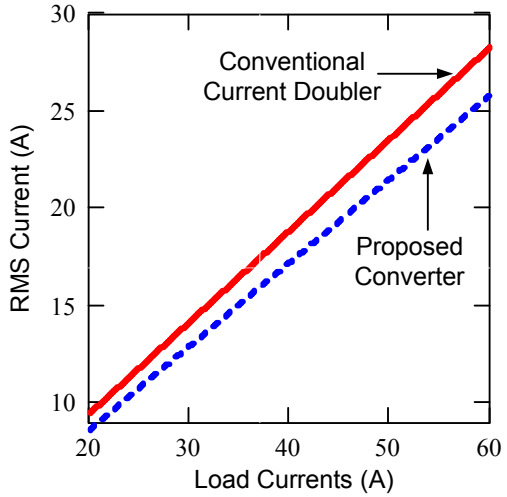


Fig. 4 RMS current comparison of SRs: conventional current doubler vs. proposed converter

Assuming $R_{DS(on)}$ of each SR is 1.6mΩ and 6 SRs are used, Fig. 5 illustrates the total conduction loss comparison of the SRs. It is noted that at 60A, the RMS current reduction translates into the SR conduction loss reduction of 1.3W (7.7W-6.4W), which is a reduction of 17% (1.3W/7.7W) of the total SR conduction loss. This is 1.1% of the output power, 1.3W/(1.0V×120A).

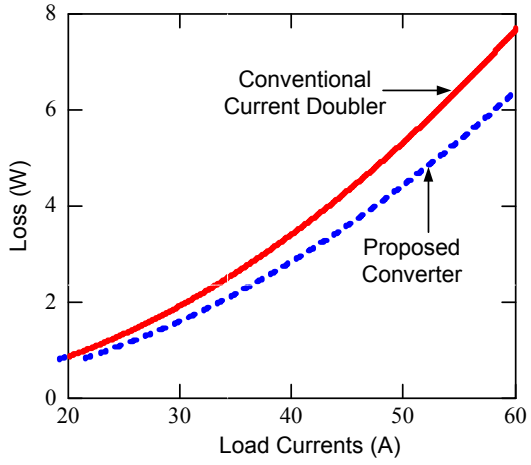


Fig. 5 Conduction loss comparison of SRs: conventional current doubler vs. proposed converter

From the waveform of i_{ab} in Fig. 2, the current RMS value of the primary windings with current tripler is

$$I_{Sec\_RMS} = \frac{1}{n}\cdot\sqrt{\frac{1}{3}\cdot\left(\frac{2I_o}{9}\right)^2+\frac{2}{3}\cdot\left(\frac{I_o}{9}\right)^2} = \frac{\sqrt{2}}{9n}I_o \approx 0.16\frac{I_o}{n} \quad (12)$$

The current RMS value of the primary windings with the current doubler is

$$I_{Sec\_RMS} = \frac{1}{n}\cdot\frac{I_o}{2} = 0.5\frac{I_o}{n} \quad (13)$$

According to (12) and (13), Fig. 6 shows the RMS current comparison of the transformer primary windings between the conventional current doubler and the proposed self-driven converter. It is seen that at 60A, the RMS current value is reduced from 6.7A to 3.1A with the proposed converter. Assuming the same primary winding AC resistance R_{ac_pri}, the winding loss of the current tripler is $P_{pri\_tripler}$=3.1^2×6R_{ac_pri} since there are 6 secondary windings, while the winding loss of the current doubler is $P_{pri\_doubler}$=6.7^2×3R_{ac_pri} since there are 3 secondary windings. Therefore, the total secondary winding loss reduction is 57.2% (1-$P_{pri\_tripler\ c}$/$P_{pri\_doubler}$).

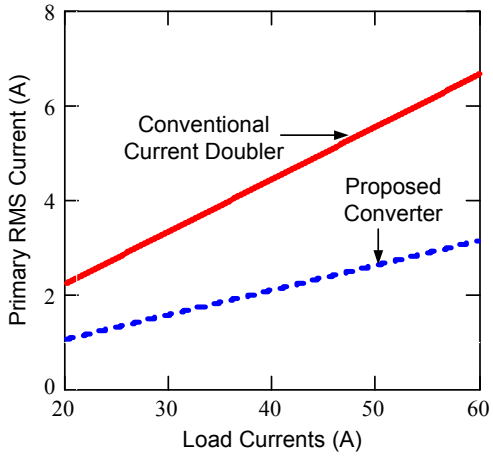


Fig. 6 RMS current comparison of primary windings: conventional current doubler vs. proposed converter

Similarly, the RMS value of the secondary winding current with current tripler is

$$I_{Sec\_RMS} = \sqrt{\frac{1}{3}\cdot\left(\frac{2I_o}{9}\right)^2+\frac{2}{3}\cdot\left(\frac{I_o}{9}\right)^2} = \frac{\sqrt{2}}{9}I_o \approx 0.16I_o \quad (14)$$

The RMS value of the secondary winding current with the current doubler is

$$I_{Sec\_RMS} = \frac{I_o}{2} = 0.5I_o \quad (15)$$

According to (14) and (15), Fig. 7 shows the RMS current comparison of the transformer secondary windings between the conventional current doubler and the proposed self-driven

converter. It is can be seen that at 60A, for the high current secondary winding loss, the RMS current is reduced from 20A to 9.6A with the proposed topology. Assuming the same secondary winding AC resistance R_{ac_sec}, the winding loss of the current tripler is $P_{sec\_tripler}=9.6^2\times6R_{ac\_sec}$ since there are 6 secondary windings, while the winding loss of the current doubler is $P_{sec\_doubler}=20^2\times3R_{ac\_sec}$ since there are 3 secondary windings. Therefore, the total secondary winding loss reduction is 53.9% ($1-P_{sec\_tripler\ c}/P_{sec\_doubler}$).

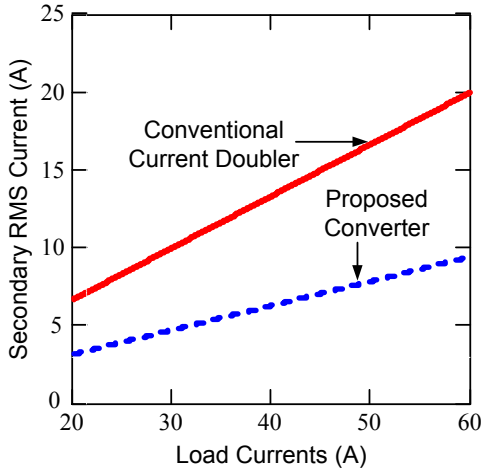


Fig. 7 RMS current comparison of secondary windings: conventional current doubler vs. proposed converter

IV. Advantages of Proposed Topology

The advantages of the proposed converter are highlighted as follows:

(1) Extension of Duty Cycle

According to the voltage gain of $V_o=(V_{in}/n)D$, in order to achieve V_{in}=12V and V_o=1.0V, with n=3, the required duty cycle is D=0.25. However, for the same output voltage and input voltage, the duty cycle of a buck converter is only 0.08. Therefore, the duty-cycle is extended by 3 times.

(2) ZVS of the Control MOSFETs

With the control strategy proposed, all the control MOSFETs can achieve ZVS and this will reduce the switching losses significantly at high frequency (>1MHz).

(3) Gate Energy Recovery of SR MOSFETs and Reduced Body Diode Conduction

One of the most important advantages of the proposed topology is the self-driven capability for the SRs and no external drive ICs are needed any more. Also, with the self-driven control, the dead time is minimized inherently to reduce the body diode conduction loss significantly. More importantly, the self-driven circuit actually forms a current-source driver by using the leakage inductance of the transformer to ensure the fast turn-on and turn-off transition of the SRs and recover gate energy at the same time, which is very critical at switching frequency of MHz. And it also provides high gate drive voltage (input voltage, usually 12V) for SR MOSFETs with lower $R_{DS(on)}$ to reduce the conduction losses further.

(4) Reduced Conduction Loss of SRs and Body Diode Reverse Recovery Loss

The most important advantage of this proposed topology is that the RMS currents of the SRs and transformer windings are significantly reduced compared to non-isolated converters with current doubler rectifier. Compared to the current doubler rectifier, the freewheeling load currents are shared by two SRs rather than one SR, which reduces the current RMS value significantly. According to the loss analysis in Section III, the proposed topology achieve the SR conduction loss reduction of 17%, the primary winding conduction loss reduction of 57.2% and the secondary winding conduction loss reduction of 53.9%

V. Experimental Results and Discussion

A 1MHz prototype was built to verify the operation principle of the proposed converter. The specifications are as follows: input voltage V_{in}=12V; output voltage V_o=1.0V and output current up to I_o=60A. The PCB uses six-layer 2 oz copper. The components used are listed as follows: Q_1: Si7860DP; Q_2: Si7336ADP; output filter inductance: $L_1=L_2=L_3$=190nH, control MOSFETs driver: Intersil 6208 (buck driver). One custom designed EE core is used as the integrate transformer. Fig. 8 illustrates the photo of the prototype.

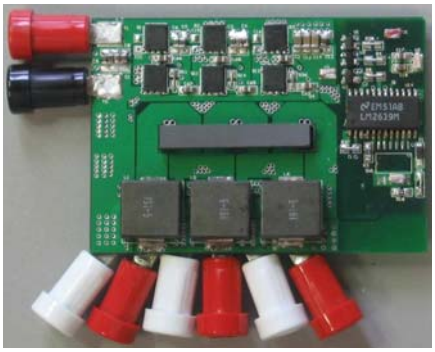


Fig. 8 Photo of prototype

Fig. 9 shows the gate signal v_{GS} and drain-to-source voltage v_{DS} of the control MOSFET Q_2, which indicates that ZVS has been achieved. This also means the gate drive energy of SR S_1 has been recovered to the input voltage source V_{in} since the gate drive voltage v_a (i. e. drain voltage of Q_2) is fully discharged to zero.

Fig. 10 and Fig. 11 illustrate the primary-side voltages, v_{ab}, v_{bc}, v_{cb}, and secondary-side voltages, v_{AB}, v_{BC}, v_{CB} of the transforms respectively. All waveforms agree with the theory in Fig. 2. Most notably, the phase voltages are 120 degrees phase-shifted, which means the magnetic flux cancellation is achieved.

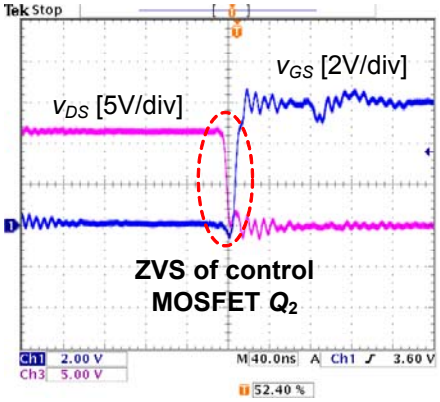


Fig. 9 v_{DS} and v_{GS} of Q_2 @ I_o=50A

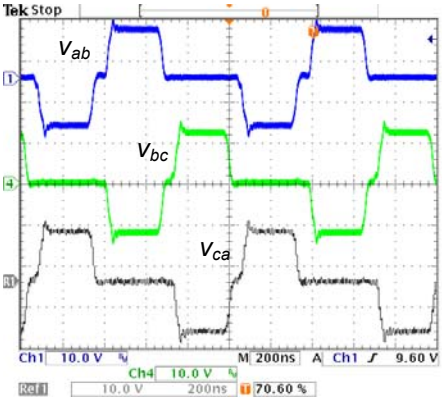


Fig. 10 Primary-side voltages of the transformer at I_o=50A

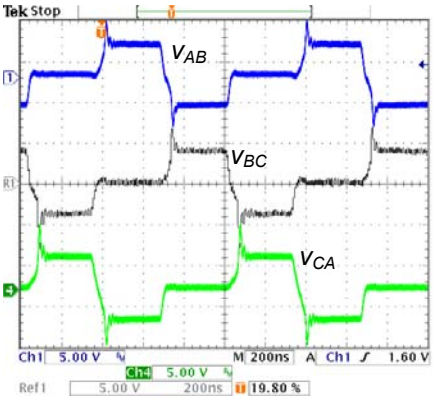


Fig. 11 Secondary-side voltages of transformer at I_o=50A

Fig. 12 illustrates the gate signal v_{GS} and drain-to-source voltage v_{DS} of the SR MOSFET S_1. It is noted that the gate drive voltage is 12V, which means the $R_{DS(on)}$ of SRs is only 1.6 mΩ (IRF 6691) compared to 2.2 mΩ with 5V gate drive voltage (a reduction of 20%). Moreover, there is no body diode conduction time for the turn-on transition of the SRs since the gate voltage has been applied before v_{DS} reaches zero. It is noted that the peak voltage of v_{DS} is less than 10V, which also means a significant reduction of reverse recovery losses. It should also be noted that the future low voltage rating MOSFETs can be used to reduce the $R_{DS(on)}$ loss further.

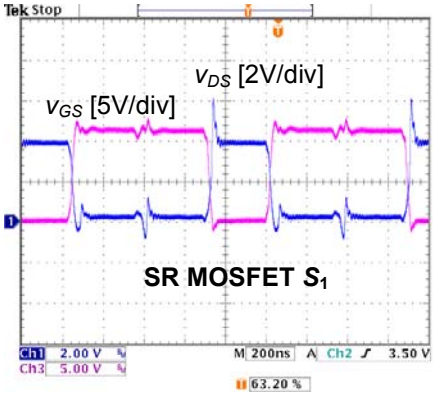


Fig. 12 Gate drive signal and v_{DS} of SR S_1 at I_o=50A

Fig. 13 illustrates the rectified voltages across the output filters, which are 120 degrees phase-shifted so that rippler cancellation can be achieved.

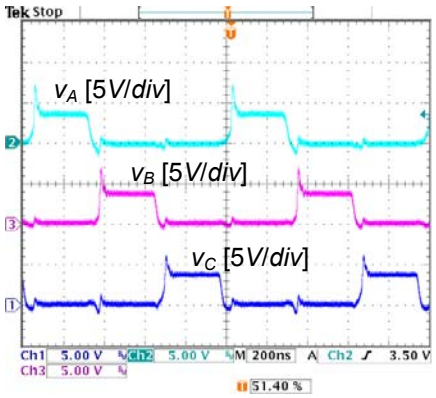


Fig. 13 Rectified voltages at I_o=50A

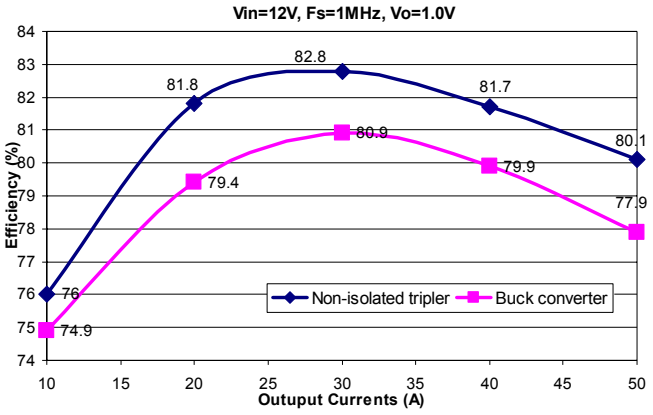


Fig. 14 Efficiency comparison with different load currents

Fig. 14 gives the measured efficiency comparison between the proposed topology and the conventional buck converter at 1.0V output. It is observed that at 40A, the efficiency is improved from 79.9% to 81.7% (an improvement of 1.8%) and at 50A, the efficiency is improved from 77.9% to 80.1% (an improvement of 2.2%). The efficiency improvement is due to the reduction of the frequency dependent losses.

VI. CONCLUSION

A new non-isolated ZVS current tripler topology for high current and low voltage applications is proposed in this paper. The most important advantage of the proposed topology is reduced current stress and conduction losses of the SRs and transformer windings, which is beneficial for high current applications. Other features of the new topology are: 1) duty-cycle extension; 2) ZVS of all the control MOSFETs; 3) reduced voltage stress over the SRs and reduced reverse recovery loss; 4) gate energy recovery of SRs MOSFET and no external drive IC with the dead time control needed. A 12V input, 1.0V/50A output, 1MHz prototype was built to verify the functionality of the proposed topology.

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