A Nonisolated ZVS Asymmetrical Buck Voltage Regulator Module With Direct Energy Transfer

Zhiliang Zhang, *Member, IEEE*, Wilson Eberle, *Member, IEEE*,
Yan-Fei Liu, *Senior Member, IEEE*, and Paresh C. Sen, *Fellow, IEEE*

***Abstract*—This paper presents a new nonisolated asymmetrical buck voltage regulator module. A transformer is used to extend the extremely low duty cycle of a conventional buck converter. Turn-off losses can be significantly reduced due to the extension of duty cycle, and there are no turn-on losses owing to the zero-voltage turn-on condition. At the same time, the voltage stress over the synchronous rectifier MOSFETs is also reduced. Therefore, the reverse-recovery losses of the body diode can be reduced. Furthermore, the MOSFETs with lower voltage rating and lower $R_{\mathrm{DS(on)}}$ can be used to reduce the conduction losses. In order to reduce the turn-off losses above the switching frequency of 1 MHz further, a new current-source driver is also proposed, which is suitable to this new topology. A 12-V input prototype with the switching frequency of 1 MHz was implemented. Simulation and experimental results verify the functionality and benefits of the proposed topology.**

***Index Terms*—Buck converter, current-source driver (CSD), synchronous rectifier (SR), voltage regulator module (VRM), zero-voltage switching (ZVS).**

I. Introduction

With FAST development of microprocessor technology, the output voltage of a voltage regulator module (VRM) keeps reducing, while the output current is increasing further due to the high power consumption of the processors. In order to meet the strict transient requirements [1] and achieve high power density on the mother board, the switching frequency of a VRM has moved into the megahertz (MHz) range recently [2]–[5].

Among different high-frequency dc–dc converters [6]–[9], presently multiphased buck converters are very popular for 12-V VRMs in high-current and low-voltage application due to their simplicity and low cost. However, the buck converter suffers from an extremely low duty cycle, which increases the switching losses and the reverse-recovery losses of the body diode significantly. More importantly, it has been noticed that the parasitic inductance, particularly the common source inductance, has a serious propagation effect during the switching transition and thus leads the switching losses to increase even higher [10]. Furthermore, the excessive gate driver losses also come to a penalty at switching frequency of several megaHertz, particularly for the synchronous rectifier (SR) MOSFETs with high total gate charge. Resonant gate driver technique has very strong potential to achieve gate energy recovery. Self-oscillating resonant gate drive with a resonant network was used in radio-frequency power amplifiers (>30 MHz) [11], [12]. The self-oscillating resonant gate driver (soft gating driver) is also applied to a high-frequency (>30-MHz) dc–dc converter to achieve high gate loss recovery in [13]. The resonant drivers using a coupled inductor [14] and using a transformer [15] are able to drive two MOSFETs. A full-bridge (FB) topology drive circuit with one inductor is proposed to drive two ground-sharing MOSFETs in a 1-MHz boost converter in [16]. Although current-source drivers (CSDs) proposed in [17]–[19] can improve the efficiency of a buck converter, the main power MOSFET still operates under hard-switching condition. Therefore, soft-switching converters would be preferred to reduce the switching losses further for high-current and high-frequency (>1-MHz) application.

In order to extend the extremely low duty cycle, a tapped inductor (TI) buck converter is proposed in [20], and the efficiency is improved greatly over the buck converter. The introduction of a transformer can provide the capability of soft switching; however, the control MOSFET in the TI buck converter is still under hard-switching condition. In other words, the TI buck converter does not take the full advantage of the introduced transformer, and at the same time, the nonideal coupling of the transformer may also result in high voltage stress over the main MOSFETs and increases the switching loss. A nonisolated half-bridge (NHB) converter with extended duty cycle is proposed in [21]–[23]. In order to design planar transformers used in the aforementioned converters properly, the loss estimation method proposed in [24] can be applied. In [25], quasi-square-wave (QSW) buck converters are proposed using the multiphase interleaving technique to achieve zero-voltage switching (ZVS). Nevertheless, the concern of the QSW converter is that high inductor current ripples result in a high rms value and high conduction losses and also increase the output voltage ripples. A family of buck-type dc–dc converters taking advantages of the autotransformers is proposed in [26]. The advantage of the autotransformer is to reduce the current stress and thus the conduction losses. However, these topologies cannot achieve the feature of direct energy transfer compared

Manuscript received July 24, 2008; revised May 5, 2009. First published May 19, 2009; current version published July 24, 2009.

Z. Zhang was with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada. He is now with the Aero-Power Sci-tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: zlzhang@nuaa.edu.cn).

W. Eberle is with the School of Engineering, University of British Columbia—Okanagan, Kelowna, BC V1V 1V7, Canada (e-mail: wilson.eberle@ubc.ca).

Y.-F. Liu and P. C. Sen are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: yanfei.liu@queensu.ca; senp@post.queensu.ca).

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Digital Object Identifier 10.1109/TIE.2009.2023102

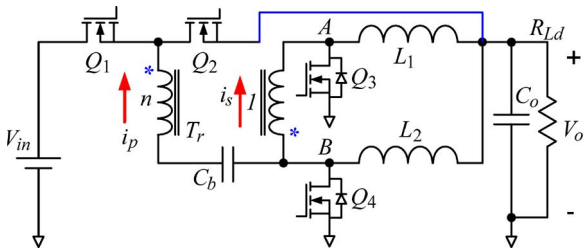

Fig. 1. Proposed asymmetrical buck converter with direct energy transfer.

to the NHB converter in [22]. In addition, for the forward push–pull half-bridge topologies with autotransformers, although the duty cycle is extended, the power MOSFETs do not feature soft-switching condition, which results in high switching losses at high frequency (>1 MHz). Twelve-volt nonisolated FB topologies featuring ZVS and reduced SR conduction losses are proposed in [27] and [28]. Furthermore, an improved self-driven 12-V VRM topology is proposed based on a phase-shift buck converter to recover the gate drive losses of the SRs [29], [30]. However, these nonisolated FB topologies need four control switches, which results in complex control and high cost. In this paper, a new nonisolated asymmetrical buck converter is proposed for 12-V VRM applications in Section II. Section III gives the steady-state analysis and the advantages of the proposed topology. Section IV proposes a new CSD that is applied to the proposed topology. Section V provides the simulation results. Section VI contains the experimental results and discussion. Section VII provides a brief conclusion.

II. Proposed Nonisolated ZVS Asymmetrical Buck Converter

Fig. 1 shows the proposed nonisolated ZVS asymmetrical buck converter. In the circuit, Q_1-Q_2 are the control MOSFETs, Q_3-Q_4 are the SRs, C_b is the blocking capacitor, L_1 and L_2 are output filter inductors, T_r is the power transformer, n is the primary-to-secondary turn ratio, and i_p and i_s are the primary and secondary currents, respectively. i_{L1} and i_{L2} are the inductor currents. The key waveforms are shown in Fig. 2. The two control MOSFETs (Q_1 and Q_2) are controlled complementarily with the dead time to achieve ZVS.

It should be noted from Fig. 1 that the source of Q_2 is connected to the output capacitor to achieve direct energy transfer. Owing to the direct energy transfer capability, the proposed topology is able to transfer part of the energy directly to load. This helps to reduce the rms value of the current of the transformer windings and SRs. At the same time, during energy transfer stage, the primary winding and the secondary winding form an autotransformer structure, which further reduces the current stress of both the primary and secondary sides significantly and leads to the reduction of the winding and conduction losses of the SRs to improve the efficiency. In addition, compared to other ZVS FB structure topologies, the proposed converter has no zero-state interval. Therefore, there is no circulating current during the operation mode, which further reduces the circulating losses in the control MOSFETs and the windings of the transformer.

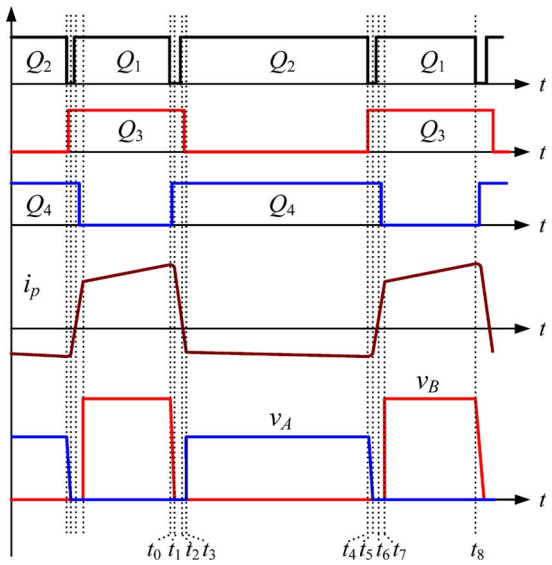

Fig. 2. Key waveforms.

There are six switching modes in one switching period, and the equivalent circuits are shown in Fig. 3 accordingly. D_1-D_2 and C_1-C_2 are the body diodes and the intrinsic capacitors of Q_1 and Q_2, respectively.

1) Mode 1 $[t_0, t_1]$ [Fig. 3(a)]: Prior to t_0, Q_1 and Q_3 are on, and the energy transfers from the input to the output through the autotransformer, which reduces both copper losses of the primary-side and the secondary-side winding. At t_0, Q_1 turns off, and the primary current i_p charges C_1 and discharges C_2. As C_1 and C_2 limit the rise rate of the voltage of C_1, Q_1 is approximately under zero-voltage turn-off condition. During this stage, the energy to discharge C_2 is from the leakage inductance of the transformer. The voltage over C_1 rises, and the voltage over C_2 decays in a resonant manner with the leakage inductance. The inductor current i_{L1} freewheels through Q_3.
2) Mode 2 $[t_1, t_3]$ [Fig. 3(b)]: At t_1, D_2 conducts, which provides zero-voltage turn-on condition for Q_2. As i_p is not enough to power the load, the body diode of Q_4 conducts and Q_4 turns on; both primary-side and secondary-side voltages are zero. The voltage V_{C_b} of the blocking capacitor is applied on the leakage inductance of the transformer and causes i_p to decrease linearly. At t_2, i_p increases inversely but is still not enough to power the load. Q_3 and Q_4 continue freewheeling.
3) Mode 3 $[t_3, t_4]$ [Fig. 3(c)]: At t_3, i_p rises to the reflected load current, and Q_3 turns off. During this stage, part of the energy directly transfers through the primary-side winding to the output capacitors instead of passing through the output inductor L_1, which further reduces the inductor loss

$$I_{s\_t43} = I_{L1} \tag{1}$$
$$I_{L1} + I_{L2} = I_o \tag{2}$$

where I_{s_t43} is the secondary average current during $[t_3, t_4]$.

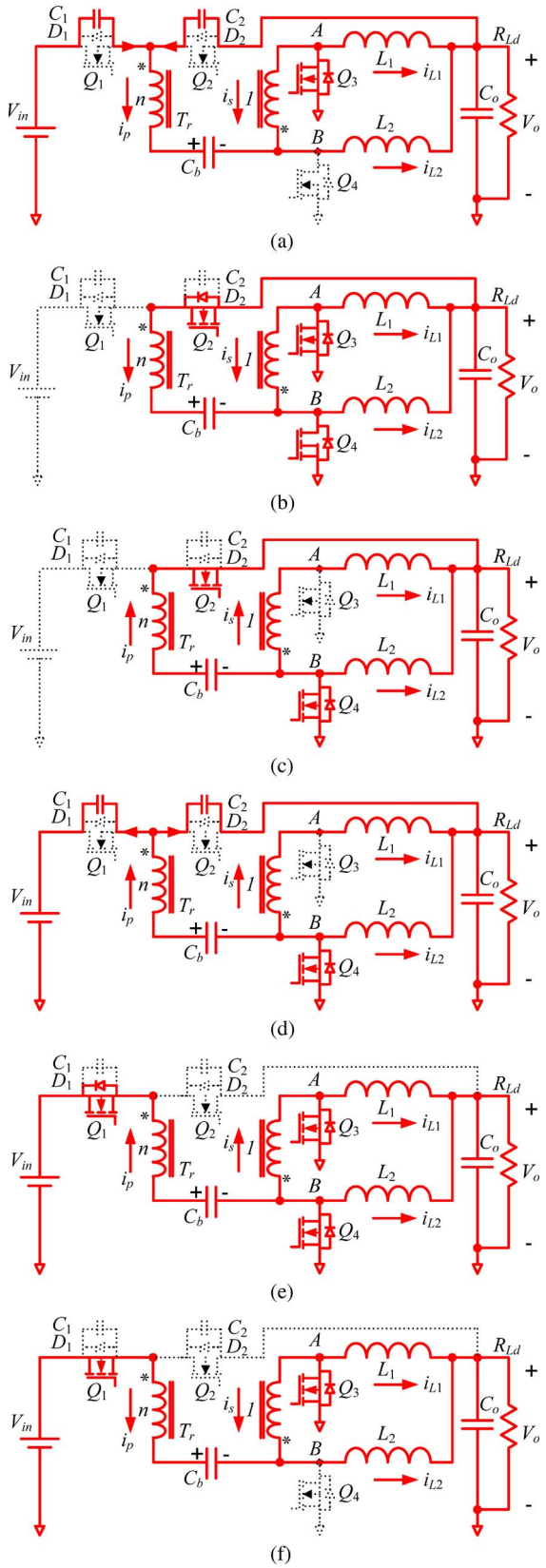

Fig. 3. Equivalent circuits of operation. (a) $[t_0, t_1]$. (b) $[t_1, t_3]$. (c) $[t_3, t_4]$. (d) $[t_4, t_5]$. (e) $[t_5, t_7]$. (f) $[t_7, t_8]$.

4) Mode 4 $[t_4, t_5]$ [Fig. 3(d)]: At t_4, Q_2 turns off, and the primary current i_p charges C_2 and discharges C_1. As C_1 and C_2 limit the rise rate of the voltage of C_2, Q_2 is approximately under zero-voltage turn-off condition. Due to the transformer, the turn-off currents of Q_2 are reduced by n (transformer turn ratio) compared to the buck converter. This gives a significant reduction of the turn-off losses, although some turn-off losses still exist. During this stage, the energy to discharge C_1 is also from the leakage inductance. The voltage across C_2 rises linearly, and the voltage across C_2 decays in a resonant manner. i_{L2} freewheels through Q_4.
5) Mode 5 $[t_5, t_7]$ [Fig. 3(e)]: At t_5, D_1 conducts, which provides zero-voltage turn-on condition for Q_1. As i_p is not enough to power the load, the body diode of Q_4 conducts and Q_4 turns on; both primary and secondary voltages are zero. $(V_{\text{in}} - V_{C_b})$ is applied on the leakage inductance of the transformer and causes i_p to increase linearly. At t_6, i_p increases inversely but is still not enough to power the load. Q_3 and Q_4 continue freewheeling.
6) Mode 6 $[t_7, t_8]$ [Fig. 3(f)]: At t_7, i_p rises to the reflected load current, and Q_4 turns off. The energy transfers through the autotransformer structure again

$$I_{s\_t87} + I_{p\_t87} = I_{L2} \tag{3}$$

where I_{s_t87} and I_{p_t87} are the primary and secondary average currents during $[t_7, t_8]$, respectively.

At t_8, the next switching cycle starts.

III. Steady-State Analysis and Advantages of Proposed Topology

A. Analysis of Steady State

The voltage transfer ratio can be derived from the volt–second balance condition across the output inductors L_1 and L_2.

For L_1, the volt–second balance is

$$\left(\frac{V_{C_b} - V_o}{n} - V_o\right) \cdot D \cdot T_s = V_o \cdot (1 - D) \cdot T_s \tag{4}$$

where V_{C_b} is the voltage over C_b, D is the duty cycle of Q_2 and equals $T_{\text{on\_}Q2}/T_s$, T_s is the switching period, V_o is the output voltage, and n is the transformer primary-to-secondary turn ratio.

For L_2, the volt–second balance is

$$\left(\frac{V_{\text{in}} - V_{C_b}}{n+1} - V_o\right) \cdot (1 - D) \cdot T_s = V_o \cdot D \cdot T_s. \tag{5}$$

Solving (4) and (5), the voltage gain of the converter and the voltage across the blocking capacitor C_b are expressed in the following equations, respectively:

$$\frac{V_o}{V_{\text{in}}} = \frac{(1 - D) \cdot D}{n + 1 - D} \tag{6}$$

$$V_{C_b} = \frac{n \cdot D \cdot V_{\text{in}}}{n + 1 - D}. \tag{7}$$

Fig. 4 shows the curves of the voltage gain of the proposed converter with different transformer ratios. It should be noted that the dc voltage gain is a parabolic curve, and therefore, in

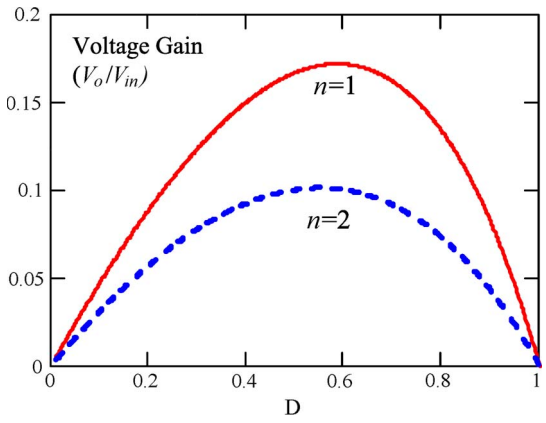

Fig. 4. Voltage gain of the proposed converter.

order to make the converter in stable operation, the duty cycle can range from 0 to 0.6 when the turn ratio $n = 1$.

B. Realization of ZVS for Switches

For the analysis of the principle of operation in Section II, during Mode 1 $[t_0, t_1]$, in order to realize zero-voltage turn-on condition for the control MOSFET Q_2, it needs enough energy to charge C_1 to $V_{\text{in}} - V_o$ and discharge C_2 to zero. Similarly, during Mode 4 $[t_4, t_5]$, in order to realize zero-voltage turn-on condition for the control MOSFET Q_1, it needs enough energy to charge C_2 to $V_{\text{in}} - V_o$ and discharge C_1 to zero. The energy to realize ZVS for the Q_1 is provided by the leakage inductance of the transformer, so the following equation should be satisfied:

$$\frac{1}{2}L_k \cdot \left(\frac{I_o/2}{n+1}\right)^2 \geq C \cdot (V_{\text{in}} - V_o)^2 \tag{8}$$

where I_o is the output current, n is the turn ratio of the transformer, and L_k is the leakage inductance of the transformer, assuming $C_1 = C_2 = C$.

C. Duty-Cycle Loss

Since the leakage inductance of the transformer limits the rise (or decay) slope of i_p, it needs time for i_p to transit from the positive (or negative) direction to the negative (or positive) reflected filter inductance current, i.e., $[t_0, t_3]$ and $[t_4, t_7]$ in Fig. 2. During that time, v_{AB} is $+(V_{\text{in}} - V_b)$ or $-V_b$, i_p is not enough to provide the output current, and all the rectifier diodes conduct, which makes the secondary rectified voltages v_A and v_B zero; thus, v_A and v_B lose the voltage in $[t_0, t_3]$ and $[t_4, t_7]$, respectively.

Thus, the duty-cycle losses during $[t_0, t_3]$ and $[t_4, t_7]$ are expressed, respectively, as

$$D_{\text{loss\_}t0-t3} = \frac{I_o}{2 \cdot n \cdot T_s} \cdot \frac{L_k}{V_{\text{in}} - V_{C_b}} \tag{9}$$

$$D_{\text{loss\_}t4-t7} = \frac{I_o}{2 \cdot n \cdot T_s} \cdot \frac{L_k}{V_{C_b}} \tag{10}$$

where I_o is the output current, n is the turn ratio of the transformer, L_k is the leakage inductance of the transformer, T_s is the switching period, and V_{C_b} is the voltage over the capacitor C_b.

For $I_o = 40$ A, $L_k = 20$ nH, and $n = 1$ from (7), (9), and (10), the calculated $D_{\text{loss\_}t0-t3} = 0.04$ and $D_{\text{loss\_}t4-t7} = 0.13$. At the same time, it is noted that, in Fig. 4, the maximum duty cycle should be limited below 0.6 to guarantee the stability of the converter. Therefore, the effective maximum duty cycle is 0.47 $(0.6 - D_{\text{loss\_}t4-t7})$, which should be satisfied in the design procedure.

D. Current Ripples of Output Filter Inductors

According to the analysis of operation principle in Section II, the output voltage V_o is applied over the output inductor L_1 during [0, DT_s] and is applied over L_2 during [DT_s, $(1-D)T_s$] in one switching cycle. Then, the output voltage applied to the inductors leads to the current ripples in the inductors. By using the volt–second law over each inductor, the current ripples of L_1 and L_2 can be derived, respectively, as

$$\Delta i_1 = \frac{V_o D}{L_1 \cdot f_s} \tag{11}$$

$$\Delta i_2 = \frac{V_o(1-D)}{L_2 \cdot f_s}. \tag{12}$$

It is noted from (11) and (12) that the current ripples in L_1 and L_2 are related to duty cycle D and the inductor values for the given V_o and the switching frequency f_s.

E. Advantages of Proposed Asymmetrical Buck Converter

Based on the principle of operation, the advantages of the nonisolated asymmetrical buck converter are highlighted as follows.

1) Extend Extremely Low Duty Cycle of Buck Converter: According to the voltage gain of (6), in order to achieve $V_{\text{in}} = 12$ V, $V_o = 1$ V, and $n = 1$, the required duty cycle is $D = 0.25$. However, for the same output voltage and input voltage, the duty cycle of a buck converter is only 0.1. Therefore, the duty cycle is extended by three times, which leads to better ripple cancellation, and lower output inductances could be used to keep the same amount of output bulk capacitors.

For a buck converter, the switching losses of the control MOSFETs are

$$P_{Q1} = \frac{1}{2} \cdot V_{\text{in}} \cdot I_{(\text{on})\_Q1} \cdot t_{\text{sw(on)}\_Q1} \cdot f_s + \frac{1}{2} \cdot V_{\text{in}} \cdot I_{(\text{off})\_Q1} \cdot t_{\text{sw(off)}\_Q1} \cdot f_s \tag{13}$$

where $I_{(\text{on})\_Q1}$ and $I_{(\text{off})\_Q1}$ are the turn-off currents, $t_{\text{sw(on)}\_Q1}$ and $t_{\text{sw(off)}\_Q1}$ are the turn-on and the turn-off time, and f_s is the switching frequency.

For the nonisolated asymmetrical buck converter, due to zero-voltage turn-on, there are no turn-on losses. The switching losses are

$$P_{Q1} = \frac{1}{n+1} \cdot \frac{1}{2} \cdot V_{\text{in}} \cdot I_{(\text{off})\_Q1} \cdot t_{\text{sw(off)}\_Q1} \cdot f_s. \tag{14}$$

In a practical design, with $n = 1$, at least 50% of the total switching losses are saved. As a specific example, when

$V_{\rm in} = 12$ V, $V_o = 1$ V, the switching frequency of 1 MHz, the output inductance $L_f = 300$ nH, and the total output current $I_o = 60$ A, for two-phase buck converters, the turn-off current of each control MOSFET is 34 A. However, for the new converter, the turn-off currents of control MOSFETs are 25 A (Q_1, a reduction of 26%) and 10 A (Q_2, a reduction of 70%), respectively, which means a significant reduction of turn-off losses due to the duty-cycle extension.

2) ZVS of Control MOSFETs: The voltage stresses of the primary-side MOSFETs are

$$V_{\rm DS\_Q1} = V_{\rm in} - V_o. \tag{15}$$

In order to realize ZVS for the control MOSFETs, we need enough energy to charge C_1 to $V_{\rm DS\_Q1}$ and discharge C_2 to zero. We can take advantage of the energy of the leakage inductance of the transformer, which is very similar to the ZVS condition of the lagging leg of the traditional FB converter [31]. Therefore, no additional resonant inductor is required. However, in order to reduce the duty-cycle loss, the leakage inductance should be reduced. In a practical design, the tradeoff between the ZVS range and the duty-cycle loss should be compromised for the transformer design.

3) Reduced Body-Diode Reverse-Recovery Losses of SR MOSFETs: For a conventional buck converter, due to the reverse recovery of the body diode with the circuit parasitics and variation of the input voltage, the peak voltage of the switching node with the ringing is more than 20 V, and therefore, 30-V rated MOSFETs are generally used for the SRs and control MOSFETs. However, due to the duty-cycle extension of the asymmetrical buck converter, the voltage stresses of the SRs, including the ringing, are reduced to less than 15 and 10 V, respectively. Therefore, according to the equation $P_{\rm rr} = Q_{\rm rr} \cdot V_s \cdot f_s$, where V_s is the peak voltage of the switching node, the reverse-recovery losses are reduced by 37.5% and 58.3%. Moreover, the voltage stresses of the control MOSFETs in the new converter are reduced to 12 V. Therefore, 20-V rated MOSFETs with lower $R_{\rm DS(on)}$ can be used for the control MOSFETs.

IV. Asymmetrical Buck Converters With Proposed New CSD

Although there are no turn-on losses due to ZVS and the turn-off losses are also reduced significantly by the factor of turn ratio $(n+1)$, the turn-off losses are still the dominant loss in the total loss breakdown. The turn-off loss would be expected even higher at above 1 MHz due to the parasitic inductance of the PCB traces and packing. Thus, in order to push switching frequency above 1 MHz, a new current source driver is proposed to further reduce the turn-off losses due to the parasitics. At the same time, the gate energy at high frequency will also be recovered.

Fig. 5 shows the new asymmetrical buck converter with the proposed CSD. The key idea is to use the CSD to further reduce the turn-off losses due to the parasitics, which are still dominant losses for a MOSFET with ZVS capability.

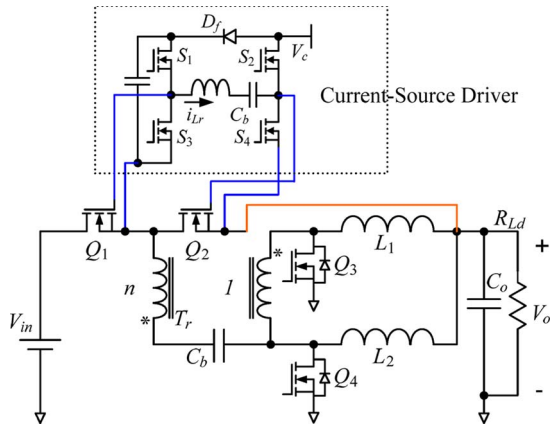

Fig. 5. Asymmetrical buck converter with proposed new CSD.

V. Design Guidelines and Simulation Results

A. Design Guidelines

In this section, a specific design example is given. For input voltage $V_{\rm in} = 12$ V, $V_o = 1.0$ V, $I_o = 40$ A, and $f_s = 1$ MHz, the turn ratio of the transformer is chosen as $n = 1$ based on (6). In this case, the designed duty cycle is $D = 0.25$, which is less than 0.47 (the effective duty cycle as discussed in Section III-C).

With $n = 1$, the primary current equals the secondary current. Therefore, we have $I_{p\_t87} = I_{s\_t87}$ and $I_{p\_t43} = I_{s\_t43}$.

From (1), (2), and (3), the following equation is obtained:

$$I_{p\_t87} + 2I_{p\_t43} = I_o. \tag{16}$$

From the charge balance of the blocking capacitor C_b, the following equation is obtained:

$$I_{p\_t87} \cdot D/f_s = I_{p\_t43} \cdot (1-D)/f_s. \tag{17}$$

Solving (16) and (17), the following equations are derived:

$$I_{p\_t87} = \frac{1-D}{2-D} \cdot I_o \tag{18}$$

$$I_{p\_t43} = \frac{D \cdot (1-D)}{2-D} \cdot I_o. \tag{19}$$

From (18) and (19), the rms currents of the control MOSFETs are

$$I_{Q1\_\rm RMS} = \frac{1-D}{2-D}\sqrt{D} \cdot I_o \tag{20}$$

$$I_{Q2\_\rm RMS} = \frac{D}{2-D}\sqrt{1-D} \cdot I_o. \tag{21}$$

Similarly, the rms currents of the SRs are

$$I_{Q3\_\rm RMS} = \frac{1}{2-D}\sqrt{D} \cdot I_o \tag{22}$$

$$I_{Q4\_\rm RMS} = \frac{2}{2-D}\sqrt{1-D} \cdot I_o. \tag{23}$$

The blocking capacitor value is chosen using

$$C_b = \frac{D \cdot (1-D)}{(2-D) \cdot \Delta V_{C_b} \cdot f_s} \cdot I_o \tag{24}$$

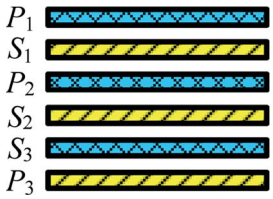

Fig. 6. Structure of planar transformer.

where ΔV_{C_b} is the voltage ripples over the blocking capacitor. For example, for $\Delta V_{C_b} = 0.12$ V (1% of the 12-V input voltage), $D = 0.25$, $I_o = 40$ A, and $f_s = 1$ MHz, then $C_b = 0.4\ \mu$F should be used. Four 0.1-μF ceramic capacitors are used to share the primary currents in the experiment prototype.

As mentioned earlier in this section, for the input voltage $V_{\rm in} = 12$ V, $V_o = 1.0$ V, $I_o = 40$ A, and $f_s = 1$ MHz, the turn ratio of the transformer is chosen as $n = 1$ based on (6). EE18 planar cores (material: 3F5) and PCB windings are employed to build the power transformer. The transformer has one turn in primary winding and one turn in secondary winding. A six-layer 2-oz copper PCB is used to build the primary and secondary windings. In order to reduce the leakage inductance of the planar transformer, the primary and secondary windings are interleaved with each other as shown in Fig. 6. The magnetizing inductances of the primary and the secondary side are the same as 1.6 μH at 1 MHz since the turn ratio $n = 1$ in this design.

From (11) and (12), the inductor values are chosen from

$$L_1 = \frac{V_o D}{\Delta i_1 \cdot f_s} \tag{25}$$

$$L_2 = \frac{V_o(1-D)}{\Delta i_2 \cdot f_s}. \tag{26}$$

For $V_o = 1.0$ V, $D = 0.25$, $f_s = 1$ MHz, $\Delta i_1 = 2$ A, and $\Delta i_2 = 4$ A, L_1 can be chosen as 150 nH and L_2 can be chosen as 220 nH.

B. Simulation Resuts

In order to verify the functionality of the proposed topology, the asymmetrical buck converter with direct energy transfer was simulated. The parameters of the simulated converter were as follows: $V_{\rm in} = 12$ V, $V_o = 1.0$ V, $I_o = 40$ A, and $f_s = 1$ MHz; control MOSFETs Q_1 and Q_2: Si7368DP; SRs Q_3 and Q_4: Si7866ADP; and output filter inductance: $L_1 = 150$ nH, $L_2 = 220$ nH. The Spice models of Si7368DP and Si7866ADP from Visay are used in the simulation. Two coupled inductors with the coupling coefficient of 0.998 are used as the PSPICE mode of the power transformer. The two inductors are the same values as 1.6 μH. The winding resistances are 20 mΩ to model the winding loss. A resistance of 200 Ω is also paralleled with the inductor to model the core loss.

Fig. 7 shows the drain-to-source voltages (v_A and v_B) of the SR MOSFETs Q_3 and Q_4. The ringing of the voltage is due to the oscillation between the leakage inductance of the transformer and the junction capacitance of the body diodes. The reverse-recovery loss of the body diode is $P_{\rm rr} = Q_{\rm rr} \cdot V_s \cdot f_s$, where V_s is the peak voltage over the switching diode. For the conventional buck converter, the switching node voltage V_s is more than 20 V, given the oscillation due to the parasitics. However, due to the duty-cycle extension with the transformer, the peak voltage V_s of the proposed converter is reduced to 11 V (v_A) and 6 V (v_B), considering the oscillation (see Fig. 7), compared to 20 V in the buck converter. Therefore, the reverse-recovery losses of the body diode are reduced by 45% and 70%, respectively, in turn. Moreover, it is observed that the drain-to-source voltages of Q_3 and Q_4 are less than 15 and 6 V, respectively; therefore, the SRs can use the MOSFETs with lower voltage rating and lower $R_{\rm DS(on)}$.

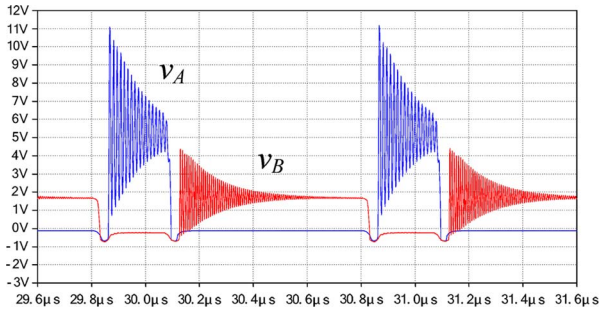

Fig. 7. Simulated waveforms: Drain-to-source voltages v_A and v_B of SRs Q_3 and Q_4.

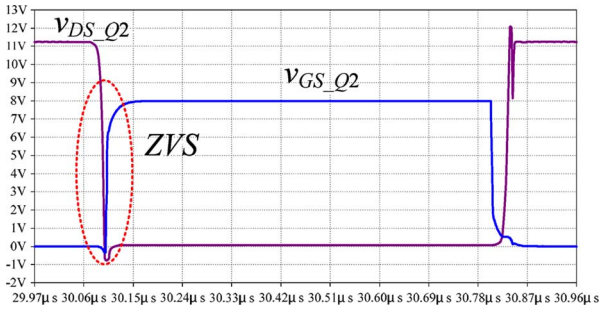

Fig. 8. Simulated waveforms: Drain-to-source voltage $v_{\rm DS\_Q2}$ and gate voltage $v_{\rm GS\_Q2}$ of Q_2.

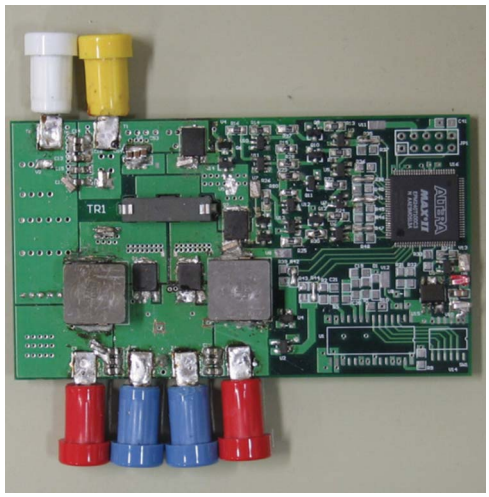

Fig. 9. Photo of the prototype.

Fig. 8 shows the drain-to-source voltage $v_{\rm DS\_Q2}$ and gate drive voltage $v_{\rm GS\_Q2}$ of Q_2. The drain-to-source voltage $v_{\rm DS\_Q2}$ drops to zero before the gate voltage $v_{\rm GS\_Q2}$ begins to rise and ZVS is achieved. This, in turn, reduces the switching losses significantly.

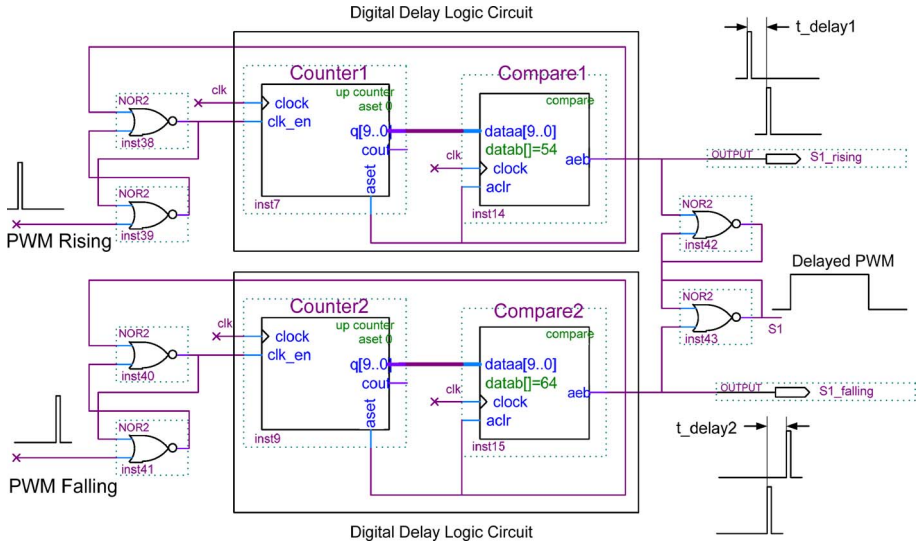

Fig. 10. Schematic of the PWM gate control signals for one channel in Quartus II software.

VI. Experimental Verification and Discussion

In order to verify the functionality of the proposed topology, a prototype of the asymmetrical buck converter was built. Fig. 9 shows the photo of the experimental prototype. The specifications are as follows: input voltage $V_{\rm in} = 12$ V, output voltage $V_o = 1.0$ V, output current $I_o = 40$ A, and $f_s = 1$ MHz. The PCB is a six-layer 2-oz copper PCB. The components used in the circuit are listed as follows: control MOSFETs Q_1 and Q_2: Si7368DP (20 V N-channel, $R_{\rm DS(on)} = 8.5$ mΩ at $V_{\rm GS} = 4.5$ V, Vishay); SRs Q_3 and Q_4: Si7866ADP (20 V N-channel, $R_{\rm DS(on)} = 3$ mΩ at $V_{\rm GS} = 4.5$ V, Vishay); and output filter inductances: $L_1 = 150$ nH and $L_2 = 220$ nH (IHLP-5050CE-01, Vishay).

From Fig. 2, it is noted that the complimentary control (i.e., D and $1 - D$) is applied to the two control MOSFETs Q_1 and Q_2. Therefore, any pulsewidth modulation (PWM) complementary control chips with the output D and $(1 - D)$ for a synchronous buck converter can achieve the desired control scheme. The control signals for the SRs can also be achieved based on the control MOSFET gate signals. In order to simplify the analysis and verify the operation of the proposed converter, we use digital complex programmable logic device (CPLD) in the experimental work.

Fig. 10 shows the schematic of the digital circuit in Quartus II software. The basic idea is presented as follows. First, the rising edge of the input PWM signal is used to enable one counter chain. Then, later on, the falling edge of the input PWM signal is used to enable the other counter chain. When the first chain times out, a single pulse is generated to set an SR latch and reset that chain; meanwhile, when the second chain times out, a single pulse is generated to set an SR latch and reset that chain. Then, the output of the latch will be the delayed version of the input PWM signal if the two counter chains have the same delay. On the other hand, by setting the different delay time of the two counters, the output of the latch will be the PWM signal with the desired width and sequence.

By using the CPLD, the four control signals can be generated according to the required signals in Fig. 2. Fig. 11 shows the gate drive signals of the four switches $(Q_1 - Q_4)$ according to the control strategy in Fig. 2. The control signals for the SRs Q_3 and Q_4 are fed into a totem gate driver structure using two bipolar transistors. The outputs of the totem driver are used to drive the SRs Q_3 and Q_4 directly. Fig. 12 shows the drain-to-source voltage v_A and gate-to-source voltage $v_{\rm GS\_Q4}$ of SR Q_4. By using the CPLD, the SR control signals can be implemented with precise dead time, which reduces the body-diode conduction time and losses in turn.

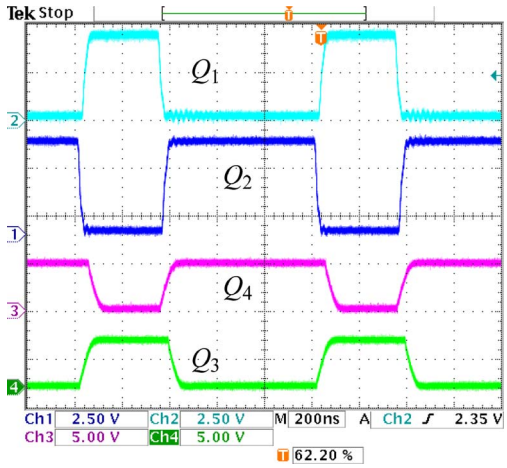

Fig. 11. Gate signals (control MOSFETs Q_1 and Q_2; SRs Q_3 and Q_4).

Fig. 13 shows the drain-to-source voltages (v_A and v_B) of the SRs Q_3 and Q_4. The oscillation of the voltage is due to the reverse recovery of the body diode and the leakage inductance. It is observed that the drain-to-source voltages of Q_3 and Q_4 are less than 15 and 10 V, respectively; therefore, the SRs can use the MOSFETs with lower voltage rating and lower $R_{\rm DS(on)}$. Since the voltages across the body diode across the SRs are significantly reduced compared to a buck converter, the reverse-recovery losses of the body diode can be reduced significantly.

Fig. 14 shows the drain-to-source voltage and gate drive voltage of Q_2. It is noted that the drain-to-source voltage drops

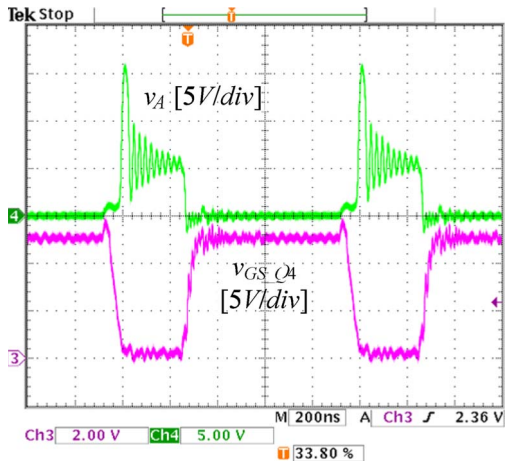

Fig. 12. Drain-to-source voltage v_A and gate-to-source voltage $v_{\mathrm{GS\_}Q4}$ of SR Q_4.

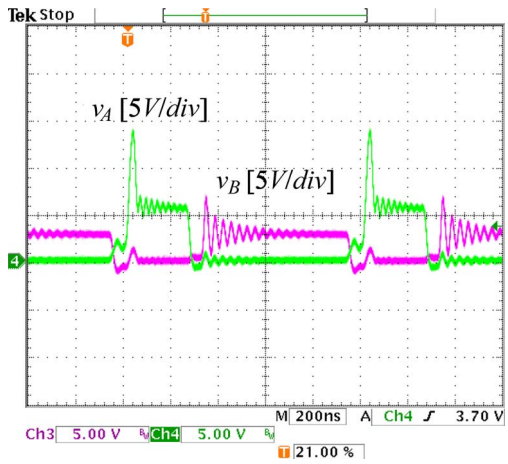

Fig. 13. Drain-to-source voltages of SRs Q_3 and Q_4.

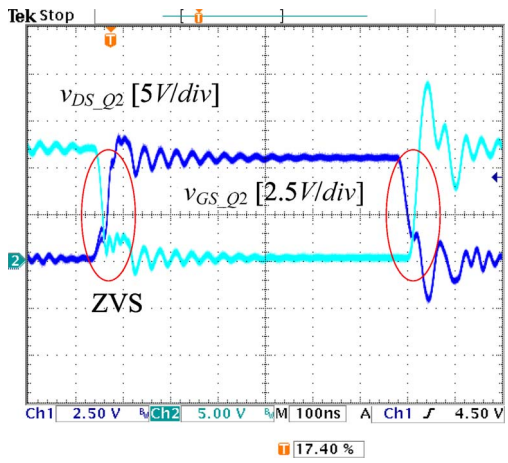

Fig. 14. Drain-to-source voltage $v_{\mathrm{DS\_}Q2}$ and gate voltage $v_{\mathrm{GS\_}Q2}$ of Q_2.

to zero before the gate voltage begins to rise and ZVS is achieved, which reduces the switching losses significantly.

Figs. 15 and 16 show the output voltage variations during the load step-up from no load to full load (see Fig. 15) and full load to no load (see Fig. 16), respectively. It is observed that the proposed converter is able to response fast during the load transient events.

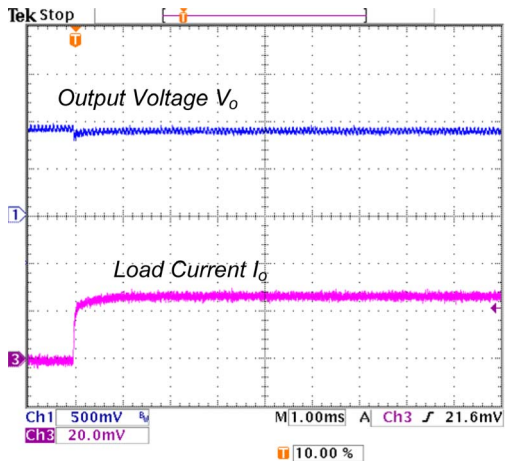

Fig. 15. Output voltage and the load current step-up: From no load to full load.

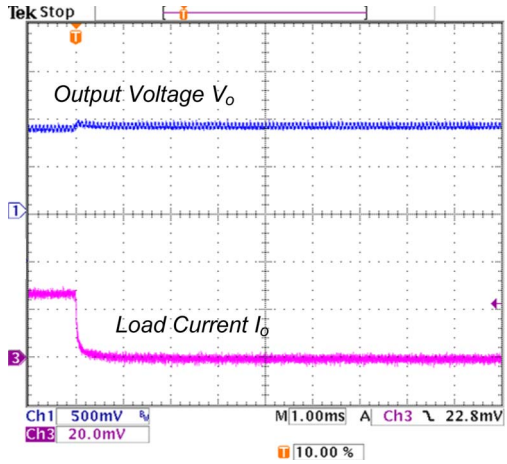

Fig. 16. Output voltage and the load current step-down: From full load to no load.

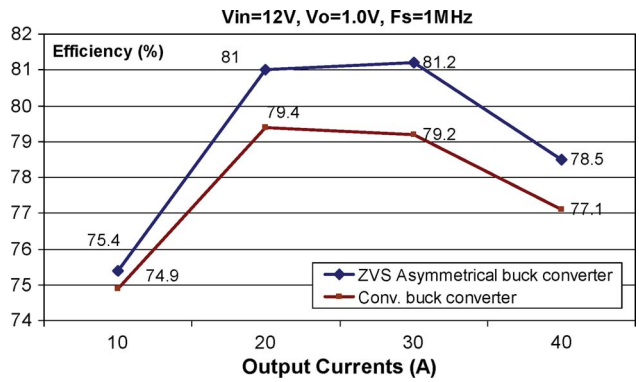

Fig. 17. Efficiency comparison at 1.0-V/40-A condition.

The two-phase buck converters using the same MOSFETs were chosen as the benchmark for the efficiency comparison. Fig. 17 shows the efficiency comparison of the proposed converter and the conventional buck converter at 1.0-V output voltage. It is observed that at 30 A, the efficiency is improved from 79.2% to 81.2% (an improvement of 2%), and at 40 A, the efficiency is improved from 77.1% to 78.5% (an improvement of 1.4%). Close efficiency is achieved at 1.0-V output voltage

compared to the topologies in [28]. It is also noted that the topologies in [27] and [28] have more control MOSFETs than the proposed converter, which increases the control complexity and total cost. The further efficiency improvement can be achieved with low-voltage-rating SR MOSFETs and the optimization of the high-frequency transformer.

VII. Conclusion

A new nonisolated ZVS asymmetrical buck converter with direct energy transfer is proposed in this paper. The transformer is used to extend the extremely low duty cycle of a conventional buck converter. The turn-off losses can be significantly reduced due to the extension of duty cycle, and there are no turn-on losses owing to the zero-voltage turn-on condition. At the same time, the voltage stress over the SRs is also reduced. Therefore, the reverse-recovery losses of the body diode can also be reduced. Furthermore, MOSFETs with lower voltage rating and lower $R_{\mathrm{DS(on)}}$ can be used to further reduce the conduction losses. Simulation and experimental results verify the functionality of the new converter and demonstrate the advantages of the proposed topology.

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Zhiliang Zhang (S'03–M'09) received the B.S. and M.Sc. degrees in electrical and automation engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2002 and 2005, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2009.

From June to September 2007, he was a Design Engineering Intern with Burlington Design Center, Linear Technology Corporation, Burlington, VT. He is currently an Associate Professor with the Aero-Power Sci-tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics. His research interests include high-frequency dc/dc converters for microprocessors, novel soft-switching topologies, power integrated circuit, digital control techniques for power electronics, and current-source gate driver techniques.

Dr. Zhang was a recipient of the Graduate Scholarship through Lite-On Technology Corporation in 2004 and a winner of "United Technologies Corporation Rong Hong Endowment" in 1999. He won an award from the Power Source Manufacture's Association to present papers at APEC 2009, Washington D.C.

Wilson Eberle (S'98–M'07) received the B.Sc., M.Sc., and Ph.D. degrees from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2000, 2003, and 2008, respectively.

He was with Ford Motor Company, Windsor, ON, and with Astec Advanced Power Systems, Nepean, ON. He is currently an Assistant Professor with the School of Engineering, University of British Columbia—Okanagan, Kelowna, BC, Canada. His research interests include the development, simulation, and modeling of improved switching power supplies using techniques such as synchronous rectification, soft-switching, resonant gate drive, and advanced control techniques. He has one U.S. and international patents pending and over 20 technical papers published at conferences and IEEE journals.

Dr. Eberle is a past recipient of the Ontario Graduate Scholarship and has won awards through the Power Source Manufacturer's Association and Ontario Centres of Excellence to present papers at international conferences.

Yan-Fei Liu (M'94–SM'97) received the B.Sc. and M.Sc. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1984 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

From February 1994 to July 1999, he was a Technical Advisor with the Advanced Power System Division of Astec (formerly Nortel Networks), where he was responsible for high-quality design, new products, and technology development. In August 1999, he joined the Department of Electrical and Computer Engineering, Queen's University, as an Associate Professor, where he is currently a full Professor. His research interests include digital control technologies for dc–dc switching converter and ac–dc converter with power factor correction, EMI filter design methodologies for switching converters, topologies and controls for high switching frequency, low-switching-loss converters, modeling and analysis of core loss and copper loss for high-frequency planar magnetics, topologies and control for voltage regulator module, and large-signal modeling of switching converters.

Dr. Liu is the winner of "Premiere's Research Excellent Award" in 2001 and the Golden Apple teaching award in 2000, both in Queen's University, and the "1997 Award in Excellence in Technology" in Nortel.

Paresh C. Sen (M'67–SM'74–F'89) was born in Chittagong, Bangladesh. He received the B.Sc. degree (with honors) in physics and the M.Sc. (Tech.) degree in applied physics from the University of Calcutta, West Bengal, India, in 1958 and 1961, respectively, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1965 and 1967, respectively.

He is currently an Emeritus Professor of electrical and computer engineering with Queen's University, Kingston, ON. He has written more than 160 research papers in the area of power electronics and drives. He is the author of two internationally acclaimed textbooks: *Principles of Electric Machines and Power Electronics* (New York: Wiley, 1989, 2nd ed., 1997) and *Thyristor DC Drives* (New York: Wiley, 1981). His fields of interest include power electronics, electric drive systems, switching power supplies, power-factor-correction circuits, modern control techniques for high-performance drive systems, and applications of fuzzy logic control in power electronics and drive systems.

Dr. Sen has served as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS (1975–1982) and as Chairman of the Technical Committees on Power Electronics (1979–1980) and Energy Systems (1980–1982) of the IEEE Industrial Electronics Society. He served as an NSERC (Natural Science and Engineering Research Council of Canada) Scientific Liaison Officer evaluating university–industry-coordinated projects (1994–1999). As an Emeritus Professor, he continues to be active in research and in several IEEE societies. He was the recipient of the IEEE Canada Outstanding Engineering Educator Award in 2006 for his outstanding contributions over four decades as an author, teacher, supervisor, researcher, and consultant. He received the Prize Paper Award from the Industrial Drives Committee for technical excellence at the IEEE Industry Applications Society Annual Meeting in 1986.