A Digital Two-Switching-Cycle Compensation Algorithm for Input-Voltage Transients in DC–DC Converters

Guang Feng, *Member, IEEE*, Eric Meyer, *Student Member, IEEE*, and Yan-Fei Liu, *Senior Member, IEEE*

***Abstract*—In this paper, a new control algorithm is proposed to achieve excellent dynamic performance for dc–dc converters undergoing an input-voltage change. Using the concept of capacitor charge balance, the proposed algorithm predicts the two-switching-cycle duty ratio series to drive the converter back to steady state following an input-voltage transient. The equations needed to calculate the required duty cycle series are presented. By using the proposed algorithm, good transient performance, such as small output-voltage overshoot/undershoot and short recovery time, is achieved. Simulations and experiments are performed using a synchronous buck converter to verify the effectiveness of the proposed algorithm. Results show that the proposed method produces superior dynamic performance over that of a conventional current-mode PID controller.**

***Index Terms*—DC–DC power conversion, digital control, transient response.**

I. Introduction

As VOLTAGE regulation requirements for high-performance digital circuits become increasingly stringent, it has become necessary to rethink the long-perceived concept that analog, linear controllers are the most suitable candidate for dc–dc converters. Bandwidth limitations of conventional controllers have forced power electronics engineers to increase switching frequency, increase output capacitance, and/or decrease output inductance to improve the dynamic response of buck converters. Such hardware modifications result in lower efficiency and/or higher component cost. However, by improving the *controller's* dynamic response, the transient performance of a power converter can be improved without topology modification. Therefore, it is not only necessary but also practical to explore dynamic performance improvements for controllers of dc–dc power converters.

Recently, numerous nonlinear analog control strategies have been introduced to provide improved dynamic performance during transient conditions. Voltage-mode and current-mode hysteretic controllers are presented in [1]–[6]. Various sliding-mode controllers are presented in [7]–[11]. Unfortunately, both hysteretic controllers and sliding-mode controllers possess at least one of the following undesired attributes: 1) variable switching frequency; 2) nonzero steady-state error; and 3) operating frequencies dependant on the load current and/or the equivalent series resistance (ESR) of the output capacitor. In general, all forms of analog control suffer from at least one of the following conditions: 1) large component count for complex control methods; 2) vulnerability to noise, thermal conditions, component age, and tolerance; and 3) tedious parameter modification procedures. Most importantly, it is difficult for any of the aforementioned analog controllers to achieve superior dynamic performance (with minimal voltage deviation and settling time), as it requires complex derivation and calculation, which can only be practically derived digitally.

An increasing amount of research has been performed in the field of digital control of dc–dc power converters. However, the majority of research has been concentrated on the digital implementation of classical, linear controllers. Various voltage-mode and current-mode digital linear controllers are presented in [12]–[21]. In these papers, issues such as analog/digital conversion quantization, digital pulsewidth modulation quantization, sampling delay effects, z-domain small signal modeling, and compensator design are examined. While investigation of these factors is crucial to the development of digital control of power converters, linear controllers fail to utilize the mathematical capabilities of digital systems. One of the core advantages of digital control is its ability to effectively implement nonlinear controllers that require complex operations (multiplication, division, etc.), which were previously very difficult to be realized through analog schemes.

An ideal dc–dc converter controller would behave linearly during steady-state conditions for tight voltage regulation and nonlinearly during transient conditions for fast response. It is demonstrated in [22] and [23] that by employing two separate controllers for steady-state operation and transient operation, the dynamic response can be significantly improved while not sacrificing steady-state accuracy. Control methods are presented, which utilize a linear control scheme during steady-state conditions and saturate the duty cycle to either 0% or 100% when a load transient occurs. While these methods effectively reduce voltage deviation caused by load transients, imprecise timing of the saturation period leads to suboptimal settling times in most cases.

To address the shortcomings of [22] and [23], dc–dc controllers are presented in [24]–[26], which utilize a conventional

Manuscript received May 18, 2008; revised September 8, 2008; accepted September 8, 2008. Current version published February 6, 2009. Recommended for publication by Associate Editor P. Jain.

G. Feng was with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada. He is now with Argonne National Laboratory, Argonne, IL 60439 USA (e-mail: gfeng@aps.anl.gov).

E. Meyer and Y.-F. Liu are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: eric.meyer@ece.queensu.ca; yanfei.liu@queensu.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2008.2006612

linear control method during steady-state conditions and employ a capacitor charge balance technique during transient conditions. By monitoring the charge removed or absorbed by the output capacitor during a transient event, the controllers are capable of determining the precise duty cycle series that allows the converter to recover from a transient event in minimal time.

Controllers based on linear and nonlinear "optimal" switching surfaces are presented in [27]–[30]. This category of controllers, termed either sliding-mode control or boundary control, successfully attempts to drive the converter such that it may recover from a transient event in minimal time.

However, the focus of the papers [24]–[30] deals exclusively with output-voltage transients caused by rapid output current transients and/or rapid voltage reference transients.

It is known that the output voltage of a dc–dc converter may be affected by load current transients as well as large input-voltage transients. Large-signal input-voltage transients are common for mobile devices that generally possess different battery and ac–dc adapter input voltages. Therefore, relatively fast input-voltage transients can occur when these devices switch from an ac source to battery power and vice versa. In this paper, a new compensation algorithm is proposed to achieve a two-switching-cycle transient response for dc–dc converters undergoing an input-voltage transient. Based on the concept of capacitor charge balance, the proposed algorithm predicts the two-switching-cycle duty ratio series to drive the converter back to steady state after an input-voltage change. Using the proposed algorithm, excellent transient performance, such as small output-voltage overshoot/undershoot and short recovery time, is achieved. By combining the proposed algorithm with the control method presented in [25], a buck converter with exceptional dynamic response to both input-voltage transients and load transients may be realized. The proposed two-switching-cycle compensation algorithm and the mathematical equations to calculate the duty cycle series are fully discussed in Sections II and III. Sections IV and V show simulation and experimental results of a synchronous buck converter to verify the effectiveness of the proposed compensation algorithm. The results confirm that by using the proposed algorithm, good dynamic performance, such as small overshoot/undershoot and short recovery time, is achieved.

II. Operation Principle of the Two-Switching-Cycle Compensation Algorithm for Input-Voltage Transients

This section introduces the two-switching-cycle compensation algorithm to improve the dynamic performance of a buck converter under an input-voltage change. First, the transient response of a conventional control method during an input-voltage change is analyzed.

A. Transient Response of a Conventional Control Method Following an Input-Voltage Change

Fig. 1 illustrates the dynamic response of a buck converter under the control of a conventional control method (such as a linear voltage-mode or current-mode control scheme) following a positive input-voltage step. Initially, the input voltage varies

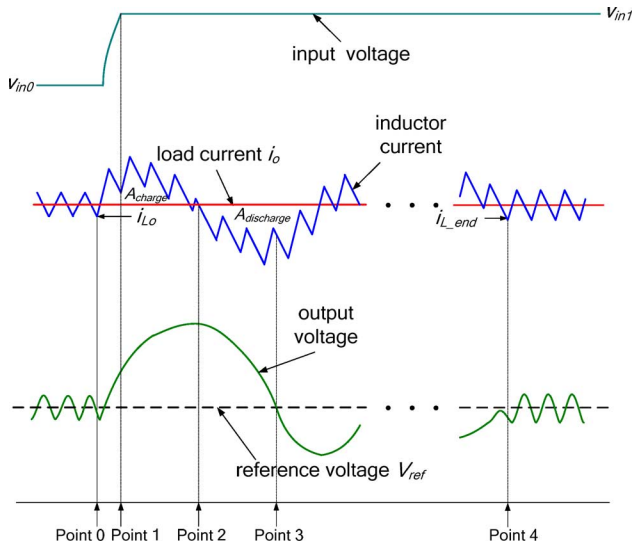

Fig. 1. Transient response of a conventional control method following an input-voltage change.

from $v_{\rm in0}$ to $v_{\rm in1}$ between point 0 and point 1 (as shown in Fig. 1). It is assumed that before point 1, the output-voltage increase has not been sensed by the control system; therefore, the duty cycle remains constant. As a result, the inductor current will increase and the capacitor will charge causing the output voltage to increase. At point 1, the increase of the output voltage is sensed by the control system. The conventional control method will begin to decrease the duty cycle, which eventually causes the inductor current to decrease. Before point 2, the average inductor current over one switching cycle is still higher than the load current. As a result, the average capacitor voltage will continue to increase. At point 2, the inductor current is equal to the load current, and thus, the capacitor stops charging. At this point, the voltage overshoot is at its maximum.

After point 2, the inductor current will continue to decrease and become lower than the load current. As a consequence, the capacitor discharges and the output voltage will drop toward the reference voltage $V_{\rm ref}$. When the capacitor charge $A_{\rm charge}$ is equal to the capacitor discharge $A_{\rm discharge}$, the capacitor voltage reaches its reference value $V_{\rm ref}$ (shown as point 3 in Fig. 1). However, at this point, the inductor current and the duty cycle are usually not equal to their new steady-state values. Therefore, for the switching cycle after point 3, the average capacitor current i_C does not equal zero, and the output voltage is not equal to the reference voltage $V_{\rm ref}$. In addition, since i_C is not zero for the switching cycle after point 3, the capacitor will continue to discharge or charge, causing the output voltage to continue to fluctuate.

The converter will eventually enter new steady-state several switching cycles later (shown as point 4 in Fig. 1). At this time, the inductor current reaches its new steady-state valley value $i_{L\_\rm end}$, the duty cycle reaches its new steady-state value $D_{\rm new}$, and the average value of the output voltage converges to the nominal reference voltage $V_{\rm ref}$.

It can be observed from the aforementioned analysis that a conventional linear control method cannot achieve superior

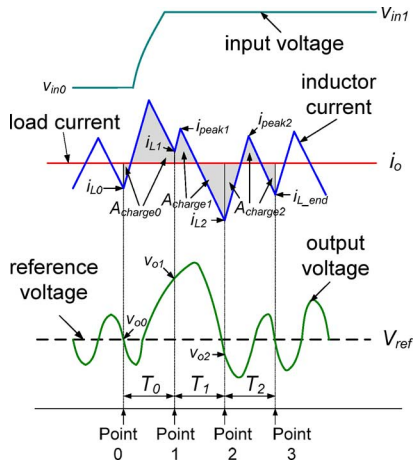

Fig. 2. Proposed two-switching-cycle transient response for a positive input-voltage change.

transient response following an input-voltage change for the following reasons.

1) When the charge delivered to the capacitor $A_{\rm charge}$ is equal to the charge delivered by the capacitor $A_{\rm discharge}$ for the first time (shown as point 3 in Fig. 1), the inductor current is not equal to its new steady-state valley value $i_{L\_\rm end}$. Furthermore, the duty cycle does not reach its new steady-state value $D_{\rm new}$. Thus, it requires additional time for the output voltage and the inductor current to converge to their new steady-state values.
2) Since conventional linear control methods are bandwidth-limited, their duty cycles vary at a finite rate. Thus, linear control methods cannot guarantee the minimization of the capacitor charge and discharge areas $A_{\rm charge}$ and $A_{\rm discharge}$ following an input-voltage change. This will prevent the converter from achieving a short recovery time and a small overshoot/undershoot during the transient.

B. Proposed Two-Switching-Cycle Transient Response Following an Input-Voltage Change

By satisfying the following conditions, the proposed compensation algorithm can drive a dc–dc converter back to steady state in two switching cycles, following an input-voltage step change. These conditions are as follows.

1) The charge delivered to the capacitor is equal to the charge delivered by the capacitor at the end of the second switching cycle.
2) At the end of the second switching cycle, the inductor current is equal to its new steady-state valley value $i_{L\_\rm end}$.
3) At the end of the second switching cycle, the duty cycle is set to the new steady-state value $D_{\rm new}$ for the new input-voltage condition.

To satisfy the aforementioned conditions, the transient response of a buck converter under the control of the proposed algorithm is illustrated in Fig. 2.

As shown in Fig. 2, it is assumed that before point 0, the input voltage is kept constant at $v_{\rm in0}$. During switching cycle T_0 (between point 0 and point 1), the input voltage is increased from $v_{\rm in0}$ to $v_{\rm in1}$. It is noted that for higher power devices (such as microprocessors), larger input capacitor banks will slow the input-voltage transient; however, this algorithm can handle slower input-voltage transients as well. The input-voltage change need not be a step change for the proper operation of the algorithm. Before point 1, the input-voltage change has not been sensed by the control system; thus, the duty cycle is kept unchanged. As a result, the inductor current will increase, which, in turn, will cause the output voltage to increase. In the proposed control system, the input voltage is sensed at every switching cycle. If at point 1, the sensed input-voltage deviation exceeds a predefined threshold, the two-switching-cycle compensation algorithm is activated. A duty cycle series (d_1 for the first switching cycle T_1 and d_2 for the second switching cycle T_2) is predicted for the two switching cycles following point 1. In addition, when the transient ceases at the end of the second switching cycle (shown as point 3 in Fig. 2), the duty cycle value for the next switching cycle is set to the new steady-state value $D_{\rm new}$ for the new input-voltage condition.

If the conditions (1)–(3) are satisfied at the end of the transient (shown as point 3 in Fig. 2), the average output voltage will recover back to the nominal reference voltage $V_{\rm ref}$, the inductor current will decay to its new steady-state valley value $i_{L\_\rm end}$, and the duty cycle will be set to its new steady-state value $D_{\rm new}$. As a result, in the switching cycle after point 3, the average inductor current is equal to the load current i_o. Thus, the average capacitor current will be zero. Therefore, the average output voltage will be equal to $V_{\rm ref}$. It can be concluded that in the switching cycle after point 3, the inductor current, the duty cycle, and the output voltage will reach their new steady-state values. The converter will immediately enter the new steady state without any switchover between the transient and the steady state.

It should be mentioned that in the proposed compensation algorithm, at least two switching cycles are needed. The explanation will be given as follows.

It is assumed that at point 1, the output-voltage error is represented as Δv_o. The error between the inductor current and the new steady-state inductor current valley value $i_{L\_\rm end}$ is represented as Δi_L. The relationship between the duty cycle d and the variation of the output voltage and the inductor current in one switching cycle can be expressed as

$$\begin{cases} \Delta v_o = f_1(d) \\ \Delta i_L = f_2(d) \end{cases} \tag{1}$$

where $f_1(d)$ and $f_2(d)$ are the mathematical functions related to the dc–dc converter.

In order to drive the output voltage and the inductor current to their new steady-state values in one switching cycle, (2) must be satisfied

$$\begin{cases} \Delta v_o = f_1(d_1) \\ \Delta i_L = f_2(d_1). \end{cases} \tag{2}$$

However, (2) usually has no solution mathematically, since the number of unknowns is fewer than the number of equations.

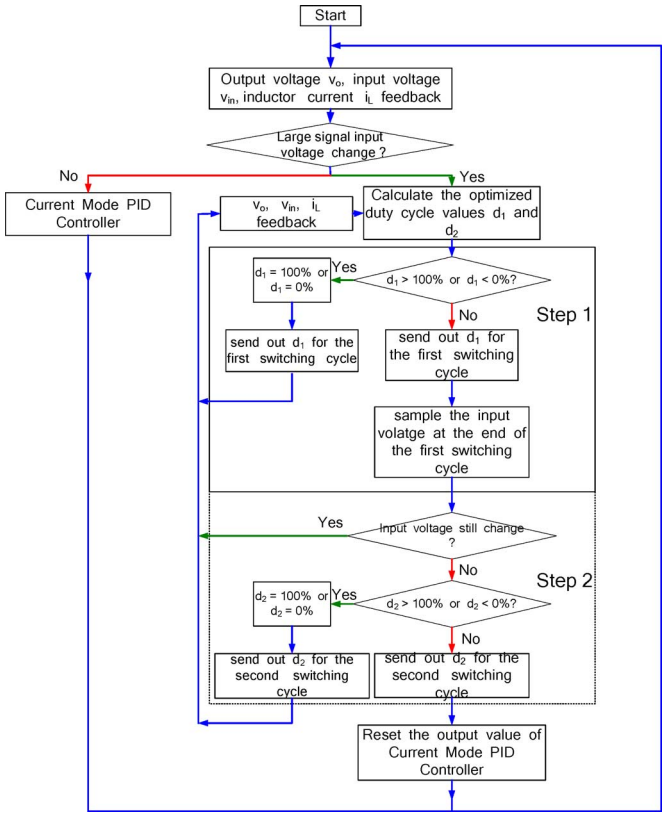

Fig. 3. Flowchart of the improved two-switching-cycle compensation algorithm.

Therefore, at least two switching cycles are required, as follows:

$$\begin{cases} \Delta v_o = f_1(d_1) + f_1(d_2) \\ \Delta i_L = f_2(d_1) + f_2(d_2). \end{cases} \tag{3}$$

Fig. 2 shows that in the two-switching-cycle transient response, the input-voltage step change is assumed to be completed before point 1. However, in typical applications, the input-voltage variation is usually slow due to the input filter. Thus, it may take several switching cycles for the input voltage to reach its new steady-state value. To resolve this problem, the improved two-switching-cycle compensation algorithm is proposed, as shown in Fig. 3.

In the improved algorithm, the input voltage is sensed at every switching cycle. If a large-signal input-voltage change is sensed, the compensation algorithm will be activated immediately. A two-switching-cycle duty ratio series is predicted for the proposed transient response. If the input voltage sampled at the end of the first switching cycle (shown as point 2 in Fig. 2) is different from that sampled at the end of the previous switching cycle (shown as point 1 in Fig. 2), the compensation algorithm will be reset, and a new two-switching-cycle compensation process will be restarted (shown in Fig. 3). The compensation algorithm will keep restarting until the input voltage stops changing. Then, the algorithm enters the second-switching-cycle period (shown as step 2 in Fig. 3). The transient will end one switching cycle later. When the transient ends, the control system will be switched back to the current-mode PID controller, which is used to control the steady-state and small-signal condition. The compensation algorithm calculates the new steady-state values $i_{L\mathrm{new}}$ and D_{new} for the current-mode PID controller and resets the outputs of the current-mode PID controller to these calculated values. Therefore, the controller will undergo a smooth transition from transient to steady-state mode with minimal switchover effects. A "slow" PID controller is not required in order to maintain stability during mode switchovers.

It is possible that the calculated duty cycle value d_1 or d_2 is greater than 100% or less than 0% if the input-voltage step change or the inductor value is very large. Thus, three or more switching cycles may be required for the dc–dc converter to enter the new steady-state condition. In this case, at the beginning of step 1 or step 2 of the algorithm, the duty cycle will be set to 100% if the calculated value is greater than 100%, or set to 0% if it is lower than 0%. In addition, the two-switching-cycle compensation process will be restarted to regulate the converter (as shown in Fig. 3).

III. Mathematical Equations to Calculate the Two-Switching-Cycle Duty Ratio Series for an Input-Voltage Transient

The analysis in Section II shows that the key point to achieve the two-switching-cycle transient response is to precisely predict the duty cycle series d_1, d_2, the new steady-state inductor current value $i_{L\mathrm{new}}$, and the new steady-state duty cycle value D_{new} for the new input-voltage condition. Based on these predicted values, the buck converter will enter the new steady state in two switching cycles without any switchover between the transient and the steady state. As a result, small overshoot/undershoot and short recovery time can be achieved.

For a synchronous buck converter operating at a fixed frequency, it is assumed that the inductor value L, the capacitor value C, and the switching frequency f_s are known. In addition, the inductor current i_L, the input voltage v_{in}, and the output voltage v_o can be measured directly. In order to simplify the calculation, three assumptions are made.

1) Using the proposed compensation algorithm, the output-voltage variation during the transient is very small so that in the algorithm calculation, the output voltage is assumed to be equal to its reference value V_{ref}.
2) The load current i_o is kept unchanged during the transient. Therefore, its value can be obtained from the average inductor current value of one switching cycle before the transient.
3) The input voltage does not change again during the switching cycle T_1 and T_2.

Based on the aforementioned assumptions, the duty cycle $d_1, d_2, D_{\mathrm{new}}$, and i_{new} can be calculated in advance to compensate for the influence of the input-voltage change. It should be mentioned that if the input-voltage variation is slow such that assumption (3) is not satisfied, or the calculated duty cycle value d_1 or d_2 is greater than 100% or lower than 0%, the improved algorithm (as shown in Fig. 3) will be utilized.

In order to achieve condition (2) described in Section II, (4) must be satisfied

$$i_{L\_\mathrm{end}} - i_{L1} = (d_1 v_{\mathrm{in}1} - v_o')\frac{T_s}{L} + (d_2 v_{\mathrm{in}1} - v_o')\frac{T_s}{L} \quad (4)$$

where i_{L1} is the inductor current measured at point 1 (shown in Fig. 2). T_s is the switching period. The equivalent output voltage v_o' and the new steady-state inductor current valley value i_{L_end} are calculated in (5) and (6), respectively

$$v_o' \approx V_{\mathrm{ref}} + i_o r_{\mathrm{loss}} \quad (5)$$

$$i_{L\_\mathrm{end}} = i_o - \frac{1}{2}\frac{v_o'}{L}T_S\frac{v_{\mathrm{in}1} - v_o'}{v_{\mathrm{in}1}} \quad (6)$$

where i_o is the load current and r_{loss} is derived as

$$r_{\mathrm{loss}} = R_L + R_{\mathrm{ON}} + R_{\mathrm{switching}} \quad (7)$$

where R_L is the winding resistor of the inductor, R_{ON} is the MOSFET ON resistance, and $R_{\mathrm{switching}}$ is the MOSFET switching loss equivalent resistance. The values of R_L, R_{ON}, and $R_{\mathrm{switching}}$ can be found or estimated from the component data sheets.

The relationship between d_1 and d_2 can be directly derived as

$$d_1 + d_2 = \frac{(i_{L\_\mathrm{end}} - i_{L1})(L/T_s) + 2v_o'}{v_{\mathrm{in}1}} = k. \quad (8)$$

As previously mentioned, under the control of the proposed algorithm, the charge delivered to the capacitor is equal to the charge delivered by the capacitor at the end of the transient

$$A_{\mathrm{charge}0} + A_{\mathrm{charge}1} + A_{\mathrm{charge}2} = 0 \quad (9)$$

where $A_{\mathrm{charge}0}$ is the change of capacitor charge at point 1 (shown in Fig. 2), and $A_{\mathrm{charge}1}$ and $A_{\mathrm{charge}2}$ represent the capacitor charge variation during the switching cycles T_1 and T_2, respectively.

Assuming that the capacitor voltage ripple is very small, $A_{\mathrm{charge}0}$ can be calculated from (10) using the output voltage v_{o1} measured at point 1 of Fig. 2, and (11) and (12)

$$\begin{aligned} A_{\mathrm{charge}0} &= C(v_{C1} - v_{C0}) \approx C(v_{C1} - V_{\mathrm{ref}}) \\ &= C(v_{o1} - i_{C1}\mathrm{ESR} - V_{\mathrm{ref}}) \\ &= C(v_{o1} - (i_{L1} - i_o)\mathrm{ESR} - V_{\mathrm{ref}}) \end{aligned} \quad (10)$$

$$C\frac{dv_C}{dt} = i_c = i_L - i_o \quad (11)$$

$$v_o = v_C + i_C\mathrm{ESR} \quad (12)$$

where v_{C0} and v_{C1} are the capacitor voltage at point 0 and point 1, i_{C1} is the capacitor current at point 1 (shown in Fig. 2), and ESR is the equivalent series resistance of the capacitor.

The capacitor charge variation $A_{\mathrm{charge}1}$ during the switching cycle T_1 can be calculated as

$$\begin{aligned} A_{\mathrm{charge}1} = {} & \frac{1}{2}d_1 T_s\left[(i_{L1} - i_{L2}) + (i_{\mathrm{peak}1} - i_{L2})\right] \\ & + \frac{1}{2}(1 - d_1)T_s(i_{\mathrm{peak}1} - i_{L2}) - (i_o - i_{L2})T_S \end{aligned} \quad (13)$$

where i_{L2} is the inductor current value measured at point 2 and $i_{\mathrm{peak}1}$ is the peak inductor current value during the switching cycle T_1 (shown in Fig. 2). $i_{\mathrm{peak}1}$ and i_{L2} can be calculated using (14) and (15), respectively

$$i_{\mathrm{peak}1} = i_{L1} + d_1 T_s\frac{(v_{\mathrm{in}1} - v_o')}{L} \quad (14)$$

$$i_{L2} = i_{L1} + (d_1 v_{\mathrm{in}1} - v_o')\frac{T_s}{L}. \quad (15)$$

The capacitor charge variation $A_{\mathrm{charge}2}$ during the switching cycle T_2 is expressed as

$$\begin{aligned} A_{\mathrm{charge}2} = {} & \frac{1}{2}d_2 T_s(i_{\mathrm{peak}2} - i_{L2}) + \frac{1}{2}(1 - d_2)T_s\left[(i_{\mathrm{peak}2} - i_{L2})\right. \\ & \left. + (i_{L\_\mathrm{end}} - i_{L2})\right] - (i_o - i_{L2})T_S \end{aligned} \quad (16)$$

where $i_{\mathrm{peak}2}$ is the peak inductor current value during the switching cycle T_2 (shown in Fig. 2), which can be obtained as

$$i_{\mathrm{peak}2} = i_{L2} + d_2 T_s\frac{(v_{\mathrm{in}1} - v_o')}{L}. \quad (17)$$

By substituting (6), (8), and (12)–(17) into (9), the duty cycle d_1 is calculated to be (18) or (19), and d_2 can be derived by using (20), where (18)–(20) are shown at the bottom of this page.

It is observed from the simulation results in Figs. 4 and 5 that (19) and (20) should be used in the calculation as they yield suitable duty cycle values (between 0% and 100%).

When the two-switching-cycle transient response ends, the control algorithm will be switched back to the current-mode PID controller, which is used to control the steady-state and small-signal condition. In order to allow the buck converter to enter the new steady-state condition smoothly, the compensation algorithm calculates the new steady-state values $i_{L\mathrm{new}}$ and D_{new} for the current-mode PID controller, and resets the outputs of the current-mode PID controller to these calculated values. The new steady-state duty cycle value D_{new} can be obtained by using (21). Since the new steady-state inductor current valley value is i_{L_end} and the inductor current is sampled $0.3T_s$ before

$$d_1 = \frac{1}{2}\left[(1+k) + \sqrt{(1+k)^2 + \frac{4L}{v_{\mathrm{in}1}T_s}\left(i_{L1} - 2i_o + i_{L\_\mathrm{end}} - \frac{1}{2}k^2 v_{\mathrm{in}1}\frac{T_s}{L} + \frac{A_{\mathrm{charge}0}}{T_s}\right)}\right] \quad (18)$$

$$d_1 = \frac{1}{2}\left[(1+k) - \sqrt{(1+k)^2 + \frac{4L}{v_{\mathrm{in}1}T_s}\left(i_{L1} - 2i_o + i_{L\_\mathrm{end}} - \frac{1}{2}k^2 v_{\mathrm{in}1}\frac{T_s}{L} + \frac{A_{\mathrm{charge}0}}{T_s}\right)}\right] \quad (19)$$

$$d_2 = k - d_1. \quad (20)$$

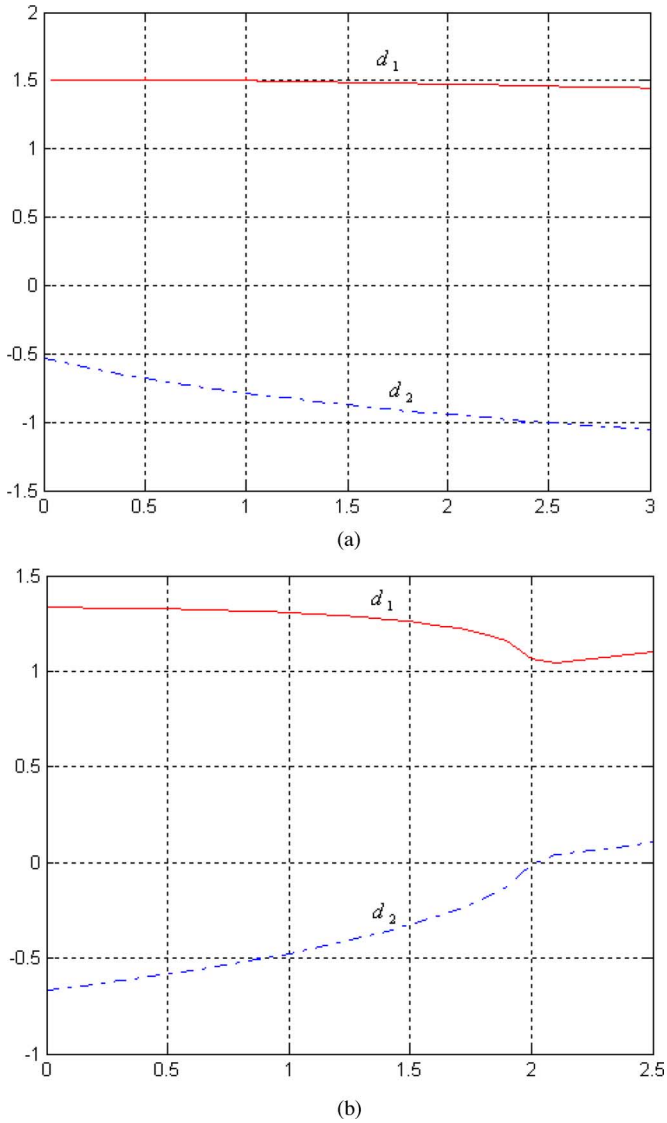

Fig. 4. Calculated duty cycle values under different input-voltage step changes using (18) and (20) (X-axis: input-voltage step change $\Delta v_{\rm in}$ (V); Y-axis: duty cycle value) (solid line: d_1, dashed line: d_2). (a) $v_{\rm in0} = 5$ V, $v_{\rm in1} = v_{\rm in0} + \Delta v_{\rm in}$. (b) $v_{\rm in0} = 7.5$ V, $v_{\rm in1} = v_{\rm in0} - \Delta v_{\rm in}$.

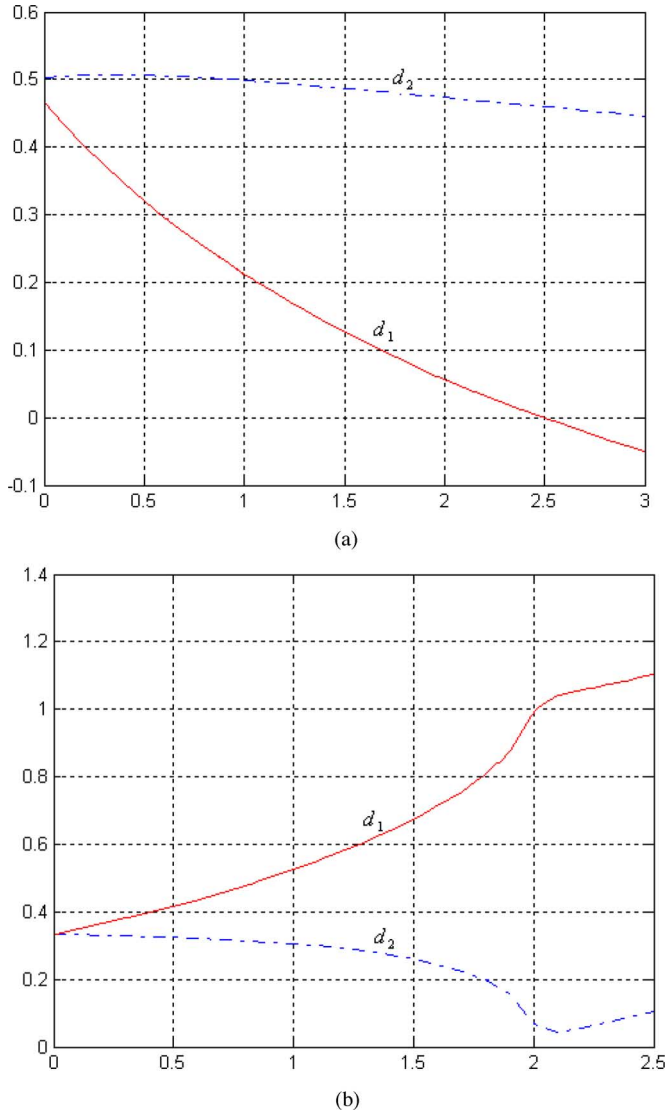

Fig. 5. Calculated duty cycle values under different input-voltage step changes using (19) and (20) (X-axis: input-voltage step change $\Delta v_{\rm in}$ (V); Y-axis: duty cycle value) (solid line: d_1, dashed line: d_2). (a) $v_{\rm in0} = 5$ V, $v_{\rm in1} = v_{\rm in0} + \Delta v_{\rm in}$. (b) $v_{\rm in0} = 7.5$ V, $v_{\rm in1} = v_{\rm in0} - \Delta v_{\rm in}$.

the switch is turned on, the new steady-state inductor current reference value $i_{L\rm new}$ can be obtained using (22)

$$d_{\rm new} = \frac{v_o'}{v_{\rm in1}} \tag{21}$$

$$i_{L\rm new} = i_{L\_\rm end} + 0.3 v_o' \frac{T_s}{L}. \tag{22}$$

Compared to current-mode control, only one additional real-time measurement is required for the proposed algorithm: the input voltage. This addition can be accomplished without significant cost. While some converter parameters must be estimated by the designer, small errors will not significantly affect the performance of the proposed algorithm, which is verified in the experiments.

In order for the proposed controller to be transferred from one converter to another, the power train parameters and switching speed can be reprogrammed. This proves advantageous over traditional analog designs that require the compensator's components to be replaced.

In order to estimate the effective range of the proposed algorithm, simulations were performed to calculate the values of d_1 and d_2 under different input-voltage step changes. Here, it is assumed that the worst case occurs, such that at point 0, as shown in Fig. 2, the input voltage is changed from $v_{\rm in0}$ to $v_{\rm in1}$ instantly. For this case, $A_{\rm charge0}$ can be derived as

$$\begin{aligned} A_{\rm charge0} = {} & \frac{1}{2} D_0 T_s D_o (v_{\rm in1} - v_0) \frac{T_s}{L} + \frac{1}{2}(1 - D_0) T_s \\ & \times \left[D_o (v_{\rm in1} - v_0) \frac{T_s}{L} + (D_o v_{\rm in1} - v_0) \frac{T_s}{L} \right] \\ & - (i_o - i_{L0}) T_S \end{aligned} \tag{23}$$

where i_{L0} is the inductor current value at point 0 and D_0 is the duty cycle value for the switching cycle T_0 (shown in Fig. 2).

The values of D_0 and i_{L0} can be obtained from (24) and (25), respectively

$$D_0 = \frac{V_{\rm ref}}{v_{\rm in0}} \tag{24}$$

$$i_{L0} = i_o - \frac{1}{2}\frac{v_o'}{L}(1 - D_0)T_S. \tag{25}$$

In the simulation, it is assumed that before the transient, the input voltage is $v_{\rm in0}$. Then, a step change of $\Delta v_{\rm in}$ is imposed on the input voltage at point 0, as shown in Fig. 2. The duty cycles d_1 and d_2 can be calculated using (18)–(20), where $A_{\rm charge0}$ is obtained by using (23). The parameters of the synchronous buck converter used in the simulation are $V_o = 2.5$ V, $L = 1$ μH, $C = 235$ μF, and $T_s = 2.56$ μs ($f_s = 390.6$ kHz). In order to simplify the calculation, all the losses are neglected.

Figs. 4 and 5 illustrate the calculated duty cycles d_1 and d_2 under different input-voltage step changes. In Fig. 4, d_1 and d_2 are calculated using (18) and (20). In Fig. 5, d_1 and d_2 are calculated from (19) and (20). It can be seen from Fig. 4 that either d_1 or d_2 or both are out of range of (0%, 100%). On the other hand, by using (19) and (20), the values of d_1 and d_2 are both within 0%, 100% if the input-voltage step change is less than 2 V (shown in Fig. 5). Therefore, (19) and (20) should be used to calculate d_1 and d_2.

In addition, Fig. 5(a) shows that if the input-voltage positive step change is less than 2.5 V, d_1 and d_2 are both within the range (0%, 100%). If the input-voltage negative step change is less than -2 V, d_1 and d_2 are both within the range (0%, 100%) [shown in Fig. 5(b)]. In the proposed buck converter, due to the effect of the input filter, it will take approximately 20–40 μs for the input voltage to change from 5 to 7.5 V or from 7.5 to 5 V. The input-voltage change in one switching cycle is about (7.5–5 V)/(20 μs/T_s) = 0.32 V $\ll$ 2 V, where the switching period $T_s = 2.56$ μs. Thus, it can be observed from Fig. 5 that in this input-voltage variation speed, d_1 and d_2 are all within the range (0%, 100%). Therefore, the proposed two-switching-cycle algorithm can work properly in the real-time implementation.

IV. Simulation Results

Simulations were performed using MATLAB to verify the effectiveness of the proposed two-switching-cycle compensation algorithm. The parameters of the buck converter are listed as follows: input voltage $V_{\rm in} = 5$ V, output voltage $V_o = 2.5$ V, rated load power = 25 W, $L = 1$ μH, $C = 235$ μF, ESR = 1 mΩ, and $R_L = 2$ mΩ. The switching frequency/sampling frequency f_s is 390.6 kHz.

The proposed algorithm was tested against a digitally implemented current-mode PID controller. Although numerous controllers for dc–dc converters exist, a comparison was made with a current-mode controller because it is most frequently used in voltage regulator module (VRM) applications and produces superior results over voltage-mode control.

A block diagram of the current-mode PID controller is illustrated in Fig. 6. The current-mode PID controller is composed of two loops: an outer loop (voltage loop) and an inner loop (current loop). The z-domain transfer functions of the outer PID loop and the inner PI loop are expressed in (26) and (27), respectively. The PID controller was designed in the frequency domain with a bandwidth of 70 kHz and a phase margin of 50°. In order to ensure stability of the current-mode PID controller, the sampling delay is compensated. The sampling delay does not affect the stability of the proposed large-signal algorithm

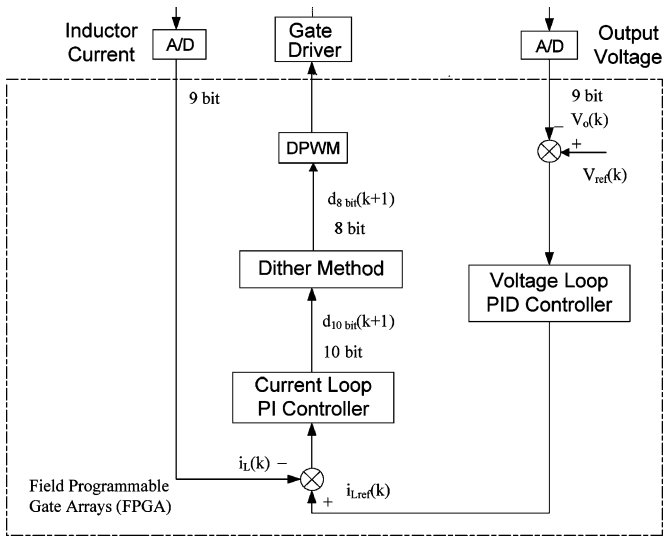

Fig. 6. Block diagram of current-mode PID controller.

$$G(z) = \frac{42.26 - 49.56z^{-1} + 8.82z^{-2}}{1 - z^{-1}} \tag{26}$$

$$G(z) = \frac{0.0856 - 0.078z^{-1}}{1 - z^{-1}}. \tag{27}$$

In the experiment, a 9-bit A/D converter is used to sense the output voltage with a range of 0–4 V. Therefore, the resolution of the A/D converter is 4 V/512 = 7.8 mV. Similarly, in the simulation, the LSB of the sensed output voltage is set to 7.8 mV.

To verify the proposed algorithm under 5–7.5 V and 7.5–5 V, input-voltage step changes were simulated on a buck converter (shown in Figs. 7–9).

Fig. 7 illustrates the output-voltage response of the buck converter when the input voltage changes from 5 to 7.5 V in 20 μs with a 5-A load current. It is shown in Fig. 7(a) that using the current-mode PID controller, the overshoot of the output voltage is 40 mV, and the recovery time is approximately 50 μs after the input voltage stabilizes. Fig. 8 shows the output-voltage response of the buck converter when the input voltage changes from 5 to 7.5 V in 20 μs with no load. It can be observed from Fig. 8(a) that by using the current-mode PID controller, the overshoot of the output voltage is 62 mV and the recovery time is 110 μs after the input voltage stabilizes. Fig. 9 illustrates the output-voltage response of the buck converter when the input voltage changes from 7.5 to 5 V in 40 μs with a 5-A load current. It is shown in Fig. 9(a) that by using the current-mode PID controller, the undershoot is 32 mV and the recovery time is 40 μs after the input voltage stabilizes.

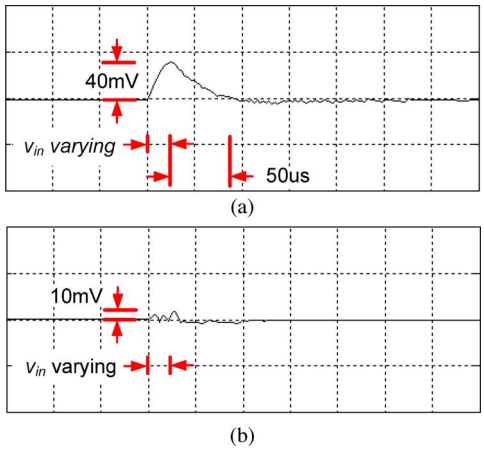

Fig. 7. Simulation result of output-voltage response to input-voltage change from 5 to 7.5 V when load current is 5 A (X-axis (time): 40 μs/division; Y-axis (output voltage): 50 mV/division). (a) Current-mode PID controller. (b) Proposed compensation algorithm.

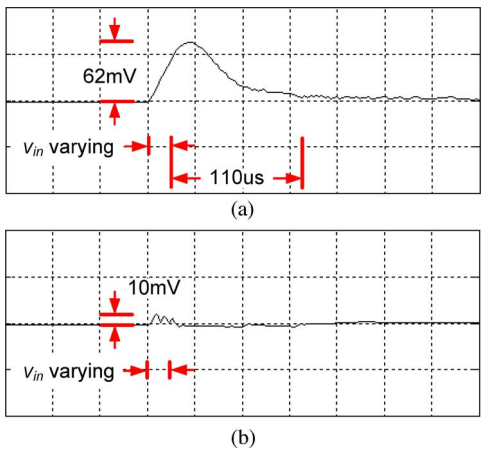

Fig. 8. Simulation result of output-voltage response to input-voltage change from 5 to 7.5 V when load current is 0 A (X-axis (time): 40 μs/division; Y-axis (output voltage): 50 mV/division). (a) Current-mode PID controller. (b) Proposed compensation algorithm.

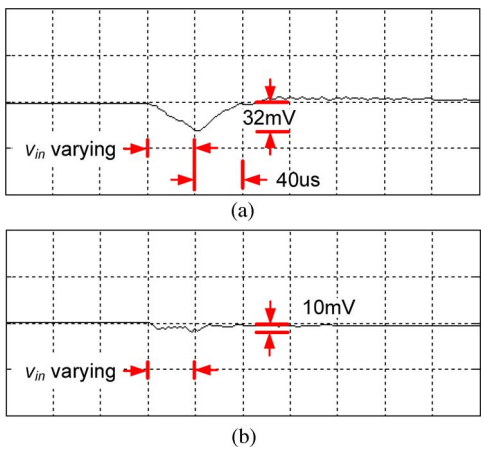

Fig. 9. Simulation result of output-voltage response to input-voltage change from 7.5 to 5 V when load current is 5 A (X-axis (time): 40 μs/division; Y-axis (output voltage): 50 mV/division). (a) Current-mode PID controller. (b) Proposed compensation algorithm.

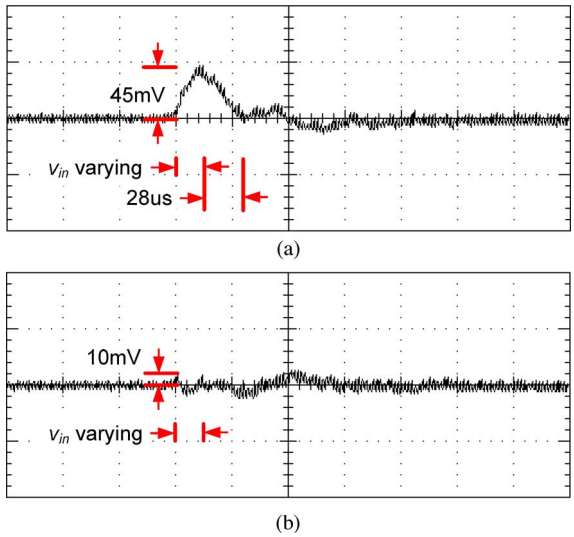

Fig. 10. Experimental result of output-voltage response to input-voltage change from 5 to 7.5 V when load current is 5 A (X-axis (time): 40 μs/division; Y-axis (output voltage): 50 mV/division). (a) Current-mode PID controller. (b) Proposed compensation algorithm.

However, using the proposed two-switching-cycle compensation algorithm, the magnitude of the overshoot/undershoot during the entire transient is always less than 10 mV (shown in Figs. 7(b), 8(b), and 9(b), respectively).

Simulation results show that the proposed algorithm has significantly improved the transient performance of the buck converter undergoing an input-voltage change.

V. Experimental Results

In the experiments, a buck converter with the proposed two-switching-cycle algorithm was built to verify functionality. The parameters of the buck converter, the compensation algorithm, and the current-mode PID controller are identical to those used in the simulation. In the experiment, a Xilinx field-programmable gate array (FPGA) was used. The digitally implemented PID current-mode controller requires approximately 10 000 gates. For the proposed algorithm, the gate number was approximately 150 000 gates. It should be noted that 12-bit arithmetic was used in the FPGA design in order to prove the concept. Since only large signal deviations are considered, 8-bit arithmetic should be adequate for practical implementation. In this implementation, the computationally intensive arithmetic operations (such as division and square-root operations) were performed using lookup tables in order to increase calculation speed. By reducing the operations to 8-bit arithmetic, the lookup tables will significantly decrease in size, reducing the number of gates required. By using 8-bit arithmetic and lookup tables, it is estimated that less than 50 000 gates would be required to implement the control algorithm with an FPGA. It is noted that with an application-specific IC (ASIC) design, further gate number reduction can be achieved. It is estimated that the control algorithm can be implemented with 20 000 gates using ASIC technology.

Fig. 10 illustrates the experimental results of the output-voltage response when the input voltage changes from 5 to

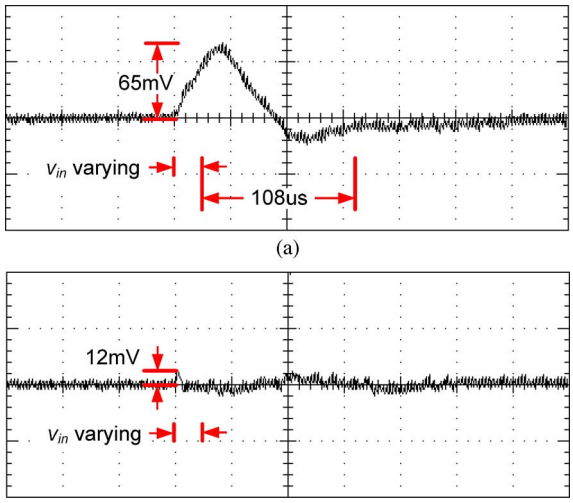

Fig. 11. Experimental result of output-voltage response to input-voltage change from 5 to 7.5 V when load current is 0 A (X-axis (time): 40 μs/division; Y-axis (output voltage): 50 mV/division). (a) Current-mode PID controller. (b) Proposed compensation algorithm.

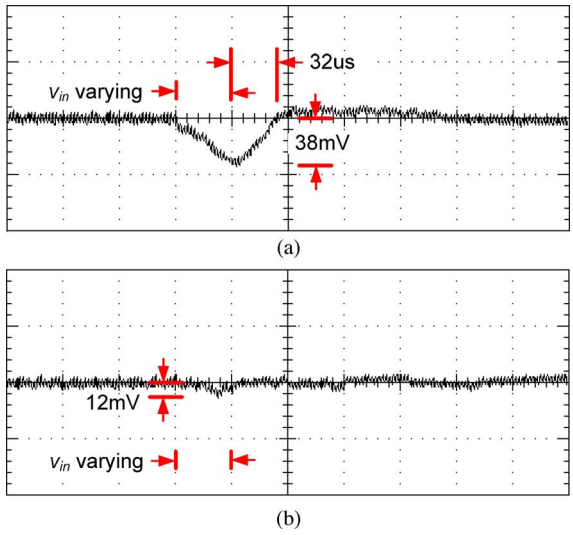

Fig. 12. Experimental result of output-voltage response to input-voltage change from 7.5 to 5 V when load current is 5 A (X-axis (time): 40 μs/division; Y-axis (output voltage): 50 mV/division). (a) Current-mode PID controller. (b) Proposed compensation algorithm.

7.5 V in 20 μs with a 5-A load current. It is shown in Fig. 10(a) that using the current-mode PID controller, the overshoot of the output voltage is 45 mV and the recovery time is 28 μs after the input voltage stabilizes. Fig. 11 shows the experimental results of the output-voltage response when the input voltage changes from 5 to 7.5 V in 20 μs with no load. It can be observed from Fig. 11(a) that using the current-mode PID controller, the overshoot is 65 mV and the recovery time is 108 μs after the input voltage stabilizes. Fig. 12(a) illustrates the experimental results of the output-voltage response when the input voltage changes from 7.5 to 5 V in 40 μs with a 5-A load current. It is shown in Fig. 12(a) that using the current-mode PID controller, the undershoot of the output voltage is 38 mV and the recovery time is 32 μs after the input voltage stabilizes.

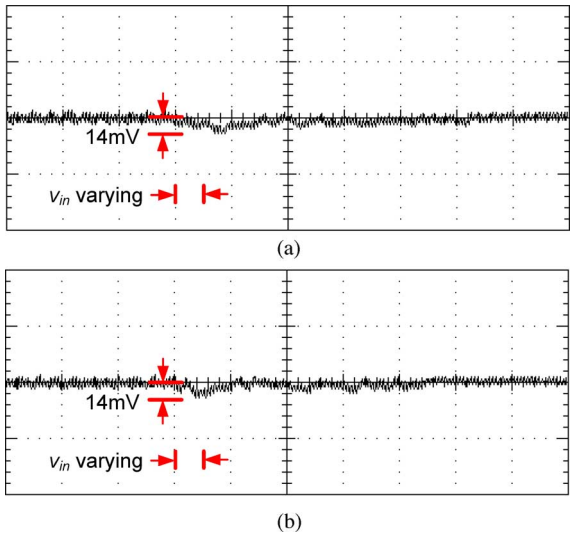

Fig. 13. (a) L: nominal, C: $+20\%$, (b) L: nominal, C: -20%.

However, using the proposed two-switching-cycle compensation algorithm, the overshoot/undershoot during the entire transient period is always less than 12 mV [shown in Figs. 10(b)–12(b)]. The recovery time is also significantly shorter than that of the current-mode PID controller.

Comparing Figs. 10–12 with Figs. 7–9, it can be observed that the simulation results are very close to the experimental results.

It can be observed in Figs. 10–12 that following the switchover from the proposed compensation algorithm to the current-mode PID controller, a small oscillation is observed. Although the proposed algorithm minimizes switchover effects by estimating the new duty cycle and inductor current states, the previous states required by the PID controller may not be accurate. Thus, a small oscillation may occur; however, it is observed that the oscillation is equal to or less than the initial output-voltage deviation caused by the input-voltage transient.

Considering the influence of parameter variations on the performance of the proposed two-switching-cycle compensation algorithm, experiments were conducted to verify the robustness of the proposed algorithm under different capacitor and inductor values. Usually, a $\pm 20\%$ tolerance of L- and C-values can be guaranteed. Therefore, the capacitor or inductor value was increased or decreased by 20%, and the same input-voltage change was performed on the buck converter.

Fig. 13 illustrates the output-voltage response to an input-voltage change from 7.5 to 5 V under different C-values. Table I summarizes the overshoot/undershoot of the proposed algorithm (for different values of L and C) and the current-mode PID controller. It can be observed from Fig. 13 and Table I that the proposed algorithm can still achieve excellent dynamic performance even when the parameters of the buck converter are ill-defined. The maximum overshoot/undershoot during the input-voltage change is still less than 15 mV when the input voltage is changed from 5 to 7.5 V and when the input voltage is changed from 7.5 to 5 V. Therefore, it can be concluded that

TABLE I
EXPERIMENTAL RESULTS OF THE TWO-SWITCHING-CYCLE COMPENSATION ALGORITHM AND THE CURRENT-MODE PID CONTROLLER UNDER INPUT-VOLTAGE CHANGE

Control algorithm	Parameter value		Vin changes from 5V to 7.5V (Io=5A)	Vin changes from 7.5V to 5V (Io=5A)
	L	C	Δvo (mv)	Δvo (mv)
Two switching cycle compensation algorithm	nominal	nominal	11	-12
	nominal	-20%	12	-14
	nominal	+20%	11	-14
	-20%	nominal	12	-15
	+20%	nominal	15	-13
Current mode PID controller	nominal	nominal	45	-38

poorly defined parameters will degrade performance slightly but still allow the algorithm to function.

The aforementioned experimental results verify that compared with the current-mode PID controller, proposed two-switching-cycle compensation algorithm yields significantly improved dynamic performance, such as smaller overshoot/undershoot and shorter recovery time following an input-voltage change. In addition, the proposed compensation algorithm can still maintain good dynamic performance under $\pm 20\%$ range of L, C parameter change.

VI. CONCLUSION

In this paper, a new two-switching-cycle compensation algorithm is proposed to achieve excellent dynamic performance of dc–dc converters undergoing an input-voltage change. Based on the concept of capacitor charge balance, two duty cycles are predicted in advance to drive the buck converter to steady state with minimal voltage deviation and recovery time.

The proposed compensation algorithm is tested on a synchronous buck converter. Simulation and experimental results demonstrate that the voltage deviation, due to a rapid input-voltage change, was reduced by more than 68% over that of a digital current-mode PID controller in all test cases. Results also show a significant decrease in settling time in all cases. While the proposed algorithm relies on output filter information of the converter, experimental results confirm that the controller still yields favorable results when the converter parameters are poorly defined.

The proposed algorithm is very effective for converters undergoing a rapid input-voltage change. Since the algorithm is digital, the combining of the proposed algorithm with a nonlinear digital controller specified to handle load transients (as presented in [25]) is rather straightforward and will yield a converter with excellent dynamic response to an arbitrary transient event.

REFERENCES

[1] S. B. Arbetter and D. Maksimovic, "DC–DC converter with fast transient response and high efficiency for low-voltage microprocessor loads," in *Proc. IEEE 13th Annu. Appl. Power Electron. Conf. Expo. (APEC 1998)*, vol. 1, pp. 156–162.

[2] C. Song and J. L. Nilles, "Accuracy analysis of hysteretic current-mode voltage regulator," in *Proc. IEEE 20th Annu. Appl. Power Electron. Conf. Expo. (APEC 2005)*, vol. 1, pp. 276–280.

[3] M. Castilla, L. G. de Vicuna, J. M. Guerrero, J. Miret, and N. Berbel, "Simple low-cost hysteretic controller for single-phase synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1232–1241, Jul. 2007.

[4] J. Abu-Qahouq, H. Mao, and I. Batarseh, "Multiphase voltage-mode hysteretic controlled DC–DC converter with novel current sharing," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1397–1407, Nov. 2004.

[5] J. Zhao, T. Sato, T. Nabeshima, and T. Nakano, "Steady-state and dynamic analysis of a buck converter using a hysteretic PWM control," in *Proc. IEEE 35th Power Electron. Spec. Conf. (PESC 2004)*, vol. 5, pp. 3654–3658.

[6] J. Sun, "Characterization and performance comparison of ripple-based control methods for voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 21, pp. 346–353, Mar. 2006.

[7] C.-Y. Chan, "A nonlinear control for DC–DC power converters," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 216–222, Jan. 2007.

[8] P. Krein, "Chapter 8: Nonlinear control and control of chaos in PE circuits," in *Nonlinear Phenomena in Power Electronics: Attractors, Bifurcations, Chaos, and Nonlinear Control*, S. Banerjee and G. C. Verghese, Eds. Piscataway, NJ: IEEE Press, 2001.

[9] G. Spiazzi and P. Mattavelli, "Chapter 8: Sliding-mode control of switched-mode power supplies," in *The Power Electronics Handbook*, T. L. Skvarenina, Ed. New York: CRC, 2002.

[10] S.-C. Tan, Y. M. Lai, C. K. Tse, and M. K. H. Cheung, "A fixed-frequency pulsewidth modulation based quasi-sliding-mode controller for buck converters," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1379–1392, Nov. 2005.

[11] S.-C. Tan, Y. M. Lai, C. K. Tse, and M. K. H. Cheung, "Adaptive feedforward and feedback control schemes for sliding mode controlled power converters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 182–192, Jan. 2006.

[12] M. Ilic and D. Maksimovic, "Digital average current-mode controller for DC–DC converters in physical vapor deposition applications," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1428–1436, May 2008.

[13] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2552–2556, Nov. 2007.

[14] S. Saggini, D. Trevisan, P. Mattavelli, and M. Ghioni, "Synchronous-asyncrhonous digital voltage-mode control for DC–DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1261–1268, Jul. 2007.

[15] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, "Modeling of quantization effects in digitally controlled DC–DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 208–215, Jan. 2007.

[16] S. Chattopadhyay and S. Das, "A digital current-mode control technique for DC–DC converters," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1718–1726, Nov. 2006.

[17] D. M. V. de Sype, K. D. Gusseme, F. M. L. L. D. Belie, A. P. V. de Bossche, and J. A. Melkebeek, "Small-signal z-domain analysis of digitally controlled converters," *IEEE Trans. Power Electron.*, vol. 21, pp. 470–478, Mar. 2006.

[18] A. R. Oliva, S. S. Ang, and G. E. Bortolotto, "Digital control of a voltage-mode synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 157–163, Jan. 2006.

[19] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 301–308, Jan. 2003.

[20] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC–DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.

[21] Y. Duan and H. Jin, "Digital controller design for switchmode power converters," in *Proc. IEEE 14th Annu. Appl. Power Electron. Conf. Expo. (APEC 1999)*, vol. 2, pp. 967–973.

[22] A. Barrado, A. Lazaro, R. Vazquez, V. Salas, and E. Olias, "The fast response double buck DC–DC converter (FRDB): Operation and output filter influence," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1261–1270, Nov. 2005.

[23] M. Shi, J. Sun, and P. Enjeti, "A dual-loop digital controller for switching DC–DC converters," in *Proc. IEEE 28th Annu. Int. Telecommun. Energy Conf. (INTELEC 2006),* sec. 29, 2009, pp. 1–5.

[24] Z. Zhao and A. Prodic, "Continuous-time digital controller for high-frequency DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 564–373, Mar. 2008.

[25] G. Feng, E. Meyer, and Y.-F. Liu, "A new digital control algorithm to achieve optimal dynamic performance in DC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1489–1498, Jul. 2007.

[26] E. Meyer, Z. Zhang, and Y.-F. Liu, "An optimal control method for buck converters using a practical capacitor charge balance technique," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1802–1812, Jul. 2008.

[27] M. Oronez, M. T. Iqbal, and J. E. Quaicoe, "Selection of a curved switching surface for buck converters," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1148–1153, Jul. 2006.

[28] K. K. S. Leung and H. S. H. Chung, "Derivation of a second-order switching surface in the boundary control of buck converters," *IEEE Power Electron. Lett.*, vol. 2, no. 2, pp. 63–67, Jun. 2004.

[29] K. K. S. Leung and H. S. H. Chung, "A comparative study of boundary control with first- and second-order switching surfaces for buck converters operating in DCM," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1196–1209, Jul. 2007.

[30] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao, and D. Maksimovic, "Proximate time-optimal digital control for synchronous buck DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2018–2026, Jul. 2008.

Guang Feng (S'98–M'05) received the B.Sc. degree in electrical engineering from Tsinghua University, Beijing, China, in 1995, and the Ph.D. degree in power electronics from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2005.

Since August 2005, he has been an Assistant Power Electronics Engineer at Argonne National Laboratory, Argonne, IL. His current research interests include analog/digital control of switching power converters, power factor correction techniques, adjustable-speed motor drives, and high power ac/dc, dc/dc converters.

Eric Meyer (S'06) received the B.Sc. degree in 2005 from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, where he is currently working toward the Ph.D. degree.

His current research interests include novel topologies and control methods to improve the dynamic response of voltage regulator module devices. He has one patent pending, and has authored nine technical papers in conferences and IEEE journals.

Mr. Meyer has been awarded a Natural Sciences and Engineering Research Council (NSERC) scholarship.

Yan-Fei Liu (S'91–M'95–SM'97) received the B.Sc. and M.Sc. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1984 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

From February 1994 to July 1999, he was a Technical Advisor with the Advanced Power System division, Astec (formerly Nortel Networks), where he was responsible for high-quality design, new products, and technology development. Since August 1999, he has been an Associate Professor in the Department of Electrical and Computer Engineering, Queen's University. His current research interests include digital control technologies for dc–dc switching converter and ac–dc converter with power factor correction, electromagnetic interference (EMI) filter design methodologies for switching converters, topologies and controls for high switching frequency, low switching loss converters, modeling and analysis of core loss and copper loss for high-frequency planar magnetics, topologies and control for voltage regulator module (VRM), and large-signal modeling of switching converters.

Prof. Liu is was the winner of Premiere's Research Excellent Award (PREA) in 2001, the Golden Apple Teaching Award in 2000, both from Queen's University, and the 1997 Award in Excellence in Technology from Nortel.