An Optimal Control Method for Buck Converters Using a Practical Capacitor Charge Balance Technique

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***Abstract*—A novel control method is presented in this paper which utilizes the concept of capacitor charge balance to achieve optimal dynamic response for Buck converters undergoing a rapid load change. The proposed charge balance method is implemented with analog components and is cheaper and more effective than its digital counterparts since complex arithmetic and sampling delay is eliminated. The proposed controller will consistently cause the Buck converter to recover from an arbitrary load transient with the smallest possible voltage deviation in the shortest possible settling time. Since the controller is nonlinear during transient conditions, it is not limited by bandwidth/switching frequency. Unlike conventional linear controllers, the dynamic response (voltage deviation, settling time) of the proposed controller can be estimated using a set of equations. This greatly simplifies the design process of the output filter. Simulation and experimental results show the functionality of the controller and demonstrate the superior dynamic response over that of a conventional linear controller.**

***Index Terms*—Capacitor charge balance, dc–dc converters, load transient response, nonlinear control.**

I. Introduction

TRADITIONALLY, linear analog controllers (such as voltage-mode and current-mode schemes) have been utilized to control Buck converters. These controllers offer benefits such as zero steady-state error and predictable switching frequency. However, the dynamic response of linear controllers is limited by their bandwidth. Therefore, numerous alternative controllers have been proposed to overcome bandwidth limitations.

Various hysteretic based controllers have been presented in [1]–[6] which are designed to improve the dynamic response of a Buck converter. A hysteretic controller, based on the output inductor current, is presented in [1]. This type of controller is capable of improving dynamic response by eliminating the need of compensation circuitry. Without the compensator, the bandwidth of the converter is significantly improved. Unfortunately, hysteretic current-mode controllers operate at unpredictable frequencies making electromagnetic compatibility (EMC) design difficult. Furthermore, it is shown in [2] that due to nonidealities of the output capacitor [equivalent series resistance (ESR) and equivalent series inductance (ESL)] combined with the inherent delay of hysteretic comparators, the steady-state error of current-mode hysteretic converters can be significant. While a current-mode hysteretic converter with adjustable frequency is presented in [3], the steady-state frequency can still vary by over 30% dependant on load conditions.

Output voltage ripple hysteretic controllers are presented in [4]–[6]. Like current-mode hysteretic controllers, these controllers improve the dynamic response but are much more intuitive and simpler to implement. Unfortunately, they all possess at least one of the following undesired attributes: 1) Variable switching frequency, 2) nonzero steady-state error, and 3) operating frequencies largely dependant on the equivalent series resistance (ESR) of the output capacitor.

Several nonlinear controllers which produce a more desirable response during transients are presented in [7]–[11]. In [7], a nonlinear controller scheme is presented that can be applied to Buck and Boost converters. While the output response can be improved using [7], the controller requires an exponential function. The exponential circuit increases the complexity of the controller and limits its speed.

In [8]–[11], nonlinear sliding-mode controllers are presented. Traditionally, a large drawback of sliding-mode control is its variable frequency. In [10], [11], sliding-mode controllers with low/no frequency variation are presented. However, these controllers still suffer from nonzero steady-state error. Furthermore, [11] requires a division and a multiplication block along with series resistance sensors for the capacitor current and load current, making the controller infeasible for many VRM applications.

An ideal Buck controller would behave linearly during steady-state conditions for tight voltage regulation and behave nonlinearly during transient conditions for fast response. It is demonstrated in [12]–[16] that by employing two separate controllers for steady-state operation and for transient operation, the dynamic response can be significantly improved while not sacrificing steady-state accuracy. In [12], two linear controllers are utilized: a compensator with high dc gain and lower bandwidth for steady-state conditions and a high bandwidth compensator for transient conditions. While this method improves dynamic performance, the controller still suffers from traditional bandwidth limitations. In [13]–[15], control methods are presented which utilize a linear control scheme during steady-state conditions and saturate the duty cycle to either 0% or 100% when a load transient occurs. While these methods effectively reduce voltage deviation caused by load

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transients, imprecise timing of the saturation period leads to sub-optimal settling times in most cases. In [16], a combined linear/nonlinear control method is provided which saturates the duty cycle for a precise period to minimize the settling time of output voltage transients due to varying reference voltages. While this method is effective, little investigation was conducted regarding the controller's response to load transients.

It has been presented in [17] and [18], that to an arbitrary external disturbance, there exists an "optimal response" for a Buck converter. The optimal response is such that the settling time and voltage deviation would be reduced to its minimum possible value. While the response and theory is studied in these papers, no practical implementation of a controller is described.

In [19], a method is presented to design a linear controller that attempts to mimic the optimal response. While this controller can produce near-optimal results, it is impossible for a linear controller to accurately achieve the desired optimal response since the response is, in fact, nonlinear. In [20], a digital controller is presented which attempts to achieve the optimal response through fuzzy-logic approximation. Although the nonlinear fuzzy-logic approach is better suited than the linear approximation, the response is still sub-optimal. In [21], a near-optimal response is achieved by using a digital output capacitor estimator and a simple linear switching surface. However, in order to achieve a true optimal response, a nonlinear switching surface is required.

In [22]–[24] second-order switching surface controllers are designed to achieve the optimal response to an external disturbance. However, for [23], [24], an analog multiplier is utilized in the control scheme which is expensive and significantly limits the speed of the controller. In order to utilize the controller, the switching speed of the converter was set to 20 kHz.

In [25] and [26], equations to determine the optimal response to a disturbance are presented for Boost and Buck converters respectively. In [25], the derived equations are used in MATLAB simulation to drive a Boost converter with optimal dynamic performance; however, the paper does not provide information regarding practical hardware implementation. In [26], the optimal response, to a large range of disturbances, is calculated using MATLAB offline and programmed into a digital controller. The controller successfully achieves a minimal, predictable settling time to an external disturbance. Unfortunately, the controller is only functional in open-loop configuration. The time instant when the disturbance occurs and the magnitude of the load variation must be defined in advance, which is an impossible situation for most Buck converter applications.

In [27]–[29], digital controllers are presented which can calculate the optimal response to an arbitrary load variation "on-the-fly". The controllers significantly improve the dynamic response of a converter undergoing a fast load transition. However, the controllers perform multiplication, division and square-root operations resulting in costly implementation. Furthermore, it is determined that the response of [27]–[29] could further be improved if the initial load transient detection delay were eliminated.

In this paper, a novel analog controller is presented which causes a Buck converter to achieve a virtually optimal dynamic response, yet can be implemented using a low-cost analog scheme. The proposed controller does not require multipliers or dividers to achieve the desired response. The proposed controller can be implemented using only simple OPAMP mathematical functions (such as addition, subtraction, integration, etc.). Since the controller is analog, the sampling delay is removed resulting in faster reaction to a transient event than that of [27]–[29]. As some recent VRM drivers utilize diode emulation to operate in discontinuous current mode (DCM) in order to boost light-load efficiency, the controller is capable of operation in continuous current mode (CCM) and DCM. The controller utilizes a linear loop during steady-state operation to achieve fixed frequency and zero steady-state error and utilizes a nonlinear loop for optimal dynamic performance during load transient conditions. Section II describes the general concept of the controller, Section III derives the equations necessary to achieve the optimal dynamic response and Section IV describes the step-by-step operation of the proposed controller. Section V derives the estimated voltage deviation and settling time of a converter under the proposed control method. Section VI and Section VII contain simulation and experimental results, respectively. Section VIII provides a brief conclusion.

II. Controller Concept

The principle of capacitor charge balance has been utilized extensively for the purpose of steady-state modeling and analysis of dc–dc converters. The principle of capacitor charge balance states that, in steady state, the average of the capacitor current over one switching period must be equal to zero. This condition must be satisfied in order for the output voltage to be equal at the beginning and the end of a switching cycle. Equation (1) represents the principle of capacitor charge balance for a Buck converter under steady state

$$v_c(T_s) - v_c(0) = \frac{1}{C} \cdot i_{cavg} = 0 \rightarrow \frac{1}{T_s} \int_0^{T_s} i_c(t)dt = 0 \quad (1)$$

where v_c is the capacitor voltage (neglecting ESR and ESL), i_c is the capacitor current, C represents the output capacitor value and T_s is the switching period of the converter. By recognizing that the integral period of (1) may be extended over the total transient time of a dc–dc converter, (2) is developed

$$v_c(t_b) - v_c(t_a) = \frac{1}{C} \cdot i_{cavg} = 0 \rightarrow \frac{1}{t_b - t_a} \int_{t_a}^{t_b} i_c(t)dt = 0 \quad (2)$$

where t_a represents the beginning of the transient period and t_b represents the end of the transient period. Thus, if at t_b the inductor current i_L equals the load current and (2) has been satisfied, the output voltage will have returned to its reference voltage and, therefore, the converter has recovered from the transient event. This concept can be used to minimize the voltage deviation and settling time of a converter undergoing a load current step change.

A. Minimize Voltage Deviation

Referring to Fig. 1, immediately following a positive load current step, the inductor current cannot change instantaneously to supply the load. Therefore, a portion of the load current must be supplied by the output capacitor. This, in turn, causes the output capacitor to lose charge and causes the output voltage to decrease. The output capacitor will finish discharging when the

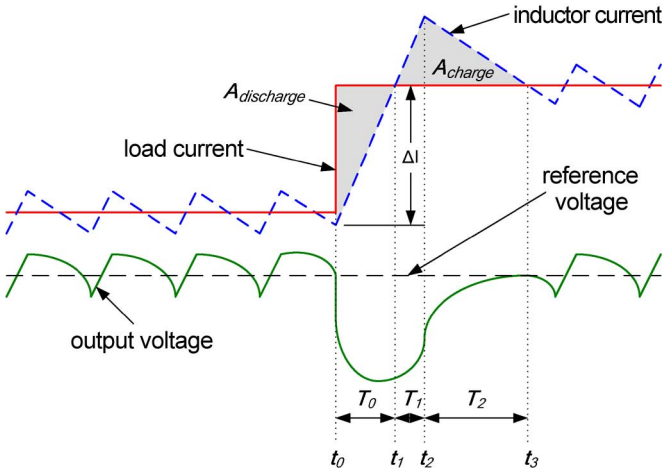

Fig. 1. Proposed controller response to a positive load current step.

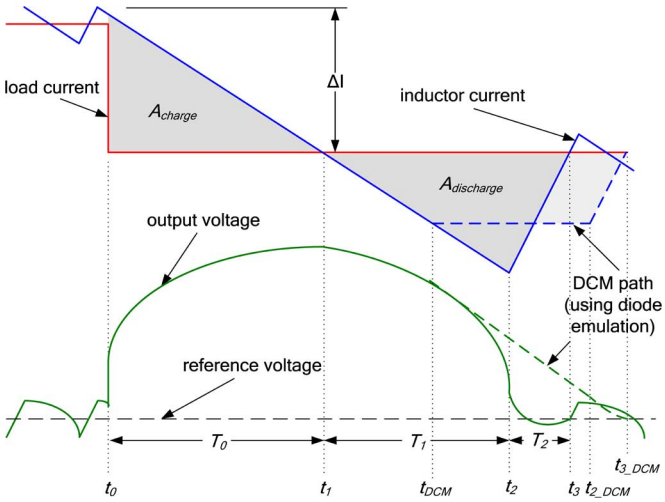

Fig. 2. Proposed controller response to a negative load current step.

inductor current reaches the new load current (at t_1). In order to minimize the output voltage undershoot, the inductor current must be allowed to increase at its maximum slew rate (PWM = high) for T_0.

Referring to Fig. 2, following a negative load current step, the capacitor must absorb the excess inductor current until it equals the new load current (at t_1). This causes the capacitor to charge and causes the output voltage to increase. In order to minimize the output voltage overshoot, the inductor current must be allowed to decrease at its maximum slew rate (PWM = low) for T_0.

B. Minimize Settling Time

Referring to Fig. 1, the output capacitor will start to recharge and the output voltage increase when the inductor current begins to exceed the new load current. In order to minimize the time required to recharge the capacitor, the PWM will remain high for T_1. At t_2, the PWM will be set low causing the inductor current to decrease at its maximum slew rate. t_2 should be such that at the instant that the inductor current returns to the new load current (at t_3), $A_{\text{discharge}}$ equals A_{charge}. The calculation of t_2 is critical to ensure that the settling time is minimized and to ensure the output voltage does not overshoot the reference voltage

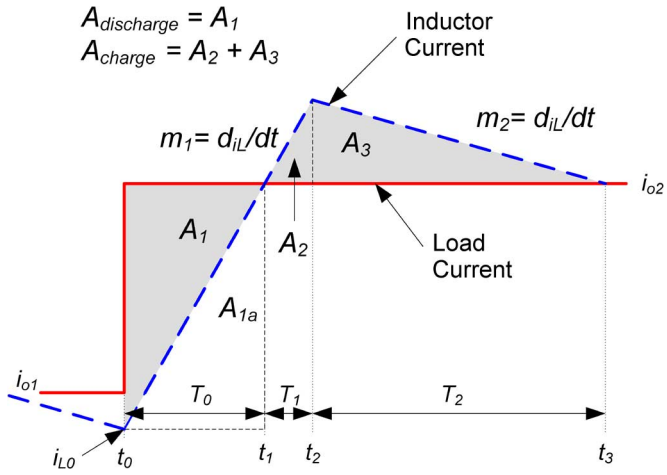

Fig. 3. Proposed inductor current response to a positive load step.

after the voltage dip. Assuming t_2 was determined correctly, at t_3, the output voltage and the inductor current will reach their steady-state values simultaneously and the converter will have fully recovered from the positive load step.

Referring to Fig. 2, for a negative load step, the PWM will remain low for T_1 in order to minimize the time required to remove the necessary charge from the capacitor. At t_2, the PWM will be set high causing the inductor current to increase at its maximum slew rate. As above, t_2 should be such that at the instant that the inductor current returns to the new load current (at t_3), $A_{\text{discharge}}$ equals A_{charge}. Fig. 2 depicts a negative load current step for a continuous current mode (CCM) controller and a discontinuous current mode (DCM) controller.

In summary, the two key points of the proposed control method are as follows.

1) Immediately detect the load current step change and react by setting the PWM to high (for a positive step change) or to low (for a negative step change).
2) Set the PWM low (for a positive load step) or high (for a negative load step) at t_2. t_2 should be such that A_{charge} will equal $A_{\text{discharge}}$ at time t_3. This will cause the output voltage to equal the reference voltage at the exact moment that the inductor current equals the load current.

III. Mathematical Analysis of the Proposed Controller Response

Fig. 3 illustrates the charge and discharge areas for a positive load current step change. The controller is designed for applications in which the load current slew rate is significantly larger than the inductor current slew rates. Therefore, in this analysis, it is assumed that the load current steps rapidly from i_{o1} to i_{o2} and that the controller is able to react to the step with negligible delay. It is also assumed that the load current remains constant for the duration of the transient period.

Time Period T_0: It is apparent in Fig. 3, that the total discharge area A_1 is equal to A_{1a}, thus (3) is true

$$A_1 = \int_{t0}^{t1} [i_{o2} - i_L(t)]\,dt = A_{1a} = \int_{t0}^{t1} [i_L(t) - i_{L0}]\,dt \quad (3)$$

m_1 represents the rate at which $i_L(t) - i_{L0}$ is increasing, such that (4) and (5) are true

$$m_1 = \frac{d\left[i_L(t) - i_{L0}\right]}{dt} \tag{4}$$

$$i_L(t) - i_{L0} = \int_{t0}^{t} m_1 dt. \tag{5}$$

Therefore, by combining (3) and (5), the total discharge area $A_{\text{discharge}}$ can be expressed in

$$A_{discharge} = A_1 = A_{1a} = \iint_{T0} m_1 (dt)^2. \tag{6}$$

Time Period T_1*:* The charge area A_2 is expressed in

$$A_2 = \int_{t1}^{t2} \left[i_L(t) - i_{o2}\right] dt. \tag{7}$$

By inspection, it is obvious that m_1 also represents the rate that $i_L(t) - i_{o2}$ is increasing, as expressed in

$$m_1 = \frac{d\left[i_L(t) - i_{o2}\right]}{dt} \tag{8}$$

$$i_L(t) - i_{o2} = \int_{t1}^{t} m_1 dt. \tag{9}$$

Therefore, by combining (7) and (9), the charge area A_2 can be expressed as

$$A_2 = \iint_{T1} m_1 (dt)^2. \tag{10}$$

Using basic geometry, a relationship for A_2 and A_3 is found in (11), in terms of the rising and falling slew rates of the inductor current

$$\frac{A_3}{A_2} = \frac{m_1}{-m_2}. \tag{11}$$

Thus, by combining (10) and (11), an expression for the total charge area A_{charge} is presented in

$$\begin{aligned} A_{charge} &= A_2 + A_3 = \iint_{T1} m_1 (dt)^2 + \iint_{T1} \frac{m_1^2}{-m_2} (dt)^2 \\ &= \iint_{T1} \frac{m_1 m_2 - m_1^2}{m_2} (dt)^2. \end{aligned} \tag{12}$$

By using (12), it is possible to predict the total charge area at time t_2. In order to satisfy the principle of capacitor charge balance at t_3, (13) must be true

$$\begin{aligned} A_{discharge} - A_{charge} &= 0 \\ \iint_{T0} m_1 (dt)^2 - \iint_{T1} \frac{m_1 m_2 - m_1^2}{m_2} (dt)^2 &= 0 \\ \iint_{T0} (dt)^2 - \frac{m_2 - m_1}{m_2} \iint_{T1} (dt)^2 &= 0. \end{aligned} \tag{13}$$

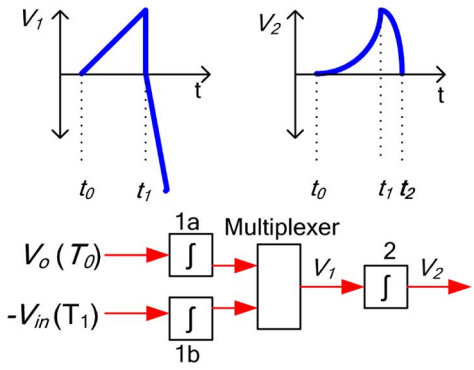

Fig. 4. Proposed double integrator to predict t_2 for positive load current step.

Assuming that the input voltage and the output voltage remain relatively constant during the transient, the inductor current slew rates of a Buck converter are known ($m_1 = (V_{\text{in}} - V_o)/L$; $m_2 = -V_o/L$) and are substituted into (13) to produce (14). A note regarding this assumption is presented after the following analysis:

$$\begin{aligned} \iint_{T0} (dt)^2 - \frac{\frac{-V_o}{L} - \frac{(V_{\text{in}} - V_o)}{L}}{\frac{-V_o}{L}} \iint_{T1} (dt)^2 &= 0 \\ \iint_{T0} (dt)^2 - \frac{V_{\text{in}}}{V_o} \iint_{T1} (dt)^2 &= 0. \end{aligned} \tag{14}$$

Since analog division is costly, the equation is simplified by multiplying V_o to both sides, as expressed in

$$\begin{aligned} A_{discharge} - A_{charge} &= 0 \\ V_o \iint_{T0} (dt)^2 - V_{\text{in}} \iint_{T1} (dt)^2 &= 0. \end{aligned} \tag{15}$$

Using (15), it is possible to use an analog double integrator, to calculate the time t_2 that will allow $A_{\text{charge}} - A_{\text{discharge}}$ to equal zero when the inductor current reaches the new load current (at t_3). The aforementioned concept is illustrated in Fig. 4.

It is apparent that an additional advantage of the aforementioned double integration method is that the nominal value of the output inductor is not required.

In the case of a positive load current step, the PWM would be set low when V_2 equals zero (at time t_2). This will allow the inductor current to fall and reach the output current at the exact moment that the charge previously removed from the capacitor equals the charge delivered to the capacitor.

A similar analysis is performed for a negative load current step change (and a CCM converter). The result of the analysis is expressed in

$$\iint_{T0} m_2 (dt)^2 - \iint_{T1} \frac{m_1 m_2 - m_2^2}{m_1} (dt)^2 = 0 \tag{16}$$

$$\begin{aligned} A_{charge} - A_{discharge} &= 0 \\ (V_{\text{in}} - V_o) \iint_{T0} (dt)^2 - V_{\text{in}} \iint_{T1} (dt)^2 &= 0. \end{aligned} \tag{17}$$

For a negative load current step (and a CCM converter) the double integrator function is depicted in Fig. 5.

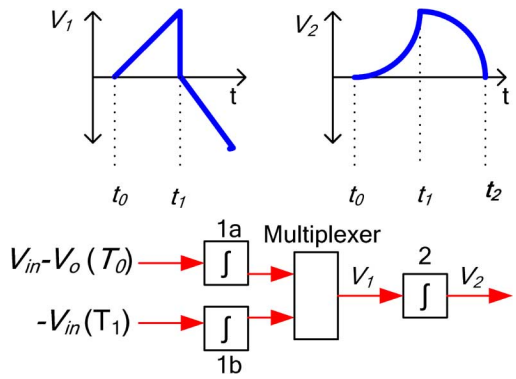

Fig. 5. Proposed double integrator to predict t_2 for negative load current step (CCM converter).

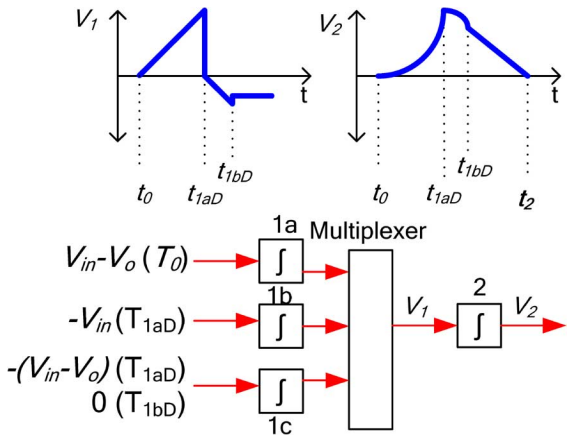

Fig. 6. Proposed double integrator to predict t_2 for negative load current step (DCM converter).

For a negative load current step change (and a DCM converter), the result of the analysis is expressed in (18) and (19). It is assumed that the converter operates with a synchronous MOSFET and uses a "diode emulation" driver to determine when the sync FET is to be deactivated; therefore, no diode drop is accounted for

$$\iint_{T0} m_2(dt)^2 - \iint_{T1aD} \frac{m_1 m_2 - m_2^2}{m_1}(dt)^2 - \int_{T1bD} \left(\int_{T1aD} m_2 dt \right) dt = 0 \tag{18}$$

$$\iint_{T0} (V_{\text{in}} - V_o)(dt)^2 - \iint_{T1aD} V_{\text{in}}(dt)^2 - \int_{T1bD} \left(\int_{T1aD} (V_{\text{in}} - V_o) dt \right) dt = 0. \tag{19}$$

For a negative load current step (and a DCM converter) the double integrator function is depicted in Fig. 6. This analysis is valid for a transient from continuous to discontinuous mode and for a transient from discontinuous to discontinuous mode.

It is noted that m_1 and m_2 will not remain constant in actuality during a load transient due to the varying output voltage. This simplification was made in order to allow for a practical implementation of a charge balance controller. However, the simplification does not degrade the performance significantly due to the following reasons:

1) for a low duty ratio Buck (eg. 12 V to 1.5 V), the undershoot (due to a positive load current step) will be much smaller than the overshoot (due to a negative load current step). Thus, for a properly designed Buck, the output voltage deviation during a positive load transition would be very small;
2) for a negative load transition, the output voltage can vary significantly (typically 10% of the steady-state voltage). However, since the controller's double integrator is fed by (V_{in}) and $(V_{\text{in}} - V_o)$ during a negative load transition, $(V_{\text{in}} - V_o)$ would only vary by approximately 1.5%, causing a very small inaccuracy.

IV. Operation of Proposed Control Method

During steady-state conditions, the controller uses a conventional, linear control scheme (such as voltage-mode control) in order to control the converter. The controller switches from its conventional control scheme to the proposed controller immediately following a load step change. In order to prevent linear loop upsetting during the transient period, the linear control voltage is held constant for the duration of the transient. While it is known that for a practical Buck converter, the steady-state duty cycle is dependant on the load current, the switchover effect due to this is minimal. Fig. 7 illustrates the aforementioned concept.

Fig. 8 illustrates the block diagram of the proposed control method. The operation of the controller and its logic is described below.

The controller operation can be described in 4 steps.

Step 1: Detect Load Current Step Change (T_0)*:* The controller indirectly senses the capacitor current using a noninvasive transimpedance amplifier, connected to the output voltage (as shown in Fig. 8).

When the capacitor current exceeds a predetermined threshold, the controller will immediately set the PWM to high (for a positive load step), or low (for a negative load step). The threshold should be chosen such that it is significantly larger than the steady-state capacitor current ripple to prevent false triggering. Since the controller is designed for relatively large current steps, this is a practical design criterion.

The controller logic will release the "reset" switch of integrator 1a and integrator 2. The output of integrator 1a will begin to increase linearly with a slope of V_o (for a positive step change), or $V_{\text{in}} - V_o$, (for a negative step change). The output of integrator 2 will begin to increase exponentially (see Fig. 9).

Step 2: Detect Capacitor Current Cross-Over (t_1)*:* A comparator, fed by the capacitor current sensor, is used to determine the point at which the capacitor current changes direction. This point indicates that the inductor current has reached the new load current as illustrated in Fig. 9 at point t_1. At this point, integrator 1a will be "reset" and integrator 1b will be activated. The output of integrator 1b will begin to decrease linearly with a slope of $-V_{\text{in}}$. The output of integrator 2 will begin to decrease exponentially, as shown in Fig. 9.

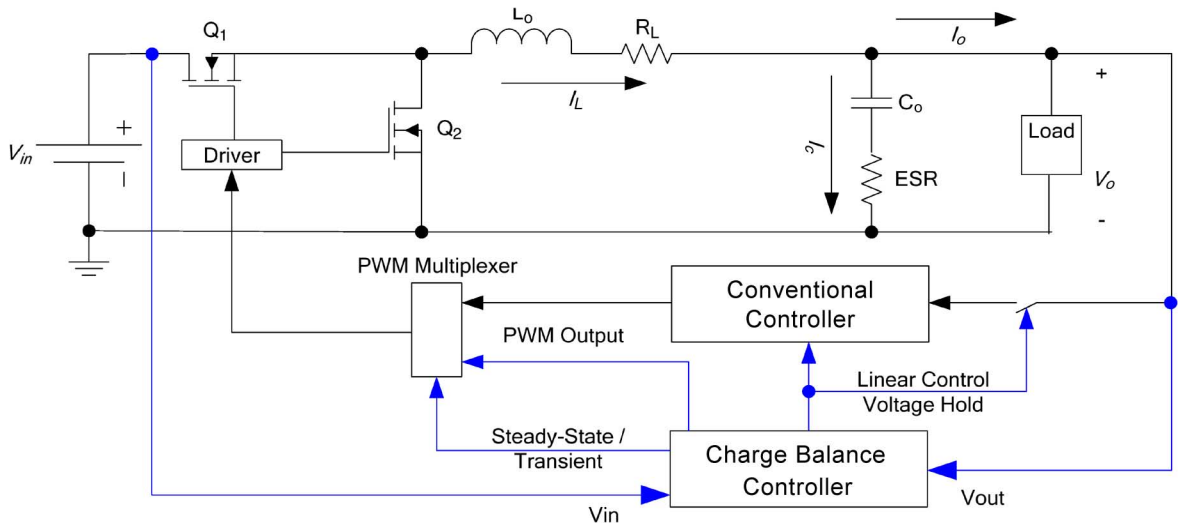

Fig. 7. Steady-state versus transient control of buck converter.

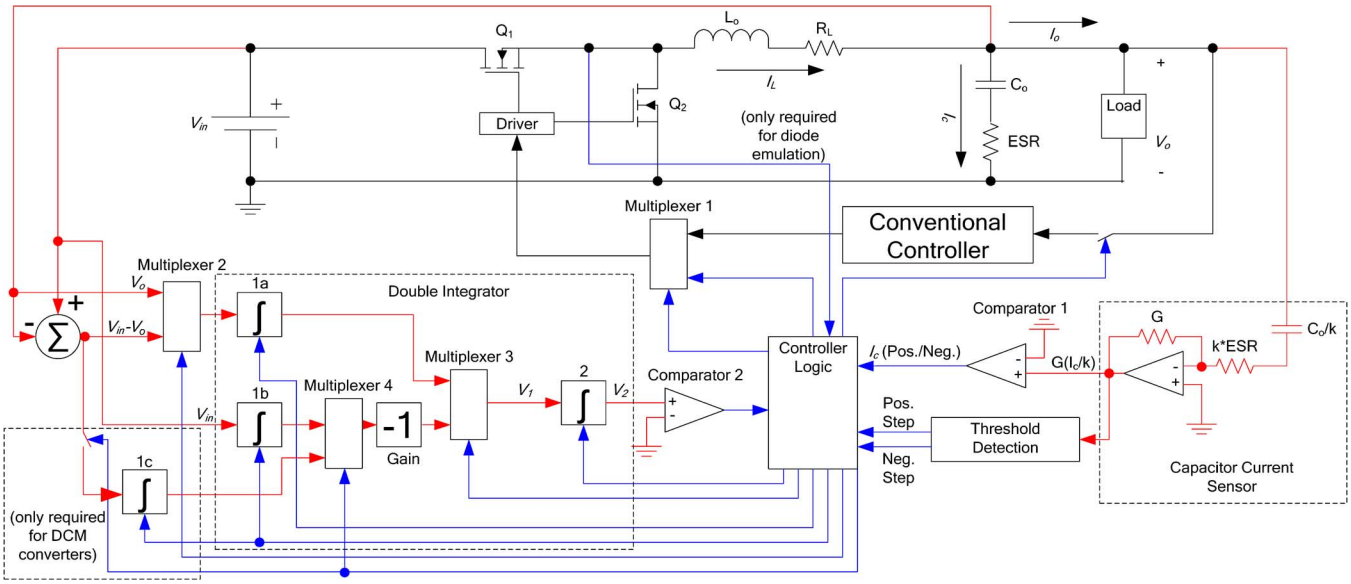

Fig. 8. Block diagram of proposed controller.

Step 2a): Detect DCM (for DCM Converters Undergoing a Negative Current Step Change Only) (t_{DCM})*:* By observing the drain voltage of the synchronous FET while the main FET is off, the moment that the converter enters DCM can be detected. Referring to Fig. 2, this moment is represented by t_{DCM}. At this point, the "hold" switch of integrator 1c is opened and multiplexer 4 is switched to the output of integrator 1c, as per (19). The output of integrator 2 will begin to decrease linearly.

Step 3: Alter PWM State (t_2)*:* At the moment that the output of integrator 2 returns to zero (at t_2), the PWM will be set low (for a positive load step change) or high (for a negative load step change). At this point, the inductor current will be at its maximum (in the case of a positive load step change) or its minimum (in the case of a negative load step change). The inductor current will begin to decrease toward the new load current in the case of a positive load step change. In the case of a negative load step change, the inductor current will begin to increase toward the new load current.

Step 4: De-Activate Controller (t_3)*:* At t_3, the inductor current reaches the new load current (determined by a second capacitor current switchover) and the output voltage returns to its reference value. At this point, the proposed controller deactivates and the conventional controller resumes control of the converter.

The controller operation for a positive load current step change is illustrated in Fig. 9.

V. Analysis of Voltage Deviation and Settling Time

In addition to improving the dynamic performance of a Buck converter, the proposed controller also simplifies the design of the output filter since its response to a large-signal load transient is predictable. It is possible to estimate the dynamic response (settling time, voltage deviation) to a converter experiencing an arbitrary load variation. For simplification, the following analysis assumes a properly designed converter in which the input and output voltage remains relatively constant during the transient period.

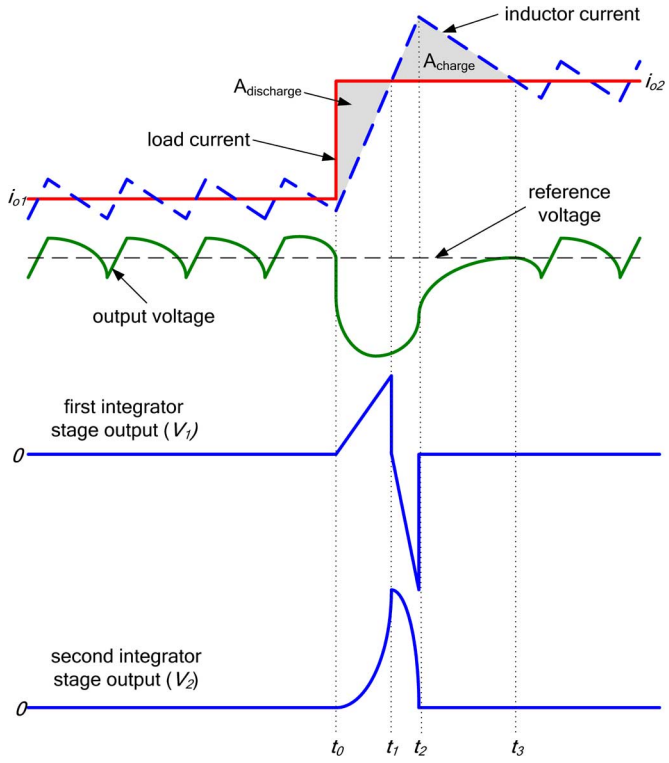

Fig. 9. Controller operation for a positive load current step change.

Referring to Fig. 1, T_0 and $A_{\text{discharge}}$ (for a positive load step) are calculated using

$$T_0 = \Delta I \frac{L}{V_{\text{in}} - V_o} \tag{20}$$

$$A_{discharge} = \frac{1}{2} T_0 \Delta I = \Delta I^2 \frac{L}{2(V_{\text{in}} - V)_o}. \tag{21}$$

For a positive load step, A_{charge} is calculated using

$$A_{charge} = T_1^2 \frac{V_{\text{in}}(V_{\text{in}} - V_o)}{2V_o L}. \tag{22}$$

In order for (2) to be satisfied, $A_{\text{discharge}}$ must equal A_{charge}. Therefore, (21) can be substituted into (22) and T_1 can be isolated as shown in

$$T_1 = \sqrt{\frac{V_o L^2 \Delta I^2}{V_{\text{in}}(V_{\text{in}} - V_o)^2}} = \frac{L\Delta I}{V_{\text{in}} - V_o} \sqrt{\frac{V_o}{V_{\text{in}}}}. \tag{23}$$

A relationship between T_1 and T_2 is defined in

$$T_2 = \frac{V_{\text{in}} - V_o}{V_o} T_1. \tag{24}$$

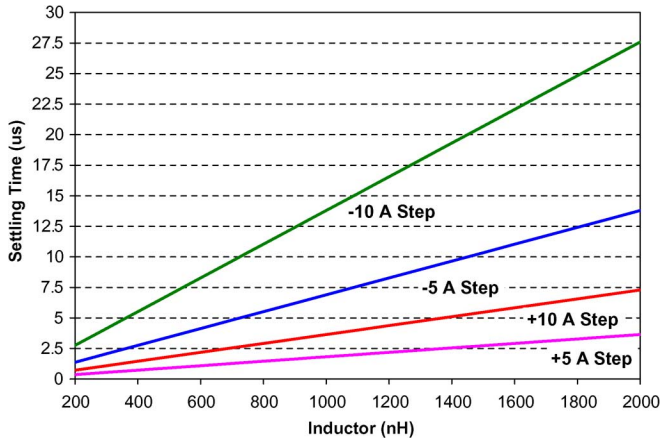

Fig. 10. Estimated settling time for a converter under the proposed control method ($V_{\text{in}} = 12$ V, $V_o = 1.5$ V).

Therefore, the total settling time for a positive load step is calculated in

$$T_{set\_pos} = T_0 + T_1 + T_2 = \frac{L\Delta I}{(V_{\text{in}} - V_o)} \left(1 + \frac{V_{\text{in}}}{V_o} \sqrt{\frac{V_o}{V_{\text{in}}}}\right). \tag{25}$$

Similarly, the settling time for a negative load step is calculated in

$$T_{set\_neg} = T_0 + T_1 + T_2 = \frac{L\Delta I}{V_o} \left[1 + \left(\frac{V_{\text{in}}}{V_{\text{in}} - V_o}\right) \sqrt{\frac{(V_{\text{in}} - V_o)}{V_{\text{in}}}}\right]. \tag{26}$$

Fig. 10 illustrates the estimated settling times for a Buck converter controlled by the capacitor charge balance method.

Using (25) and (26), the settling time for a Buck converter ($V_{\text{in}} = 12$ V, $V_o = 1.5$ V, $L = 1$ μH) undergoing a $+10$ A load step and a -10 A load step is calculated to be 4 μs and 14 μs, respectively.

By modifying (23), it is possible to calculate the maximum inductor current peak, for a positive load current step change, at time t_2, as shown in (27)

$$I_{L\_peak} = I_{\max} \left(1 + \sqrt{\frac{V_o}{V_{\text{in}}}}\right) \tag{27}$$

where I_{max} is the maximum rated current of the converter. The saturation current of the inductor should be greater than I_{L_peak} since the proposed control method assumes linear inductor behavior.

Under the proposed controller, it is also possible to estimate the voltage deviation due to an arbitrary load current step change.

For a positive step change, it is evident in Fig. 1 that the capacitor is discharging during time period T_0. The output voltage over time period T_0 (letting $T_0 = t = 0$) is derived in (28), shown at the bottom of the page.

$$v_o(t) = V_{ref} - EST\left(\Delta I - \frac{(V_{\text{in}} - V_o)t}{L}\right) - \frac{\frac{1}{2}\left(\frac{\Delta I^2 L}{V_{\text{in}} - V_o} - \left(\frac{\Delta I \cdot L}{V_{\text{in}} - V_o} - t\right)\left(\Delta I - \frac{(V_{\text{in}} - V_o)t}{L}\right)\right)}{C}$$

$$v_o(t) = V_{ref} - \frac{2ESR \cdot C(V_o t + \Delta I \cdot L - V_{\text{in}} t) - t^2(V_{\text{in}} - V_o) + 2L \cdot \Delta I \cdot t}{2L \cdot C} \tag{28}$$

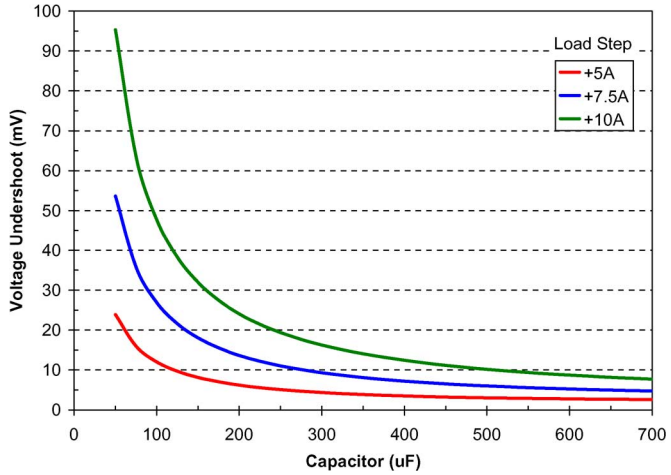

Fig. 11. Estimated undershoot for a Buck converter under the proposed control method ($V_{\text{in}} = 12$ V, $V_o = 1.5$ V, $L = 1\ \mu$H, ESR $= 0.5$ mΩ).

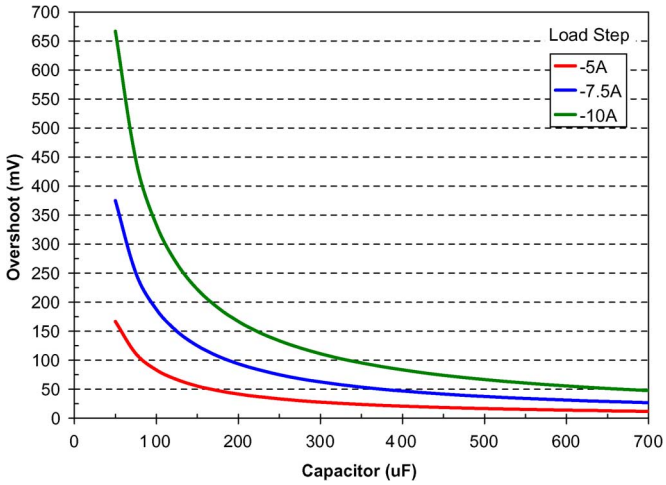

Fig. 12. Estimated overshoot for a Buck converter under the proposed control method ($V_{\text{in}} = 12$ V, $V_o = 1.5$ V, $L = 1\ \mu$H, ESR $= 0.5$ mΩ).

In order to determine the time at which the voltage is at its minimum (t_{min}), it is necessary to calculate the derivative of the output voltage with respect to time, as derived in

$$\frac{dv_o}{dt} = \frac{ESR \cdot C(V_{\text{in}} - V_o) + t(V_{\text{in}} - V_o) - \Delta I \cdot L}{L \cdot C}. \quad (29)$$

By setting (29) equal to zero and solving for t, t_{min} is calculated in

$$t_{\text{min}} = \frac{ESR \cdot C(V_o - V_{\text{in}}) + \Delta I \cdot L}{V_{\text{in}} - V_o}. \quad (30)$$

By substituting (30) into (28), Δv_{o_pos} is solved in

$$\Delta v_{o\_pos} = -\frac{ESR^2 \cdot C\left(V_{\text{in}}^2 - 2V_{\text{in}}V_o + V_o^2\right) + \Delta I^2 L^2}{2(V_{\text{in}} - V_o)L \cdot C}. \quad (31)$$

Similarly, the overshoot for a negative current step is calculated in

$$\Delta v_{o\_neg} = \frac{ESR^2 \cdot C^2 \cdot V_o^2 + \Delta I^2 L^2}{2V_o \cdot L \cdot C}. \quad (32)$$

Figs. 11 and 12 illustrate the estimated voltage deviation for a Buck converter controlled by the capacitor charge balance method.

Using (31) and (32), the voltage deviation for a Buck converter ($V_{\text{in}} = 12$ V, $V_o = 1.5$ V, $L = 1\ \mu$H, $C = 180\ \mu$F, ESR $=$ 0.5 mΩ) undergoing a $+10$ A load step and a -10 A load step is calculated to be -27 and 185 mV, respectively.

VI. Simulation Results

In order to verify the functionality of the charge balance method, a Buck converter, undergoing a load current step, was simulated. The parameters of the simulated Buck converter were as follows: $V_{\text{in}} = 12$ V, $V_{\text{out}} = 1.5$ V, $f_s = 400$ kHz, $L =$ 1 μH, $C = 180\ \mu$F, ESR $= 0.5$ mΩ, ESL $= 100$ pH.

Fig. 13 shows the response of a Buck converter undergoing a 0 A $\rightarrow$ 10 A load step change. For reference, the proposed

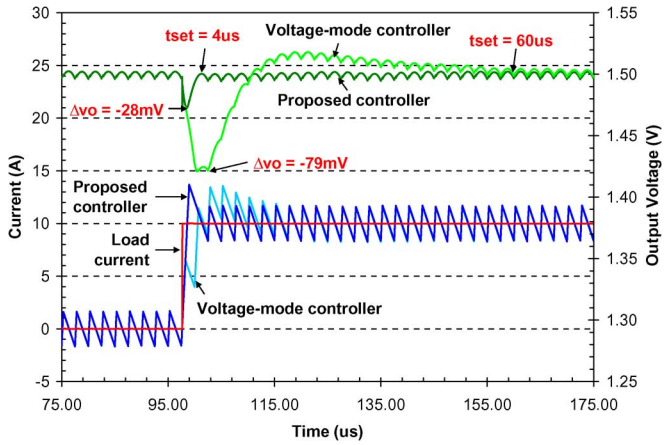

Fig. 13. Simulated response to a 0 A $\rightarrow$ 10 A load current step change (top: Output voltage, bottom: load current and inductor current).

controller response is compared to a voltage-mode controller response. The bandwidth of the voltage-mode controller was designed to be 71 kHz and the phase margin was 42°.

It is demonstrated through simulation that the settling time of the converter with the proposed controller is improved by 93% compared to that of the voltage-mode controlled converter. It is also shown that the voltage undershoot of the converter with the proposed controller is improved by 65% compared to that of the voltage-mode controlled converter. The simulation results of the proposed controller are in close correspondence with the theoretical results calculated in (25) and (31).

It should be noted that depending on the steady-state switching frequency and the output filter parameters, the moment at which the controller switches modes may effect the settling time minimally. For example, the absolute worst case scenario would occur if the controller switched from nonlinear mode to linear mode immediately following the linear PWM pulse ending. This could result in an additional 19 mV voltage dip following the transition (which would require 2 additional switching cycles to rectify). However, if one were to assume

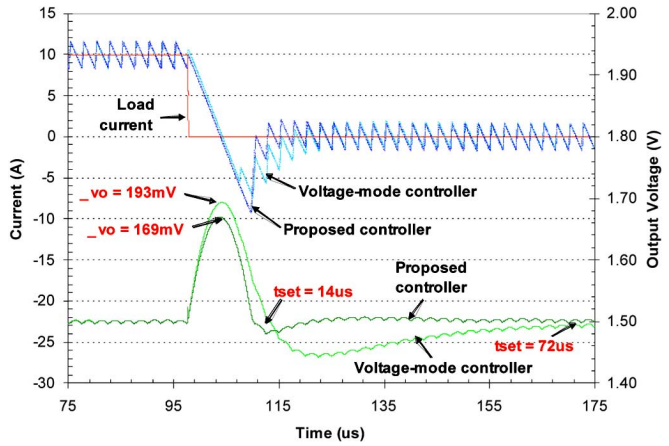

Fig. 14. Simulated response to a 10 A → 0 A load current step change (CCM) (top: load current and inductor current, bottom: output voltage).

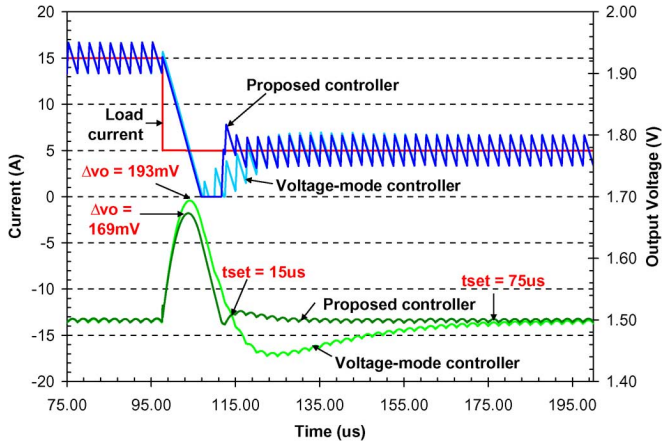

Fig. 15. Simulated response to a 15 A → 5 A load current step change (DCM) (top: load current and inductor current, bottom: output voltage).

that the switch-over occurred mid-way between switching cycles, the corresponding dip would be a modest 4.7 mV (which is equivalent to the steady-state output voltage ripple).

Fig. 14 shows the response of a CCM Buck converter undergoing a 10 A → 0 A load step change. For reference, the proposed controller response is compared to the response of the aforementioned voltage-mode controller.

For a negative load step (CCM), the settling time of the converter with the proposed controller is improved by 80% compared to that of the voltage-mode controlled converter. It is also shown that the voltage overshoot of the converter with the proposed controller is improved by 12% compared to that of the voltage-mode controlled converter. It is apparent that the simulated output voltage deviation varies from the estimated value by 9%. This error is caused by the assumption that the output voltage remains relatively constant during the transient period.

Fig. 15 shows the response of a DCM Buck converter (utilizing diode emulation) undergoing a 15 A → 5 A load step change. For reference, the proposed controller response is compared to the response of the aforementioned voltage-mode controller.

For a negative load step (DCM), the settling time of the converter with the proposed controller is improved by 80% compared to that of the voltage-mode controlled converter. It is also

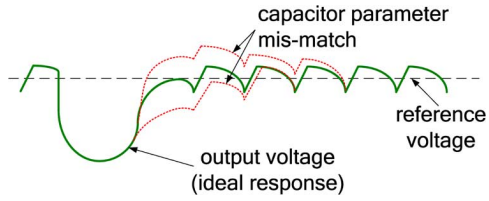

Fig. 16. Output voltage response due to capacitor parameter mismatch.

TABLE I
SIMULATED RESULTS WHEN CAPACITOR PARAMETERS ARE INCORRECT

	Ic Sensor Capacitor	Vo-Vref @ t_3	Total Settling Time
10A Load Step Down	+20%	7mV	7us
	Ideal	0mV	4us
	-20%	-5mV	11us
10A Load Step Up	+20%	-6mV	20us
	Ideal	0mV	14us
	-20%	5mV	20us

shown that the voltage overshoot of the converter with the proposed controller is improved by 12% compared to that of the voltage-mode controlled converter.

It is noted that the capacitor parameters must be known in order to obtain an accurate detection of the capacitor zero crossover point (t_1). Due to tolerance, the exact parameters of the output capacitors may not be known. This will effect the timing of t_1, t_2, and t_3. A capacitor parameter mismatch will not effect the voltage deviation but will effect the settling time, as shown in Fig. 16.

Table I provides the simulated results for the aforementioned Buck converter when the I_c sensor capacitor parameters are incorrect.

VII. EXPERIMENTAL RESULTS

A prototype of the proposed control method was designed and implemented with the aforementioned converter. In order to reduce noise amplification, the capacitor current sensor bandwidth was limited to approximately 15 MHz by adding a capacitor in parallel with the feedback resistor. The capacitor current sensor constant k was chosen to be 1800.

For reference, the proposed controller was compared with a voltage-mode controlled buck with an approximate bandwidth of 71 kHz.

Figs. 17 and 18 show a voltage-mode controlled Buck converter and the proposed controller undergoing a 0-A → 10-A load step change, respectively.

It is demonstrated, for a positive 10-A load current step change, that the settling time of the converter with the proposed controller is improved by 82% compared to that of the voltage-mode controlled converter. It is also shown that the undershoot of the converter with the proposed controller is improved by 76% compared to that of the voltage-mode controlled converter.

Figs. 19 and 20 show a voltage-mode controlled Buck converter (with a bandwidth of approximately 71 kHz) and the proposed controller undergoing a 10 A → 0 A load step change, respectively.

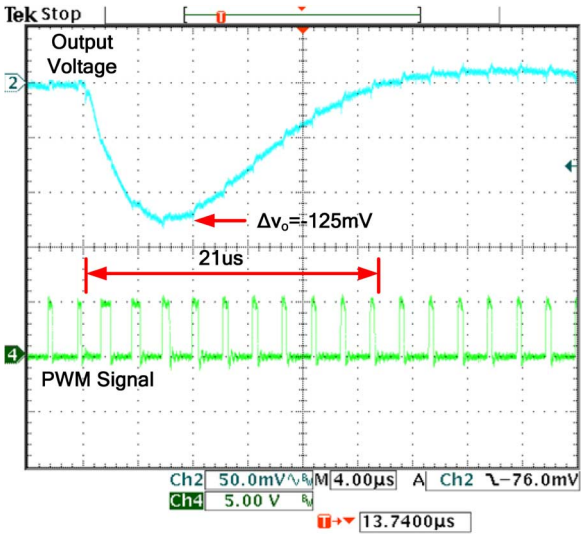

Fig. 17. Voltage-mode controller response to a 0 A → 10 A load current step change.

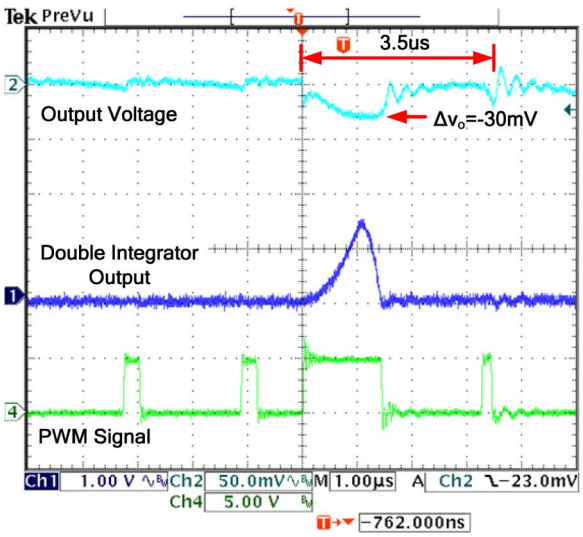

Fig. 18. Proposed controller response to a 0 A → 10 A load current step change.

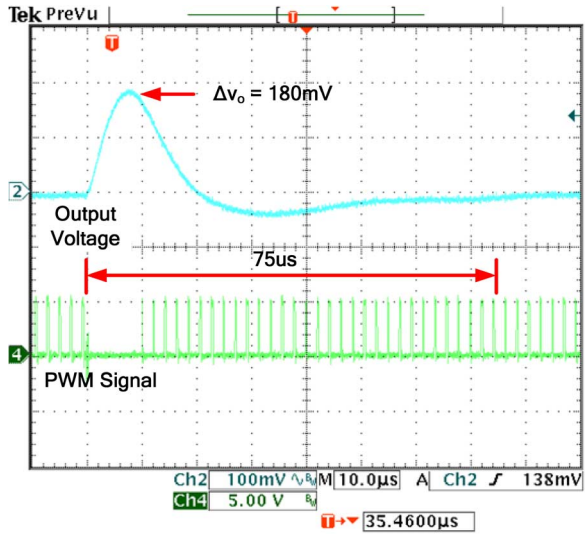

Fig. 19. Voltage-mode controller response to a 10 A → 0 A load current step change.

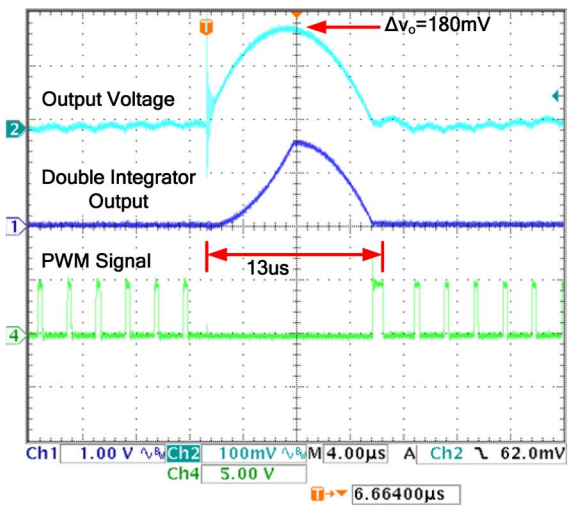

Fig. 20. Proposed controller response to a 10 A → 0 A load current step change.

It is demonstrated, for a 10-A negative load current step change (CCM), that the settling time of the converter with the proposed controller is improved by 84% compared to that of the voltage-mode controlled converter. Due to the quick reaction of the voltage-mode controller to reduce the duty cycle from approximately 13% to 0%, there is no overshoot improvement. Overshoot improvements would be apparent for higher duty cycle applications (e.g., 5 V to 2.5 V).

VIII. Conclusion

A practical optimal controller has been presented in this paper. The proposed control method only requires simple analog functions (such as comparison and integration) and is therefore not limited by the slow response of analog multipliers. The controller ensures a predictable response to a load variation, with the minimum possible voltage deviation and settling time. The predictable response greatly simplifies the design procedure of the output filter of a Buck converter. Using a set of simple equations, a designer can be guaranteed that the converter will be stable and operate within output voltage regulation criteria. Simulation and experimental results confirm the operation of the controller and demonstrate the significant improvement in dynamic response over tradition linear controllers.

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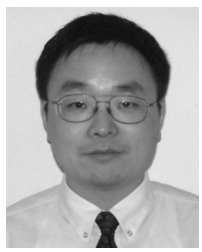

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