Recent Developments in Digital Control Strategies for DC/DC Switching Power Converters

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(Invited Paper)

***Abstract*—In this paper, an overview of recent advances in digital control of low- to medium-power dc/dc switching converters is presented. Traditionally, such dc/dc converters have been almost exclusively controlled through analog electronics methods. However, with the steadily decreasing cost of ICs, the feasibility of digitally controlled dc/dc switching converters has increased significantly. This paper outlines some of the existing design challenges related to digital control and reviews a sample of recently proposed solutions. In addition, present-day research pertaining to applications such as online efficiency optimization, controller autotuning, and specialized nonlinear control is presented. Such applications demonstrate the true advantages and potential of digital control as their complexity prevents practical implementation in the analog domain.**

***Index Terms*—DC/DC power conversion, digital control.**

I. Introduction

OVER THE past decade, digital control has emerged as a viable candidate for low- to medium-power dc/dc switching converters. With the steadily decreasing cost of digital ICs, the cost-prohibitive attribute of digital control technology has begun to fade. Therefore, over the past few years, research focus has shifted toward the unique advantages that digital control has to offer to dc/dc switching power converters.

It is well known that digital control offers advantages over analog control such as reprogrammability, better noise immunity, and low susceptibility to age and environmental factors. Thus, a vast amount of investigation was conducted in the late 1990s to design linear digital controllers that performed as well as their analog counterparts.

Although it was often predicted in the 1990s that digital control would soon become the new standard for all dc/dc switching converters, the adoption into the industry has been nearly nonexistent. From the customer's point of view, the adoption of a new technology that tended to be more expensive and typically did not function as well as present-day technology (in terms of steady-state accuracy and dynamic performance) did not make sense. From the designer's point of view, digital control compensation development tends to be less intuitive than the tried-and-true analog design methodologies. Furthermore, early digital designs required much larger areas of silicon and consumed more power than analog controllers, effectively prohibiting their adoption into low-power dc/dc power converters.

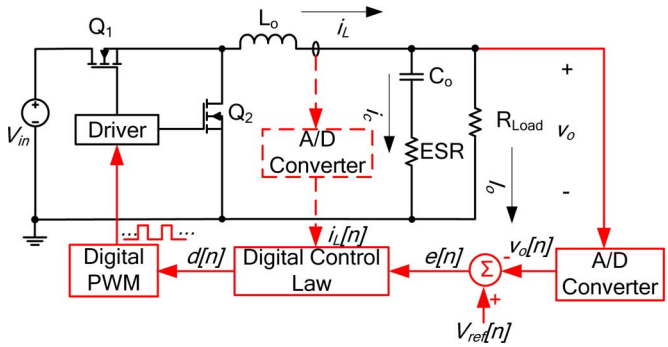

Fig. 1. Digitally controlled synchronous buck converter.

However, with the cost and size of digital circuits exponentially shrinking, and researcher's imaginations being sparked by the true power and capabilities of digital control, the opinion that digital control may eventually replace analog controllers is beginning to resurface. Although early research laid the stepping stones for further digital control development, it did not capitalize on the truly unique tools that digital control brings to switching power converters. Thus, recent research has been conducted on digital controllers, which perform functions that are not realizable in the analog domain such as communication- and system-level integration, controller autotuning, on-the-fly efficiency monitoring and optimization, and complex nonlinear control for improved dynamic performance.

This paper will outline the current challenges and the proposed solutions to digital control of switching power converters, and will also present an overview of recent developments that are truly unique to digital controllers.

II. Digital Control Challenges and Proposed Solutions

Fig. 1 illustrates the implementation of a digitally controlled synchronous buck converter. The controller consists of at least one analog-to-digital converter (ADC) for feedback,

Manuscript received March 8, 2009; revised May 26, 2009. Current version published December 18, 2009. This work was supported in part by the National Natural Science Foundation of China under Grant 50877001 and Grant 50407017 and in part by the Excellent Youth Foundation of Anhui Province, China, under Grant 08040106809. Recommended for publication by Associate Editor A. Prodic.

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Digital Object Identifier 10.1109/TPEL.2009.2030809

a programmable digital control law, and a digital pulsewidth modulator (DPWM) in order to convert the control output to a modulated pulse waveform with duty cycle d.

This section will focus on the control law and the DPWM design of a digital controller.

A. Control Law of the Linear Compensator

Although digital control offers many advantages to dc/dc switching power converters, its adoption into industry applications has met with reluctance from power electronics engineers. The decreasing cost of silicon real estate allows digital control to become more cost-feasible; however, one factor that continues to inhibit digital control use is the engineers' unwillingness to design control compensators in the digital domain.

Typically, power electronics' engineers feel more comfortable designing controllers using traditional analog techniques (e.g., pole/zero placement using Bode diagrams). Therefore, various digital design techniques have been proposed that incorporate the intuitiveness of analog design [1]–[4].

Analog-to-digital redesign of the compensator is a popular technique as it requires minimal design in the discrete z-domain. Essentially, a linear compensator is devised in the analog domain using traditional design methods. Using one of a variety of discretization methods (1)–(3), the continuous s-domain transfer function can be easily mapped to the discrete z-domain.

Backward Euler:

$$s = \frac{1 - z^1}{T_{\text{samp}}}. \tag{1}$$

Bilinear:

$$s = \frac{2}{T_{\text{samp}}} \frac{1 - z^{-1}}{1 + z^{-1}}. \tag{2}$$

Pole/zero matching:

$$\begin{aligned} s + a &= 1 - z^{-1} e^{-aT_{\text{samp}}} \\ s \pm ja &= 1 - 2z^{-1} e^{-aT_{\text{samp}}} \cos bT_{\text{samp}} + z^{-2} e^{-2aT_{\text{samp}}}. \end{aligned} \tag{3}$$

Although the backward Euler method and the pole/zero matching method produce simpler transfer functions in the z-domain, the bilinear method (also known as Tustin's approximation) provides the truest transformation as it preserves the gain and phase of the analog transfer function up to approximately one-tenth of the sampling frequency f_{samp}.

Although analog-to-digital redesign is capable of providing a good response, it suffers due to discretization effects (such as frequency warping using the bilinear method) and its often disregard for acquisition, computation, and zero-order-hold (ZOH) delays. It is demonstrated in [2]–[4] that direct digital design provides superior performance.

In [3], an exact small-signal discrete-time model is proposed for digitally controlled dc/dc converters. The model, which is based on well-known approaches to discrete-time modeling and the standard Z-transform, takes into account modulator effects and delays in the control loop. It shows that the zero of the control-to-output transfer function is dependent on the total delay time in the control loop, while the poles are not affected. One interesting observation of this method is that the equivalent series resistance (ESR) effect of the output capacitor does not add another zero. Rather, it just shifts the zero in the direction opposite to the delay time.

Many direct digital design methods require discretization of the converter transfer function, which may be computationally intensive and is not intuitive to a primarily analog designer. Thus, a direct digital method is proposed in [4], which is similar to traditional analog compensation techniques.

In [4], discrete zeroes, poles, and complex zero/pole pairs are defined, as shown in (4)–(6), and mapped to the continuous domain using the relation $z^{-1} = e^{-sT_{\text{samp}}} = e^{-2j\pi f T_{\text{samp}}}$

$$H_{\text{zero}}(z) = 1 - \left(1 - \frac{1}{a}\right) z^{-1} \tag{4}$$

$$H^{\text{hard}}_{\text{zero pair}}(z) = 1 - \left(2 - \frac{1}{b}\right) z^{-1} + z^{-2} \tag{5}$$

$$H^{\text{soft}}_{\text{zero pair}}(z) = 1 - \left(2 - \frac{1}{b}\right) z^{-1} + \left(1 - \frac{1}{c}\right) z^{-2} \tag{6}$$

where a, b, and c are digital zero constants. Nonzero poles are realized by taking the reciprocals of (4)–(6). Integration (to allow zero steady-state error) can be easily implemented using the Euler integrator function, which is defined as

$$H^{\text{Euler}}_{\text{integrator}}(z) = \frac{1}{1 - z^{-1}}. \tag{7}$$

The ZOH effect of the digital compensator can be accounted for by adding (8) to the continuous control loop

$$\text{ZOH}(s) = \frac{1 - e^{-sT\text{samp}}}{s} \approx \frac{1}{1 + (T_{\text{samp}}/2)s}. \tag{8}$$

The continuous-time Bode diagram can be plotted easily using MATLAB or similar mathematical programs. By adjusting the coefficients a, b, c, etc., the frequencies of the poles and zeros shift (just as they would by adjusting resistor or capacitor values in an analog compensator).

The three main advantages of mapping the poles and zeros to the continuous domain and designing using this method are:

1) intuitive design using continuous-domain Bode plots;
2) frequency analysis is valid for all frequencies, regardless of the sampling frequency;
3) ability to design complex zeros, which allow for a 180° phase boost at the double pole frequency of the buck converter LC filter.

The result of using a redesign method or the direct digital design method is a transfer function in the z-domain, which can be formatted to a difference equation for implementation. For example, a PID controller would have the following form after being transformed into the discrete time domain:

$$d[n+1] = d[n] + av_{\text{err}}[n] + bv_{\text{err}}[n-1] + cv_{\text{err}}[n-2]. \tag{9}$$

The implementation of the aforementioned PID compensator is illustrated in Fig. 2.

Coefficient multiplication may be performed through a digital multiplier; however, this will cause an increase in computational delay and/or system clock frequency. For high-frequency

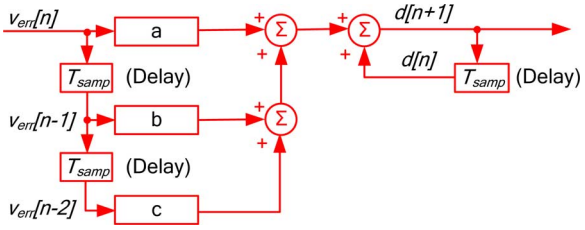

Fig. 2. Implementation of a digital PID compensator.

switching converters, the resultant delay may be unacceptable. Therefore, it is recommended in [5] that lookup tables (LUTs) of size 1×2^N (where N is the ADC bit resolution) be employed, which will decrease the computation delay significantly. This reduction of delay comes at the cost of an increase in physical controller real estate. However, it is noted in [4] and [5] that if the coefficients are restricted to multiples of 2, the multiplication can be performed simply by bit-shifting, thereby saving silicon real estate.

B. Current-Programmed Control

Current-programmed control, with advantages such as simple compensation, inherent overcurrent protection, and excellent audiosusceptibility, presents an interesting challenge to digital control. For example, analog peak-current-mode control requires instantaneous inductor current information in order to determine the duty cycle. For digital control, this would result in high-frequency sampling of the inductor current (thus increasing the cost and power consumption of the controller). Therefore, numerous digital control strategies have been proposed [6]–[8]. In [6], the inductor current is sampled once per switching cycle, and the subsequent duty cycle is determined based on the digitally calculated positive and negative inductor current slew rates. However, this method requires continuous measurement of the converter input voltage and precise knowledge of the inductor value.

In [7], a controller is presented that compares the sampled inductor current to a digital compensator ramp, and thus, does not require inductor current slew rate information. However, this method does not provide overcurrent protection as the precise peak inductor current is not calculated by the controller.

As shown in Fig. 3, both the aforementioned methods will have degraded audiosusceptibility properties when compared to their analog counterparts due to their inherent acquisition and computational delays. To rectify this, a mixed-signal controller is presented in [8], which converts the digitally calculated control current (with a 1-bit Δ–Σ digital-to-analog converter) to the analog domain for comparison with the inductor current using an analog comparator. This method significantly improves the response at the cost of added control complexity.

C. Digital Pulsewidth Modulator

Limit cycle oscillation (LCO) is a common problem associated with digitally controlled switching converters due to the quantization effects of the ADC and the DPWM [9]. Fig. 4

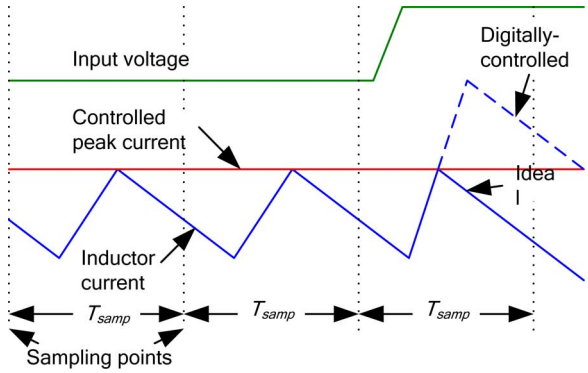

Fig. 3. Digital peak current-mode control delay effect on audiosusceptibility.

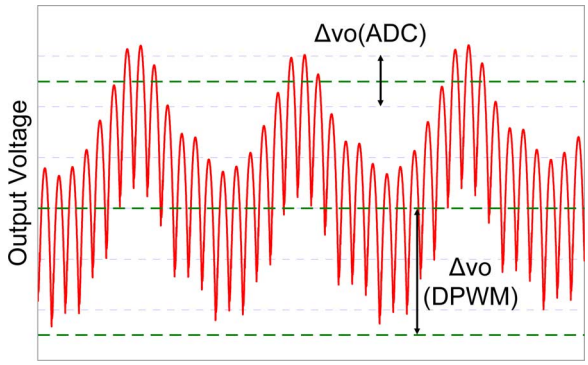

Fig. 4. Simulated example of LCO due to coarse DPWM.

illustrates a simulated example of a digitally controlled buck converter experiencing LCO.

According to [9], significant LCO may occur when the compensator integrator gain is set too high or the quantization step of the DPWM is too coarse. To prevent LCO, the following inequality must be true: $\Delta d_{\mathrm{LSB}} V_{\mathrm{in}} < \Delta v_{o\_\mathrm{LSB}}$.

Accomplishing such fine DPWM resolution through a digital counter would typically require a system clock frequency in the gigahertz range. Therefore, numerous alternative DPWM methods have been proposed. Tapped delay lines [10] and ring oscillators [11] may be used to create ultrafine DPWM resolutions. However, these methods require large amounts of physical area to implement the string of delay elements and a multiplexor of size 2^N:1 (where N is the number of DPWM bits). Moreover, voltage reference and temperature variations may drastically affect the performance of a delay line.

In order to benefit from the ultrafine resolution of a tapped delay line without suffering from a massive increase in physical area, hybrid counter/delay-line DPWMs (such as the architecture illustrated in Fig. 5) are frequently implemented. However, in order to avoid DPWM nonlinearity, care must be taken to ensure that the maximum delay of the tapped delay line is appropriately matched with the delay associated with the counter's LSB. This may prove difficult due to the aforementioned voltage reference and temperature variations that can affect the delay line. To address this issue, a hybrid DPWM is proposed in [12], which utilizes a tapped delay line consisting of adjustable delay cells. The cell delays are continuously monitored and adjusted

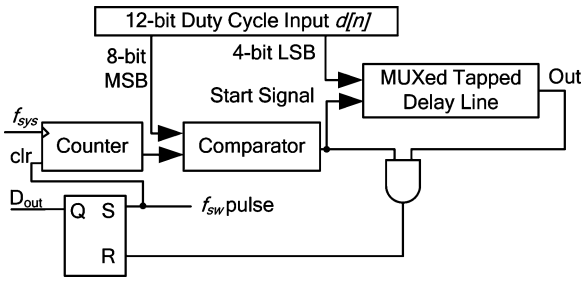

Fig. 5. Block diagram of hybrid DPWM architecture.

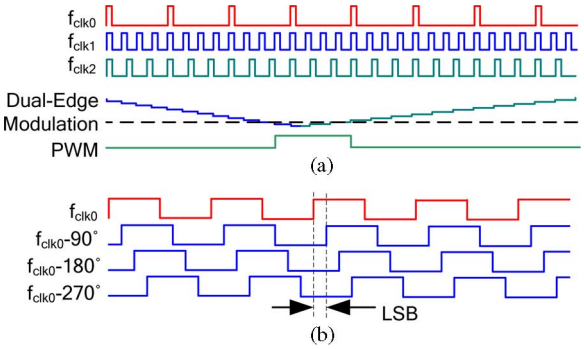

Fig. 6. DPWM methods utilizing multiple clocks. (a) Dual-clock dual-edge DPWM. (b) Phase-shifted clock DPWM.

by a delay-locked loop (DLL), ensuring that the tapped delay line yields constant delays, regardless of external factors.

In [13], two clocks with similar frequencies are utilized with a dual-edge modulation scheme [see Fig. 6(a)] in order to increase the effective system clock frequency as

$$f_{\text{clk-eff}} = \frac{f_{\text{clck1}} f_{\text{clk2}}}{f_{\text{clck1}} - f_{\text{clk2}}}. \tag{10}$$

This can be accomplished by frequency multiplication of a slow clock signal by a phase-locked-loop (PLL) circuit. However, the resolution is limited by the capabilities of the PLL. As the clock frequency difference decreases, the effective DPWM resolution becomes finer. In [13], two clocks with 100 and 101 MHz are used as an example for designing a DPWM with an effective resolution of 10 GHz. However, this would require a PLL multiplication factor of 100 and 101 of a 1-MHz clock, which is very difficult to implement practically.

PLLs may also be utilized to phase-shift a clock signal by $360°/N$ to produce N number of clocks [14]. This effectively increases the DPWM by a factor of N, as shown in Fig. 6(b).

The dither method involves applying a pattern to successive DPWM signals in order to generate an effectively higher DPWM resolution. In the example illustrated in Fig. 7, the effective resolution is increased by 2 bits. Dither patterns, using either a first-order Σ–Δ generator [15] or an LUT with preprogrammed patterns [16], are well-known approaches to increasing the effective resolution of a DPWM through averaging a set of duty cycles. However, low-frequency tones tend to be produced by such methods.

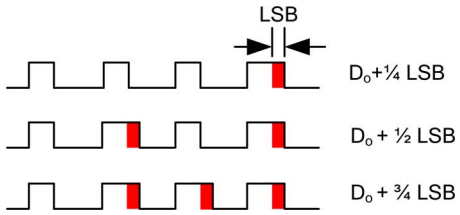

Fig. 7. Dither method increasing DPWM resolution by 2 bit.

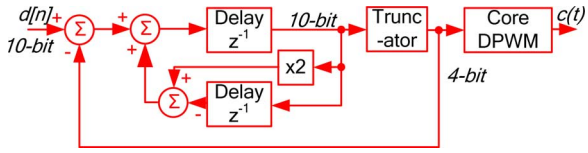

Fig. 8. Second-order multibit Σ–Δ generator.

Therefore, a second-order multibit Σ–Δ generator (see Fig. 8) is presented in [17], which increases the effective resolution of the DPWM with lesser magnitude low-frequency tones due to the decreased periodicity of the resultant patterns.

However, a common drawback with any type of dither DPWM method is a decrease in responsiveness since multiple switching cycles are required in order to increase/decrease the effective duty cycle.

Fine-resolution DPWM strategies will continue to be a topic of interest since their need is further increased as converter's switching frequencies continue to rise.

This section presented a brief overview of present-day challenges that are being faced by digitally controlled switching converters; however, research focus has shifted toward unique features that may be accomplished only through digital control.

III. Communication- and System-Level Integration

With the complexity of modern devices, it is a very rare occurrence that a single power converter will be responsible for powering an entire digital system. For example, a typical motherboard will possess a CPU, a graphics processing unit (GPU), RAM, audioprocessing, associated logic, etc. Each device will have specific power specifications, and thus, have its own power converter. As the operation of the aforementioned devices is typically highly integrated, it is also necessary that there be some level of power management communication between the devices.

Such a need for complex system integration has significantly contributed to digital control's emergence into the mainstream marketplace. Linear Technology [18], Maxim IC [19], Texas Instruments Incorporated [20], and Zilker Laboratories [21] (recently acquired by Intersil) have all developed dc/dc digital controllers that are capable of communicating through the PMBus power management protocol.

Through serial communication, up to 127 dc/dc digital converters may be addressed and accessed by a central system controller, as illustrated in Fig. 9 [22]. The PMBus protocol defines a communication language of more than 100 power-management-specific commands. The advantages of such a system-wide

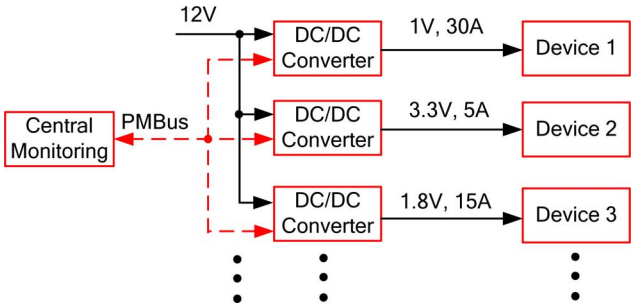

Fig. 9. Multiple converters communicating through PMBus.

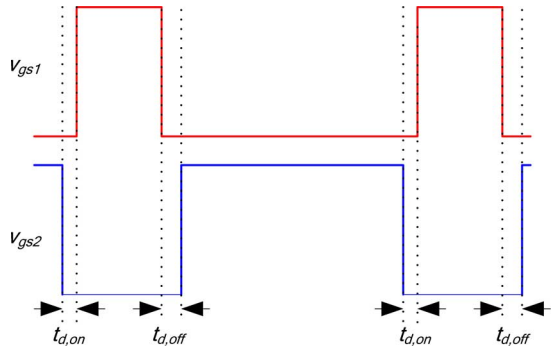

Fig. 10. Operation of a synchronous buck converter with dead time.

communication network are vast; however, some obvious advantages include the following.

1) *Power-Up/Power-Down Sequencing:* For complex systems such as a motherboard, there is typically a specified power-up/power-down sequence for the various devices. For example, it may be required that converter A's output voltage be at least 75% of its nominal voltage before converter B's soft-start procedure is to begin. Digital communication of devices allows for a simplified and systematic approach to such sequencing issues.
2) *Fault Detection and Reaction:* Through the PMBus protocol, pertinent information such as input/output voltage, load current, operating temperature (along with any corresponding operating faults) can be monitored by a central system controller. Through the use of a central controller, a fault detected in one converter will result in the intelligent shutdown of subsequent controllers in order to minimize the possibility of damage. Without such a communication network, faults would merely cascade through the system in an uncontrolled manner, thus increasing the risk of damage.
3) *"Field" Reconfiguration of Power Converters:* Typically, modification of a converter's control parameters (i.e., switching speed, compensator coefficients, fault tolerances, etc.) would require the recall and removal of the converter. However, through the PMBus interface, it is possible to reconfigure the nonvolatile memory of digital converters in order to permanently modify the control parameters. Such a firmware update is significantly less expensive and requires less offline time.

With the recent emergence of the PMBus interface, there has been increasing development of digital controllers in the power electronics industry as the complexity of digital systems continues to increase.

IV. Efficiency Optimization

Energy efficiency of switching converters has become an increasingly important topic, both due to the booming market of mobile electronic devices and the rising concern of environmental impact. It is possible, by the use of digital control, to make on-the-fly adjustments to the operating parameters of a switching converter in order to optimize efficiency.

In [23] and [24], continuous modifications are made to the dead time parameters $t_{d,\mathrm{on}}$ and $t_{d,\mathrm{off}}$ (see Fig. 10) in order to decrease the switching loss due to conduction of the synchronous MOSFET's body diode.

In [23], predicted optimal dead time values are initially programmed into the digital controller in relation to the converter's output current. To compensate for parameter variation/drift, slow dead time perturbations are added, and the resultant converter efficiency is measured by monitoring the input/output voltage/current. The new optimal dead times for various output currents are mapped by use of an extremum-seeking adaptation algorithm.

The algorithm presented in [24] does not map optimal dead times to specified output currents, but rather dynamically varies the dead time of the algorithm searching for duty cycle minima points (which indicate peaks in efficiency).

The main advantage of the optimization scheme presented in [23] is its rapid response to dynamic load conditions; however, the optimization scheme presented in [24] may be easier to implement as it is effectively sensor-less and possesses a significantly simpler algorithm.

Digital control can play an important role in improving efficiency for multiphase buck converter applications. By digitally scheduling the activation and deactivation of phases dependent on load/thermal conditions, the efficiency of a converter can be improved significantly. This practice is commonly referred to as "phase-shedding." During light-to-heavy load transitions, additional phases will be activated to provide current to the increased load; however, under traditional linear current sharing schemes, it will take many switching cycles for the inductor phases to achieve current balance, causing some phases to conduct more than their rated current levels. In [25], during phase activation, the controller quickly balances the activated phase through a nonlinear predictive control scheme, as shown in Fig. 11. This controller behavior would be very difficult to achieve through analog control. By rapid current balancing, the control method decreases the conduction loss following phase activation. However, experimental results are presented only for slowly varying load currents. Further investigation is required to determine the controller's proper response when the dI_o/dt value is very large.

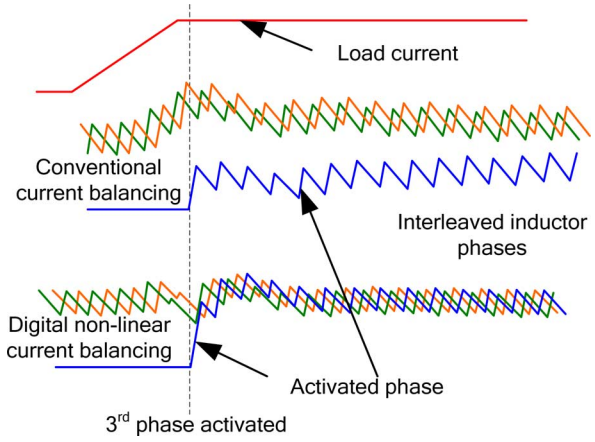

Fig. 11. Nonlinear digital phase balancing following phase activation.

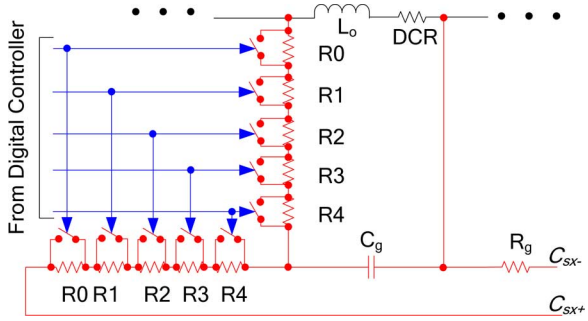

Fig. 12. Digital tuning of an analog RC inductor current sensor.

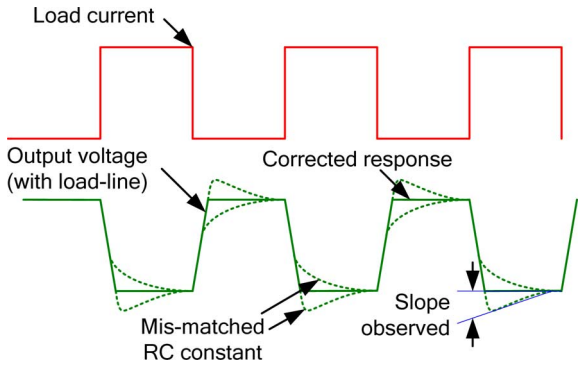

Fig. 13. Autotuning effect on a buck converter with load-line regulation.

In [26], a digital current balance scheme is presented, which intelligently adjusts the phase duty cycles based on efficiency, rather than nominal inductor current values. It is demonstrated that efficiency is suboptimal when the current is balanced perfectly and the phase resistance is mismatched. Thus, the controller operates by iteratively attempting to minimize the difference between the duty cycles of each phase while maintaining proper voltage regulation, which is demonstrated to minimize the total conduction loss of the converter. By adjusting the phase currents in this fashion, conduction loss and thermal management are significantly improved for mismatched multiphase converters.

V. Digital Autotuning

"Autotuning" is an exclusively digital tool that has tremendous marketing potential. The idea of a "plug-and-play" controller that can automatically identify and control a converter has attracted interest from both industry and academia.

Typically, analog inductor current measurement has only been as accurate as the model of the converter. Inductor current measurement is often necessary for overcurrent protection, multiphase current balancing, and load-line regulation. A popular analog current measurement method is to add a parallel RC branch across the output inductor and measure the voltage across the capacitor of the parallel branch. For correct current measurement, the time constant of the RC branch should be equal to the time constant of the inductor and its parasitic dc resistance (DCR). However, inductor tolerances along with varying thermal conditions that cause varying DCR present challenges to precise inductor current measurement.

In [27], a controller is presented that automatically tunes an analog RC current measurement sensor by use of a digital potentiometer (see Fig. 12). It accomplishes this by simply observing the output voltage slope of a load-line regulated converter, following a large-load transient. As shown in Fig. 13, when the RC filter is properly tuned to the inductor RL constant, the output voltage response is relatively flat when the load current is known to be flat. If the magnitude of the output voltage slope is greater than a specified threshold, the RC constant is adjusted using the digital potentiometer. This improves the load-line regulation response of the system. Two potential drawbacks of the scheme demonstrated in [27] are that no extension for multiphase operation is presented, and it will be difficult to correctly measure the output voltage slope if the load transient frequency is relatively high.

In [28] and [29], a sensor-less digital inductor current measurement algorithm is employed to calculate the average inductor current per switching cycle. By measuring the input voltage and the output voltage and by observing the duty ratio on a cycle-by-cycle basis, the controller is capable of emulating an RC-type filter through the use of a digital first-order low-pass filter. The proper corner frequency of the digital filter is automatically calibrated using a small precise current sink at the output of the converter that is activated for a short duration. In its present form, the proposed algorithm provides only dc inductor current information on a cycle-by-cycle basis; thus, it is not suitable for instantaneous overcurrent protection. However, since the input voltage, output voltage, and estimated inductor value are known, a simple extension should be capable of providing this feature.

Current sharing for multiphase digitally controlled converters is an important challenge due to measurement delay effects and possible inaccuracies of phase current measurement. Thus, the above-mentioned digital sensor-less current measurement scheme has been extended to multiphase applications [29]. For multiphase inductor current measurement tuning, the precise current sink is activated while only one phase current is permitted to vary (the others are held constant). This method is cycled

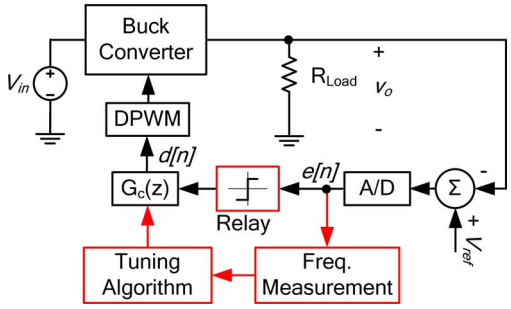

Fig. 14. Nonlinear relay to induce LCOs.

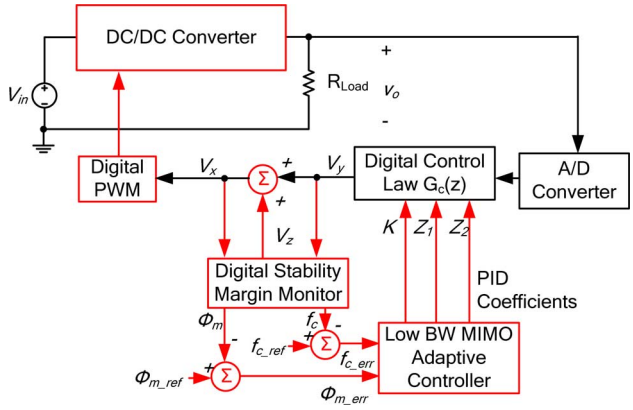

Fig. 15. Autotuning based on continuously measuring phase margin.

until calibration is complete for each phase. One disadvantage of this method is that voltage-mode control cannot be utilized (only average current-mode control can be used) since it is important to force all phases but one to remain constant during the calibration period.

By use of digital control, it is also possible to model the converter parameters L, C, ESR, etc., and automatically calculate control coefficients based on bandwidth and phase margin requirements.

This is accomplished in [30]–[33] by injecting a specified frequency into the control loop or by adding/amplifying a nonlinearity that causes the output voltage to oscillate.

In [30], the DPWM resolution is intentionally degraded for a short period. As noted in Section II, coarse DPWM resolution will lead to LCO. In order to amplify the LCO effect, the digital compensator is temporarily replaced with a PI configuration. By measuring the frequency of the resultant LCO, information related to the converter resonant frequency and output capacitance can be calculated. By measuring the amplitude of the resultant LCO, it is possible to calculate the Q-factor of the converter (and thus, the load resistance/current). The information is used to design a proper PID by extracting appropriate parameters from LUTs (provided that the load current remains relatively constant). An advantage of this method is that it does not require the addition of a relay in the circuit, but only a temporary modification of the DPWM. A disadvantage of this method is that it requires the measurement of the amplitude of the LCO, which may be very sensitive to the quantization noise effect of the ADC.

In [31], a frequency component is added to the system, which is equal to the desired controller bandwidth. The same frequency component is added to a digitized "reference" loop that is designed with the desired response of the system based on the model of the buck converter. The output response of both the actual loop and the reference loop is measured/calculated digitally, and the difference of the amplitude and phase is calculated. Using this information, the controller parameters are adjusted such that the response of the actual converter loop equals that of the reference loop.

In [32] and [33], autotuning is accomplished by introducing a nonlinear relay into the control loop, as shown in Fig. 14.

The relay essentially acts as a 1-bit quantizer, causing LCO at the output. When $G_c(z)$ is adjusted to an integrator (causing a 90° phase lag in the loop), the output voltage will oscillate at the resonant frequency of the converter. This frequency is measured and stored. This allows for the proper placement of the first zero of a PID compensator. The new PID controller is passed through a low-pass filter to force the desired phase margin at the desired crossover frequency. The second zero is then iteratively placed until the output oscillates at the crossover frequency. After the two zeroes are placed, the compensator gain is set by using the desired bandwidth, zero placement, and an asymptotic Bode plot estimation. The relay function is disabled after the tuning process is completed, allowing for normal loop operation. The advantage of the aforementioned method is that only the frequency of the output voltage oscillation is required to be measured; the amplitude is not required, allowing for more robust operation.

The above-mentioned autotuning algorithms induce a relatively large voltage oscillation at the output of the converter for a short period of time in order to tune the controller. However, the autotuning algorithm presented in [34] follows a different approach, as illustrated in Fig. 15. The system operates by continuously injecting a varying frequency square wave V_z into the DPWM input signal V_x. The DPWM input signal and the digital compensator output signal V_y are passed though a bandpass filter (bandpass equal to the injected frequency) and measured by the digital stability monitor. The injected frequency is adjusted until the magnitude of the two measured filtered signals are equal (indicating the crossover frequency f_c). By comparing the zero-crossover points of the two signals V_y and V_x (when the injected signal is equal to the determined crossover frequency), the phase margin ϕ_m of the system can also be calculated. The measured crossover frequency and phase margin are subtracted from the desired crossover frequency and phase margin to produce crossover frequency and phase margin errors (f_{c_err} and ϕ_{m_err}, respectively). A relatively low-bandwidth multiinput–multioutput (MIMO) controller continuously adjusts the controller's coefficients in an attempt to minimize the f_{c_err} and ϕ_{m_err}. One apparent drawback of this autotuning method is a continuous-output-voltage oscillation at the injection frequency. However, a control algorithm is used to ensure that the oscillation magnitude is no more than ± 1 LSB of the ADC.

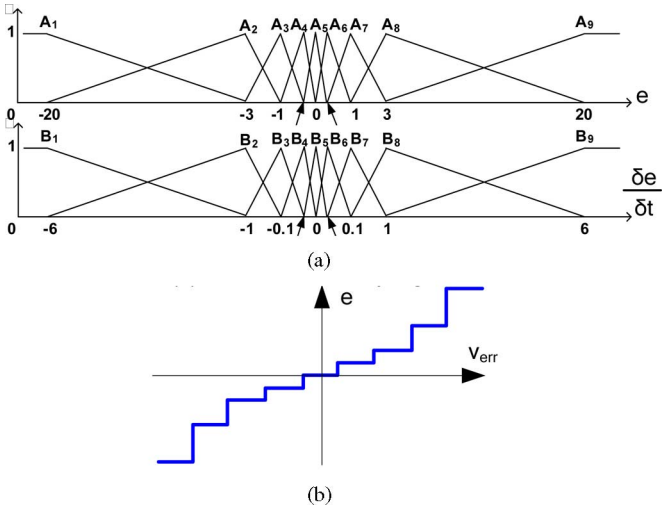

Fig. 16. Nonuniform controller behavior. (a) Nonuniform fuzzy logic sets. (b) Nonuniform quantizer.

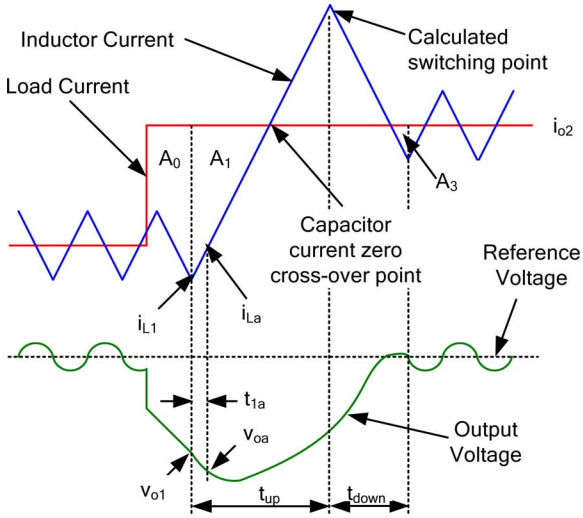

Fig. 17. Charge balance controller response to a fast load current change.

VI. Nonlinear and Charge Balance Control

It is known that nonlinear control is capable of improving the dynamic response of a converter since it is able to quickly react to transient conditions. However, analog nonlinear controllers tend to possess undesirable characteristics such as nonzero steady-state error and variable switching frequency. Furthermore, high-performance analog nonlinear controllers such as the boundary control presented in [35] and [36] require multiplication and division functions, which are prohibitively expensive and slow in analog implementation. Digital control, however, is capable of performing complex mathematical functions typical of nonlinear control. In addition, digital control is well-suited for the development of hybrid linear/nonlinear controllers, which possess the fast reaction of a nonlinear controller during transient conditions with the precision of a linear controller during steady state.

In [37] and [38], digital controllers are presented that behave as a linear controller for conditions when the output voltage error is small and a nonlinear controller when the output voltage error is large. As shown in Fig. 16(a), this is accomplished in [37] by use of a PI-like fuzzy logic controller and nonuniform fuzzy sets. The controller mimics a PI controller during steady-state conditions; however, when either the output voltage error or derivative of the output voltage is relatively high, the duty cycle varies at a faster nonlinear rate.

In [38], a nonuniform ADC is used to acquire the output voltage [see Fig. 16(b)]. This nonlinear control method is powerful, yet very simple, as it does not require any multiplier or division blocks to implement.

In [39], a digital controller is presented that employs a linear PID scheme during steady-state conditions and uses a nonlinear sliding-mode-like controller during large output voltage deviations. Digital control facilitates smooth transitions between the two modes.

Charge balance control (also known as time optimal control) involves attempting to drive a converter to steady state in the theoretically minimum time possible. As illustrated in Fig. 17, for a buck converter undergoing a load transient, it involves a single switching transition at a precise moment. Due to the complex derivation involved, this is well-suited for digital control and has received considerable research attention [41]–[48]. Charge balance controllers typically behave as a linear controller when the converter experiences steady-state conditions and as a nonlinear controller following a transient event.

The concept involves determining the capacitor current zero-crossover point by either estimating the load current step change [39]–[43] or by using an asynchronous ADC to estimate the output voltage valley point [44]–[46]. Typically, LUTs store precise timing information to determine the switching instant to achieve minimal settling time. The LUT values are calculated based on geometrically derived charge balance formulas.

For example, in [42] (also see Fig. 17), the inductor current and output voltage deviation is sampled twice following the load transient. The information is used to first estimate new load current using (11) and next to determine the optimal switching periods $t_{\rm up}$ and $t_{\rm down}$ period using (12):

$$i_{o2} = \frac{1}{2}(i_{L1} + i_{La}) - \frac{C(v_{0a} - v_{o1}) - C(i_{La} - i_{L1})\mathrm{ESR}}{t_{1a}} \tag{11}$$

$$t_{\rm up} = \sqrt{\frac{A_0 + A_1 + A_3}{(1/2)(V_{\rm in}/V_o)\{(V_{\rm in} - V_o)/L\}}}$$

$$t_{\rm down} = t_{\rm up}\frac{V_{\rm in} - V_o}{V_o} \tag{12}$$

where A_0, A_1, and A_3 are the capacitor charge integral areas that can be easily geometrically calculated using the estimated load current i_{o2}.

One drawback of nonlinear digital controllers that rely on the ADC to detect load transients is the inherently delayed response due to the sampling delay. Such delays are not as prevalent in analog nonlinear controllers as voltage-mode hysteretic

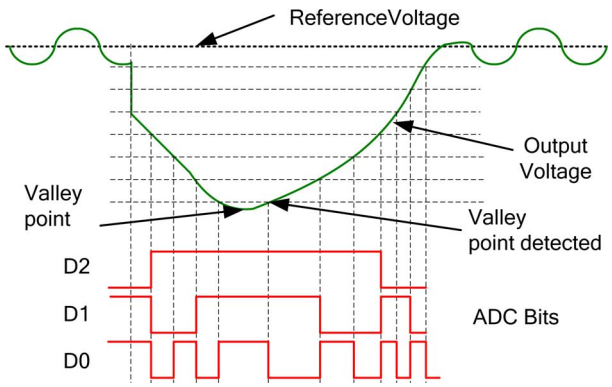

Fig. 18. Asynchronous ADC operation to estimate output voltage valley point.

control. Thus, recent nonlinear digital controllers have begun to adopt analog load transient detection or the use of asynchronous ADCs. For example, with the use of asynchronous ADCs, it is possible to detect the load transient with delays comparable to fully analog controllers.

As shown in Fig. 18, an asynchronous analog-to-digital controller can also be used to determine the voltage valley point (both magnitude and time instant). The controller proposed in [44] uses this information to calculate the optimal switching time instant, while in [45] and [46], the information is used to calculate the output voltage level at which the controller should alter its switching state. An advantage of the controller presented in [45] and [46] is that the inductor and capacitor values are not required; however, it is assumed that the ESR of the capacitor is negligible. If this is not the case, the capacitor and ESR values would be required in order to compensate.

Although asynchronous sampling can be used for charge balance control, there are two potential drawbacks. In order to function correctly, the ADC acquisition delay must be extremely low and the timing resolution of the controller (its system clock) must be very fine. Furthermore, as shown in Fig. 18, the output voltage valley point is always detected after it occurs. In low-duty-cycle conversion applications (i.e., 12 V $\rightarrow$ 1 V), there is the potential that the valley point may be detected after the optimal switching time instant.

It is important to note that the above nonlinear controllers can be easily extended to multiphase operation. In this case, the interleaving operation ceases, following a transient event, and the phases are controlled in parallel by a single control signal. In this manner, the initial charge removed/absorbed by the capacitor can be minimized since the capacitor current will slew at its maximum possible rate. Since the majority of charge balance controllers rely on estimation of the capacitor current (rather than the inductor current), the algorithm operation will be virtually identical to the single-phase operation. Following recovery of the transient event, the phases will continue to operate in an interleaving fashion.

In [47], a digital controller is presented that allows a buck converter to recover from a large input voltage variation in minimal time. Similar to [41]–[46], the principle of capacitor charge balance is used to minimize the transient period. Although it was

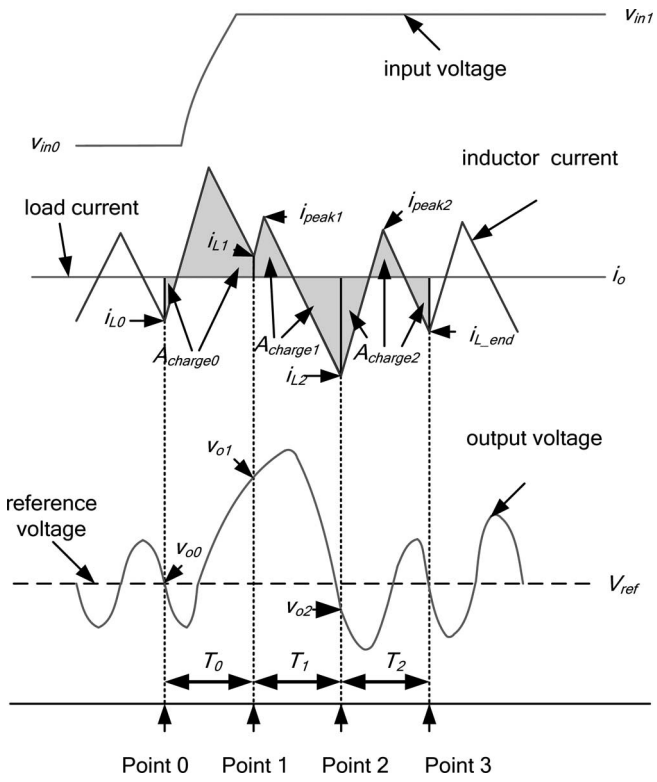

Fig. 19. Charge balance controller response to an input voltage transient.

previously stated that a buck converter can recover from a fast load variation with a single switching transition, it is demonstrated in [47] that at least two switching cycles are required to recover from a fast input voltage transient. The operation of the controller is illustrated in Fig. 19.

The duty cycles of the two switching periods following the input voltage transient (d_1 and d_2) are calculated using a complex set of algorithms, which ensure that $A_{\mathrm{charge0}} + A_{\mathrm{charge1}} + A_{\mathrm{charge2}} = 0$, i.e., the net capacitor charge integral area is zero between *point 0* and *point 3*. After the input voltage change is detected, the converter is capable of compensating for the input voltage change in the minimum possible time. However, it can be argued that if an analog current-programmed controller were used, the converter could be capable of reacting to the input voltage change faster than the nonlinear digital controller.

By combining the charge balance controller presented in [47] with one of the charge balance controller presented in [39]–[46], a controller that can intelligently react to a load current or input voltage transient will be yielded.

There have been many cases where digital controllers are designed based on analog designs. Interestingly, the introduction of digital control for power electronics sometimes spawns ideas in the analog domain. Although charge balance control has typically been thought of as an exclusively digital solution, due to its complexity, a subsequent analog design has been proposed in [48]. The method presented in [48] uses an analog differentiator to determine the output voltage valley point and uses double integrators to determine the proper switching instant based on the principle of capacitor charge balance. The approach may

not have been pursued had it not been for previous successful digital implementations.

Charge balance control is a concept that has generated numerous digital controllers and subsequent analog designs. The end result is a very fast reaction to transient events with minimal settling time. The main drawback is that charge balance control methods often require precise information regarding converter parameter information such as L and C or assume that the capacitor ESR is negligible.

VII. Conclusion

This paper has provided a brief review of the present-day topics in digital control of switching converters. As the cost of such controllers decrease and the controller requirements of switching converters become increasingly stringent, it is inevitable that digital controllers will become an integral part of the switching converter industry. Although there still exist some drawbacks to digital control, their unique capabilities such as efficiency optimization, autotuning, and nonlinear control will create a spot that cannot be filled by any analog controller.

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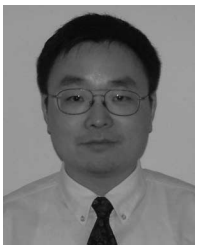

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