A 1-MHz, 12-V ZVS Nonisolated Full-Bridge VRM With Gate Energy Recovery

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***Abstract*—In this paper, a new self-driven zero-voltage-switching (ZVS) nonisolated full-bridge converter is presented for 12-V input VRM applications. The advantages of the new circuit are: 1) duty cycle extension; 2) ZVS of all the control MOSFETs; 3) lower voltage stress and reduced reverse recovery loss of the synchronous rectifier (SR) MOSFETs; 4) high-drive voltage to reduce $R_{DS(ON)}$ and the conduction loss of the SRs due to gate energy recovery capability; and 5) reduced body-diode conduction and no external drive IC chips with dead time control needed for SRs. Existing multiphase buck controllers and buck drivers can be directly used in the proposed converter. The experimental results verify the principle of operation and significant efficiency improvement. At 12 V input, 1.3 V output voltage, and 1 MHz switching frequency, the proposed converter improves the efficiency, using the buck converter from 80.7% to 83.6% at 50 A, and from 77.9% to 80.5% at 60 A. With two parallel SRs, the efficiency is further improved from 83.6% (single SR) to 84.7% (two SRs) and at 60 A, the efficiency is improved from 80.5% (single SR) to 83.2% (two SRs).**

***Index Terms*—Current-source driver (CSD), full-bridge (FB), self-driven, synchronous rectifier (SR), voltage regulator module (VRM), zero-voltage-switching (ZVS).**

I. Introduction

In HIGH-CURRENT and low-voltage applications, the output voltage of a voltage regulator module (VRM) keeps reducing, while the output currents are increasing consistently due to the high-power consumption of microprocessors. Meanwhile, the strict transient requirement [1] of the microprocessors is another serious challenge to VRMs. A large amount of expensive output capacitors are required to reduce the output voltage deviation during a transient event. On the other hand, due to limited real estate of the motherboard, the power density of VRMs has to be increased. Therefore, high-switching frequency (>1 MHz) operation of VRMs is strongly desired [2]–[6].

As it is known, frequency-dependent loss is one of the major barriers to achieve high-switching frequency operation, especially in the megahertz range. Multiphase buck converters are very popular for 12 V VRMs due to their simplicity and low cost. Nevertheless, buck converters suffer from extremely low duty cycle, which significantly increases the switching losses (especially during turn-OFF) and the reverse recovery loss of the body diode. More importantly, it has been noticed that the parasitic inductance, especially the common source inductance, has a serious propagation effect during the turn-OFF transition, and thus, leads the switching losses to increase even higher [7], [8]. Another important frequency-dependent loss is the excessive gate driver losses of the synchronous rectifier (SR) MOSFETs, which possess high total gate charge [9]–[11] for VRM applications above megahertz switching frequency.

In order to extend the extremely low duty cycle, the tapped inductor buck converter is proposed in [12], however, the leakage inductance due to the nonideal coupling of the coupled inductor causes high-voltage spikes over the main power MOSFET. Nonisolated half-bridge (NHB) converters with extended duty cycle are proposed in [13]–[16], which reduce the current stresses of the power MOSFETs and improve efficiency. A family of buck-type dc–dc converters including forward, push-pull, and half-bridge topologies, which take advantages of autotransformers, are proposed in [17]. Similarly, an autotransformer version converter with input current shaper for VRM applications is proposed in [18]. A two-stage approach is another promising alternative for 12 V VRM applications, as it can also achieve duty cycle extension and reduce the turn-OFF losses of the high-side power MOSFETs in a buck converter [19]–[22]. The issue of the two-stage approach is how to optimize the conversion efficiency of the two power stages in series. More power switches and passive components in two converters may also lead to an overall cost increase. Also, additional design efforts are required for the control design of the two-power stage approach. Unfortunately, in the aforementioned topologies, the control power MOSFETs are still under hard-switching condition, which results in high-switching losses at high frequencies (>1 MHz).

A phase-shift buck (PSB) converter featuring zero-voltage-switching (ZVS) and reduced SR conduction loss is proposed in [23]. This topology is able to form an autotransformer structure during the power transfer stages, which can significantly reduce the current stress of the transformer windings. However, as more active MOSFETs are used in the PSB converter and all control MOSFETs have floating grounds, the gate drive signals become complex, and therefore, external level-shift drive circuits must be used. In addition, paralleling more power MOSFETs, such as SRs, results in high-gate drive losses and makes the SRs, a hot spot in the VRM system.

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In order to recover the gate drive losses of the SRs, an improved self-driven 12 V VRM topology is proposed based on the PSB converter in [24]–[26], which achieves high efficiency and is attractive in VRM applications. Though a simple level-shift drive scheme is used, the drive path of the control MOSFETs goes through the synchronous MOSFETs, which increases the parasitic inductance, especially the common source inductance. This may result in high turn-OFF losses. Additionally, the drain-to-source voltage oscillation of the SRs due to the reverse recovery of the body diode, may cause high-voltage spikes over the control MOSFETs.

A nonisolated full-bridge (NFB) topology with direct energy transfer capability is proposed in [27] and [28]. Due to direct energy transfer capability, the current stresses of the transformer windings and the power MOSFETs are reduced. In this NFB topology, traditional phase-shift control is applied and auxiliary transformer windings are used to drive the SRs. The disadvantage of using the drive transformer self-driven scheme is that the leakage inductance causes the propagation delay of the SR drive signals, which results in high-conduction loss of the body diodes.

The objective of this paper is to present a new ZVS self-driven NFB converter, which can use existing multiphase buck controllers and buck drivers directly. The proposed topology achieves duty cycle extension and features ZVS, self-driven capability with SR gate energy recovery and reduced voltage stress over the SRs. Owing to the duty cycle extension, lower output inductors can be used and the reverse recovery losses of the body diodes can also be reduced. All these advanced features improve the efficiency significantly to achieve high-switching frequency and fast dynamic response. Section II presents the derivation of the proposed ZVS VRM and principle of operation. Section III presents the analysis of duty cycle loss, ZVS condition, and loss comparison. Section IV demonstrates the advantages of this new VRM topology. Section V contains the experimental results and discussion. Section VI provides a conclusion.

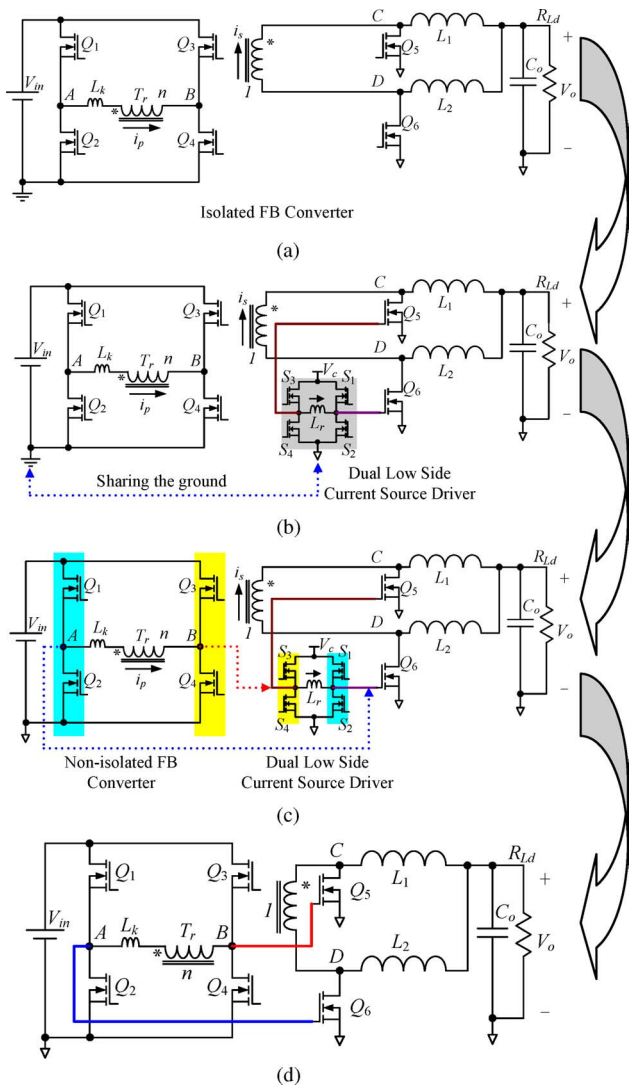

Fig. 1. Proposed ZVS self-driven NFB converter.

II. Proposed ZVS Self-Driven NFB VRM

In this section, the derivation of the proposed nonisolated topology and its operation will be described in detail. The target of the paper is to propose a new topology so that exiting drivers and controllers can be directly used with low cost and design efforts. The basic idea is to combine the two bridge legs of the isolated FB converter as the drive switches for the SRs. This driver is actually a current-source gate driver for the SRs and it eliminates any external SR drivers or auxiliary driver winding. Furthermore, due to the current-source gate driver structure, the gate energy of the SRs can also be recovered. This will help to apply high-gate drive voltage to the SRs with lower $R_{\mathrm{DS(ON)}}$ to reduce the conduction losses.

A. Derivation of Proposed ZVS NFB VRM

Fig. 1 illustrates the derivation of the proposed ZVS self-driven converter. Fig. 1(a) shows the conventional isolated FB converter with current-doubler rectifier for high-current applications. V_{in} is the input voltage, Q_1–Q_4 are the control MOSFETs, T_r is the power transformer (n is the turns ratio), L_k is the leakage of the transformer, and Q_5 and Q_6 are the SRs. L_1 and L_2 are the output filter inductors, and C_o is the output filter capacitor.

The derivation of the new converter includes the following steps.

1) In order to achieve fast switching and gate energy recovery, the dual low-side current source MOSFET driver, proposed in [29], is used to drive SR Q_5 and Q_6, as shown in Fig. 1(b). In this current-source driver (CSD), S_1–S_4 are the gate drive switches, L_r is the resonant inductor, and V_c is the drive voltage. According to the operation given in [29], in order to achieve the desired drive waveforms for Q_5 and Q_6, the asymmetrical control is applied to drive S_1–S_4.
2) It should be observed that for 12 V input VRM applications, there is no requirement for isolation. Therefore, it is possible to have the primary side of the transformer share the same ground of the secondary side as indicated in Fig. 1(b).

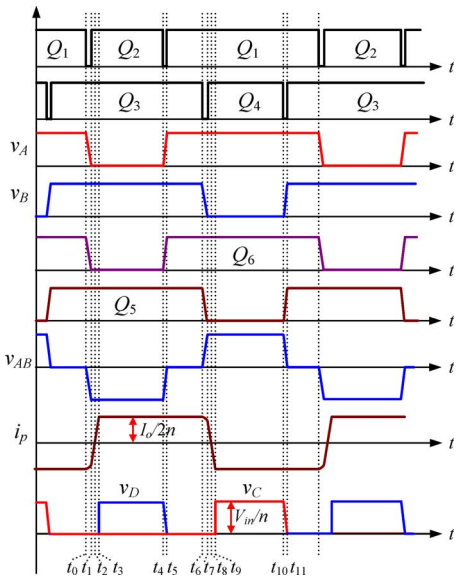

Fig. 2. Key waveforms of the proposed topology.

3) It is interesting to notice that the dual low-side current source gate drive circuit is also a FB structure. Though phase-shift control is generally used for the conventional FB converter, the asymmetrical control featuring ZVS capability can also be applied to two bridge legs of the FB converter, respectively, while the voltage applied to the primary side of the transformer is still symmetrical. The other benefit of the asymmetrical control is that existing buck drivers can be directly used to drive the upper and lower MOSFET in one bridge leg. Therefore, the drive switch pair (S_1 and S_2, and S_3 and S_4) can merge with the control MOSFETs (Q_1 and Q_2, and Q_3 and Q_4) of the primary side, respectively, as indicated in Fig. 1(c). At the same time, the resonant inductor L_r can merge with the leakage inductance L_k. The primary side of the transformer shares the same ground as the secondary side, which can provide the gate drive currents a path for the SRs Q_5 and Q_6. Therefore, by connecting the bridge leg midpoints of A and B to the gate terminals of Q_5 and Q_6, as shown in Fig. 1(d), the proposed FB VRM can be derived. Thus, $V_{\rm in}$ becomes the SR gate drive voltage.

Since the MOSFETs in the CSD emerge with the main power MOSFETs in the proposed circuit, there is no additional dead time control required for the SRs. In addition, the resonant inductor is eliminated, which helps to shrink the size of the converter and increase the power density. Meanwhile, owing to the gate energy recovery of the current-source gate driver, high-gate drive voltage can be applied to the SRs Q_5 and Q_6 to reduce the conduction losses further.

B. Principle of Operation

The key waveforms of the proposed topology are shown in Fig. 2. The purpose of the asymmetrical control, for each leg, is that Q_1 and Q_2, and Q_3 and Q_4 are complementarily controlled with the dead time set to achieve ZVS. It is noted that the primary voltage $v_{\rm AB}$ is still a symmetrical waveform. In this case, Q_1 and Q_3 are the upper control MOSFETs; Q_2 and Q_4 are the lower control MOSFETs. The duty cycle D of the new converter is defined as follows:

$$D = \frac{T_{\text{ON\_}Q_2}}{T_s} \tag{1}$$

where $T_{\text{ON\_}Q_2}$ is the ON time of Q_2 and T_s is the switching period.

There are twelve switching modes in a switching period. Accordingly, the equivalent circuits in half of a switching cycle are shown in Fig. 3. D_1–D_4 are the body diodes and C_1–C_4 are the intrinsic output capacitors of Q_1–Q_4, respectively, assuming $C_1 = C_2 = C_3 = C_4 = C_{\rm oss}$. $C_{\text{gs\_}Q_5}$ and $C_{\text{gs\_}Q_6}$ are the input capacitors of SRs Q_5 and Q_6, respectively, assuming $C_{\text{gs\_}Q_5} = C_{\text{gs\_}Q_6} = C_{\rm gs}$. The output inductors are large enough to be regarded as current sources. The inductor currents $i_{L_1} = i_{L_2} = I_0/2$, where I_o is the total output current.

1) Mode 1 [t_0, t_1] [see Fig. 3(a)]. Prior to t_0, Q_1 and Q_3 are on, the voltage over the primary side and the secondary side of the transformer is zero. The gate drive voltages of the SR Q_5 and Q_6 are all clamped high to the input voltage. At t_0, Q_1 turns off, the primary current i_p charges C_1 and discharges C_2 and $C_{\text{gs\_}Q_6}$ at the same time. As C_1 and C_2, and $C_{\text{gs\_}Q_6}$ limit the slew rate of the voltage of C_1, Q_1 is under zero-voltage turn-OFF condition. It should be noted that the gate drive energy of the SR capacitance $C_{\text{gs\_}Q_6}$ is returned to the input voltage source so that the high-gate drive losses of SRs can be significantly reduced.
During this stage, the energy to discharge C_2 and $C_{\text{gs\_}Q_6}$ is provided by the leakage inductance of the transformer. i_p decreases resonantly as follows:

$$i_p(t) = \frac{I_o}{2n}\cos\omega_r(t - t_0) \tag{2}$$

$$v_{c_2} = v_{\text{gs\_}Q_6} = V_{\rm in} - Z_r\frac{I_o}{2n}\sin\omega_r(t - t_0) \tag{3}$$

where

$$\omega_r = 1/\sqrt{L_k(2C_{\rm oss} + C_{\rm gs})},\ Z_r = \sqrt{L_k/(2C_{\rm oss} + C_{\rm gs})}.$$

At t_1, $v_{c_1} = V_{\rm in}$ and $v_{c_2} = 0$, D_2 conducts, which provide a zero-voltage turn-ON condition for Q_2. The interval of [t_0, t_1] and the value of i_p at t_1 are as follows:

$$t_{1,0} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{2nV_{\rm in}}{Z_r I_o}\right) \tag{4}$$

$$I_p(t_1) = \frac{I_o}{2n}\sqrt{1 - \left(\frac{2nV_{\rm in}}{Z_r I_o}\right)^2}. \tag{5}$$

2) Mode 2 [t_1, t_3] [see Fig. 3(b)]. During this stage, i_p decreases and is not enough to power the load. i_{L_1} freewheels through the body diode of Q_5 and i_{L_2} freewheels through Q_6. At t_2, i_p increases inversely, but is still not large enough to power the load.
3) Mode 3 [t_3, t_4] [see Fig. 3(c)]. At t_3, i_p rises to the reflected load current causing D_3 to turn-OFF. During this stage, the voltage over the transformer is the input voltage and the

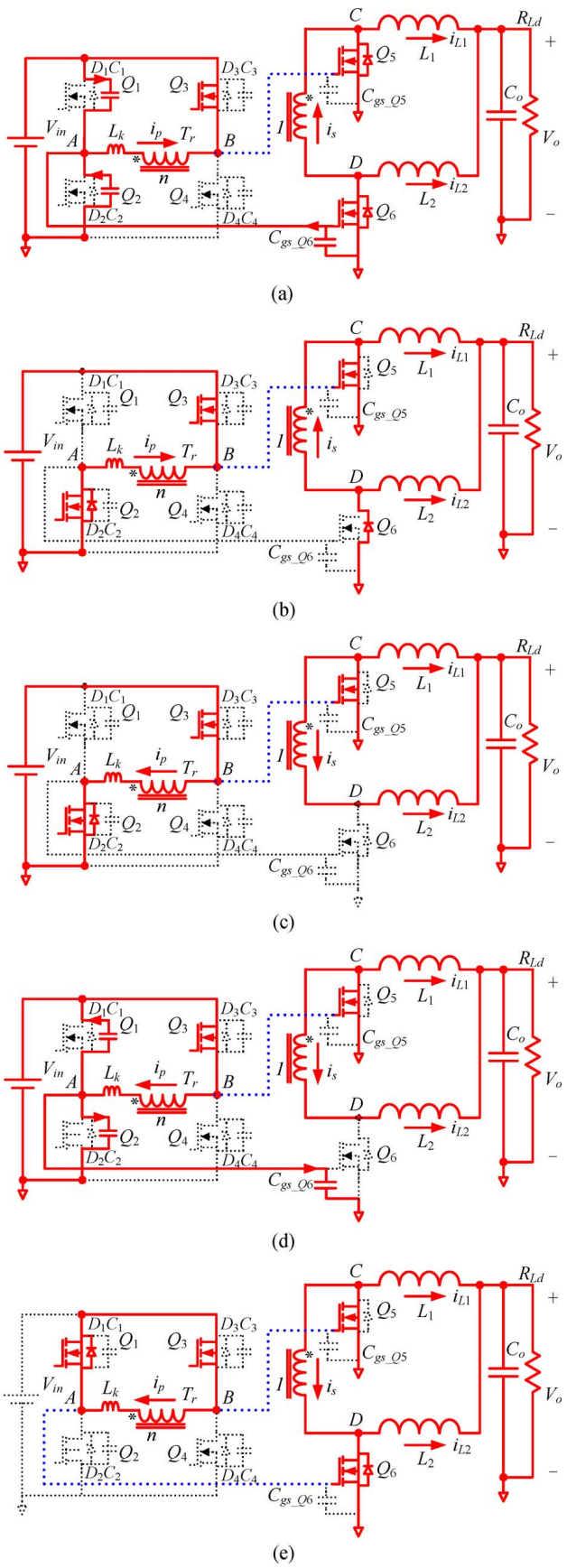

Fig. 3. Equivalent circuits of operation. (a) $[t_0, t_1]$. (b) $[t_1, t_3]$. (c) $[t_3, t_4]$. (d) $[t_4, t_5]$. (e) $[t_5, t_6]$.

energy transfers from the primary side of the transformer to the load.

4) Mode 4 $[t_4, t_5]$ [see Fig. 3(d)]. At t_4, Q_2 turns off, the primary current i_p charges C_2 and $C_{\mathrm{gs}\_Q_6}$ and discharges C_1. As C_1 and C_2, and $C_{\mathrm{gs}\_Q_6}$ limit the slew rate of the voltage of C_2, Q_2 is under zero-voltage turn-OFF condition. During this stage, the energy to discharge C_1 is provided by the leakage inductance and L_1. L_1 is large enough to be regarded as a constant current source so that the primary current i_p keeps the value $I_{p_2} = I_{L_1}/n$, where I_{L_1} is the dc current of L_1. The voltage C_2 rises linearly and the voltage of C_2 decays linearly.

$$t_{5,4} = \frac{2nV_{\mathrm{in}}(2C_{\mathrm{oss}} + C_{\mathrm{gs}})}{I_o}. \tag{6}$$

5) Mode 5 $[t_5, t_6]$ [see Fig. 3(e)]. At t_5, D_1 conducts, which provides a zero-voltage turn-ON condition for Q_1. The voltage over the primary side is zero. The gate drive voltages of the SRs Q_5 and Q_6 are all clamped high to the input voltage again. At t_6, the other half of switching cycle starts and the principle of operation is similar except for polarity changes.

III. Topology Extension

A. Multiphase Interleaving Nonisolated ZVS Self-Driven Converters

With the increasing high current demanding of the microprocessors, the output current of the VRMs for desktop and server is beyond 100 A, and will reach 150 A in the near future. In order to meet this high current requirement, multiphase buck converters are widely used as the solution of today's VRM architecture. However, as mentioned earlier, the buck converter has low efficiency due to the high turn-OFF loss at high frequency (>1 MHz).

To provide high-output current (>100 A), two proposed nonisolated ZVS self-driven FB converters can be paralleled, as shown in Fig. 4. The gate drive control signals for each bridge can be interleaved to achieve ripple cancellation effect. All the advantages of the proposed nonisolated ZVS self-driven FB converter are maintained in this structure. Additionally, commercial available multiphase buck controllers can be directly used for the control of the converter.

B. ZVS Self-Driven NFB Converter with Reduced Gate Drive Voltage

From the analysis in Section II, the proposed self-driven NFB converter has advantages over the conventional buck converter. On the other hand, in the near future, the low-voltage rating SRs with round 12 V can only sustain less than 10 V gate drive voltage. Therefore, the input voltage 12 V will not be suitable to drive these low-voltage rating SRs anymore. In order to solve this problem, an improved ZVS self-driven FB topology with reduced the gate drive voltage is proposed, as shown in Fig. 5.

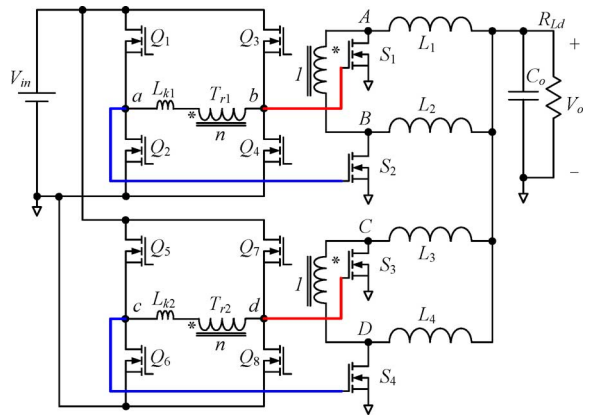

Fig. 4. Nonisolated ZVS self-driven FB converters with parallel configuration.

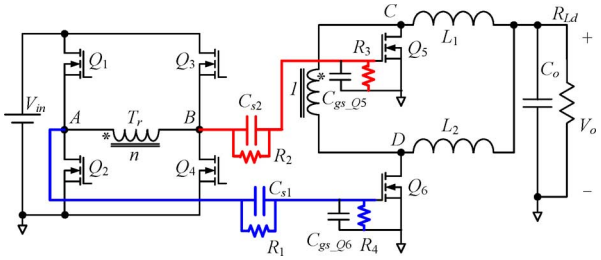

Fig. 5. Proposed ZVS self-driven FB VRM with reduced gate drive voltage using voltage dividers.

In Fig. 5, $C_{\mathrm{gs\_}Q_5}$ and $C_{\mathrm{gs\_}Q_6}$ are the internal gate capacitance of SR Q_5 and Q_6. C_{s_1}, C_{s_2}, $R_1, R_2, R_3,$ and R_4 with $C_{\mathrm{gs\_}Q_5}$ and $C_{\mathrm{gs\_}Q_6}$ form voltage dividers.

Assuming $R_1 = R_2 = R_s$, $R_3 = R_4 = R_p$, and $C_{s_1} = C_{s_2} = C_s$, the gate drive voltage across of the SRs is as follows:

$$V_{\mathrm{gs\_}Q_5} = V_{\mathrm{gs\_}Q_5} = \frac{C_s V_{\mathrm{in}}}{C_s + C_{\mathrm{gs}}}. \tag{7}$$

At the same time, in order to make the simultaneous gate drive voltage has the same phase with the voltage v_A and v_B, which should be satisfied as follows:

$$C_s R_s = C_{\mathrm{gs}} R_p. \tag{8}$$

The most important advantage of the proposed converter is that the gate voltage can be chosen for optimal design and safe operation when the input voltage value is not suitable to drive low-voltage rating SRs directly. Fig. 6 illustrates the waveforms using the voltage driver. It is observed that the gate drive voltage $v_{\mathrm{GS\_}Q_5}$ is in the same phase of v_A and the gate voltage is reduced from 12 to 8 V.

IV. Duty Cycle Loss, ZVS Condition, and Loss Analysis

A. Duty Cycle Loss

As shown in Fig. 2, during $[t_0, t_3]$ and $[t_6, t_9]$, the leakage inductance of the transformer limits the rise (or decay) slope of i_p. Finite time is required for i_p to make the transition from the positive direction to the negative direction (or vice-versa). During this transition time, v_{AB} is $+V_{\mathrm{in}}$ or $-V_{\mathrm{in}}$, i_p is lower

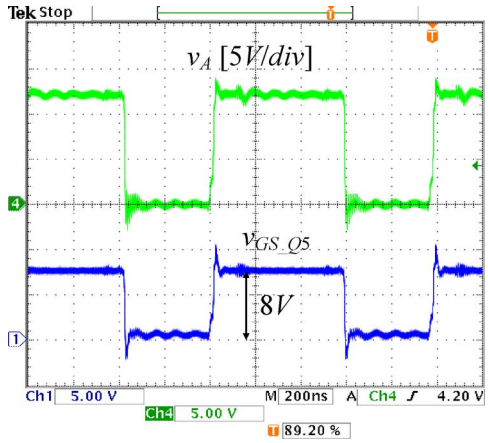

Fig. 6. Waveforms of v_A and reduced gate drive voltage $v_{\mathrm{GS\_}Q_5}$ using voltage dividers. $V_{\mathrm{in}} = 12$ V, $f_s = 1$ MHz, $R_1 = R_2 = 21\ k\Omega$, $R_3 = R_4 = 12\ k\Omega$, $C_{s_1} = C_{s_2} = 3.3$ nF, and $C_{\mathrm{GS\_}Q_5} = C_{\mathrm{GS\_}Q_6} = 5.7$ nF.

than the reflected load current and all the SR diodes conduct. This makes the secondary rectified voltage v_A and v_B zero, thus, v_{AB} loses the voltage in $[t_0, t_3]$ and $[t_6, t_9]$, respectively.

The duty cycle loss D_{loss} during $[t_0, t_3]$ and $[t_6, t_9]$ is as follows:

$$D_{\mathrm{loss}} = \frac{I_o}{nT_s}\frac{L_k}{V_{\mathrm{in}}} \tag{9}$$

where I_o is the output current, L_k is the leakage inductance, and n is the transformer turns ratio. It is noted that the leakage inductance of the transformer should be minimized to reduce the duty cycle loss.

B. Condition of ZVS

From Fig. 1(d), for the upper control MOSFETs (Q_1 and Q_3), the energy to achieve ZVS is provided by the output inductors,therefore it should be satisfied as follows:

$$\frac{1}{2}L_f\left(\frac{I_o}{2n}\right)^2 \geq \frac{1}{2}C_1 V_{\mathrm{in}}^2 + \frac{1}{2}(C_2 + C_{\mathrm{gs\_}Q_5})V_{\mathrm{in}}^2$$
$$= C_{\mathrm{oss}} V_{\mathrm{in}}^2 + \frac{1}{2}C_{\mathrm{gs\_}Q_5} V_{\mathrm{in}}^2 \tag{10}$$

where L_f is the output filter inductance, $C_1 = C_2 = C_{\mathrm{oss}}$ (output capacitances of Q_2 and Q_4) and $C_{\mathrm{gs\_}Q_5}$ is the gate capacitance of Q_5. Since, L_f is usually large enough to provide the energy, Q_1 and Q_3 can achieve ZVS in a wide load range.

From Fig. 1(a), for the lower control MOSFETs (Q_2 and Q_4), the energy to realize ZVS is provided by the leakage inductance of the transformer, therefore it should be satisfied as follows:

$$\frac{1}{2}L_k\left(\frac{I_o}{2n}\right)^2 \geq \frac{1}{2}C_1 V_{\mathrm{in}}^2 + \frac{1}{2}(C_2 + C_{\mathrm{gs\_}Q_5})V_{\mathrm{in}}^2$$
$$= C_{\mathrm{oss}} V_{\mathrm{in}}^2 + \frac{1}{2}C_{\mathrm{gs\_}Q_5} V_{\mathrm{in}}^2 \tag{11}$$

where L_k is the leakage inductance of the transformer. It is noted that the larger leakage inductance, the easier to achieve ZVS. However, the larger leakage inductance results in higher duty cycle loss. The leakage inductance L_k can be chosen based on

(11) depending on ZVS range

$$L_k \geq \frac{2C_{\rm oss}V_{\rm in}^2 + C_{{\rm gs}\_Q_5}V_{\rm in}^2}{(I_{o\_{\rm ZVS}}/2n)^2}. \quad (12)$$

As an example, for $V_{\rm in} = 12$ V, $V_o = 1.3$ V, $n = 3$, $C_{\rm oss} = 0.65$ nF, and $C_{{\rm gs}\_Q_5} = 6.6$ nF, in order to achieve ZVS at $I_{o\_{\rm ZVS}} = 40$ A, from (12), the leakage inductance can be calculated as 25 nH.

C. Loss Analysis

A detailed loss analysis of the proposed converter in Fig. 1(d) is given in this section. These losses include: 1) switching loss; 2) gate drive loss and conduction loss of control MOSFETs; 3) body-diode-conduction loss and reverse recovery loss; 4) gate drive loss and conduction loss of SRs; 5) loss of planar transformer; and 6) conduction loss of output inductors.

1) Switching Losses: Due to ZVS, there is no turn-ON losses for the control MOSFETs. To calculate the turn-OFF loss, the piecewise linear loss mode in [30] is used here. The turn-OFF losses of the control MOSFETs are as follows:

$$P_{\rm turn\_OFF} = 4I_{\rm OFF}V_{\rm ds}t_{\rm sw\_OFF}f_s = 4\frac{I_o}{2n}V_{\rm in}t_{\rm sw\_OFF}f_s = \frac{2}{n}I_oV_{\rm in}t_{\rm sw\_OFF}f_s \quad (13)$$

where $I_{\rm OFF}$ is the turn-OFF current, $V_{\rm ds}$ is the drain-to-source voltage, $t_{\rm sw\_OFF}$ is the turn-OFF transition time, f_s is the switching frequency, and I_o is the output current.

2) Conduction Losses of Control MOSFETs: The rms current flowing through Q_1 and Q_3 is as follows:

$$I_{\rm rms1} = \frac{1}{2}I_o\sqrt{1-D} \quad (14)$$

where D is the duty cycle.

The rms current flowing through Q_2 and Q_4 is as follows:

$$I_{\rm rms2} = \frac{1}{2}I_o\sqrt{D}. \quad (15)$$

From (14) and (15), the total conduction losses of Q_1–Q_4 is as follows:

$$P_{\rm cond\_control\ FET} = I_{\rm rms1}^2R_{\rm DS\_control\ FET}2 + I_{\rm rms2}^2R_{\rm DS\_control\ FET}2 = \frac{I_o^2}{2n^2}R_{\rm DS\_control\ FET} \quad (16)$$

where $R_{\rm DS\_control\ FET}$ is the on-resistance of Q_1–Q_4, assuming Q_1–Q_4 are the same.

3) Gate Drive Losses of Control MOSFETs: For the conventional driver, the gate energy loss due to charging and discharging the gate capacitance of Q is given by following equation, where Q_g represents the total gate charge, $V_{\rm gs}$ is the driving voltage, and f_s is the switching frequency.

$$P_g = Q_gV_{\rm gs}f_s. \quad (17)$$

From (17), therefore, the gate drive losses of Q_1–Q_4 are as follows:

$$P_{\rm controlFET} = 4P_g = 4Q_gV_{\rm gs}f_s \quad (18)$$

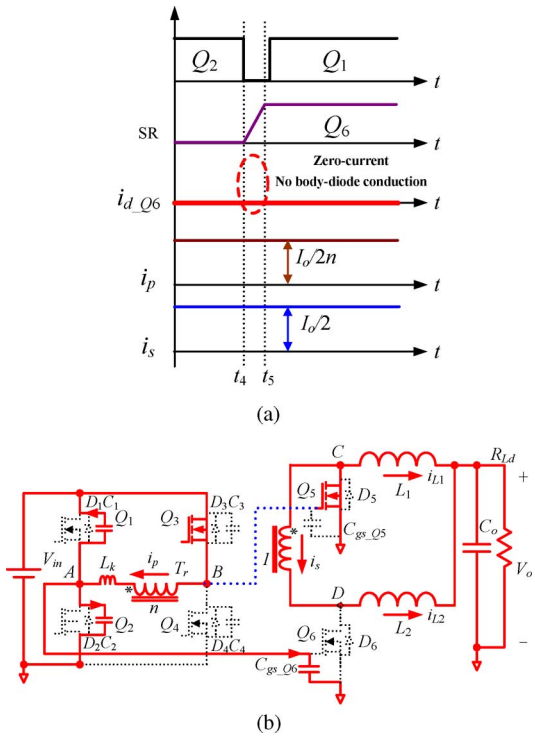

Fig. 7. Key waveforms of turn-ON transition and equivalent circuit of SR Q_6. (a) Turn-ON transition. (b) $[t_4, t_5]$.

assuming Q_1–Q_4 are the same and $V_{\rm gs}$ is usually 5 V. It should be pointed out that the gate drive loss can be reduced, since the $Q_{\rm gd}$ charge is eliminated due to the zero-voltage turn-ON condition of the control MOSFETs. For example, for Vishay Si7368DP with $Q_{\rm gd} = 4.5$ nC and $Q_g = 17$ nC at $V_{\rm gs} = 5$ V, the gate drive loss can be reduced by 26% for the primary power MOSFETs owing to ZVS.

4) Body-Diode Loss and Reverse Recovery Loss of SR: SR Q_6 is used to illustrate the calculating of the body-diode-conduction loss. Fig. 7 illustrates the waveforms of SR Q_6 turn-ON transition and its corresponding equivalent circuit.

In Fig. 7(b), for the turn-ON transition $[t_4, t_5]$ of SR Q_6, the primary current i_p is the reflected current from the load and charges C_2 and $C_{{\rm gs}\_Q_6}$ linearly until $v_{{\rm gs}\_Q_6}$ reaches the input voltage at t_5 causing SR Q_6 to turn-ON. Then the primary side of the transformer is clamped at zero-state and i_p equals $I_o/2n$. Though SR Q_6 turns on before t_6, the drain current of Q_6 remains zero during the zero-state. Therefore, there is no body-diode conduction for the turn-ON transition of SR Q_6, as shown in Fig. 7(a).

Fig. 8 illustrates the waveforms of the turn-OFF transition of SR Q_6 and its corresponding equivalent circuit. In Fig. 8(b), for the turn-OFF transition $[t_0, t_1]$, at t_0, Q_1 turns off and the leakage inductance L_k starts to resonate with the capacitance C_2 and $C_{{\rm gs}\_Q_6}$ until $v_{{\rm gs}\_Q_6}$ reaches zero at t_1, which means SR Q_6 turns off. The current through Q_6 then transfers to the body diode D_6 until i_p changes its polarity and reaches the load current of $I_o/2n$ at t_3. Therefore, from t_1 to t_3, as shown in the shaded area, the body diode conducts as shown in Fig. 8(a).

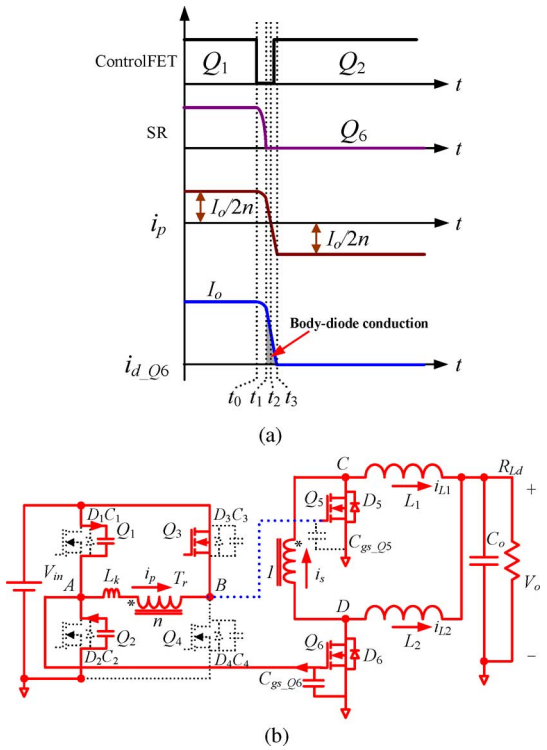

Fig. 8. Key waveforms of turn-OFF transition and equivalent circuit of SR Q_6. (a) Turn-OFF transition. (b) $[t_0, t_1]$.

From (5), at t_1, the current of the body diode $I_{d\_Q_6}(t_1)$ is as follows:

$$I_{d\_Q_6}(t_1) = \frac{I_o}{2}\left(1 + \sqrt{1 - \left(\frac{2nV_{\text{in}}}{Z_r I_o}\right)^2}\right) \tag{19}$$

where $Z_r = \sqrt{L_k/(2C_{\text{oss}} + C_{\text{gs}})}$.

At t_3, $I_{d\_Q_6}$ reaches zero, therefore the conduction time of the body diode is as follows:

$$t_{13} = \frac{L_k I_o}{2nV_{\text{in}}}\left(1 + \sqrt{1 - \left(\frac{2nV_{\text{in}}}{Z_r I_o}\right)^2}\right). \tag{20}$$

From (19) and (20), the total conduction losses of the body diodes of the two SRs is as follows:

$$P_{\text{body\_diode}} = \frac{1}{2} I_{d\_Q_6}(t_1) V_F t_{13} f_s 2$$

$$= \frac{L_k I_o^2 V_F f_s}{4nV_{\text{in}}}\left(1 + \sqrt{1 - \left(\frac{2nV_{\text{in}}}{Z_r I_o}\right)^2}\right)^2 \tag{21}$$

where V_F is the forward voltage drop of the body diode and f_s is the switching frequency. It is noted that the conduction loss of the body diode is proportional to the leakage inductance of the transformer. The larger leakage inductance results in a longer time required $[t_1, t_3]$, as shown in Fig. 8(b), for the primary current to change its polarity, thus resulting in a higher body-diode-conduction loss.

TABLE I
CIRCUIT PARAMETERS FOR LOSS ANALYSIS COMPARISON

Switching Frequency f_s	1 MHz
Input Voltage V_{in}	12 V
Output Voltage V_o	1.3 V
Output Current I_o (two phases)	Up to60 A
Control MOSFET	**Si7368DP**
Q_g@V_{GS}=5V	17 nC
$R_{DS(on)}$@V_{GS}=5V	8.2 mΩ
R_g	1.5 Ω
SR	**IRF6691**
$R_{DS(on)}$@V_{GS}=12V	1.7 mΩ
Q_g@V_{GS}=12V	100 nC
V_f	0.7 V
R_g	0.6 Ω
Q_{rr}	40 nC
Power Transformer	**PQ50**
Turns ratio	n=3:1
Core materials	3F5
Output Inductor	**LP02-191-5**
Inductance	190 nH
DCR	0.2 mΩ

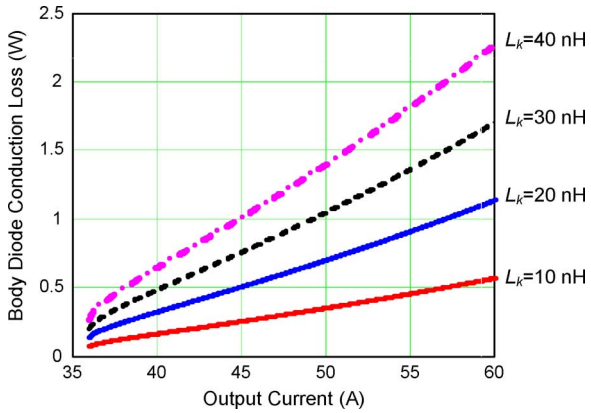

Fig. 9. Body-diode-conduction loss as a function of output current (two phases) with different leakage inductances.

The parameters for the loss analysis and comparison are given in Table I. The leakage inductance of the power transformer has a direct impact on the body diode and ZVS range of the circuit. The effect of the leakage on the body-diode-conduction loss from (21) is given in Fig. 9. In order to reduce the body-diode-conduction loss, the leakage inductance needs to be minimized, using the printed circuit board (PCB) planar transformer technique. At the same time, the lower leakage inductance will also help to reduce the duty cycle loss from (9) when the switching frequency is above 1 MHz, but it will reduce the range of ZVS operation and increase the switching losses. Using the parameters in Table I and according to (12), if the range of ZVS operation is 2/3 of the load current (I_o = 60 A), the leakage inductance should be chosen as 25 nH.

The reverse recovery loss of the body diode is $P_{\text{rr}} = Q_{\text{rr}} \cdot V_s \cdot f_s$, where $V_s = V_{\text{in}}/n$, which is the block voltage of the SR body diode. For the buck converter, the switching node voltage V_s is

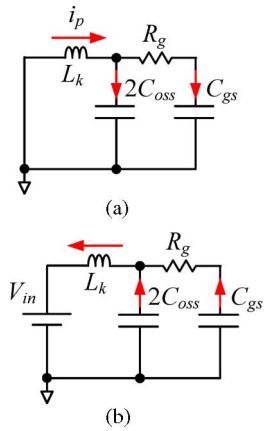

Fig. 10. Key waveforms of turn-ON transition and turn-OFF transition of SR Q_6. (a) Turn-ON transition $[t_4, t_5]$. (b) Turn-OFF transition $[t_0, t_1]$.

12 V. For the proposed NFB converter with $n = 3$, V_s is 4 V. Therefore, the reverse recovery loss can be reduced by 67%.

5) Conduction Loss of SRs: The rms current of the SR is as follows:

$$I_{\mathrm{SR\_rms}} = I_o\sqrt{(1-D)}. \tag{22}$$

Therefore, the conduction loss of the SRs is as follows:

$$P_{\mathrm{cond\_SR}} = 2I_{\mathrm{SR\_rms}}^2 R_{\mathrm{DS(ON)\_SR}} = 2I_o^2(1-D)R_{\mathrm{DS(ON)\_SR}} \tag{23}$$

where $R_{\mathrm{DS(ON)\_SR}}$ is the on resistance of the SRs.

6) Gate Drive Loss of SRs: As discussed in Section II, the gate driver for the SRs is actually a CSD, which can achieve gate energy recovery. The efficiency of the gate energy recovery depends on the gate mesh resistance R_g. The equivalent circuits of the turn-ON transition and turn-OFF transition of the SRs are given in Fig. 10, assuming the output capacitance $C_{\mathrm{oss\_}Q_3} = C_{\mathrm{oss\_}Q_4} = C_{\mathrm{oss}}$, gate capacitance $C_{\mathrm{gs\_}Q_5} = C_{\mathrm{gs\_}Q_6} = C_{\mathrm{gs}}$, and $R_{\mathrm{g\_}Q_5} = R_{\mathrm{g\_}Q_6} = R_{\mathrm{g}}$. As seen from Fig. 10, the gate drive current goes through the MOSFET internal mesh resistance and causes resistive loss at R_g.

During the charging transition $[t_4, t_5]$, the primary current i_p is the reflected load current, which means it can be regarded as a constant current source. The resistive loss through R_g is as follows:

$$P_{R\_\mathrm{ON}} = 2\left(\frac{C_{\mathrm{gs}}}{2C_{\mathrm{oss}}+C_{\mathrm{gs}}}\frac{I_o}{2n}\right)^2 R_g t_{54} f_s \tag{24}$$

where $t_{54} = \frac{2nV_{\mathrm{in}}(2C_{\mathrm{oss}}+C_{\mathrm{gs}})}{I_o}$, from (6).

During the discharging transition $[t_0, t_1]$, the primary current i_p resonates with C_{oss} and C_{gs}. The resistive loss over R_g is as follows:

$$P_{R\_\mathrm{OFF}} = 2\int_{t_0}^{t_1}\left(\frac{C_{\mathrm{gs}}}{2C_{\mathrm{oss}}+C_{\mathrm{gs}}}\frac{I_o}{2n}Cos\omega_r t\right)^2 R_g dt\cdot$$

$$f_s = \frac{2C_{\mathrm{gs}}^2}{(2C_{\mathrm{oss}}+C_{\mathrm{gs}})^2}R_g f_s\int_{t_0}^{t_1}\left(\frac{I_o}{2n}Cos\omega_r t\right)^2 dt \tag{25}$$

where $t_{1,0} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{2nV_{\mathrm{in}}}{Z_r I_o}\right)$, from (4).

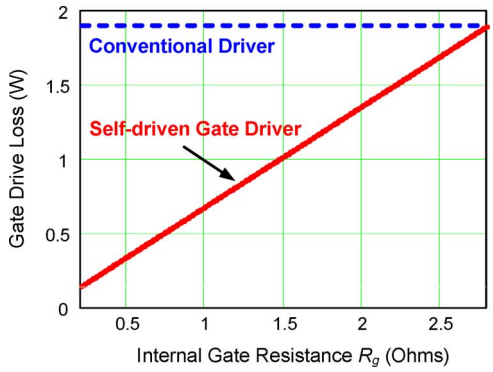

Fig. 11. SR gate drive loss as function of MOSFET internal mesh resistance R_g.

Using the parameters given in Table I, a curve of the self-driven gate circuit loss as a function of R_g is given in Fig. 11 to demonstrate the potential benefits of using MOSFETs with lower R_g.

7) Loss of Planar Transformer: The loss of the power transformer includes the copper loss and the core loss.

The copper loss of the inductor winding is as follows:

$$P_{\mathrm{copper}} = R_{\mathrm{ac}}\left(\frac{I_o}{2n}\right)^2 \tag{26}$$

where R_{ac} is the ac resistance of the primary winding and n is the turns ratio.

For the core loss, RM50 (TDK 3F5) is used for the experimental prototype. The loss P_{core} can be calculated as follows:

$$P_{\mathrm{core}} = K_1 f_s^x B_{\mathrm{pk}}^y V_e \tag{27}$$

$$B_{\mathrm{pk}} = \frac{DV_{\mathrm{in}}}{2nA_e f_s}. \tag{28}$$

For RM50 (TDK 3F5), $K_1 = 0.0087$, $x = 2.045$, $y = 2.98$, $A_e = 23.7$ mm^2, and $V_e = 530$ mm^3, $P_{\mathrm{core}} = 0.2$ W.

8) Conduction Loss of Output Inductors: The conduction loss of the output inductor is as follows:

$$P_{\mathrm{ind}} = \frac{I_o^2}{2}\left[1+\left(\frac{\Delta i}{I_o/2}\right)^2\right]R_{\mathrm{dc}} \tag{29}$$

where Δi is the current ripple of the output inductor and R_{dc} is the dc resistance of the output inductor. As compared with a buck converter, in order to maintain same inductor current ripple, due to the duty cycle extension, the output inductor value of the proposed converter is reduced from 300 to 190 nH (a reduction of 35%). This gives a reduction of R_dc from 1.2 to 1.0 mΩ (a reduction of 20%), which means a reduction of 20% of the conduction loss.

D. Loss Comparison

Based on the loss analysis using the parameters in Table I, Fig. 12 illustrates the loss breakdown of the proposed converter. For comparison, Fig. 12 also illustrates the loss breakdown of the two-phase buck converter with $V_{\mathrm{in}} = 12$ V, $V_o = 1.3$ V, $I_o = 30 \times 2$ A, and $f_s = 1$ MHz. ZVS feature of the proposed

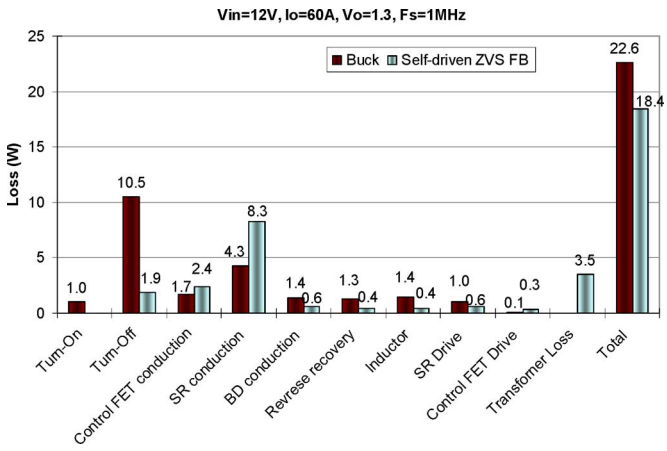

Fig. 12. Loss breakdown comparison between the buck converter and the self-driven ZVS FB converter.

topology reduces the switching loss, especially the turn-OFF loss (9.6 W, 12.3% of the output power), in the buck converter. ZVS achievement also helps to reduce the electromagnetic interference (EMI) of the switching power converter. Thus, smaller EMI filters can be used. Other frequency-dependent losses including body-diode-conduction loss, reverse recovery loss, and gate drive loss are all reduced. In additional, the output inductor conduction loss is also reduced, since lower value inductors can be used owing to the duty cycle extension. However, the SR conduction loss is increased due to the circulating currents in the FB structure topology and an additional transformer winding loss has to be taken into account. But the overall loss reduction is 4.2 W, which translates into a reduction of 5.4% of the total output power, 4.2 W/(1.3 V $\times$ 60 A).

V. Advantages of Proposed ZVS Self-Driven FB VRM

Based on the principle of operation and analysis, the advantages of the proposed nonisolated converter are highlighted as follows.

A. Duty Cycle Extension

The voltage gain of the proposed converter is given as follows:

$$V_o = \frac{V_{\rm in}}{n} D \tag{30}$$

where $V_{\rm in}$ is the input voltage, D is the duty cycle, V_o is the output voltage, and n is the transformer turns ratio.

As an example, in order to achieve $V_{\rm in} = 12$ V, and $V_o = 1.3$ V, $n = 3$, the required duty cycle is $D = 0.33$. However, for the same output voltage and input voltage, the duty cycle of a buck converter is only 0.11. Therefore, the duty cycle is extended by three times. For $V_{\rm in} = 12$ V, $V_o = 1.3$ V, $I_o = 60$ A, and $f_s = 1$ MHz, with the current ripple of 4 A, the output inductor of the proposed converter is 190 nH compared to 300 nH of the buck converter, which leads to better current ripple cancellation so that smaller output inductors with lower conduction loss can be used. The lower inductance value also helps to improve the dynamic response of the converter and reduces the number of the output capacitors during step load transient.

B. ZVS of the Control MOSFETs With Low Voltage Stress

For a buck converter, the switching loss of the control FET is as follows:

$$P_{Q_1} = \frac{1}{2} V_{\rm in} I_{({\rm ON})\_Q_1} t_{{\rm sw}({\rm ON})\_Q_1} f_s + \frac{1}{2} V_{\rm in} I_{({\rm OFF})\_Q_1} t_{{\rm sw}({\rm OFF})\_Q_1} f_s \tag{31}$$

where $I_{({\rm ON})\_Q_1}$ is the turn-ON current and $I_{({\rm OFF})\_Q_1}$ is the turn-OFF current, $t_{{\rm sw}({\rm ON})\_Q_1}$ is the turn-ON time and $t_{{\rm sw}({\rm OFF})\_Q_1}$ is the turn-OFF time.

For the proposed converter, owing to asymmetrical control used to achieve ZVS, there is no turn-ON losses. The turn-OFF losses are as follows:

$$P_{\rm turn\_OFF} = 4P_{Q_1} = \frac{2}{n} V_{\rm in} I_{({\rm OFF})} t_{{\rm sw}({\rm OFF})} f_s. \tag{32}$$

In a practical design, for instance, for $V_{\rm in} = 12$ V, $V_o = 1.3$ V, $n = 3$, switching frequency 1 MHz, output inductance $L_f = 300$ nH, and total output current $I_o = 60$ A, for two-phase buck converters, the turn-OFF current of each control MOSFETs is 35 A and the total turn-OFF current is 70 A. However, for the new converter, the turn-OFF current of the control MOSFETs is only 10 A and the total turn-OFF current is 40 A (a reduction of 43%). This results in a high reduction of turn-OFF loss due to the duty cycle extension.

For a conventional buck converter, due to the reverse recovery of the body diode, the peak voltage of the switching node with the ringing will become higher than 20 V. Therefore, a 30-V MOSFET is generally used for the control MOSFETs. However, in the proposed converter, the voltage stress of the control MOSFETs is the input voltage (12 V, usually), therefore, a 20-V MOSFETs with lower on-resistance $R_{{\rm DS}({\rm ON})}$ can be used to reduce the conduction loss.

C. Gate Energy Recovery of SRs and Reduced Body-Diode Conduction

One of the most important advantages of the proposed topology is the self-driven capability so that no drive ICs are needed, which reduces the cost of the converter. In addition, it is an inherent adaptive drive control for SRs. Therefore, no additional dead time control circuit is needed anymore.

With the self-driven control, the dead time is minimized to reduce the body-diode-conduction loss. For the turn-ON transition, there is no body-diode conduction. For the turn-OFF transition, the body-diode conduction is minimized. More importantly, the self-driven topology actually forms a CSD, using the leakage inductance of the transformer to achieve gate energy recovery of SRs. This is beneficial at high-switching frequency operation (>1 MHz) and allows for high-drive voltages (input voltage, usually 12 V) for SRs to achieve lower $R_{{\rm DS}({\rm ON})}$ and reduce the conduction loss further. Compared to 5 V drive voltage for the SRs, the $R_{{\rm DS}({\rm ON})}$ value with 12 V drive voltage is reduced by 20% [31]. This translates into a 20% reduction of the SR conduction loss.

D. Reduced Conduction Losses and Reverse Recovery Losses of SRs

Because of the voltage spikes due to the parasitics in a buck converter, 30 V rated MOSFETs are generally used as SRs in 12 V input buck converters due to the parasitics. Due to the transformer, the voltage stress of the SRs (including the ringing) are reduced to 8 V ($V_{\rm in}/n$), when $n = 3$. Thus lower voltage rating MOSFETs with lower $R_{\rm DS(ON)}$ can be chosen to reduce the conduction further. New low-voltage devices, with extremely low $R_{\rm DS(ON)}$ (sub 1 mΩ), will be in production in the near future. This provides the new topology with potential to achieve an even greater efficiency improvement. For example, if the 7 V lateral power MOSFETs, using CSP concept with 0.9 mΩ at $V_{\rm GS} = 6$ V is chosen as SRs [32], the SR conduction loss can be further reduced from 8.1 to 4.3 W. This turns to be loss reduction of 4.9% of the output power (3.8 W/1.3 V/60 A).

The reverse recovery loss of the body diode is $P_{\rm rr} = Q_{\rm rr} \cdot V_s \cdot f_s$, where $V_s = V_{\rm in}/n$, is the blocking voltage over the diode. For the proposed converter, this voltage is 8 V compared to 20 V in a buck converter. Therefore, the reverse recovery loss is also reduced by as much as 60%.

E. Design Compatibility With Existing VRM Technology

Another important advantage mentioned here is that since the control MOSFETs are located in the legs of the FB structure, low-cost commercial buck drivers can be directly used to drive these control MOSFETs without additional auxiliary circuitry. The SRs can be driven directly without extra drivers nor auxiliary windings. Exiting multiphase buck controllers can be used for the feedback control. In addition, the design procedure of the new topology is quite straightforward and similar to a traditional FB converter, which is familiar to most design engineers. Therefore, less design efforts are required.

Overall, the proposed ZVS self-driven NFB converter reduces the frequency-dependent losses including switching loss, reverse recovery loss, and gate drive loss of SRs in a cost-effectively manner. It also reduces the voltage stress of the control MOSFETs as well as SRs, and reduces the output filter inductance for better dynamic response.

VI. Experimental Verification and Discussion

A 1-MHz self-driven ZVS FB VRM was built to verify the operation of principle and demonstrate the advantages of the proposed topology. Fig. 13 shows a photograph of the prototype. The specifications are as follows: input voltage $V_{\rm in} = 12$ V; output voltage $V_o = 1.3$ V; output current up to 60 A; switching frequency $f_s = 1$ MHz, and transformer turns ratio $n = 3{:}1$. The PCB uses six-layers of 2 oz copper. The components used in the circuit are listed as follows.

Control MOSFET Q_1–Q_4: Si7368DP (20 V N-channel, $R_{\rm DS(ON)} = 8.5$ mΩ at$V_{\rm GS} = 4.5$ V, Vishay); synchronous MOSFET Q_5 and Q_6: IRF6691 (20 V N-channel, $R_{\rm DS(ON)} = 1.8$ mΩ at $V_{\rm GS} = 10$ V, International Rectifier); power transformer: RM5 (core materials 3F3); and output filter inductors: $L_1 = L_2 = 190$ nH (ice components LP02-191-5).

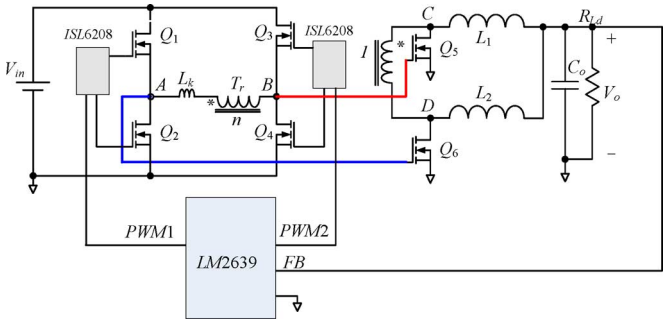

Fig. 13. Schematic of the nonisolated self-driven FB converter.

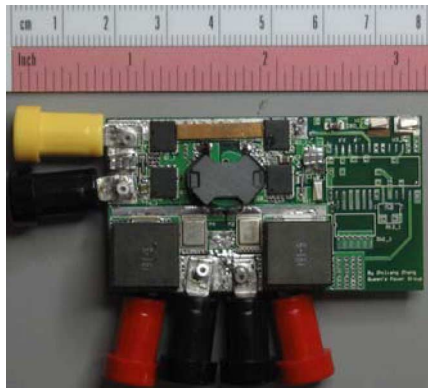

Fig. 14. Photograph of the prototype.

Fig. 13 gives the circuit diagram of the test prototype. Two Intersil ISL6208A buck drivers are used to drive four control MOSFETs in the primary side of the transformer. A four-phase buck controller LM2639 is used to generate two pulsewidth modulation (PWM) control signals for driver ISL6208A. It is noted that only two buck drivers and one multiphase phase buck controller are used for the proposed converter. Fig. 14 shows a photograph of the prototype.

Fig. 15 shows the gate drive signal $v_{\rm GS}$ and drain-to-source $v_{\rm DS}$ of the upper control MOSFET Q_1 at full load (60 A), which indicates that ZVS has been achieved for Q_1. Similarly, Fig. 16 demonstrates ZVS achievement of the lower control MOSFET Q_2.

Fig. 17 shows the gate drive signal $v_{\rm GS}$ and the drain-to-source voltage $v_{\rm DS}$ of the SR Q_6. It is noted that the gate drive voltage is 12 V, which means the $R_{\rm DS(ON)}$ of SRs is only 1.6 mΩ compared to 2.2 mΩ with 5 V gate drive voltage (a reduction of 20%). This reduces the conduction loss by 2.2 W (30% of the output power). Moreover, there is no body-diode conduction time for the turn-ON transition of Q_6, since the gate voltage has been applied before $v_{\rm DS}$ reaches zero. The high frequency ringing of $v_{\rm DS}$ is introduced by the body-diode capacitance and the leakage inductance of the transformer. There is no snubber used in the prototype. This ringing can be relatively easily removed by a small snubber. It is also noted that even with the voltage ringing, the peak value of $v_{\rm DS}$ is less than 8 V.

Fig. 18 shows the voltage $v_{\rm AB}$ across the primary side of the transformer, the rectified voltages v_C and v_D over the output filter inductors. It is observed that the voltage applied to the

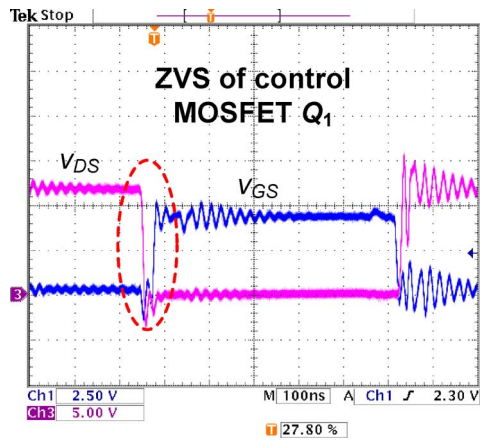

Fig. 15. Drain-to-source voltage $v_{\rm DS}$ and gate drive signals $v_{\rm gs}$ of upper control MOSFET Q_1 at $V_{\rm in} = 12$ V, $V_o = 1.3$ V, and $I_o = 60$ A.

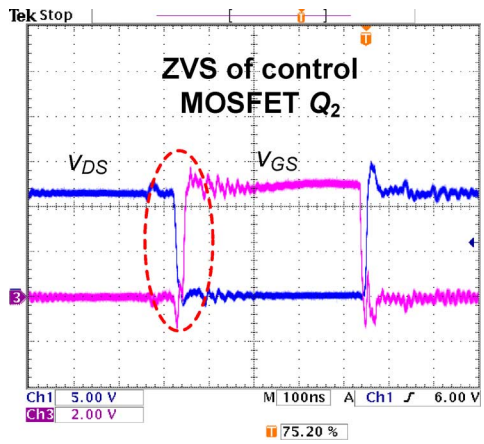

Fig. 16. Drain-to-source voltage $v_{\rm DS}$ and gate drive signals $v_{\rm GS}$ of lower control MOSFET Q_2 at $V_{\rm in} = 12$ V, $V_o = 1.3$ V, and $I_o = 60$ A.

primary side is symmetrical though asymmetrical control is applied to the control MOSFETs in the FB structure. It is also noted that the peak rectified voltages v_C and v_D (i.e., drain-to-source voltage of the SRs) is only 5 V, which means a reduction of the reverse recovery loss. It should be noted that 20 V DirectFET with $R_{\rm DS(ON)} = 1.8$ mΩ at $V_{\rm GS} = 10$ V is used in this experiment. With the fast development of low-voltage rating MOSFETs, it is expected that 8 V or 10 V MOSFETs with $R_{\rm DS(ON)}$ less than 1 mΩ will be available commercially in the near future. The emerging low voltage devices will reduce the conduction losses of the SRs by approximately 50% (i.e., 4.2 W, 5.4% of the total output power at $V_o = 1.3$ V and $I_o = 60$ A, and an efficiency improvement of around 4%). It should be noted that 12 V input buck converters are not able to take advantage of these future new low-voltage rating device with extremely low $R_{\rm DS(ON)}$.

Fig. 19 gives the measured efficiency comparison between the proposed topology and the conventional buck converter at 1.3 V output. It is observed that at 50 A, the efficiency is improved from 80.7% to 83.6% (an improvement of 2.9%) and at 60 A, the efficiency is improved from 77.9% to 80.5% (an improvement of 2.6%). The efficiency improvement is due to the reduction of the frequency-dependent losses.

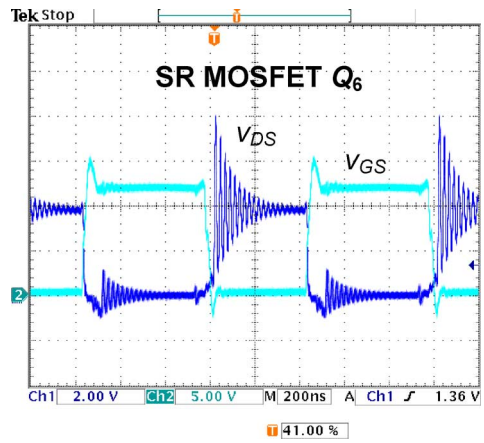

Fig. 17. Gate drive signal and drain-to-source voltage of Q_6 at $V_{\rm in} = 12$ V, $V_o = 1.3$ V, and $I_o = 60$ A.

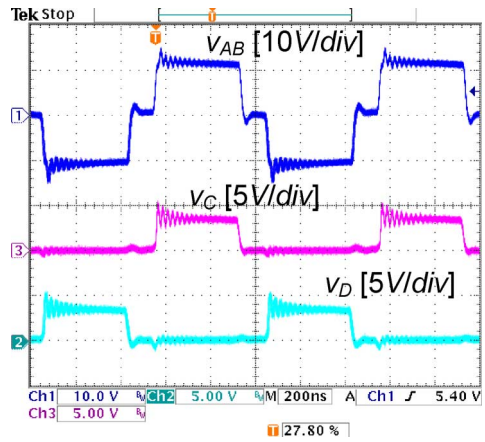

Fig. 18. Waveforms of primary voltage $v_{\rm AB}$, the rectified voltages v_C and v_D at $V_{\rm in} = 12$ V, $V_o = 1.3$ V, and $I_o = 60$ A.

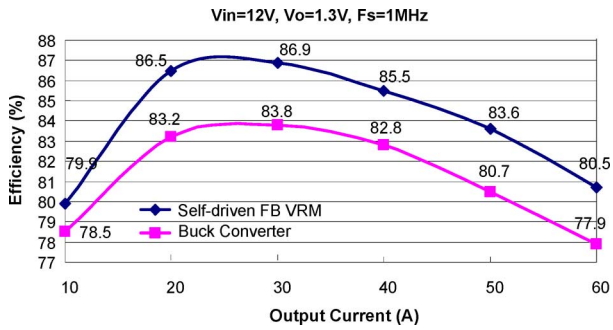

Fig. 19. Efficiency comparison with different load currents: top: self-driven FB VRM; bottom: buck converter.

Fig. 20 gives the measured efficiency comparison between the self-driven FB converter with two parallel SRs and the conventional buck converter at 1.3 V output. It is observed that at 50 A, the efficiency is further improved from 80.7% to 84.7% (an improvement of 4%) and at 60 A, the efficiency is improved from 77.9% to 83.2% (an improvement of 5.3%). The efficiency improvement is due to the SR conduction loss reduction at high-load currents. It is noted that the efficiency can be further improved, using low rating SRs to reduce the conduction loss.

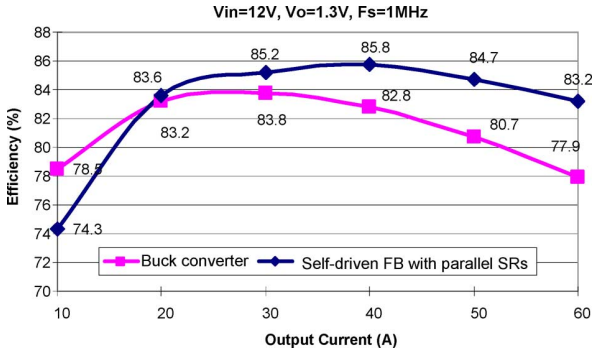

Fig. 20. Efficiency comparison: top: self-driven FB VRM with two parallel SRs; bottom: two-phase buck converters.

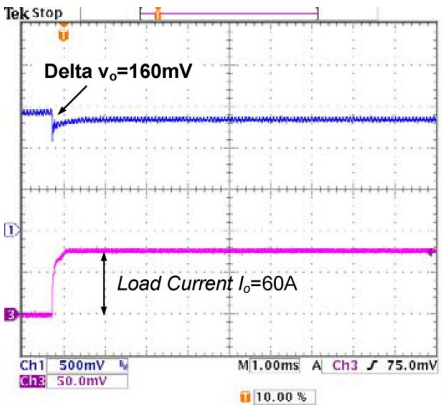

Fig. 21. Output voltage and the load current step-up: from no load to full load.

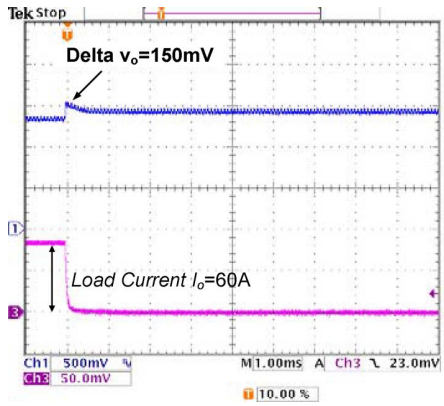

Fig. 22. Output voltage and the load current step-down: from full load to no load.

Fig. 21 illustrates the output voltage during the load step-up from no load to full load. Fig. 22 illustrates the output voltage during the load step-up from full load to no load. It is observed that from no load to full load, the voltage deviation is 160 mV, and from the full load to no load, the voltage deviation is 150 mV. The converter is stable and is able to response fast during the load transient events.

VII. Conclusion

This paper has proposed a new self-driven ZVS NFB converter is proposed for 12 V input VRM applications. The advantages are highlighted as follows: 1) duty cycle extension; 2) ZVS of all the control MOSFETs; 3) reduced reverse recovery loss and lower voltage stress of the SRs; 4) high-drive voltage to reduce the $R_{DS(ON)}$ and the conduction loss of SRs owing to gate energy recovery capability; 5) reduced body-diode conduction; and 6) no external drive IC chips with dead time control needed due to the inherent CSD structure. Existing multiphase buck controllers and buck drivers can be directly used in the proposed converter.

A 12-V input, 1.3-V output, and 1-MHz prototype of the proposed converter was built to verify the operation and demonstrates the advantages. At 50 A, the proposed converter improves the efficiency from 80.7%, using the buck converter to 83.6%, and at 60 A, from 77.9% using the buck converter to 80.5%. With two parallel SRs, the efficiency is further improved from 83.6% (single SR) to 84.7% (two SRs) and at 60 A, the efficiency is improved from 80.5% (single SR) to 83.2% (two SRs). During the load transient events, the proposed converter can also response fast.

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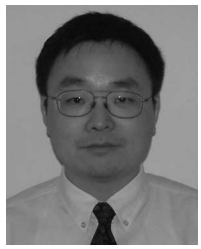

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