

Controlled Auxiliary Circuit to Improve the Unloading Transient Response of Buck Converters

Eric Meyer, *Student Member, IEEE*, Zhiliang Zhang, *Member, IEEE*, and Yan-Fei Liu, *Senior Member, IEEE*

Abstract—In this paper, a controlled auxiliary circuit is presented to improve the transient response of a Buck converter. It is well established that for converter applications with a large input/output voltage ratio, voltage overshoots (due to step-down load transients) are much larger than corresponding voltage undershoots (due to step-up load transients). Therefore, the goal of the proposed method is to reduce the overshoot. The control method only activates the auxiliary circuit during step-down load transients and operates by rapidly transferring excess load current from the output inductor of a Buck converter to the converter's input. The proposed method behaves as a controlled current source to remove a constant regulated current from the output of the Buck converter. The duration of activation of the auxiliary circuit is also regulated. The proposed circuit has the following advantages: 1) predictable behavior allowing for simplified design; 2) inherent over-current protection; and 3) low peak current to average current ratio allowing for use of smaller components. In addition, the proposed auxiliary controller estimates the magnitude of the unloading transient and sets the auxiliary current proportional to the transient magnitude. This allows for greater design flexibility and increases the auxiliary circuit efficiency for unloading transients of lesser magnitude. In this paper, it is shown through analysis, simulation, and experimental results that a large reduction of voltage overshoot and output capacitor requirements can be realized through the addition of a small MOSFET, diode, and inductor.

Index Terms—dc-dc converters, load transient response, nonlinear control.

I. INTRODUCTION

A RELATIVELY inexpensive method to improve the dynamic response of a converter is to improve its controller. Thus, extensive investigation has been performed, developing various nonlinear control methods. Control schemes are presented in [1]–[10], which improve the transient response (due to a rapid load variation) of a buck converter to its optimal level (i.e., minimizing the output voltage deviation and settling time following a load transient). However, when employing the so-called optimal control methods, it is clear that the limiting factor of dynamic performance becomes the inductor current slew rate. In fact, it is demonstrated in [6] that for low-duty-cycle conversion applications (e.g., $12 V_{dc} \rightarrow 1.5 V_{dc}$), the voltage overshoot caused by a step-down load current transient may

Manuscript received June 14, 2009; revised August 28, 2009. Current version published April 2, 2010. Recommended for publication by Associate Editor K. Ngo.

E. Meyer and Y.-F. Liu are with Queen's Power Group, Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: eric.meyer@ece.queensu.ca; yanfei.liu@queensu.ca).

Z. Zhang is with the Aero-Power Sci-tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: zlzhang@nuaa.edu.cn).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2009.2032362

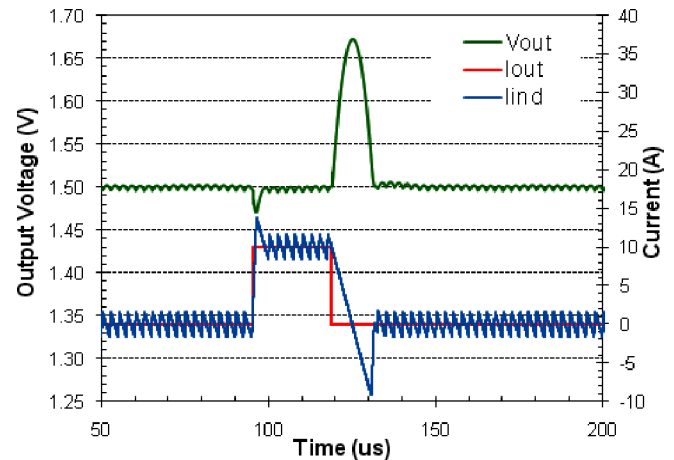


Fig. 1. Asymmetrical transient response to positive and negative load current step change.

be more than five times as large as the corresponding voltage undershoot caused by a positive current step of equal magnitude. This is illustrated in Fig. 1. Therefore, to adhere to voltage specifications, capacitor selection must be based on the larger voltage overshoot condition.

Numerous topology modifications to Buck and synchronous Buck converters have been proposed to address the aforementioned problem.

Ideally, the steady-state duty cycle would be close to 50% in order to achieve a symmetrical transient response to positive and negative load current changes. One solution is to use two synchronous Buck converters in series in order to increase the duty cycle of the second stage. For example, the first stage could convert the voltages $12 V_{dc} \rightarrow 5 V_{dc}$ and the second stage could convert the voltages $5 V_{dc} \rightarrow 1.5 V_{dc}$. Therefore, the second stage's steady-state duty cycle would be increased from 12.5% to 30%, yielding a much more symmetric transient response. This allows the use of a smaller inductor for a fixed inductor current ripple value. This concept is studied extensively in [11] and [12]. Three obvious drawbacks of this method are an increase in cost, an increase in physical size, and a decrease in efficiency. However, it is argued in [12] that if a low-enough switching frequency was used in the first stage, then the overall efficiency would not suffer.

Alternative topologies, such as nonisolated full-bridge converters with direct energy transfer, [13] have been proposed to improve this asymmetry due to their ability to extend the steady-state duty cycle through the use of a transformer. However, such converters require additional high-cost components (MOSFETs, transformer) compared to a synchronous Buck converter of equal power output.

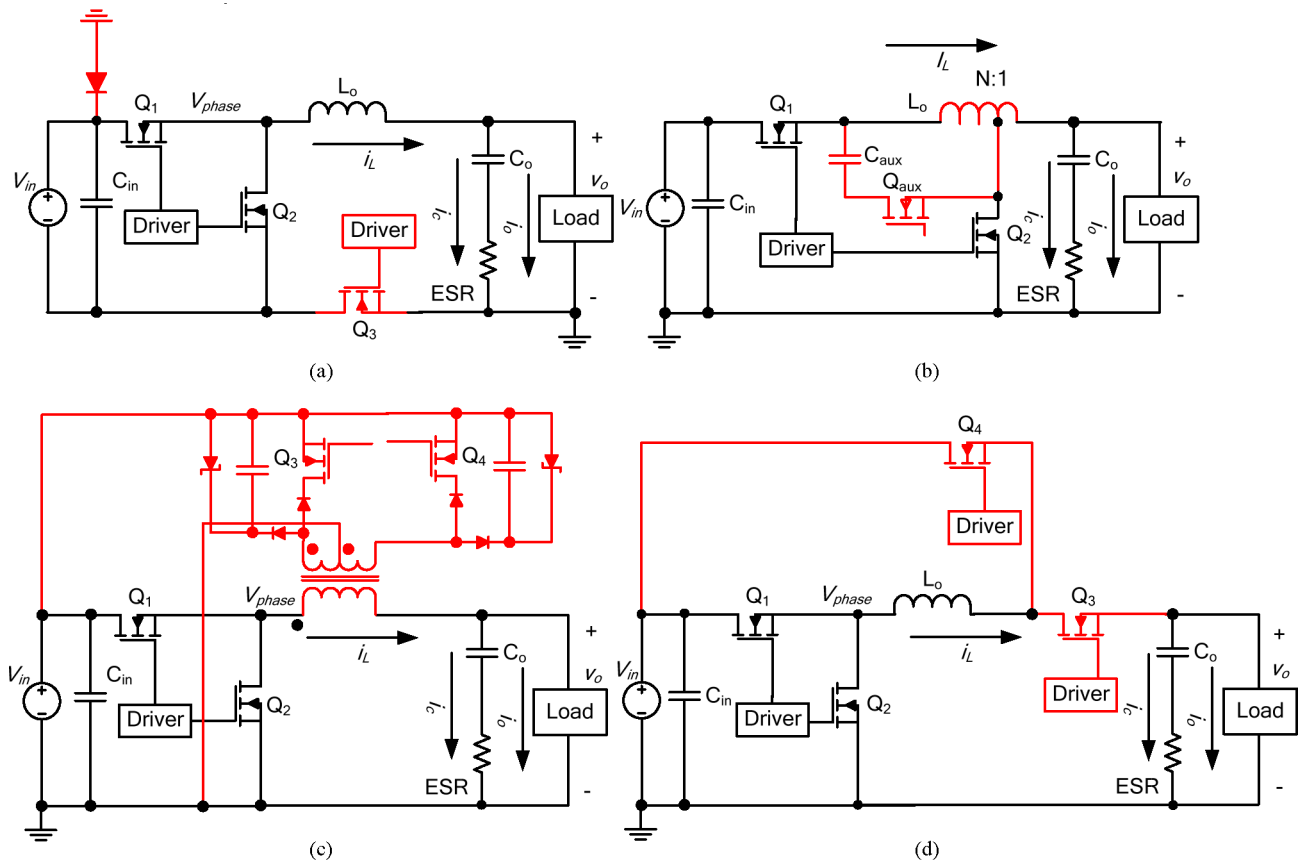


Fig. 2. Previously proposed auxiliary circuits to improve the transient response of a Buck converter.

Numerous topology modifications have been proposed to increase the negative slew rate of the output inductor during a step-down load transient. A topology modification that effectively reverses the input voltage of the converter during an unloading transient, thereby significantly increasing the negative slew rate of the output inductor has been presented in [14]. This topology modification requires a switch in series with the main powertrain. This modification is illustrated in Fig. 2(a).

A tapped inductor configuration that extends the steady-state duty cycle and increases the negative slew rate of the inductor current is presented in [15]. An auxiliary snubber circuit is typically required to mitigate the high-voltage stress imposed on the synchronous MOSFET. This modification is illustrated in Fig. 2(b).

A stepping transformer is utilized in lieu of an output inductor in [16]. During a step-down load current transient, the inductor is essentially short-circuited and the current slew rate is limited only by the leakage inductance of the transformer. This modification is illustrated in Fig. 2(c).

It is shown that by increasing the slew rate of the output inductor, the unloading transient performance of the system can be improved; however, many topology modifications have been proposed, which do not alter the inductor current slew rate but rather divert a portion of the inductor current from reaching the output capacitors.

An auxiliary circuit that operates by disconnecting the output node of the main inductor and routing it to the converter's input during an unloading transient is presented in [17]. This method also requires an additional switch in series with the powertrain. This modification is illustrated in Fig. 2(d).

A transformer that is connected across the impedance of the output trace of a synchronous Buck converter in order to inject/absorb excess load current to improve the dynamic performance is presented in [18] and [19].

An auxiliary switch in series with a small inductor is utilized in [20] to recover excess current to the input during step-down load transients. The circuit also provides a low-impedance path for step-up load transients as well. The auxiliary circuit is controlled using a differentiator in an attempt to instantaneously track the capacitor current.

The output of an isolated dc–dc converter that is connected through an auxiliary circuit (similar to [20]) to a voltage rail (fed by the rectified voltage of the secondary winding) in order to inject/absorb excess current is presented in [21]. The auxiliary circuit is controlled linearly based on the magnitude of the voltage overshoot.

An auxiliary circuit (similar to [20]) is connected to the output of a synchronous Buck converter in [22]. The switch is turned full on for the duration that the output voltage deviation exceeds a predetermined threshold.

A linear active clamp is added across the output capacitor in order to divert the excess inductor current to ground following an unloading transient in [23].

While all the aforementioned topology modifications improve the dynamic response of a dc–dc converter during a load transient, they suffer from at least one of the following conditions:

- 1) complicated transformer or tapped inductor design [13], [16], [18], [19];
- 2) auxiliary control susceptible to noise caused by auxiliary switching [20];
- 3) unpredictable auxiliary switching frequencies [16], [20], [22];
- 4) no direct current-mode control of the auxiliary circuit resulting in unpredictable and potentially damaging currents [16], [20], [22];
- 5) high auxiliary peak current to average current ratio resulting in the necessity of relatively large auxiliary switches for desired dynamic performance [20]–[22];
- 6) additional switch present in the converter's power path, causing the conduction loss of the circuit to increase even when no load transient event is occurring [14], [17];
- 7) excessive losses due to the use of an active circuit in linear mode across the output [23].

In this paper, a controlled auxiliary circuit is proposed, which significantly improves the voltage overshoot due to a step-down load transient. As will be discussed and demonstrated, the auxiliary circuit is controlled by a novel controller capable of estimating the unloading transient magnitude and driving the auxiliary circuit to transfer a proportional current from the output of a Buck converter to its input. This paper will discuss the means to estimate the unloading transient magnitude, control the auxiliary current, and the duration of auxiliary circuit activation following a load step change. Section II outlines the operation of the controlled auxiliary circuit following an unloading transient. Section III presents design guidelines and equations in addition to simulation results. Section IV analyses the power losses associated with the auxiliary circuit operation. Section V experimentally demonstrates the controlled auxiliary circuit's effectiveness of improving the unloading transient response of a Buck converter.

II. OPERATION OF AUXILIARY CIRCUIT DURING UNLOADING TRANSIENT

In order to reduce the output voltage overshoot, typical of a Buck converter undergoing an unloading transient response, it is important to reduce the current conducting through the output capacitor. Since the load current is capable of varying at a much faster rate than the inductor current, the capacitor must absorb charge (and thus increase voltage) after the load decreases rapidly. The voltage overshoot may be reduced by decreasing the size of the output inductor (resulting in decreased efficiency due to larger peak MOSFET current levels and/or increased switching frequency) or by increasing the size of the output capacitor (resulting in a significantly higher cost of the Buck converter).

Alternatively, the amount of charge absorbed by the capacitor can be reduced by transferring excess current from the output

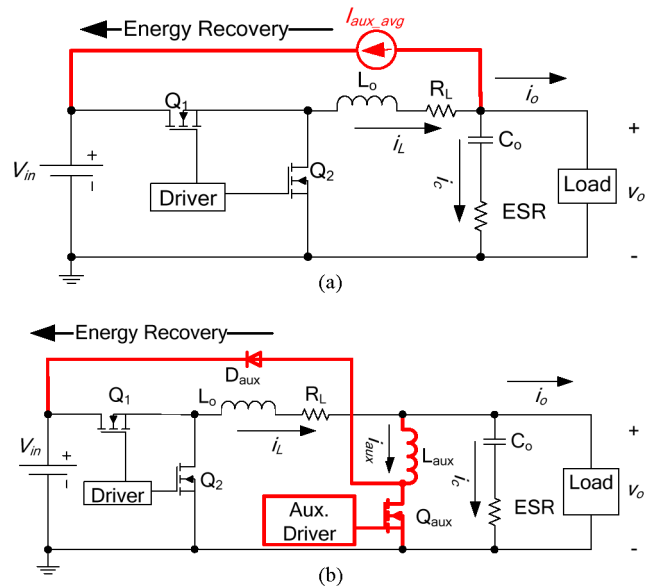


Fig. 3. (a) Model of the proposed auxiliary circuit. (b) MOSFET-diode implementation of auxiliary circuit.

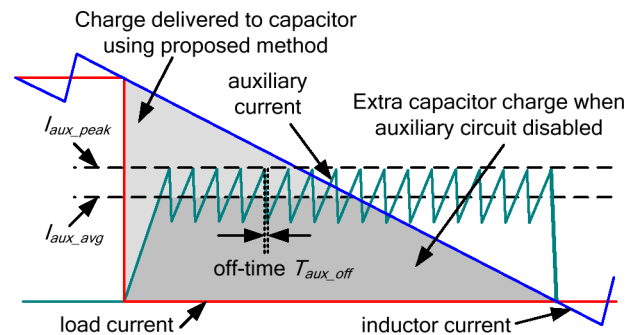


Fig. 4. Peak current mode, constant off-time operation of the proposed controller.

inductor of the Buck converter to the converter's input through operation of the proposed controlled auxiliary circuit. As will be shown, a large decrease in the output voltage overshoot can be realized by the addition of a small inductor, MOSFET, and diode.

The auxiliary circuit can be modeled as a controlled current source, drawing current from the output of the Buck converter and transferring it to the input of the Buck converter. Fig. 3(a) shows the model of the proposed method when used with a synchronous Buck converter. The proposed method may be used with a conventional Buck converter or a synchronous Buck converter; however, in this paper, a synchronous Buck converter is used as an example. The auxiliary circuit is only active during step-down load current transients (i.e., before and after an unloading transient, the circuit operates as a conventional Buck or synchronous Buck converter). Fig. 3(b) shows one possible implementation of the auxiliary circuit used in this paper. An alternate implementation would involve using a second MOSFET (in lieu of D_{aux}) for synchronous rectification. As is observed, the auxiliary circuit resembles a small boost converter connected in antiparallel with the Buck converter. The auxiliary circuit is

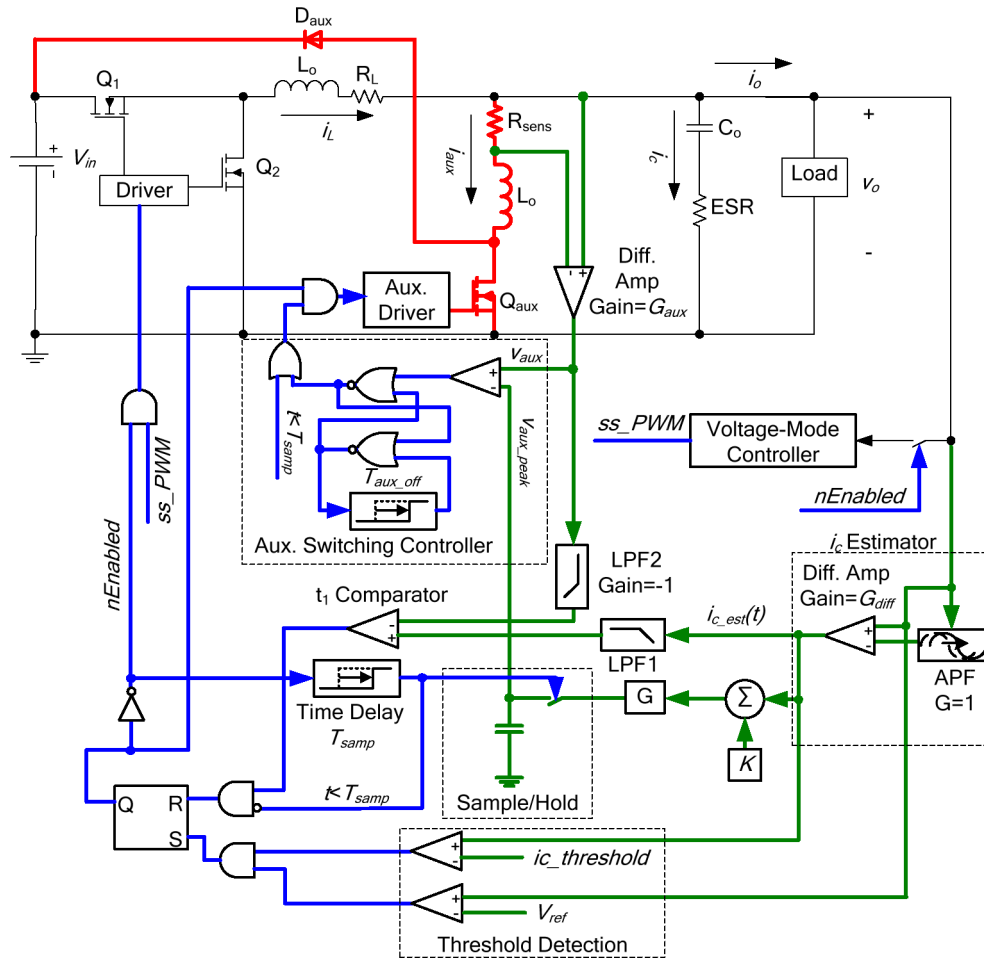


Fig. 5. Block diagram of the auxiliary circuit control.

only active during unloading transients; thus, it has no effect on the converter's efficiency when the converter is operating in steady state. In addition, since the auxiliary circuit is only active for a small percentage of the total operating duration, electromagnetic interference (EMI) effects will be short lived and will not appear significant on the frequency spectrum.

It should be noted that since current is being transferred from the Buck converter's output to its input, the converter's input must have charging capability. Large input capacitors, typical of high-current Buck converters, will aid in absorbing charge from the auxiliary circuit.

Previously proposed works [20] and [22] utilize a similar auxiliary circuit that is active, with the auxiliary switch full on (duty cycle = 100%), when either the output voltage [22] or the derivative of the output voltage [20] is outside a predetermined threshold; however, the previously proposed schemes do not directly control neither the auxiliary current nor the switching frequency. Thus, it is conceivable that the peak auxiliary current may become large (requiring large auxiliary switches), or switching frequencies may become excessive when the output voltage (or derivative of the output voltage) begins to oscillate around the threshold points.

In contrast, the proposed controlled auxiliary circuit operates at a known constant current with a relatively constant

switching frequency. Thus, the auxiliary switch and auxiliary inductor can be properly chosen based on designed current and frequency levels. When active, the auxiliary circuit is controlled using a peak current mode, constant off-time scheme, as shown in Fig. 4. Similar to a boost converter, when switch Q_{aux} is closed, current will conduct through the auxiliary inductor L_{aux} , Q_{aux} , and then to ground. This, in turn, will magnetize the auxiliary inductor. When Q_{aux} is opened, the auxiliary current will conduct through D_{aux} to the input of the Buck converter. This, in turn, will decrease the energy of the auxiliary inductor. This repetitive switching will transfer current from the Buck converter's output to its input during an unloading transient.

Assuming that the input voltage and the output voltage of the Buck converter remain relatively constant (compared to their nominal dc values) during a transient event, the control scheme will produce a constant average current through the auxiliary circuit. It is illustrated in Fig. 4 that the proposed controller will activate the auxiliary circuit until the inductor current decreases to the level of the new load current.

The shaded gray areas in Fig. 4 represent the integral of the capacitor current (proportional to the charge being absorbed by the capacitor) with and without the use of the proposed auxiliary

circuit. It is illustrated that by diverting a modest fraction of the original load current step, a significant decrease in charge is absorbed by the output capacitor.

In order to implement the peak current mode, constant off-time control, the auxiliary current can be sensed using the on-resistance of the auxiliary MOSFET Q_{aux} , a current sense resistor, or an RC network in parallel with the auxiliary inductor L_{aux} . In this paper, a small current sense resistor was employed.

Typically, the auxiliary current i_{aux} is designed to have a small peak-to-peak ripple and, as will be described, its average current is controlled based on the estimated magnitude of the load current step change.

The block diagram of the auxiliary circuit and the proposed auxiliary controller is illustrated in Fig. 5.

As shown in Fig. 5, the auxiliary circuit controller estimates the output capacitor current i_c in order to:

- 1) detect the initial load transient event;
- 2) estimate the magnitude of the load transient; and
- 3) estimate the time instant that the inductor current equals the new load current.

Previous work has demonstrated the use of a transimpedance amplifier configuration (with time constant equal to the output capacitor) [6] or a pure differentiator [22] to estimate the capacitor current; however, these methods were deemed impractical for this application since the aforementioned circuits would significantly amplify the auxiliary circuit's high-frequency switching noise caused by the capacitor's equivalent series inductance (ESL).

In order to estimate the capacitor current i_c of the Buck converter, the proposed controller monitors the time-averaged output voltage derivative by subtracting a time-shifted version of the output voltage from the output voltage. Time shifting is accomplished by the use of an all-pass filter (APF). An APF maintains the original magnitude of the input signal with a phase delay. Since the phase delay of an APF varies linearly with frequency (for frequencies below the corner frequency), the APF produces a relatively constant group delay, which will be represented by T_{apf} .

The proposed method of estimating the voltage derivative possesses higher noise immunity since high-frequency components are not amplified toward infinity. However, the accuracy of such a circuit is slightly decreased due to the linearization of the output voltage derivative over time interval T_{apf} . An implementation of the capacitor current estimator is illustrated in Fig. 6(a).

Neglecting ESL, the derivative of the output voltage of a Buck converter is calculated as follows:

$$\frac{dv_o(t)}{dt} = \frac{i_c(t)}{C_o} + \text{ESR} \frac{di_c(t)}{dt}. \quad (1)$$

Since the capacitor current estimator performs by subtracting the output voltage by a version of the output voltage time-shifted by T_{apf} , (1) can be modified to (2) (i.e., the derivative of the output voltage is estimated by linearizing the change in output

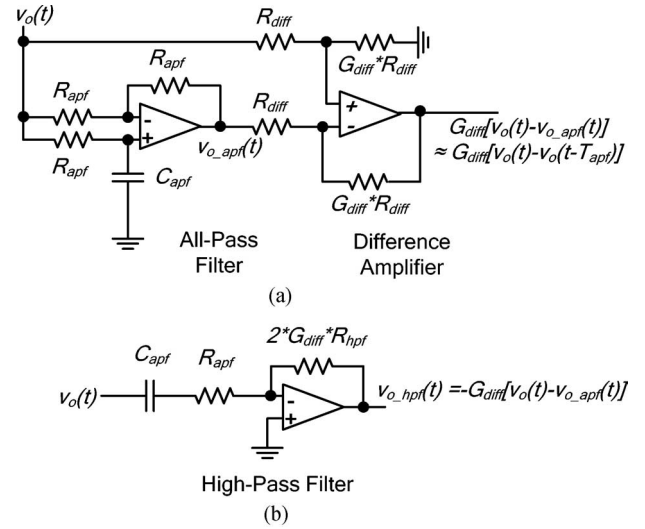


Fig. 6. Capacitor current estimator: (a) using all-pass filter configuration and (b) equivalent high-pass filter implementation.

voltage between $t - T_{apf}$ and t)

$$\frac{v_o(t) - v_o(t - T_{apf})}{T_{apf}} \approx \frac{i_c(t - (1/2)T_{apf})}{C_o} + \text{ESR} \frac{i_c(t) - i_c(t - T_{apf})}{T_{apf}}. \quad (2)$$

By multiplying both sides of (2) by T_{apf} , we get

$$v_o(t) - v_o(t - T_{apf}) \approx \frac{i_c(t - (1/2)T_{apf})}{C_o} T_{apf} + \text{ESR}(i_c(t) - i_c(t - T_{apf})). \quad (3)$$

In Fig. 6(a), the output of the capacitor current estimator is approximately equal to $G_{diff} \cdot [v_o(t) - v_o(t - T_{apf})]$; thus, the output of the capacitor current estimator $i_{c_{est}}(t)$ is calculated as follows:

$$i_{c_{est}}(t) \approx G_{diff} \left[i_c \left(t - \frac{1}{2}T_{apf} \right) \frac{T_{apf}}{C_o} + \text{ESR}(i_c(t) - i_c(t - T_{apf})) \right] \quad (4)$$

where G_{diff} equals the gain of the difference amplifier. T_{apf} is equal to the group delay of the APF below the corner frequency and is calculated as follows:

$$T_{apf} = 2R_{apf}C_{apf}. \quad (5)$$

It is observed in (4) that there exists a term proportional to the equivalent series resistance (ESR) of the output capacitor. In addition, it is observed that there is an inherent delay approximately equal to $1/2T_{apf}$ in the estimation of the capacitor current. These two issues will be addressed and rectified in Section III.

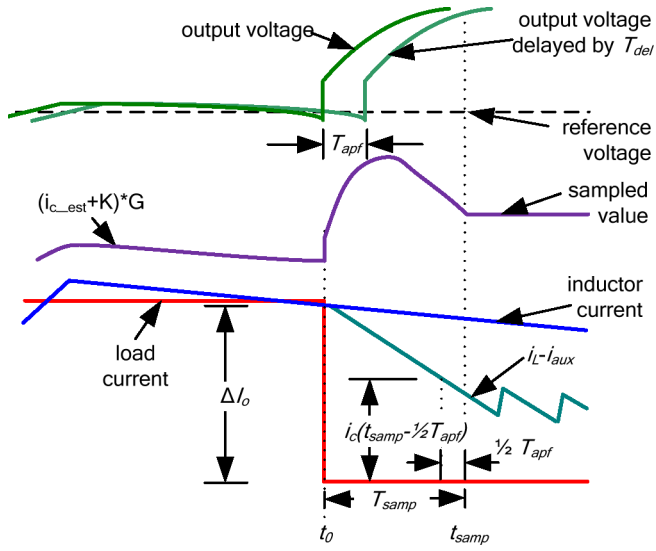


Fig. 7. Operation of auxiliary circuit during unloading transient: zoomed-in ($t_0 - t_{samp}$).

The transfer function of the capacitor current estimator is shown and simplified as follows:

$$1 - H_{apf}(s) = 1 - \frac{sC_{apf}R_{apf} - 1}{sC_{apf}R_{apf} + 1} = \frac{2}{1 + sC_{apf}R_{apf}}. \quad (6)$$

The transfer function of a first-order high-pass filter is equated in (7) as

$$H_{hpf}(s) = -\frac{G_{hpf}}{1 + sC_{hpf}R_{hpf}} \quad (7)$$

where G_{hpf} represents the passband gain of the high-pass filter. Therefore, an alternative implementation of the capacitor current estimator can be designed by using a first-order high-pass filter, as shown in Fig. 6(b).

In this paper, the auxiliary current is measured using a small series resistor and a differential amplifier, as shown in Fig. 5. In order to normalize the capacitor current estimator voltage with that of the auxiliary current sensor, the difference amplifier gain G_{diff} should be set equal to the following equation:

$$G_{diff} = \frac{C_o G_{aux} R_{sens}}{T_{apf}} \quad (8)$$

where C_o represents the nominal value of the output capacitor, G_{aux} is the gain of the auxiliary current sensor difference amplifier, and R_{sens} is the value of the current sense resistor.

In Figs. 7 and 8, the operation of the proposed circuit can be described in the following three steps.

Step 1) Detect Unloading Transient ($t = t_0$):

When the output of the capacitor current estimator exceeds a predetermined threshold and the output voltage is above the reference voltage, the auxiliary circuit is activated and the pulsewidth modulation (PWM) signal of the Buck converter is set low. The predetermined threshold is such that it is only triggered by a large unloading transient and will not be triggered by the steady-state voltage ripple. The activation of the auxiliary circuit is illustrated in Fig. 7. Due to the sharp rise in

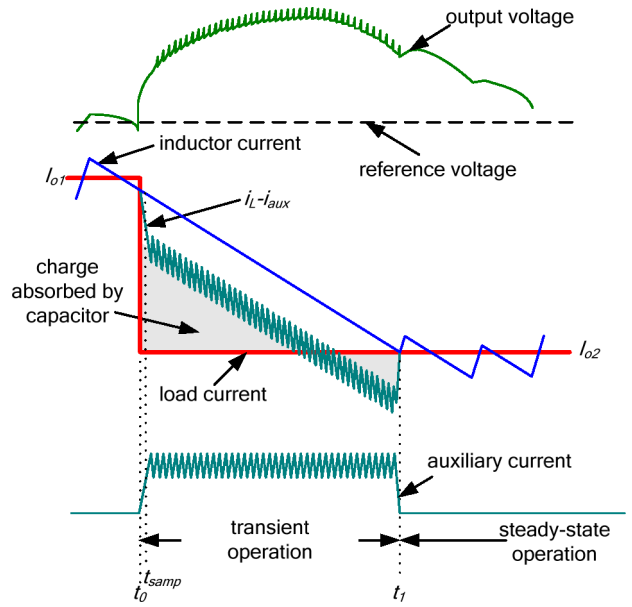


Fig. 8. Auxiliary circuit operation following a negative load current step.

output voltage following an unloading transient (due to ESR, ESL, and capacitor charging), the transient is detected virtually instantaneously.

During an unloading transient, it is necessary to disable the main control loop to prevent loop interaction. In this example, a type-III voltage-mode compensator was employed using a standard operational-amplifier (Op-amp) configuration. To freeze the output of the compensator during an unloading transient, the inverting branch of the Op-amp compensator is disconnected from the error signal using a bidirectional switch (shown in Fig. 5) controlled by the auxiliary controller logic. This, in turn, will cause the proportional (P) and derivative (D) components of the compensator to equal zero. The integrator (I) component of the compensator will remain constant when the switch is open. This method will prevent the compensator from saturating. When the transient is over, the auxiliary circuit is deactivated and the switch is closed, allowing for normal operation of the compensator circuit.

Step 2) Estimate Load Current Transient Magnitude and Set $I_{aux_peak}(t = t_{samp})$:

As illustrated in Fig. 7, after the detection of an unloading transient, the auxiliary controller samples and holds the modified output of the capacitor current estimator at t_{samp} in order to estimate the magnitude of the load current transient. The sample/hold operation is accomplished by the addition of a series switch and a shunt 100 pF capacitor, as illustrated in Fig. 5.

The auxiliary controller logic freezes the sample/hold circuit and sets I_{aux_peak} based on this information for the duration of the transient event. For proper operation, T_{samp} should be greater than T_{apf} and the auxiliary switch should be kept ON for at least the time interval T_{samp} .

As illustrated in Fig. 5, the output of the capacitor current estimator is added to a constant K and multiplied by a constant G . This can be accomplished by a simple weighted summer.

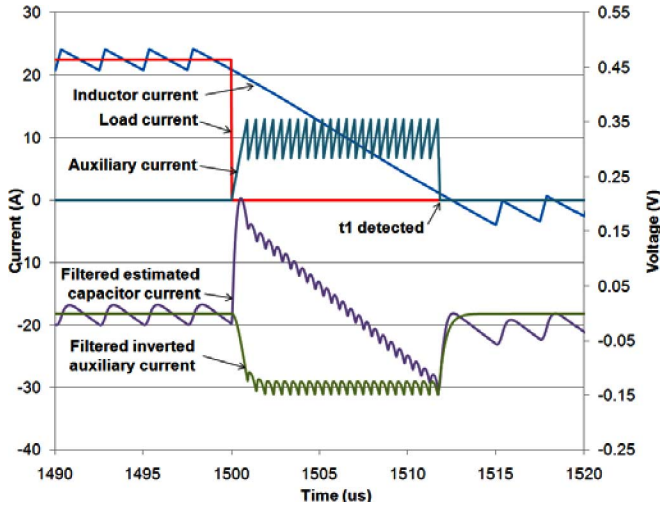


Fig. 9. Simulated example of estimation of t_1 .

These constants are design parameters based on the converter parameters, as will be described Section III.

Step 3) Terminate Auxiliary Circuit Operation ($t = t_1$):

As illustrated in Fig. 8, the auxiliary operation is terminated when the inductor current equals the new load current. At this point, the auxiliary switch is kept OFF and the converter is again controlled by a conventional linear controller. Disabling the auxiliary circuit and resuming linear control when the inductor current equals the new load current will result in minimal switch-over effect. Since $i_L = i_{aux} + i_c + I_o$, it is possible to estimate t_1 by comparing the low-pass filtered output of the capacitor current estimator with the inverted low-pass filtered output of the auxiliary current sensor, as shown in Fig. 5. Fig. 9 shows a simulated example of this detection method. Small inaccuracies of this method include the ESR, and the delays caused by the capacitor current estimator and the low-pass filter (LPF) phase shift; however, the precise determination of t_1 is not critical to the operation of the circuit.

III. DESIGN GUIDELINES AND SIMULATION RESULTS

This section will outline the guidelines to design a Buck converter with the proposed controlled auxiliary circuit. It will also present the simulation results of a converter based on the design procedure.

A. Powertrain and Filter Design of the Buck Converter

First, it is necessary to design the power stage (inductor value L_o , switching frequency f_s) of the Buck converter based on the maximum allowed steady-state inductor current ripple, the required output voltage V_o , and the converter's input voltage V_{in} . Based on this, it is assumed that a Buck converter was designed with the following parameters: $V_{in} = 12$ V, $V_o = 1.5$ V, $L_o = 1$ μ H, and $f_s = 400$ kHz.

Next, the output capacitor value C_o is chosen based on the maximum expected unloading transient and the maximum allowed voltage overshoot during unloading transients. The output voltage overshoot, using the proposed controlled auxiliary cir-

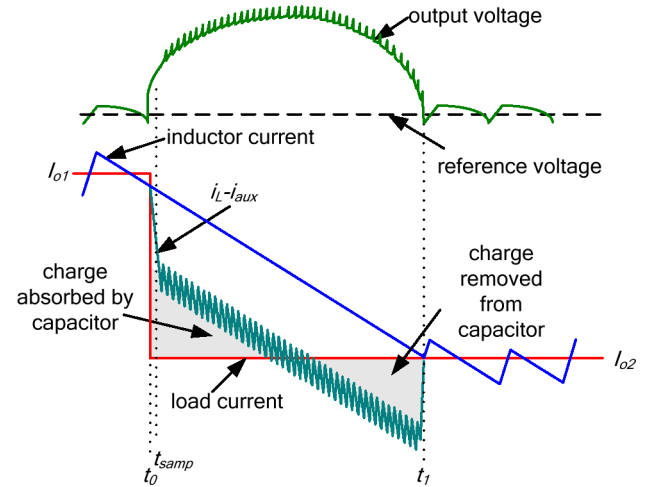


Fig. 10. Transient response when $G = 0.5$.

cuit, can be estimated using (9). The original version of (9) was fully derived in [6] and modified to account for the auxiliary current being diverted from the capacitors

$$\Delta v_o \approx \frac{ESR^2 C_o^2 V_o^2 + [\Delta I_o (1 - G)]^2 L_o^2}{2V_o L_o C_o} + \frac{(\Delta I_o G)^2 L_{aux}}{2V_o C_o} \quad (9)$$

where L_{aux} is the nominal value of the auxiliary inductor. It is recommended that the nominal value of the auxiliary inductor be significantly smaller than that of the Buck's output inductor. Thus, the auxiliary current is capable of rising to its set peak value very fast (in comparison to the slow rate of the inductor current). Ideally, the auxiliary inductor current would increase instantaneously to its peak current. However, since this is not possible, it is recommended that the auxiliary inductor be at least one order of magnitude smaller (i.e., $L_{aux} \leq 1/10 \cdot L_o$). However, this is a guideline and not a rule.

In this example, $L_{aux} = 100$ nH. G is the gain of the weighted summer illustrated in Figs. 5 and 13, which is a design parameter based on

$$G = \frac{I_{aux,avg}}{\Delta I_o}. \quad (10)$$

In other words, G represents the fraction of the load current step magnitude being diverted to the Buck converter's input. As shown in Fig. 10, when $G = 0.5$, the charge absorbed by the output capacitor equals the charge removed from the capacitor at the exact moment that the inductor current equals new load current. Thus, the output voltage and the inductor current equal their respective steady-state values simultaneously at t_1 . However, it may not be desirable to set $G = 0.5$ due to efficiency tradeoffs (as will be discussed in Section IV).

If $G < 0.5$, the inductor current will equal the new load current before the output voltage equals the reference voltage. This was illustrated earlier in Fig. 8. As shown, the auxiliary circuit is deactivated at this point and the linear controller regulates the voltage.

If $G > 0.5$, the output voltage would decrease to its reference voltage before the inductor current equals the new load current.

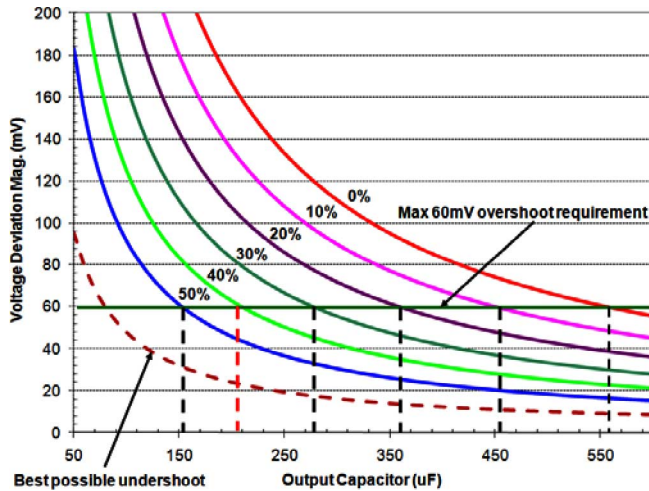


Fig. 11. Estimated voltage overshoot for various values of G and output capacitor values for an unloading transient of 10 A.

In this case, if the auxiliary circuit remained active until the inductor current equaled I_{o2} , the output voltage would undershoot the reference voltage. If the auxiliary circuit was simply deactivated at this point, a second voltage overshoot will occur. Therefore, in order to prevent “overcompensation” of an unloading transient, G should always be set less or equal to 50%. This will ensure that the inductor current reaches the new load current before the output voltage returns to its reference voltage.

Fig. 11 illustrates the estimated voltage overshoot using (9), of the previously designed converter undergoing a 10-A unloading step change, for different values of G . For this analysis, it is assumed that several ceramic output capacitors are used in parallel and that $ESR = 0.5 \text{ m}\Omega$.

If it was known that the converter would undergo unloading transients of maximum 10 A and the maximum voltage overshoot allowed was 60 mV, one could choose $G = 0.4$ and $C_o = 190 \mu\text{F}$, as shown in green in Fig. 11. If G was increased to 50%, it can be observed that C_o could be further reduced to $150 \mu\text{F}$ (for the same voltage overshoot), at a price of higher auxiliary current (and thus lower efficiency). However, it is observed that there is a diminishing return in output capacitor reduction for each increment of G . Therefore, it is recommended, in this case, to set $G = 0.4$.

The best possible voltage undershoot, to a 10-A loading transient, is added in Fig. 11 for reference. As shown, even with the overshoot improvement, the unloading transient response is still inferior to the loading condition (in terms of voltage deviation magnitude). This demonstrates the need to focus on the unloading transient for low-conversion-ratio Buck converters.

B. Auxiliary Circuit and Related Switching Controller

Next, it is necessary to design the auxiliary circuit and auxiliary switching controller. As aforementioned, the auxiliary circuit uses peak current mode, constant off-time control to switch at a relatively fixed frequency and transfer a constant average current from the output of the Buck converter to its input. The auxiliary current frequency f_{aux} and the auxiliary current

peak-to-peak ripple $I_{\text{aux_pk-pk}}$ is dependent on the selection of the auxiliary inductor L_{aux} and the constant off-time period $T_{\text{aux_off}}$, and is calculated in (11) and (12), respectively, as

$$f_{\text{aux}} \approx \frac{V_o - R_{\text{ds_on_aux}} I_{\text{aux_avg}}}{T_{\text{aux_off}} (V_{\text{in}} + V_{\text{diode}} - R_{\text{ds_on_aux}} I_{\text{aux_avg}})} \quad (11)$$

$$I_{\text{aux_pk-pk}} \approx \frac{(V_{\text{in}} + V_{\text{diode}} - V_o) T_{\text{aux_off}}}{L_{\text{aux}}} \quad (12)$$

The average auxiliary current $I_{\text{aux_avg}}$ is calculated as follows:

$$I_{\text{aux_avg}} \approx \frac{2I_{\text{aux_peak}} L_{\text{aux}} - (V_{\text{in}} + V_{\text{diode}} - V_o) T_{\text{aux_off}}}{2L_{\text{aux}}} \quad (13)$$

As observed in (13), assuming that the input voltage V_{in} , the output voltage V_o , and the forward diode voltage V_{diode} remain relatively constant, the average auxiliary current $I_{\text{aux_avg}}$ can be controlled by varying the auxiliary peak current $I_{\text{aux_peak}}$.

In this example, an auxiliary switching frequency of $f_{\text{aux}} = 2 \text{ MHz}$ is chosen based on auxiliary driver and Q_{aux} switching limits. Using (11), the auxiliary switching off time is calculated to be $T_{\text{aux_off}} = 60 \text{ ns}$.

Due to the short duration of operation, Q_{aux} can be chosen based on its “pulsed” current limit rather than its continuous current limit (allowing for the use of small SOT-23 MOSFETs for $I_{\text{aux_avg}} < 15 \text{ A}$). Since the duty cycle of the diode is typically very small ($< 15\%$), a small Schottky diode may also be used. However, it should be noted that the switch selection would have to be modified if the proposed circuit was to be used with a higher power Buck converter. For example, if a multiphase Buck converter with a load capability of 50 A was designed, then a larger MOSFET and diode, with the capability of handling 25 A pulses, would be required.

C. Activation of Auxiliary Circuit

As shown in Fig. 5, the detection of the load transient is accomplished by continuously monitoring the output of the capacitor current estimator and the output voltage. When the output of the capacitor current estimator exceeds a predetermined threshold and the output voltage is greater than the reference voltage, an unloading transient is detected and the auxiliary circuit sequence is activated.

In this example, it will be assumed that parallel ceramic capacitors are used for the output capacitor bank such that the ESR and the ESL of the output capacitors are relatively low. This is a good design choice when using the proposed auxiliary circuit, as it will limit the high-frequency output voltage ripple effect caused by the auxiliary circuit switching.

Thus, it is assumed that the ESR and the ESL are relatively low such that the steady-state output voltage ripple is primarily composed of the output capacitors charging and discharging. By modifying (4), the peak-to-peak voltage ripple of the capacitor current estimator (during steady state) can be estimated as

$$I_{\text{c_est_pk-pk}} \approx G_{\text{diff}} I_{\text{c_pk-pk}} \frac{T_{\text{apf}}}{C_o} \quad (14)$$

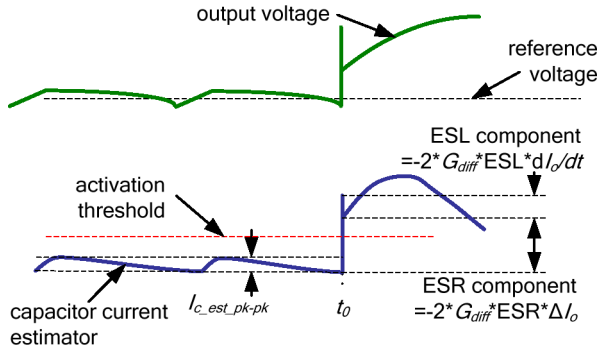


Fig. 12. Output of capacitor current estimator following an unloading transient.

where $I_{c_{pk-pk}}$ is equal to the steady-state capacitor current peak-peak ripple, which is equivalent to the steady-state inductor current peak-peak ripple of the Buck converter. Thus, when operating in steady-state conditions, the peak-peak ripple of the capacitor current estimator is equated in (15)

$$I_{c_{est\ pk-pk}} \approx G_{diff} \frac{V_{in} - V_o}{f_s L_o} \frac{V_o}{V_{in}} \frac{T_{apf}}{C_o}. \quad (15)$$

Therefore, the activation threshold should be more than half of $I_{c_{est\ pk-pk}}$ in order to differentiate unloading transients from steady-state conditions. However, it is not necessary to set the threshold this narrow in order to obtain a fast response. In fact, it is not recommended to set the threshold close to the steady-state boundary since parameters in (15) will have tolerance. While the ESR and the ESL of the output capacitors may be insignificant during steady-state conditions, they will become significant, immediately following an unloading transient. Immediately following an unloading transient, the high-frequency output voltage components caused by the ESR and the ESL will pass through the capacitor current estimator with a gain of $2G_{diff}$. Fig. 12 illustrates the output of the capacitor current estimator following an unloading transient.

In Fig. 12, dI_o/dt equals the rate at which the load current changes. As shown, the ESR and the ESL aid in the detection of an unloading transient. Thus, the activation threshold can be chosen based on these parameters. It should be noted that in the case of a very small load transient, or the case where the ESR and the ESL of the output capacitor is extremely small, the activation of the auxiliary circuit may be delayed.

D. Unloading Magnitude Estimator Based on Capacitor Current Estimation

Finally, the load transient magnitude estimator, based on the capacitor current estimator described in Section II, is designed in this section.

In Fig. 7, the sampling time interval T_{samp} should be chosen based on the maximum allowable peak auxiliary current. As aforementioned, the auxiliary peak current is not set until $t = t_{samp}$; therefore, the auxiliary current will continue to rise until the capacitor current is estimated. Thus, T_{samp} should be chosen

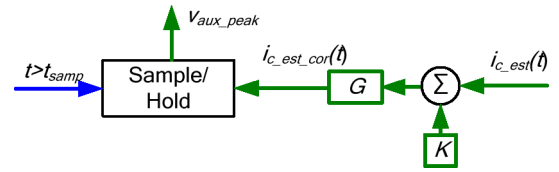


Fig. 13. Sample/hold circuit to determine I_{aux_peak} .

based on the inequality

$$T_{samp} \leq I_{aux_peak_max} \frac{L_{aux}}{V_o} \quad (16)$$

where $I_{aux_peak_max}$ represents the maximum allowable peak auxiliary current. However, T_{samp} should be large enough that effects from the initial voltage spike caused by the combination of a fast unloading transient and the capacitor's ESL have settled by $t = t_{samp}$. In this design example, the maximum recommended auxiliary current for Q_{aux} is $I_{aux_peak_max} = 15$ A; therefore, T_{samp} should be less than $1 \mu s$. The sampling time interval is chosen to be $T_{samp} = 700$ ns. In other words, the modified output of the capacitor current estimator is sampled 700 ns after the load current transient.

The group delay of the APF T_{apf} should be set smaller than the sampling time interval T_{samp} , as illustrated in Fig. 7. When T_{apf} is smaller, the capacitor current estimator will have greater accuracy; however, when T_{apf} is higher, the capacitor current estimator will have greater noise immunity. In this design example, T_{apf} is set to 400 ns as a compromise.

As aforementioned, the peak auxiliary current is calculated by the use of the sampled voltage derivative and the design parameters G and K , as shown in Fig. 13.

G has been defined earlier in (10). The variable $i_{c_{est}}(t)$ represents the output of the capacitor current estimator, described in Section II. It is important to note that the sampled output of the capacitor current estimator is equivalent to the time-averaged voltage derivative at time instant $t = t_{samp} - (1/2)T_{apf}$ and not equivalent to the capacitor current at time instant $t = t_0$ (which is what is required to set the auxiliary current). Therefore, a correction factor K must be added to $i_{c_{est}}(t)$ to compensate for the capacitor ESR, the sample time delay, and the difference between the average auxiliary current and the controlled peak auxiliary current, as will be described later.

K is defined as follows:

$$K = r_{ic_est}(K_{ESR} + K_{samp_del} + K_{rip}) \quad (17)$$

where r_{ic_est} equals the transimpedance (in volts per ampere) of the capacitor current estimator and is equated as follows:

$$r_{ic_est} = \frac{G_{diff} T_{apf}}{C_o}. \quad (18)$$

As observed in (4), the ESR will superimpose a constant on the derivative of the output voltage over the time interval of T_{samp} . The constant will be proportional to the slew rate of the capacitor current during T_{samp} (which is equal to the slew rate of the parallel combination of i_{aux} and i_L). In order to compensate and thus eliminate the ESR term in (4), K_{ESR} should be

equal to

$$K_{\text{ESR}} = V_o \left(\frac{1}{L_{\text{aux}}} + \frac{1}{L_o} \right) \text{ESR} \times C_o. \quad (19)$$

Since the capacitor current is estimated at $t = t_{\text{samp}}$ and not at $t = t_0$, a term must be added to compensate for the decrease in capacitor current over the interval T_{samp} in order to effectively estimate the load current transient magnitude. This term is equated as follows:

$$K_{\text{samp_del}} = V_o \left(\frac{1}{L_{\text{aux}}} + \frac{1}{L_o} \right) \left(T_{\text{samp}} - \frac{1}{2} T_{\text{apf}} \right). \quad (20)$$

Finally, since it is desired to control the average auxiliary current $I_{\text{aux_avg}}$, rather than the peak auxiliary current $I_{\text{aux_peak}}$, a term must be added to K to compensate for half of the peak-to-peak auxiliary ripple current. This is equated as follows:

$$K_{\text{rip}} = \frac{1}{2} I_{\text{aux_pk-pk}} / G \quad (21)$$

where $I_{\text{aux_pk-pk}}$ is calculated before in (12). In Fig. 13, by combining (4), and (17)–(21), the output of the weighted summer $i_{\text{c_est_cor}}$ at $t = t_{\text{samp}}$ is equated as follows:

$$i_{\text{c_est_cor}}(t_{\text{samp}}) = v_{\text{aux_peak}} \approx r_{\text{ic-est}} \left(G i_c(t_0) + \frac{1}{2} I_{\text{aux_pk-pk}} \right). \quad (22)$$

E. Deactivation of Controller Circuit and LPF Design

It is observed in Fig. 5 that two LPFs are utilized to determine the moment that the inductor current equals the new load current (at t_1). As aforementioned, since $i_L = i_{\text{aux}} + i_c + I_o$, it is possible to estimate t_1 by comparing the low-pass filtered output of the capacitor current estimator with the inverted low-pass filtered output of the auxiliary current sensor (as shown in Fig. 9).

The main purpose of the LPFs is to mitigate the effect of the superimposed high-frequency voltage ripple caused by the auxiliary switching. In order to attenuate the high-frequency voltage ripple, the bandwidth of the LPF fed by the capacitor current estimator should be lower than the auxiliary switching frequency. In this design, LPF1 (see Fig. 5) was chosen to be a 1-MHz second-order Bessel filter. Setting the bandwidth lower will attenuate the voltage ripple further; however, this may cause a delay in the detection of t_1 . The auxiliary switching frequency should be chosen high enough such that it can be attenuated using an LPF while allowing for the estimation of the capacitor current.

The bandwidth of the LPF2 (see Fig. 5) may be chosen substantially lower than the auxiliary switching frequency. This is due to the fact that only the dc value of the auxiliary current is required. In this example, a 500-kHz first-order filter was utilized.

The designed system was simulated undergoing a 10-A unloading transient and a 20-A unloading transient (to demonstrate the controller's ability to modify the auxiliary current), as shown in Fig. 14. As depicted, the average auxiliary current is close to

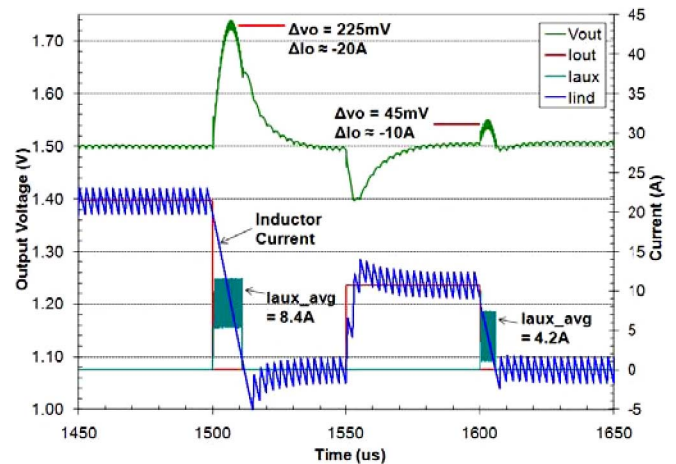


Fig. 14. Simulated transient response ($G = 0.4$).

TABLE I
SYNCHRONOUS BUCK CONVERTER AND AUXILIARY CIRCUIT PARAMETERS

Input Voltage V_{in}	12V
Output Voltage V_o	1.5V
Output Inductor L_o	1uH
Output Capacitor C_o	190uF
C_o Equivalent Series Resistance ESR	0.5 mΩ
C_o Equivalent Series Inductance ESL	100pH
Buck Converter Switching Freq. f_s	400kHz
Auxiliary Inductor L_{aux}	100nH
L_{aux} DC Resistance $R_{L_{\text{aux}}}$	0.3mΩ
Auxiliary Circuit Switching Freq. f_{aux}	2MHz
Auxiliary MOSFET On-Resis. $R_{Q_{\text{aux}}}$	30mΩ
Q_{aux} Rise Time T_{rise}	5ns
Q_{aux} Fall Time T_{fall}	2ns
Auxiliary Diode Forward Voltage V_{diode}	0.32V

the target auxiliary current. A small discrepancy is apparent due to the linearization of the output voltage derivative over T_{apf} .

IV. LOSS ANALYSIS OF THE AUXILIARY CIRCUIT

In this section, the conduction and switching losses, caused by the auxiliary circuit, are analyzed and evaluated for the designed prototype. It is important to note that the auxiliary circuit is only activated during load current step-down transient events; therefore, for scenarios in which load transients occur at low frequencies, the auxiliary circuit loss will become insignificant. The derivation used for the auxiliary circuit loss is presented in Appendix A.

A synchronous Buck converter was evaluated with the parameters summarized in Table I.

A small (SOT-23) Fairchild FDN359BN was used for Q_{aux} . It should be noted that a larger MOSFET can be easily utilized for better efficiency. The loss analysis was performed for 10-A load steps (with $I_{\text{aux}} = 4$ A) for varying values of $D_{\text{activated}}$, as shown in Fig. 15.

For example, for a 30-W converter (1.5 V/20 A), if the load was to frequently step from full load to half load such that the auxiliary circuit was activated 13.33% of the time, the power

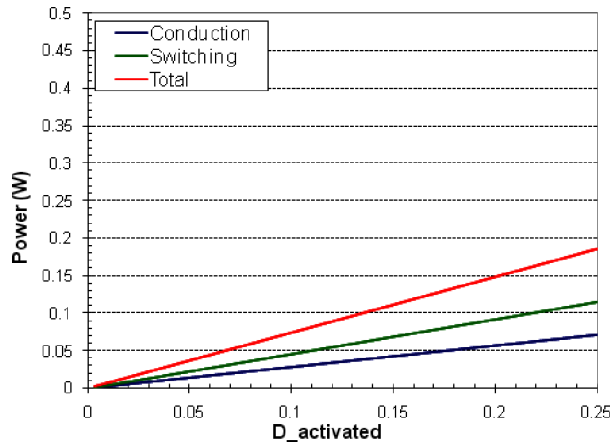


Fig. 15. Auxiliary circuit power loss for varying load step frequencies.

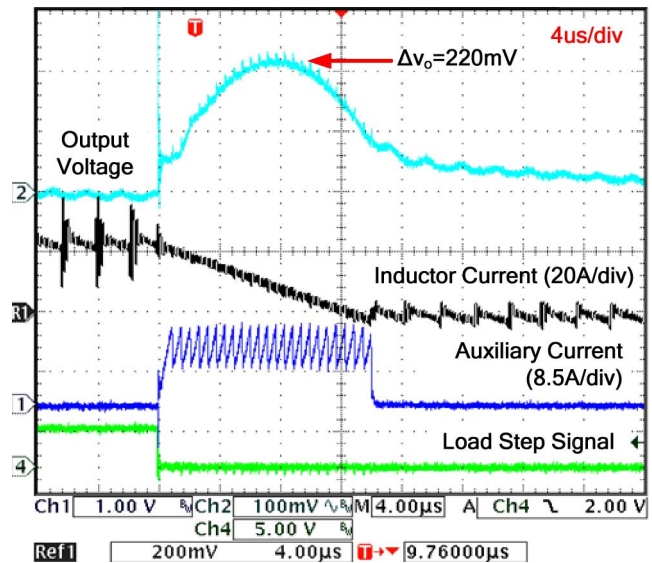


Fig. 17. Output voltage response of a synchronous Buck converter undergoing a 20 A→0 A load step change (auxiliary circuit enabled, $G = 0.4$).

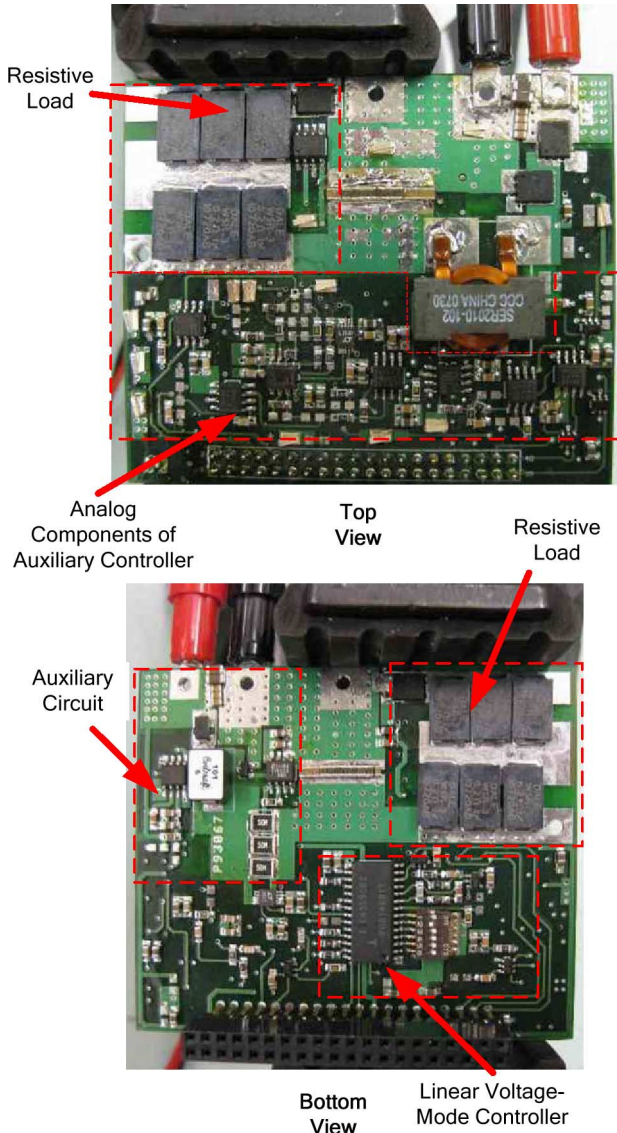


Fig. 16. Photograph of the experimental prototype.

consumption of the auxiliary circuit is approximately 0.5% of the output power. The power consumption of the proposed circuit may be improved by increasing the size of the auxiliary MOSFET and/or implementing synchronous rectification. For example, if the auxiliary MOSFET $R(ds)_{on}$ resistance was reduced to 7 m Ω , the power consumption would be reduced to 0.33% of the output power. In this scenario, the diode contributes to the majority of the conduction loss. To further reduce the conduction loss, a MOSFET could be used in lieu of the diode for synchronous rectification.

V. EXPERIMENTAL RESULTS

A prototype of the converter described in Section III was built and tested in order to verify the functionality and demonstrate the advantages of the proposed method. The prototype was designed to estimate the load current transient magnitude and set the average auxiliary current to 40% of the load step (i.e., $G = 0.4$).

The experimental parameters were identical to those outlined in Table I. All other parameters were equal to the designed controller described in Section III. The experimental prototype is illustrated in Fig. 16.

As shown, a header is connected to the experimental prototype. The prototype was connected to a field-programmable gate array (FPGA) to control the resistive load and implement the digital logic of the auxiliary controller. However, the system is primarily analog and the minimal digital logic can be implemented easily without the use of an FPGA. In addition, it is noted that the analog components for this prototype are implemented discretely. In a practical design, the real-estate requirement would be significantly decreased by combining all analog components into a single IC.

Using a fast resistive load (able to produce load slew rates approximately equal to 250 A/ μ s), the converter was subjected to a load step of approximately -20 A.

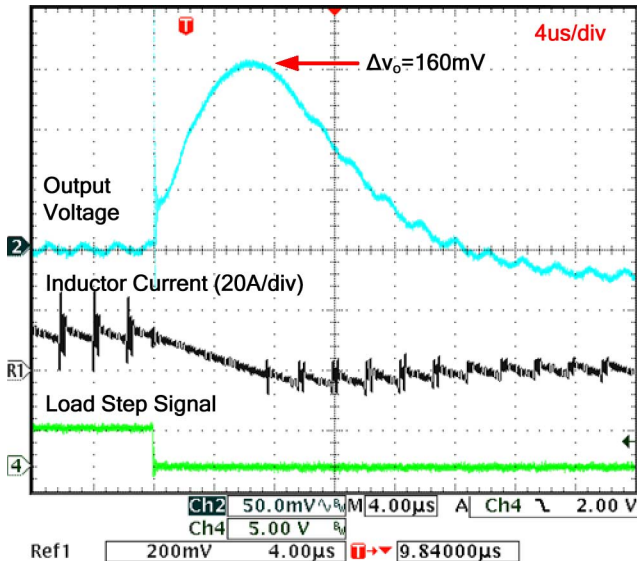


Fig. 18. Output voltage response of a synchronous Buck converter undergoing a 10 A \rightarrow 0 A load step change (auxiliary circuit disabled).

Fig. 17 illustrates the converter's response when the auxiliary circuit is activated. As illustrated, the auxiliary circuit reacts to the unloading transient and activates the auxiliary circuit with very little delay.

The measured average auxiliary current was 8.4 A (42% of the load current transient magnitude), and the measured auxiliary switching frequency was 1.9 MHz. It is observed that the output voltage overshoot is reduced to 220 mV and the recovery time is equal to approximately 32 μ s. In order for the converter to achieve a 220 mV overshoot, without the auxiliary circuit, the output capacitor would need to be increased from 190 to 600 μ F, an increase of 215%.

Fig. 18 illustrates the converter's response to a -10 -A current step change with the auxiliary circuit disabled. Fig. 19 illustrates the converter's response with the auxiliary circuit activated.

It is observed that the output voltage overshoot is reduced from 160 to 45 mV (a reduction of 72%). The recovery time is also reduced from 22 to 7 μ s (a reduction of 68%). In order for the converter to achieve a 45-mV overshoot (without the auxiliary circuit), the output capacitor would need to be increased from 190 to 750 μ F, an increase of 295%.

As observed, the overshoot of 45 mV is smaller than the previously predicted overshoot of 60 mV, calculated in Section III. This is due to the slightly larger than expected auxiliary current (42%) and the higher auxiliary current peak occurring during T_{samp} , as observed in Fig. 19.

It is also noted that at approximately 700 ns following the unloading transient, the time-averaged output voltage derivative is sampled and the peak auxiliary current is set. As shown, the controller set the average auxiliary current to a modest 4.2 A for the lesser magnitude load step, thus reducing associated losses for smaller load steps. The measured auxiliary switching frequency was 1.9 MHz.

The experimental results are summarized in Table II.

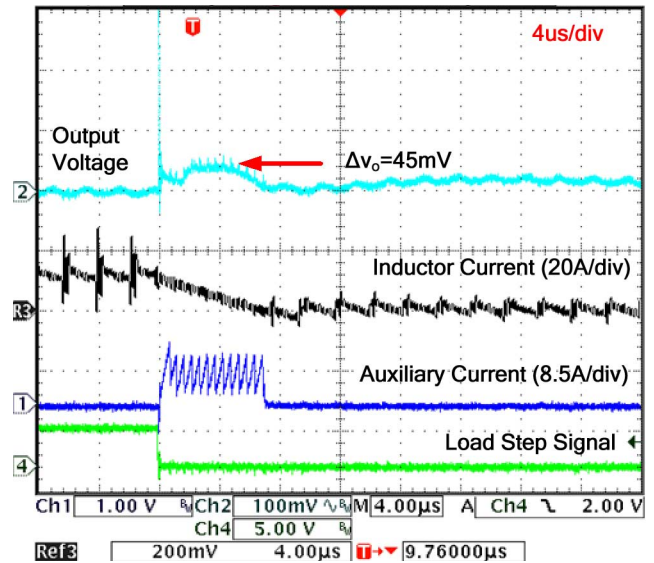


Fig. 19. Output voltage response of a synchronous Buck converter undergoing a 10 A \rightarrow 0 A load step change (auxiliary circuit enabled, $G = 0.4$).

TABLE II
EXPERIMENTAL RESULTS SUMMARY

Load Step	Measured $I_{aux, avg}$	Δv_o (mV)	Settling Time (μ s)	Capacitor Savings
20A \rightarrow 0A	8.4A	220	32	600 μ F \rightarrow 190 μ F
10A \rightarrow 0A	4.2A	45	7	750 μ F \rightarrow 190 μ F

VI. CONCLUSION

For low-duty-cycle Buck converter applications, voltage overshoots tend to be much larger than voltage undershoots for load current transients of equal magnitude. Unfortunately, engineers must design for the larger overshoot criteria when choosing output capacitors.

In this paper, a controlled auxiliary circuit was proposed that significantly reduces the voltage overshoot caused by unloading transients. This paper outlined the auxiliary controller's novel operation that is capable of:

- 1) estimating the output voltage derivative using a quasi-differentiator composed of an all-pass filter and a difference amplifier;
- 2) sampling the output of the quasi-differentiator, and correcting for ESR and sampling delay in order to estimate the magnitude of the unloading transient;
- 3) setting the average auxiliary current based on a fraction of the estimated unloading transient magnitude;
- 4) controlling the auxiliary current switching operation at a relatively constant average current and switching frequency;
- 5) determining the appropriate time instant to disable the auxiliary circuit for minimum switchover effect.

The proposed controlled auxiliary circuit allows for a more balanced overshoot/undershoot response of a Buck converter, allowing an engineer to meet voltage criteria with fewer output capacitors. The auxiliary circuit is relatively low cost as it

requires only a small MOSFET, diode, and inductor. Through simulation and experimental results, the effectiveness of the circuit is demonstrated for unloading transients of various magnitudes.

APPENDIX AUXILIARY CIRCUIT LOSS ANALYSIS

A. Conduction Loss

There are three main sources of conduction loss pertaining to the proposed circuit:

- 1) the auxiliary inductor L_{aux} ;
- 2) the auxiliary FET Q_{aux} ; and
- 3) the auxiliary diode D_{aux} .

In order to calculate the conduction loss of the inductor, the root mean square (RMS) current must first be calculated. The auxiliary inductor rms current (a dc current with a superimposed linear ripple) is calculated using

$$I_{L_aux(rms)} = I_{aux_avg} \sqrt{1 + \frac{1}{3} \left(\frac{I_{aux_pk-pk}}{2I_{aux_avg}} \right)^2}. \quad (23)$$

By calculating the rms auxiliary current in (23), the inductor conduction loss can be calculated using

$$P_{conL_aux} = I_{L_aux(rms)}^2 R_{L_aux}. \quad (24)$$

The rms current of the auxiliary FET and the average current of the auxiliary diode can be calculated using

$$I_{Q_aux(rms)} = I_{aux_avg} \sqrt{D_{aux} \left[1 + \frac{1}{3} \left(\frac{I_{aux_pk-pk}}{2I_{aux_avg}} \right)^2 \right]} \quad (25)$$

$$I_{D_aux(avg)} = I_{aux_avg} (1 - D_{aux}) \quad (26)$$

where D_{aux} can be calculated as

$$D_{aux} = 1 - f_{aux} T_{aux_off} \quad (27)$$

with f_{aux} being estimated earlier in (11). The conduction loss for the auxiliary FET and auxiliary diode can be calculated using

$$P_{conQ_aux} = I_{Q_aux(rms)}^2 R_{Q_aux} \quad (28)$$

$$P_{conD_aux} = I_{D_aux(avg)}^2 V_{diode}. \quad (29)$$

The resultant conduction loss for the auxiliary circuit can be calculated using the following equation:

$$P_{con} = D_{activated} (P_{conL_aux} + P_{conQ_aux} + P_{conD_aux}) \quad (30)$$

where $D_{activated}$ represents the time ratio that the proposed circuit is activated. As aforementioned, the ON time of the auxiliary circuit is equal to the time required for the inductor current to decrease to the new load current. $D_{activated}$ can be calculated as

$$D_{activated} = f_{Io} \frac{\Delta I_o L_o}{V_o} \quad (31)$$

where f_{Io} equals the frequency at which the load current varies and ΔI_o equals the magnitude of the load current change.

B. Switching Loss

The switching loss of the auxiliary FET is analyzed in this section. Since a Schottky diode is utilized, it is assumed that the switching loss of the diode is small compared to the FET switching loss and the total conduction loss. The switching loss for the auxiliary FET can be calculated using as follows:

$$P_{swQ_aux} = \frac{1}{2} f_{aux} V_{in} (T_{rise} I_{on} + T_{fall} I_{off}) \quad (32)$$

where T_{rise} and T_{fall} equal the typical rise time and fall time of the auxiliary FET, respectively. I_{off} equals the instantaneous auxiliary current when Q_{aux} is turned off, which is equal to the chosen peak auxiliary current. I_{on} equals the instantaneous auxiliary current when Q_{aux} is turned on and can be calculated using (33). The resultant switching loss for the proposed circuit is calculated in (34)

$$I_{on} = I_{aux_peak} - I_{aux_pk-pk} \quad (33)$$

$$P_{con} = D_{activated} P_{swQ_aux}. \quad (34)$$

REFERENCES

- [1] G. Feng, E. Meyer, and Y-F. Liu, "A new digital control algorithm to achieve optimal dynamic performance in DC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1489–1498, Jul. 2007.
- [2] T. Geyer, G. Papafotiou, R. Frasca, and M. Morari, "Constrained optimal control of step-down DC-DC converter," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2454–2464, Sep. 2008.
- [3] S. Gomariz, E. Alarcon, J. A. Martinez, A. Poveda, J. Madrenas, and F. Guinjoan, "Minimum time control of a buck converter by means of fuzzy logic approximation," in *Proc. IEEE 24th Annu. Conf. Ind. Electron. Soc. (IECON 1998)*, vol. 2, pp. 1060–1065.
- [4] K. K. S. Leung and H. S. H. Chung, "A comparative study of boundary control with first- and second-order switching surfaces for buck converters operating in DCM," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1196–1209, Jul. 2007.
- [5] K. K. S. Leung and H. S. H. Chung, "Derivation of a second-order switching surface in the boundary control of buck converters," *IEEE Power Electron. Letters*, vol. 2, no. 2, pp. 63–67, Jun. 2004.
- [6] E. Meyer, Z. Zhang, and Y-F. Liu, "An optimal control method for buck converters using a practical capacitor charge balance technique," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1802–1812, Jul. 2008.
- [7] M. Oronez, M. T. Iqbal, and J. E. Quicoe, "Selection of a curved switching surface for buck converters," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1148–1153, Jul. 2006.
- [8] A. Soto, A. de Castro, P. Alou, J. A. Cobos, J. Uceda, and A. Lofti, "Analysis of the buck converter for scaling the supply voltage of digital circuits," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2432–2443, Nov. 2007.
- [9] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao, and D. Maksimovic, "Proximate time-optimal digital control for synchronous buck DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2018–2026, Jul. 2008.
- [10] Z. Zhao and A. Prodic, "Continuous-time digital controller for high-frequency DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 564–573, Mar. 2008.
- [11] P. Alou, J. A. Cobos, R. Prieto, O. Garcia, and J. Uceda, "A two stage voltage regulator module with fast transient response capability," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun. 2003, vol. 1, pp. 138–143.
- [12] Y. Ren, M. Xu, K. Yao, Y. Meng, and F. C. Lee, "Two-stage approach for 12-V VR," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1498–1506, Nov. 2004.
- [13] S. Ye, E. Meyer, Y. F. Liu, and X. Liu, "A novel two phase nonisolated full bridge with shared primary switches," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2363–2376, Sep. 2008.
- [14] R. Singh and A. Khambadkone, "A buck derived topology with improved step-down transient performance," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2855–2866, Nov. 2008.

- [15] M. Rico, J. Uceda, J. Sebastian, and F. Aldana, "Static and dynamic modeling of tapped-inductor DC-to-DC converters," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 1987, pp. 281–288.
- [16] D. D.-C. Lu, J. C. P. Liu, F. N. K. Poon, and B. M. H. Pong, "A single phase voltage regulator module (VRM) with stepping inductance for fast transient response," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 417–424, Mar. 2007.
- [17] A. Stupar, Z. Lukic, and A. Prodic, "Digitally-controlled steered-inductor buck converter for improving heavy-to-light load transient response," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 2008, pp. 3950–3954.
- [18] X. Wang, I. Batarseh, S. A. Chickamannahalli, and E. Stanford, "VR transient improvement at high slew rate load—active transient voltage compensator," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1472–1479, Jul. 2007.
- [19] H. Zhou, X. Wang, T. Wu, and I. Batarseh, "Magnetics design for active transient voltage compensator," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Dallas, TX, 2006, p. 6.
- [20] O. Abdel-Rahman and I. Batarseh, "Transient response improvement in DC-DC converters using output capacitor current for faster transient detection," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 2007, pp. 157–160.
- [21] X. Wang, L. Qingshui, and I. Batarseh, "Transient response improvement in isolated DC-DC converter with current injection circuit," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2005, pp. 706–710.
- [22] A. Barrado, A. Lazaro, R. Vazquez, V. Salas, and E. Olias, "The Fast Response Double Buck DC-DC Converter (FRDB): operation and output filter influence," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1261–1270, Nov. 2005.
- [23] A. M. Wu and S. R. Sanders, "An active clamp circuit for voltage regulation module (VRM) applications," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 623–634, Sep. 2001.



Eric Meyer (S'05) received the B.Sc. degree in 2005 from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, where he is currently working toward the Ph.D. degree.

His current research interests include novel topologies and control methods to improve the dynamic response of voltage regulator module devices. He has authored and coauthored 16 technical papers published in various conferences and IEEE journals. He is the holder of one pending patent. He is a recipient

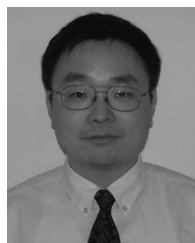
of the Natural Sciences and Engineering Research Council scholarship.



Zhiliang Zhang (S'03–M'09) received the B.S. and M.Sc. degrees in electrical and automation engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2002 and 2005, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2009.

From June to September 2007, he was a Design Engineering Intern at Burlington Design Center, Linear Technology Corporation, VT. Since 2009, he has been an Associate Professor with the Aero-Power Sci-tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics. His current research interests include high-frequency dc/dc converters for microprocessors, novel soft-switching topologies, power IC, digital control techniques for power electronics, and current-source gate-driver techniques.

Mr. Zhang was a recipient of the 2004 Graduate Scholarship through Lite-On Technology Corporation and a winner of the 1999 United Technologies Corporation Rong Hong Endowment. He was also a recipient of an award from the Power Source Manufacturer's Association to present papers at Applied Power Electronics Conference and Exposition 2009, Washington, DC.



Yan-Fei Liu (M'94–SM'97) received the B.Sc. and M.Sc. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1984 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

From February 1994 to July 1999, he was a Technical Advisor with the Advanced Power System Division, Astec (formerly Nortel Networks), where he was engaged in high-quality design, new products, and technology development. He is currently a Professor in the Department of Electrical and Computer Engineering, Queen's University. His research interests include digital control technologies for dc–dc switching converter and ac–dc converter with power factor correction, current source MOSFET drive technology, topologies and control for voltage regulator application, electromagnetic interference filter design methodologies for switching converters, topologies and controls for high switching frequency, low switching loss converters, modeling, and analysis of core loss and copper loss for high-frequency planar magnetics, and large signal modeling of switching converters.

Prof. Liu was a recipient of the 2001 Premiere's Research Excellent Award, the 2000 Golden Apple Teaching Award, both from Queen's University, and the 1997 Award in Excellence in Technology from in Nortel Networks.