Accurate Switching Loss Model and Optimal Design of A Current Source Driver Considering the Current Diversion Problem

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***Abstract*— A new analytical switching loss model for power MOSFETs driven by Current Source Drivers (CSDs) is presented in this paper. The gate current diversion problem, which commonly exists in CSDs, is analyzed. In addition, the proposed loss model considers the Miller Plateau. The optimal design of current source driver is achieved which minimizes the total power loss for the Buck converter. The experimental result verifies the theoretical analysis. Compared with previous work, the efficiency at 1MHz with the optimal current source inductor is improved from 86.1% to 87.6% at 1MHz switching frequency, with 12V input, 1.3V/20A output, and from 82.4% to 84.0% at 1MHz switching frequency, with 12V input, 1.3V/30A output.**

I. INTRODUCTION

Next generation Voltage Regulation Modules (VRMs) feature high current, low voltage and high power density [1]. In order to facilitate the complete integration of VRMs on the mother board, switched capacitors are proposed to replace the magnetic-based converter [2]. However, the large current spike, low efficiency and narrow range of the voltage regulation limit the application of the switched capacitor [3]. Another practical way to improve the dynamic performance and reduce the size of the passive components is by increasing the operating frequency of the Voltage Regulation Modules (VRMs) into MHz range [4] [5].

As the frequency increases, however, frequency dependent losses such as switching loss and gate drive loss become a penalty for switching converters driven by conventional voltage source drivers [6] [7]. In order to recover the gate driver loss that is dissipated in the charge and discharge path in the conventional voltage source driver, Resonant Gate Drive (RGD) techniques are proposed [8]-[10]. However, RGD only focuses on the gate energy loss while neglecting the potentials for minimizing switching loss, which is the dominant loss especially in high frequency applications. Recently, Current Source Drivers (CSDs) are proposed to reduce the switching loss by charging and discharging the MOSFET with a nearly constant current [11]-[14]. For example, the CSD shown in Fig 1 can turn on and turn off the power MOSFET with a discontinuous current, minimizing the circulating current and conduction loss [12].

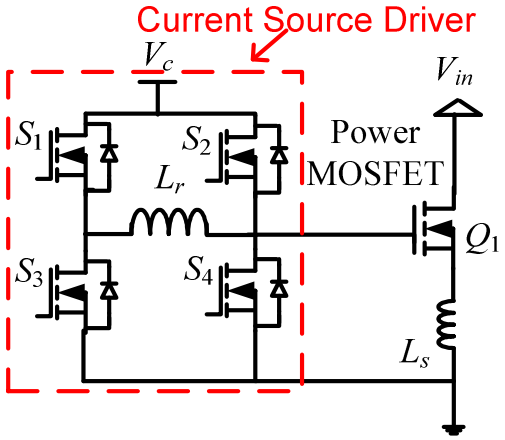

Fig 1 Topology of Current Source Driver in [12]

However, during switching transitions the current in the current source inductor is diverted, which reduces the effective current to charge or discharge the MOSFET. This is known as the Gate Current Diversion Problem and commonly exists in CSDs. Fig 2 shows the common equivalent circuits of the CSDs during turn-on and turn-off. Due to the effect of the common source inductance L_s, the gate terminal of the MOSFET is either clamped to V_c through the body diode of S_2 (D_2) during turn on or to ground through the body diode of S_4 (D_4) during turn off, causing part of driver current i_{Lr} to be diverted through D_2 or D_4 limiting the switching speed. The turn-off waveform simulated in LTspice is elucidated in Fig 3, from which it is noted that 1.8A current is diverted through D_4

in spite of a 3ampere of current in the current source driver. The CSD shown in Fig 4 presents a new concept to alleviate this problem by creating a negative voltage with D_{s1}-D_{s5} to accelerate the turn off speed [15].

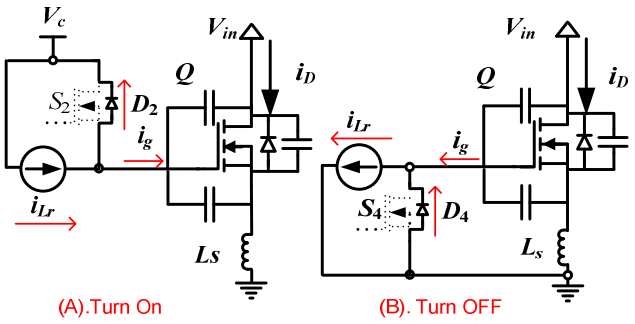

Fig 2 Equivalent Switching Circuit of CSDs

In order to evaluate the performance of the CSDs, an analytical loss model, which thoroughly analyzes the impact of the parasitic inductance in CSDs, is presented in [16]. More importantly, according to the proposed model, a generalized way to optimize the overall performance of the buck converter driven by a CSD is analyzed. A piecewise model that enables easy calculation and estimation of the switching loss is also proposed in [17]. However, the current diversion problem, which reduces the effective drive current and the switching speed, has not been analyzed in either of the two models. Therefore, a new analytical switching loss model considering every interval is presented in this paper in which the current diversion problem is analyzed and the effective charging and discharging current is accurately determined. Moreover, the optimal current source inductor is obtained in order to maximize the overall efficiency of the buck converter.

The proposed switching loss model that analyzes the current diversion problem is presented in Part II of this paper. Part III explains the procedures to obtain the optimal driver inductor of a CSD. The experimental results are shown in Part IV and finally, the conclusions are given in Part V.

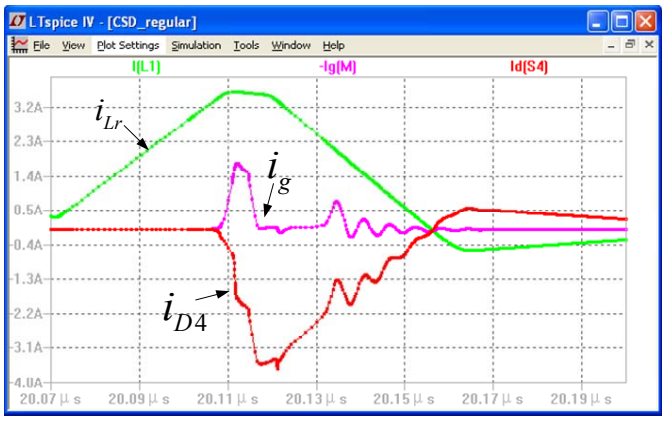

Fig 3 Simulation Waveforms of the Discharging Current of the Current Source Driver in Fig 1

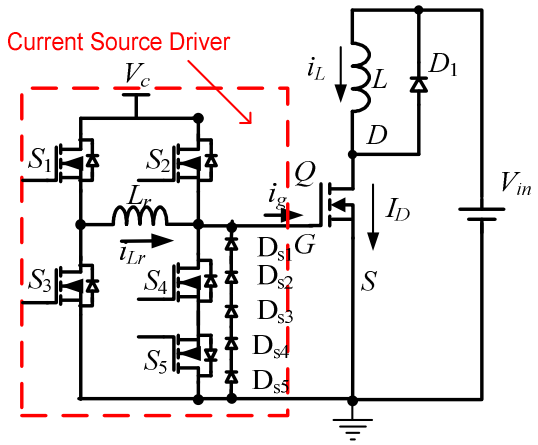

Fig 4 Inductive Clamped Load driven by CSD

II. Proposed Switching Loss Model Considering the Current Diversion

The following sub-parts will present the operation principles of the CSD and a new switching loss model which considers the gate current diversion problem.

The equivalent circuit of the MOSFET driven by proposed CSD is shown in Fig 5 , where the power MOSFET Q is represented by a typical capacitance model, L_S is the parasitic inductance including the PCB track and the bonded wire inside the MOSFET package and L_D is the switching loop inductance. For the purpose of the transient analysis, the following assumptions are made [18]:

1) $i_D=g_{fs}(v_{CGS}-V_{th})$ and MOSFET is ACTIVE, provided $v_{CGS}>V_{th}$ and $v_{DS}>i_D R_{DS(on)}$
2) For $v_{CGS}<V_{th}$, $I_D=0$, and MOSET is OFF
3) When $g_{fs}(v_{CGS}-V_{th})> v_{DS}/R_{DS(on)}$, the MOSFET is fully ON

Where i_D is the drain current of the Q, g_{fs} is the transconductance, v_{DS} is the voltage across the drain-source capacitance of the Q , v_{CGS} is the voltage across the gate-source capacitance of the Q, V_{th} is the threshold voltage of Q , $R_{DS(on)}$ is the drain-source on-state resistance. During the Active State when switching loss happens,

$$i_D = g_{fs}(v_{CGS} - V_{th}) \tag{1}$$

According to Fig 5, i_G is the effective current to charge or discharge Q as shown below,

$$i_G = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} - C_{GD}\frac{dv_{DS}}{dt} \tag{2}$$

v_{DS} is given as,

$$v_{DS} = V_{in} - L_D\frac{di_D}{dt} - L_S\frac{d(i_D + i_G)}{dt} \tag{3}$$

The detailed switching waveforms are illustrated in Fig 6, where v_{gs1}-v_{gs5} are the gate drive signals for driver switches S_1-S_5 in Fig 5, i_{Lr} is the driver inductor current of L_r; $v_{GS'}$, as shown in Equation (4), is the gate source voltage of Q including

the effect of the common source inductance and the gate resistance, p_{SW} is the switching loss of the Q.

$$v_{GS'} = -i_G R_g + V_{CGS} - L_S \frac{d}{dt}(i_{DS} + i_G) \tag{4}$$

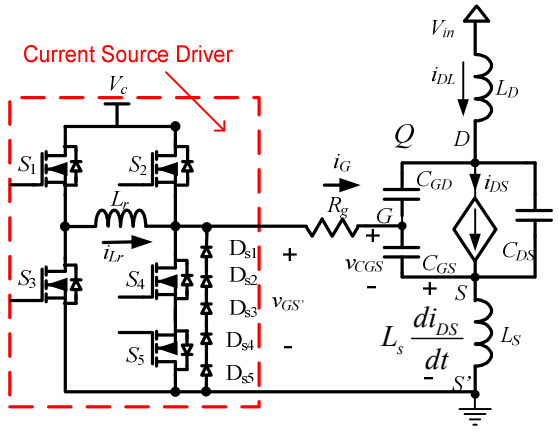

Fig 5 Equivalent circuit of MOSFET with proposed CSD

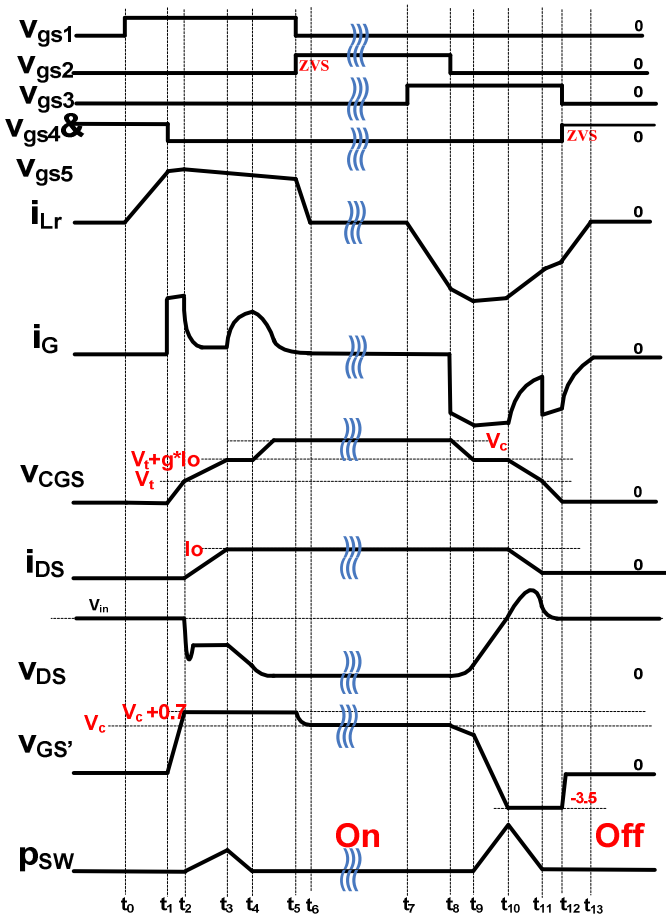

Fig 6 MOSFET Switching Transition Waveforms

The operation principle of the turn on transition is illustrated as follows. Prior to t_0, the power MOSFET is clamped in the OFF state by S_4 and S_5.

A. *Turn-ON Transition:*

Precharge[t_0, t_1]: At t_0, S_1 is turned on, and the inductor current i_{Lr} rises almost linearly and the interval ends at t_1 which is preset by the designer. The equivalent circuit is given in Fig7 (a).The inductor current i_{Lr} is given in Equation (5).

$$i_{Lr} \approx \frac{V_c \cdot (t - t_0)}{L_r} \tag{5}$$

Turn-on Delay [t_1, t_2]: At t_1, S_4 &S_5 are turned off; the inductor current i_{Lr}starts to charge the gate capacitance of Q - the equivalent circuit is given in Fig7 (b).At this interval, the effective charge current i_G equals i_{Lr}. This interval ends when v_{CGS} reaches V_{th}. In the s-domain, the KVL equation for the circuit is given in Equation (6).

$$V_c = L_r \frac{d}{dt}(i_{Lr}) + i_{Lr} R_{on} + v_{CGS},\ i_{Lr} = C_G \frac{d}{dt}(v_{CGS}) \tag{6}$$

Mathematically, there are three possible forms for the equation of the inductor current: over damped, critically damped and under damped – for practical situations, $\omega_0 > \alpha_0$, the equations for i_G, i_{Lr} and v_{CGS} are given in Equation (7) ~ (8).

$$v_{CGS} = [A_0 \cos(\sqrt{\omega_0^2 - \alpha_0^2}\,t) + B_0 \sin(\sqrt{\omega_0^2 - \alpha_0^2}\,t)] \times e^{-\alpha_0 t} + C_0 \tag{7}$$

$$\begin{aligned} i_G = i_{Lr} = C_G \times [&(-A_{01}\sqrt{\omega_0^2 - \alpha_0^2} + B_0\alpha_0) \times \sin(\sqrt{\omega_0^2 - \alpha_0^2}\,t) \\ &+ (-A_0\alpha - B_0\sqrt{\omega_0^2 - \alpha_0^2}) \times \cos(\sqrt{\omega_0^2 - \alpha_0^2}\,t)] \times e^{-\alpha_0 t} \end{aligned} \tag{8}$$

Where $\alpha_0 = \frac{R_{on}}{2(L_r + L_s)}, \omega_0 = \frac{1}{\sqrt{(L_r + L_s)C_g}}$

$$A_0 = -[2\alpha_0 i_{Lr\_0} + (V_c - 2i_{Lr\_0}R_{on})/(L_r + L_s)] \Big/ C_G\omega_0^2$$

$$B_0 = (i_{Lr\_0} + C_G\alpha_0 A_0) \Big/ C_G\omega_0^2,\ C_0 = -A_0$$

Drain Current Rising [t_2, t_3]: At t_2, $v_{CGS} = V_{th}$. During this interval, v_{CGS} keeps increasing, and i_{DS} starts to rise according to the relationship in Equation (1). Since i_{DS} flows through L_S, according to Equation (4), the large voltage induced across L_S makes $v_{GS'}$ far larger than the driver supply voltage V_c. Therefore, D_2, the body diode of the driver switch S_2, is driven on to clamp $v_{GS'}$ at V_c+0.7.The equivalent circuit is shown in Fig7 (c).At this interval, i_G drops sharply because of the voltage clamping. The subtraction of i_{Lr} and i_G is diverted into D_2. The initial condition of this interval is $I_{G\_t2} = i_G(t_2\text{-}t_1)$, *and* $V_{CGS\_t2} = V_{th}$. The interval ends at t_3 when i_{DS} equals the load current, I_o. The equations for i_G, i_{Lr},v_{CGS} and v_{DS} are given in Equation (9)~(12).

$$v_{CGS} = A_1 e^{(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2})t} + B_1 e^{(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2})t} + C_1 \tag{9}$$

$$\begin{aligned} i_G = &A_1(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2}) e^{(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2})t} \\ &+ B_1(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}) e^{(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2})t} \end{aligned} \tag{10}$$

$$i_{Lr} = (I_{G\_t2} + 0.7/R)e^{(-R/Lr)t} - 0.7/R \quad (11)$$

$$v_{DS} = V_{in} - L_S \times d\frac{i_G}{t} \quad (12)$$

where $\alpha_1=(RC_G+L_S g_{fs})/2L_S C_G$, $\omega_1=1/\sqrt{L_S C_G}$

$A_1=[(V_{th}-V_c-0.7)(-\alpha_1+\sqrt{\alpha_1^2-\omega_1^2})-I_{G\_t2}/C_G]/2\sqrt{\alpha_1^2-\omega_1^2}$

$B_1=V_{th}-V_c-0.7-A_1$, $C_2=V_c+0.7$

Miller Plateau [t_3, t_4]: At t_3, $i_{DS}= I_o$. During this interval, v_{CGS} is held at the Miller Plateau voltage. i_G mainly flows through the gate-to-drain capacitance of Q, and v_{DS} decreases accordingly. It is noted that i_G starts to rapid increase since the EMF across L_s falls sharply due to the unchanged i_{DS}, however part of the inductor current is still diverted through D_2. The equivalent circuit is given in Fig7 (d). The initial values of the interval are $I_{G\_t3}=i_G(t_3-t_2)$, $V_{CGS\_t3}=v_{CGS}(t_3-t_2)$, *and* $V_{DS\_t3}=v_{DS}(t_3-t_2)$.The interval ends when v_{DS} equals zero at t_4 . The equations for i_G , v_{CGS} and v_{DS} are given in Equation (13)~(15). i_{Lr} remains the same as the previous interval.

$$v_{CGS} = V_{CGS\_t3} \quad (13)$$

$$i_G = (I_{G\_t3} - (Vc + 0.7 - V_{CGS\_t3})/R)e^{(-R/Ls)t} + (V_c + 0.7 - V_{CGS\_t3})/R \quad (14)$$

$$v_{DS} = (\frac{I_{G\_t3} - (V_c + 0.7 - V_{CGS\_t3})/R}{C_{GD}R/L_s})e^{(-R/Ls)t} - \frac{(I_{G\_t3} - (V_c + 0.7 - V_{Cgs\_t3})/R)t}{C_{GD}} + (V_{DS\_t3} - \frac{I_{G\_t3} - (V_c + 0.7 - V_{CGS\_t3})/R}{C_{GD}R/L_s}) \quad (15)$$

Remaining Gate Charging [t_4, t_5]: At t_4, $v_{DS}= 0$ and v_{CGS} starts to rise again until it reaches V_c. $v_{GS'}$ remains at V_c+0.7, and due to the rising of the v_{CGS}, i_G decreases gradually. The equivalent circuit is given in Fig7 (f). The initial values of this interval are: $I_{G\_t4}=i_G(t_4-t_3)$, $V_{CGS\_t4}=V_{CGS\_t3}$, *and* $V_{DS\_t4}=v_{DS}(t_4-t_3)$. This interval ends at t_5 when $v_{CGS}= V_c$. The equations for i_G , v_{CGS} and v_{DS} are given in Equation (16) ~ (18) and i_{Lr} is the same as the previous interval.

$$v_{CGS} = [A_2\cos(\sqrt{\omega_1^2-\alpha_1^2}t) + B_2\sin(\sqrt{\omega_1^2-\alpha_1^2}t)]\times e^{-\alpha_1 t} + C_2 \quad (16)$$

$$i_G = C_G\times[(-A_1\sqrt{\omega_1^2-\alpha_1^2}+B_1\alpha_1)\times\sin(\sqrt{\omega_1^2-\alpha_1^2}t) + (-A_1\alpha - B_1\sqrt{\omega_1^2-\alpha_1^2})\times\cos(\sqrt{\omega_1^2-\alpha_1^2}t)]\times e^{-\alpha_1 t} \quad (17)$$

$$v_{DS} = V_{DS\_t3} - \frac{(v_{CGS} - V_{DS\_t3})(V_{DS\_t3} - I_o R_{on@Vc})}{V_c - V_{CGS\_t3}} \quad (18)$$

where $C_2=V_c+0.7$,$A_2=V_{CGS\_t3}-C_2$,$B_2=(I_{G\_t4}/C_G-A_2\alpha_1)/\sqrt{\alpha_1^2-\omega_1^2}$

and $R_{on@Vc}$ means the on-resistance of the MOSFET when $V_{CGS}=V_c$

Energy Recovery [t_5, t_6]: At t_5, S_2 is turned on to recover the energy stored in the inductor to the source as well as actively clamping Q to V_c. The initial value of this interval is $i_{Lr\_t5} = i_{Lr}(t_5- t_2)$, and this interval ends when i_{Lr} becomes zero. The equivalent circuit is illustrated in Fig7 (f). The equation for i_{Lr} is in Equation (19).

$$i_{Lr} = [I_{G\_t5} + (V_c + 0.7)/(R_{on} + R_{lr})]e^{(-R/Lr)t} - (V_c + 0.7)/(R_{on} + R_{lr}) \quad (19)$$

Prior to t_7, the power MOSFET is clamped in the ON state by S_2.

B. *Turn-OFF Transition:*

Predischarge[t_7, t_8]: At t_7, S_3 is turned on, and the inductor current i_{Lr} rises almost linearly and the interval ends at t_8 which is preset by the designer. The equivalent circuit is shown in Fig8 (a). The equation for i_{Lr} is given in Equation (20).

$$i_{Lr} \approx -\frac{V_c\cdot(t-t_7)}{L_r} \quad (20)$$

Turn-off Delay [t_8, t_9]: At t_8, S_2 is turned off. In this interval, v_{CGS} decreases until $V_{th}+ I_o*g_{fs}$ which ends the interval. The equivalent circuit is given in Fig8 (b). The way to calculate the equations for i_G, i_{Lr} and v_{CGS} are the same as the *Turn-on Delay* interval.

Miller Plateau [t_9, t_{10}]: At t_9, $v_{CGS}= V_{th}+ I_o*g_{fs}$. In this interval, v_{CGS} holds at the Miller plateau voltage, $V_{th}+ I_o *g_{fs}$. i_G (equal to i_{Lr}) strictly discharges the gate-to-drain capacitance C_{gd} of Q, and v_{DS} rises until it reaches V_{in} at t_{10}. The equivalent circuit is illustrated in Fig8 (c). The equations of this interval can be obtained in the same way as the *Miller Plateau* in turn-on interval.

Drain Current Drop [t_{10}, t_{11}]: At t_{10}, $v_{DS} = V_{in}$ and v_{CGS} continues to decrease from $V_{th}+ I_o*g_{fs}$ to V_{th}. i_{DS} falls from I_o to zero according to relationship in Equation (1). According to Equation (4), due to the induction EMF across L_s, the series connected diodes D_{s1}-D_{s5} are driven on to clamp $v_{GS'}$ at around -3.5V. The voltage across the current source inductor becomes -3.5V, so i_{Lr} decreases at a higher rate than in the turn on transition. The equivalent circuit of this interval is given in Fig8 (d). It is emphasized is that the CSD proposed in [12] only can clamp $v_{GS'}$ to -0.7V. This means that the turn off speed of the CSD proposed in this paper (Fig 4) is more than three times that of the CSD in [12]. It is worth mentioning that v_{DS} in this interval will keep rising due to effect of the *Ls*. Therefore, the derivation of the equations in this interval needs to solve the 3rd order differential equations in Equation (21).

Remaining Gate Discharging [t_{11}, t_{12}]: At t_{10}, $v_{CGS}=V_{th}$. In this interval, v_{CGS} continues to decrease until it equals zero; it is noted that v_{DS} continues to rise during this interval. The equivalent circuit is shown in Fig8 (e). 0The equations in this interval have the same form as the equations in *Remaining Gate Charging* Interval.

$$\begin{cases} L_S \times \dfrac{d}{dt}(i_{DS}+i_G)+v_{CGS}+i_G \times R_g + V_f = 0 \\ i_{DS} = g_{fs} \times (v_{CGS} - V_{th}) \\ i_G = C_g \times \dfrac{d}{dt}(v_{CGS}) - C_{gd}\dfrac{d}{dt}(v_{DS}) \\ L_S \times \dfrac{d}{dt}(i_G)+(L_D+L_S)\times \dfrac{d}{dt}(i_{DS})+v_{DS}-V_{in}-0.7=0 \end{cases} \quad (21)$$

Energy Recovery [t_{12}, t_{13}]: At t_{11}, S_4 &S_5 are turned on to recover the energy stored in the inductor to the source as well as actively clamping Q to ground. The equivalent circuit is given in Fig8 (f). This interval is the same as the *Gate Energy Recovery* at this turn-on transition.

The switching loss of power MOSFET P_{sw}, which consists of turn on loss P_{sw_on} and turn off loss P_{sw_off}, is derived according to in Equation (22). The driver loss P_{dr} is made up of conduction loss P_{dr_con}, gate drive loss P_{dr_gate} and output loss P_{dr_out} as given in Equation (23). The sum of the switching loss and the driver loss, P_{sum}, is given in Equation (24).

$$P_{sw} = \int_{t2}^{t4}(i_{DS}\cdot v_{DS}\cdot f_s)dt + \int_{t9}^{t11}(i_{DS}\cdot v_{DS}\cdot f_s)dt \quad (22)$$

$$P_{dr} = P_{dr\_con} + P_{dr\_gate} + P_{dr\_out} \quad (23)$$

$$P_{sum} = P_{dr} + P_{sw} \quad (24)$$

III. Optimal Design of Current Sourece Driver

According to Equation (5), the RMS current of the current source driver, I_{Lr_RMS}, is calculated in Equation (25). The conduction loss at this interval is proportional to the precharge time T_{pre} , and it is the same for gate energy recovery interval since during charging and discharging the current in the current source inductor roughly remains constant. Therefore, T_{pre} should be set as short as possible within the practical limits of the driver to minimize the conduction loss. Taken the logic limits into consideration, T_{pre} is set to be 20ns. And it needs to be pointed out that the design procedure presented here is also applicable to other conditions.

$$I_{Lr\_RMS} \approx \frac{V_c \cdot T_{pre}}{L_r}\sqrt{\frac{T_{pre} f_s}{3}} \quad (25)$$

In order to maximize the overall efficiency of the buck converter with the proposed CSD, P_{sum} should be minimized. The optimal design of the current source driver involves a tradeoff between driver loss and switching loss, and there exists an optimal inductor current, I_{Lr_opt}, where P_{sum} reaches the minimum value. With T_{pre} fixed to 20ns and according to Equation (25), it can also be inferred that there also exists an optimal current source inductor, L_{r_opt} as given in Equation (26).

$$L_{r\_opt} = \frac{V_c \cdot T_{pre}}{I_{Lr\_opt}} \quad (26)$$

In order to validate the analysis, the following specifications are employed: V_{in}=12V, V_o=1.3V, I_o=30A, V_c=5V, f_s=1MHz, Q: SI7386DP. Typically, the parasitic inductance value for Power PAK SO-8 package is tested by the semiconductor manufacturers in [19] [20]and range from approximately 250pH-1nH. In the models of this paper, L_s=1nH.

Fig 9 illustrates the plot of the equation P_{sum} versus the current source inductor value within practical range using MathCAD. It is noted that, in comparison with the driver loss, the switching loss is the dominant loss of the power MOSFET. It can also be observed that the optimal driver inductor is around 25nH, where P_{sum} is the minimum.

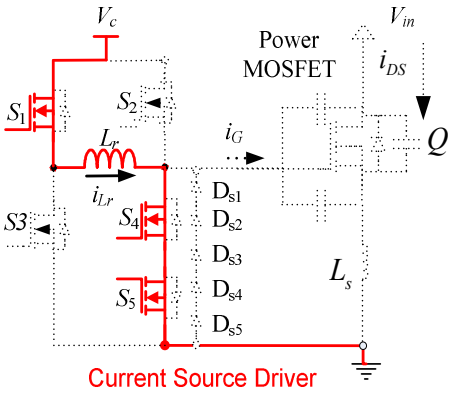

Fig 7(a): (t0, t1): Precharge

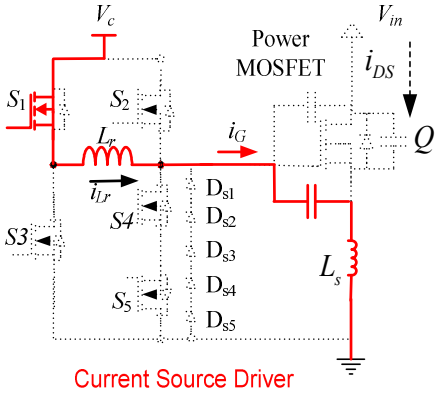

Fig 7(b): (t1 ,t2):Turn-on Delay

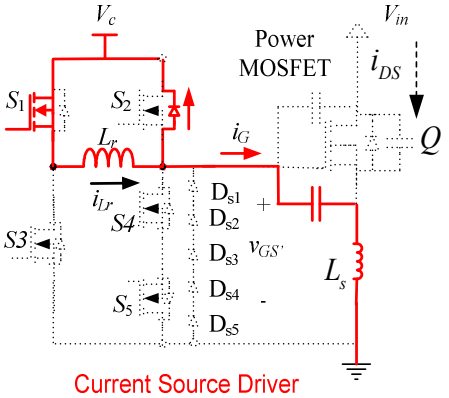

Fig 7(c): (t2, t3): Drain Current Rising

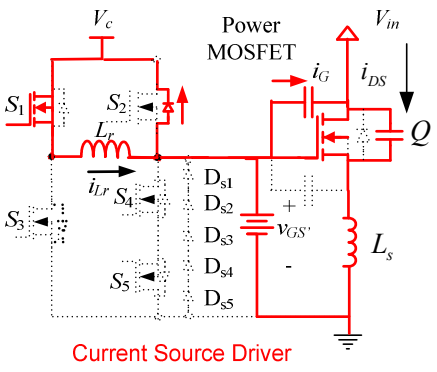

Fig 7(d): (t3, t4): Miller Plateau

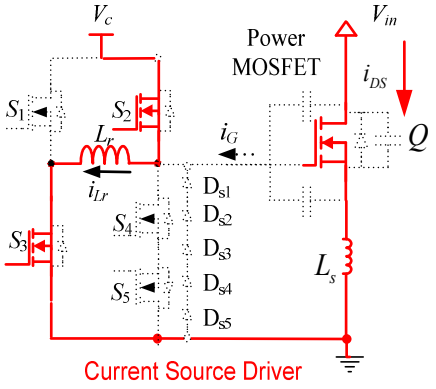

Fig 8(a): (t7, t8): Predischarge

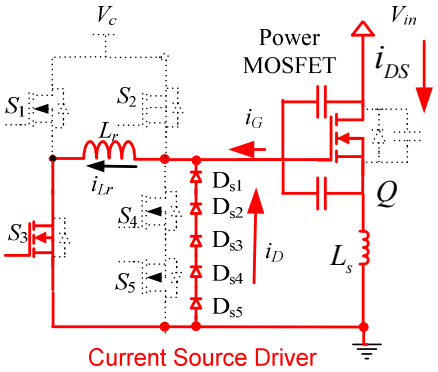

Fig 8(d): (t10, t11) Drain Current Drop

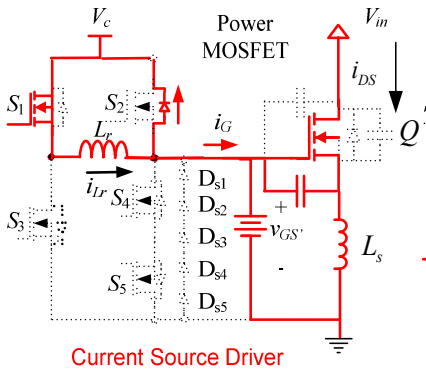

Fig 7(e): (t4, t5): Remaining Gate Charging

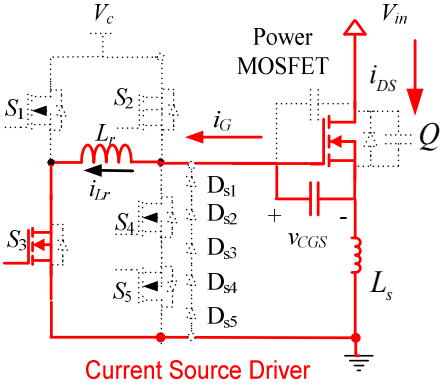

Fig 8(b): (t8 ,t9): Turn-off Delay

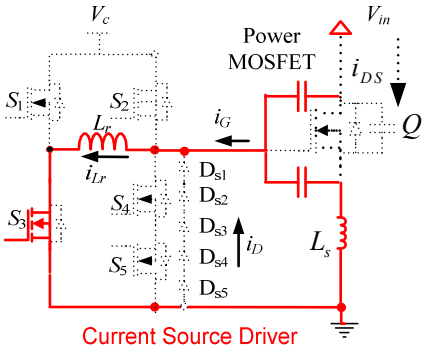

Fig 8(e): (t11, t12):Remaining Gate Discharge

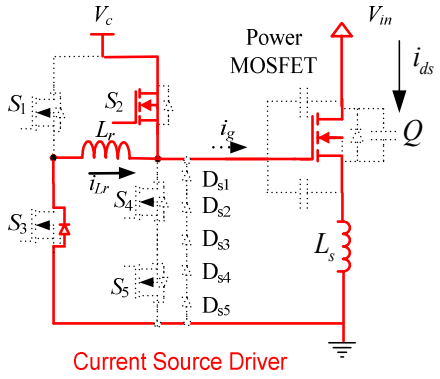

Fig 7(f): (t5, t6): Energy Recovery

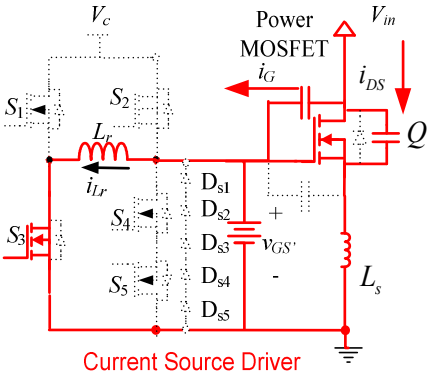

Fig 8(c): (t9 ,t10): Miller Plateau

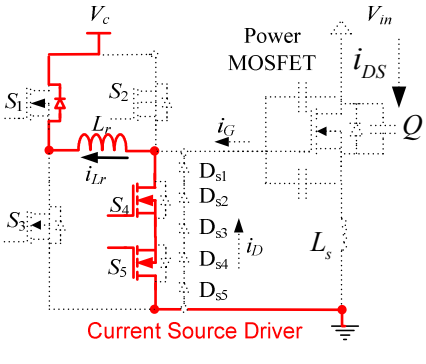

Fig 8(f): (t12, t13):Energy Recovery

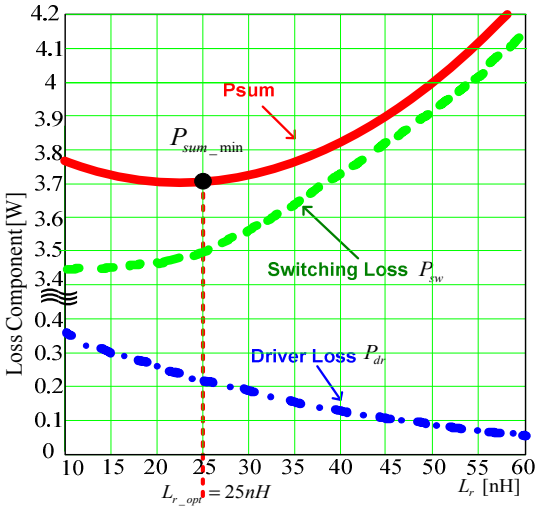

Fig 9 Total Loss Versus. Current Source Inductor

IV. Experimental Results And Discussion

A prototype of a synchronous buck converter as shown in Fig 10 was built to verify the optimal design of the current source inductor. The control FET of the converter is driven with the proposed CSD and the SR is driven with a conventional voltage source driver for simplicity.

The PCB consists of 6 layer 4 oz copper, and the picture of the prototype is shown in Fig 11. The components used in the circuit are: Q_1: Si7386DP; Q_2: IRF6691; output filter inductance: L_f=330nH (IHLP-5050CE-01); current-source inductor: L_r=23nH (Coilcraft 2508-23N_L); drive switches S_1-S_4: FDN335; Anti-diodes D_{s1} ~ D_{s5}: MBR0520. For common practice, the driver voltages for the control FET and SR are both set to be 5V. The operating conditions are: input voltage V_{in}: 12V; output voltage V_o: 1.2V~1.5V; switching frequency f_s: 500kHz~1MHz.

The gate driver signals for V_{gs_Q1} and V_{gs_Q2} are shown in Fig 12. The current waveform of the current source inductor is impossible to obtain without breaking the setup of the prototype.

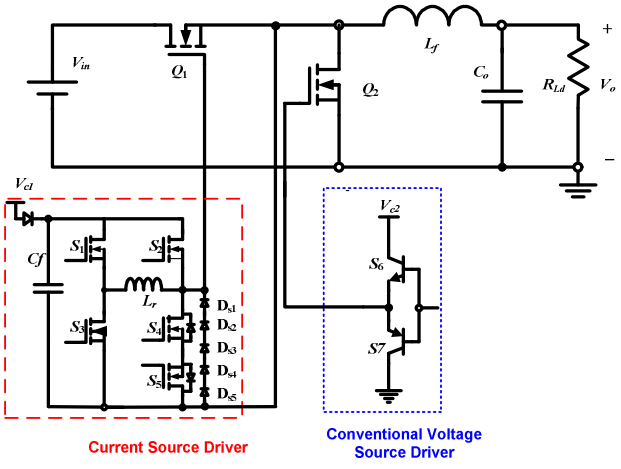

Fig 10 Buck Converter with proposed CSD

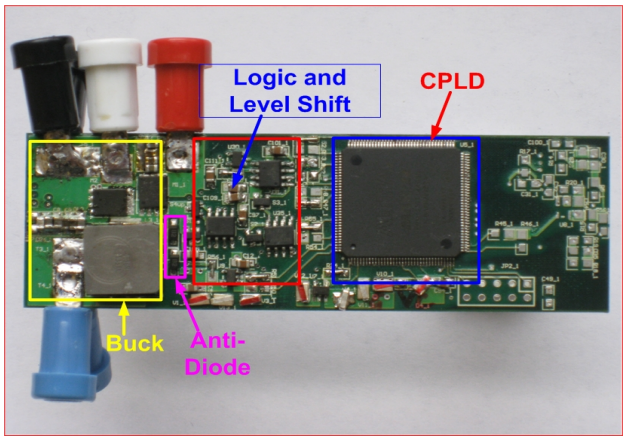

Fig 11 Photo of the buck converter with CSD in Fig 1

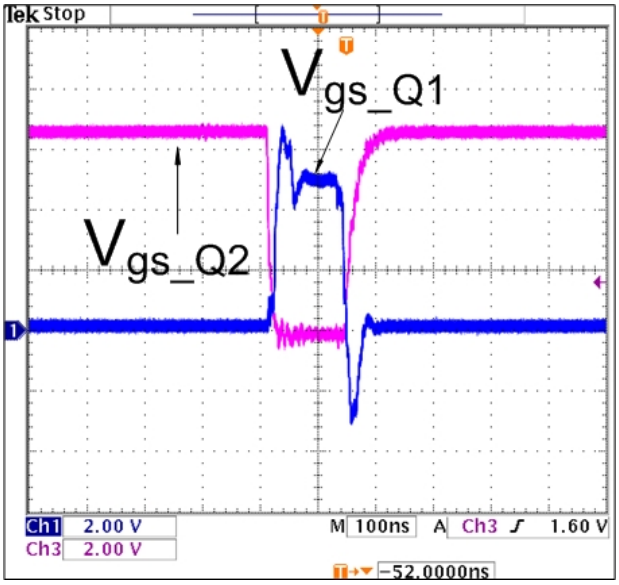

Fig 12 The waveforms of driver signals Vgs_Q1&Vgs_Q2

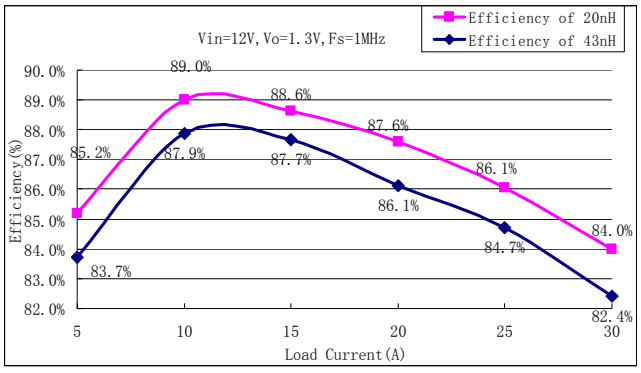

Fig 13 Efficiency comparison at 1.3V output@1MHz (Top: CSD with 23nH, Bottom :CSD with 43nH)

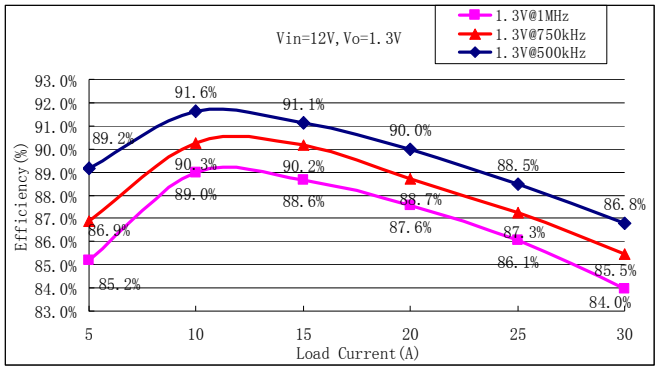

Fig 14 Efficiencies of 1.3V output @1MHz, 750kHz, 500kHz

(Top: 1MHz; Middle: 750kHz;Bottom: 500kHz)

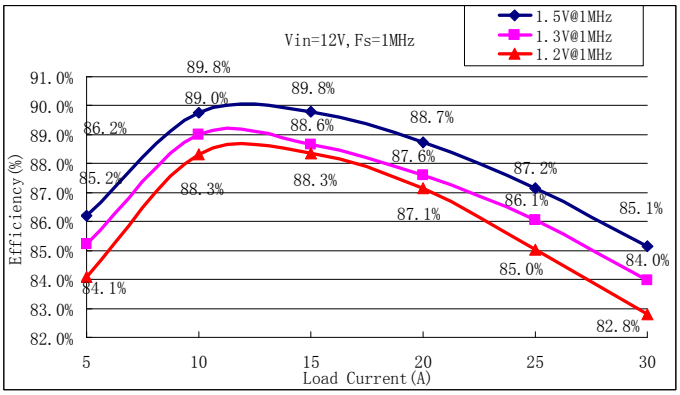

Fig 15 Efficiencies of 1.2V, 1.3V, 1.5Voutput

(Top: 1.5V; Middle:1.3V;Bottom:1.2V)

To provide a fair comparison, a similar prototype is assembled except the current source inductor is changed to 43nH. Fig 13 illustrates the efficiency comparison at 1.3V/1MHz output. It is noted that, comparing to the CSD with 43nH, the CSD with L_r=23nH increases the efficiency from 86.1% to 87.6% at a 20A load, and from 82.4% to 84.0% at 30A load.

Fig 14 also shows the efficiencies of 1.3V output at 1MHz, 750 kHz, and 500 kHz respectively. Fig 15 summarizes the efficiencies of the CSD with the optimal inductor at 1.2V, 1.3V and 1.5V output respectively. It can be observed that the highest efficiency at 1.5V output is 89.8% for a 15A load.

V. CONCLUSIONS

In this paper, a new analytical switching loss model for power MOSFET driven by a Current Source Driver which considers the current diversion is presented, and detailed equations for each interval are derived. Based on this model, the optimal current source inductor is obtained to achieve the maximum overall efficiency of switching converter. The experimental results verify the proposed switching loss model and optimal design.

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