Performance Enhancement with Digital Control Technologies for DC-DC Switching Converters

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***Abstract*— In this paper, an overview of recent advances in digital control of low- to medium-power dc-dc switching converters is presented. Traditionally, analog electronics methods have dominated in controlling such dc-dc converters. However, with the steadily decreasing cost of ICs, the feasibility of digitally controlled dc-dc switching converters has increased significantly. This paper outlines a sample of digital solutions for dc-dc switching converters to enhance the performance of dc-dc switching converters. Furthermore, latest research activities pertaining to applications for steady-state and dynamic performance improvement, such as efficiency optimization, controller autotuning, and capacitor charge balance control, are discussed. These applications demonstrate the significant advantages and potentials of digital control.**

***Index Terms*— Digital control technologies, Dc-dc switching converter, Capacitor charge balance control, Autotuning**

I. Introduction

Over the past decade, digital control has emerged as a viable candidate for low- to medium-power dc-dc switching converters. With the steadily decreasing cost of digital ICs, the cost-prohibitive attribute of digital control technology has begun to fade. Therefore, over the past few years, research focus has shifted toward the unique advantages that digital control can offer to dc-dc switching power converters.

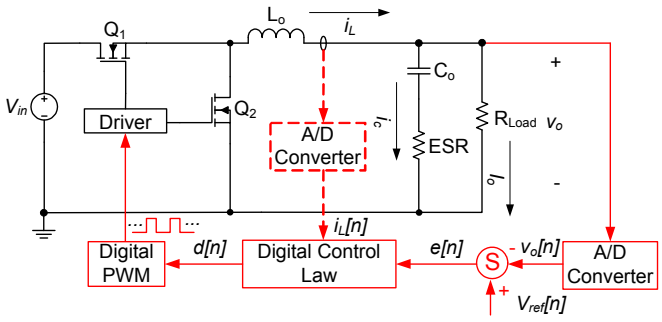

Fig. 1 Digitally controlled synchronous buck converter

Fig. 1 illustrates the implementation of a digitally controlled synchronous buck converter. The controller consists of at least one analog-to-digital converter (ADC) for feedback, a programmable digital control law, and a digital pulse width modulator (DPWM) in order to convert the control output to a modulated pulse waveform with duty cycle *d[n]*.

It is well known that digital control offers advantages over analog control such as programmability, better noise immunity, and low sensitivities to ageing and environmental factors. However, from the customer's point of view, the adoption of a new technology that tended to be more expensive and typically did not function as well as present-day technology (in terms of steady-state accuracy and dynamic response performance) did not make sense. From the designer's point of view, digital control compensation development tends to be less intuitive than the tried-and-true analog design methodologies. Furthermore, early digital designs required much larger areas of silicon and consumed more power than analog controllers, effectively prohibiting their adoption into low-power dc-dc power converters. Nevertheless, with the cost and size of digital circuits exponentially shrinking, and researcher's imaginations being sparked by the true power and capabilities of digital control, the opinion that digital control may eventually replace analog controllers is beginning to resurface. Although early research laid the foundations for further digital control development, it did not capitalize on the truly irreplaceable features that digital control brings to switching power converters. Thus, numerous recent research efforts have been conducted on digital controllers, which perform functions that are not realizable in the analog domain such as communication and system-level integration, controller autotuning, on-the-fly efficiency monitoring and optimization, and complex nonlinear control for improved dynamic performance.

This paper is organized as follows. In Section II, the digital control applications for improving steady-state are outlined in the respects of communication/system integration and efficiency optimization. In Section III, the enhancement of digital control in dynamic response is introduced, such as digital autotuning and capacitor charge balance control.

II. Steady-State Performance Enhancement

Digital controller delivers better strategies of communication and system- level integration and efficiency optimization, which highly improve the performance of dc-dc converters under steady-state condition.

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A. *Communication- and System-level Integration*

With the complexity of modern devices, it is a very rare occurrence that a single power converter is responsible for powering an entire digital system. For example, a typical motherboard will possess a central processing unit (CPU), a graphics processing unit (GPU), RAM, audio processing, associated logic, etc. Each device will have specific power specifications, and thus, requires its own power converter. As the operation of the aforementioned devices is typically highly integrated, it is also necessary that there be some level of power management communication between the different devices in one board as well as communication and control between the boards in the system.

Such a need for complex system integration has significantly contributed to digital control's emergence into the mainstream marketplace. Many semiconductor companies have developed dc-dc digital controller products which are capable of communicating through the PMBus power management protocol.

Through serial communication, up to 127 dc-dc digital converters can be addressed and accessed by a central system controller, as illustrated in Fig. 2. The PMBus protocol defines a communication language of more than 100 power-management specific commands. The advantages of such a system-wide communication network are vast; however, some obvious advantages include the following aspects:

1) *Power-Up/Power-Down Sequencing:* For complex systems such as a motherboard, there is typically a specified power-up/power-down sequence for the various devices. For example, it may be required that converter A's output voltage be at least 75% of its nominal voltage before converter B's soft-start procedure is to begin. Digital communication of devices allows for a simplified and systematic approach to such sequencing issues.

2) *Fault Detection and Reaction:* Through the PMBus protocol, pertinent information such as input/output voltage, load current, operating temperature (along with any corresponding operating faults) can be monitored by a central system controller. Through the use of a central controller, a fault detected in one converter will result in the intelligent shutdown of subsequent controllers in order to minimize the possibility of damage. Without such a communication network, faults would merely cascade through the system in an uncontrolled manner, thus increasing the risk of damage.

3) *"Field" Reconfiguration of Power Converters:* Typically, modification of a converter's control parameters (i.e., switching speed, compensator coefficients, fault tolerances, etc.) would require the recall and removal of the converter. However, through the PMBus interface, it is possible to reconfigure the nonvolatile memory of digital converters in order to permanently modify the control parameters. Such a firmware update is significantly less expensive and requires less offline time. With the recent emergence of the PMBus interface, there has been increasing development of digital controllers in the power electronics industry as the complexity of digital systems continues to increase.

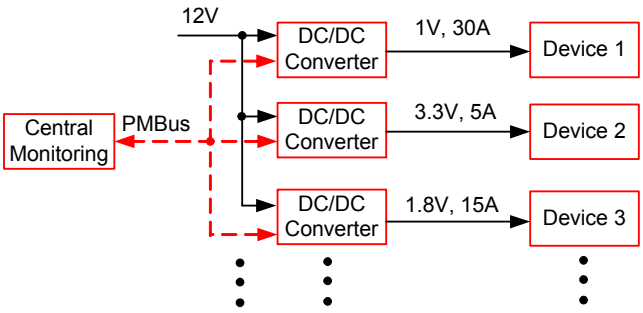

Fig. 2 PMBus Communication concept in multi-converter system

B. *Efficiency Optimization*

In [2] and [3], continuous modifications are made to the dead time parameters $t_{d,on}$ and $t_{d,off}$ (see Fig. 3) in order to decrease the switching loss due to conduction of the synchronous MOSFET's body diode. In [2], predicted optimal dead time values are initially programmed into the digital controller in relation to the converter's output current. To compensate for parameter variation/drift, slow dead time perturbations are added, and the resultant converter efficiency is measured by monitoring the input/output voltage/current. The new optimal dead times for various output currents are mapped by use of an extremum-seeking adaptation algorithm.

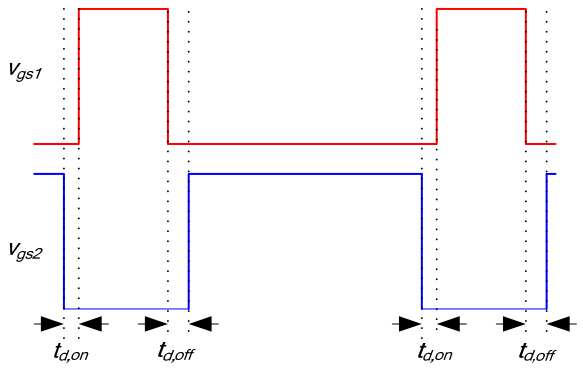

Fig. 3 Operation of a synchronous buck converter with dead time

The algorithm presented in [3] does not map optimal dead times to specified output currents, but rather dynamically varies the dead time of the algorithm searching for duty cycle minima points (which indicate peaks in efficiency).

The main advantage of the optimization scheme presented in [2] is its rapid response to dynamic load conditions; however, the optimization scheme presented in [3] may be easier to implement as it is effectively sensor-less and possesses a significantly simpler algorithm. Energy efficiency of switching converters has become an increasingly important topic, both due to the booming market of mobile electronic devices and the rising concern of environmental impact. It is possible, by the use of digital control, to make on-the-fly adjustments to the operating parameters of a switching converter for optimizing efficiency.

For example, digital control can play an important role in improving efficiency for multiphase buck converter applications. By digitally scheduling the activation and deactivation of phases dependent on load/thermal conditions, the efficiency of a converter can be improved significantly. This practice is commonly referred to as "phase-shedding". During light-to-heavy load transitions, additional phases will be activated to provide current to the increased load. In [4], during phase activation, the controller quickly balances the activated phase through a nonlinear predictive control scheme. This controller behavior would be very difficult to achieve through analog control. By rapid current balancing, the control method decreases the conduction loss following phase activation. However, experimental results are presented only for slowly varying load currents. Further investigation is required to determine the controller's proper response when the di_o/dt value is very large.

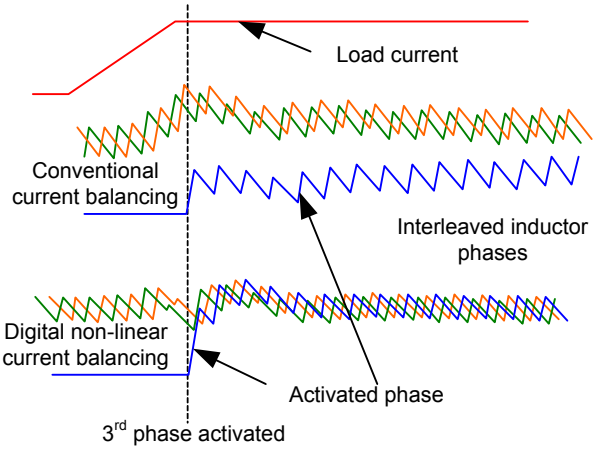

Fig. 4 Nonlinear digital phase balancing following phase activation.

In [5], a digital current balance scheme is presented, which intelligently adjusts the phase duty cycles based on efficiency, rather than nominal inductor current values (see Fig. 4). It is demonstrated that efficiency is suboptimal when the current is balanced perfectly and the phase resistance is mismatched. Thus, the controller operates by iteratively attempting to minimize the difference between the duty cycles of each phase while maintaining proper voltage regulation, which is demonstrated to minimize the total conduction loss of the converter. By adjusting the phase currents in this fashion, conduction loss and thermal management are significantly improved for mismatched multiphase converters.

III. Dynamic Performance Enhancement

Digital control is well-suited for the development of adaptive tuning and hybrid linear/nonlinear controllers, which enhance the dynamic performance of dc-dc converters significantly. In this section, the recent research on the digital autotuning and capacitor charge balance controller will be discussed.

A. Autotuning

"Autotuning" is an exclusively digital tool that has tremendous marketing potential. The idea of a "plug-and-play" controller that can automatically identify and control a converter has attracted interest from both industry and academia. Typically, analog inductor current measurement has only been as accurate as the model of the converter. Inductor current measurement is often necessary for over-current protection, multiphase current balancing, and load-line regulation. A popular analog current measurement method is to add a parallel *RC* branch across the output inductor and measure the voltage across the capacitor of the parallel branch. For correct current measurement, the time constant of the *RC* branch should be equal to the time constant of the inductor and its parasitic dc resistance (DCR). However, inductor tolerances along with varying thermal conditions that cause varying DCR present challenges to precise inductor current measurement.

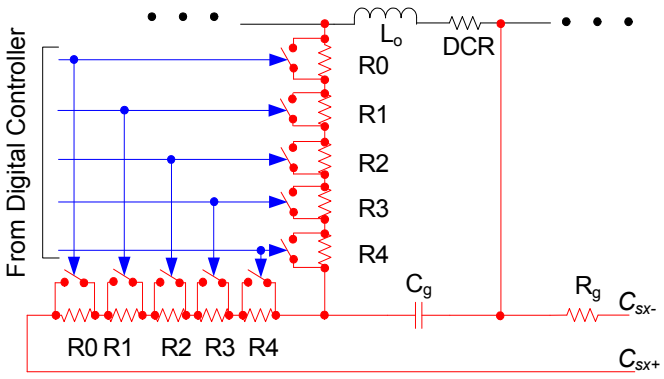

Fig. 5 Digital tuning of an analog *RC* inductor current sensor

In [6], a controller is presented that automatically tunes an analog *RC* current measurement sensor by use of a digital potentiometer (see Fig. 55). It accomplishes this by simply observing the output voltage slope of a load-line regulated converter, following a large-load transient. As shown in Fig. 6 6, when the *RC* filter is properly tuned to the inductor *RL* constant, the output voltage response is relatively flat when the load current is known to be flat. If the magnitude of the output voltage slope is greater than a specified threshold, the *RC* constant is adjusted.

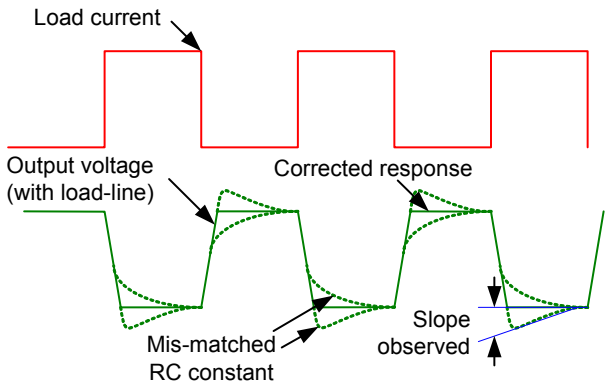

Fig. 6 Autotuning effect on a buck converter with load-line regulation

By use of digital control, it is also possible to predict the converter parameters L, C, ESR, etc., and automatically calculate the compensation coefficients based on bandwidth and phase margin requirements. This is accomplished in [7]–[11] by injecting a specified frequency into the control loop or by adding/amplifying a nonlinearity that causes the output voltage to appear limit cycle oscillation. In [5], the DPWM resolution is intentionally degraded for a short period such that the coarse DPWM resolution will lead to controlled (limit cycle oscillation) LCO. In order to amplify the LCO effect, the digital compensator is temporarily replaced with a PI configuration. By measuring the frequency of the resultant LCO, information related to the converter resonant frequency and output capacitance can be calculated. By measuring the amplitude of the resultant LCO, it is also possible to estimate the Q-factor of the converter (and thus, the load resistance/current). The information is used to design a proper PID by extracting appropriate parameters from LUTs (provided that the load current remains relatively constant).

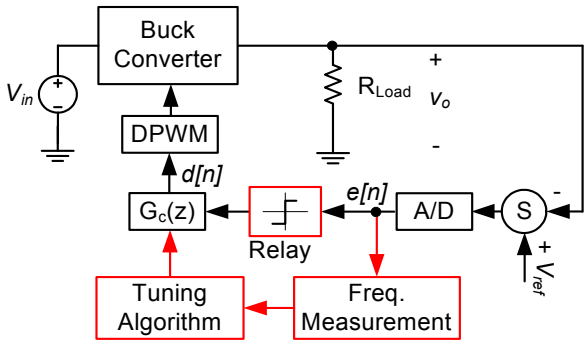

Fig. 7 Nonlinear relay to induce LCOs

In [12] and [13], autotuning is accomplished by introducing a nonlinear relay into the control loop, as shown in Fig. 77. The relay essentially acts as a 1-bit quantizer, causing LCO at the output. When G_c (z) is adjusted to an integrator (causing a 90° phase lag in the loop), the output voltage will oscillate at the resonant frequency of the converter. This frequency is measured and stored. This allows for the proper placement of the first zero of a PID compensator. The new PID controller is passed through a low-pass filter to force the desired phase margin at the desired crossover frequency. The second zero is then iteratively placed until the output oscillates at the crossover frequency. After the two zeroes are placed, the compensator gain is set by using the desired bandwidth, zero placement, and an asymptotic Bode plot estimation. The relay function is disabled after the tuning process is completed, allowing for normal loop operation. The advantage of the aforementioned method is that only the frequency of the output voltage oscillation is required to be measured; the amplitude is not required, allowing for more robust operation.

On the other hand, the above-mentioned autotuning algorithms [7]-[10] induce a relatively large voltage oscillation at the output of the converter for a short period of time in order to tune the controller. However, the autotuning algorithm presented in [11] follows a different approach, as illustrated in Fig. 88. The system operates by continuously injecting a varying frequency square wave V_z into the DPWM input signal V_x. The DPWM input signal and the digital compensator output signal V_y are passed though a bandpass filter (bandpass equal to the injected frequency) and measured by the digital stability monitor. The injected frequency is adjusted until the magnitude of the two measured filtered signals are equal (indicating the crossover frequency f_c). By comparing the zero-crossover points of the two signals V_y and V_x, the phase margin φ_m of the system can also be calculated. The measured crossover frequency and phase margin are subtracted from the desired crossover frequency and phase margin to produce crossover frequency and phase margin errors (f_{c_err} and φ_{m_err}, respectively). A relatively low-bandwidth multi-input–multi-output (MIMO) controller continuously adjusts the controller's coefficients in an attempt to minimize the f_{c_err} and φ_{m_err}.

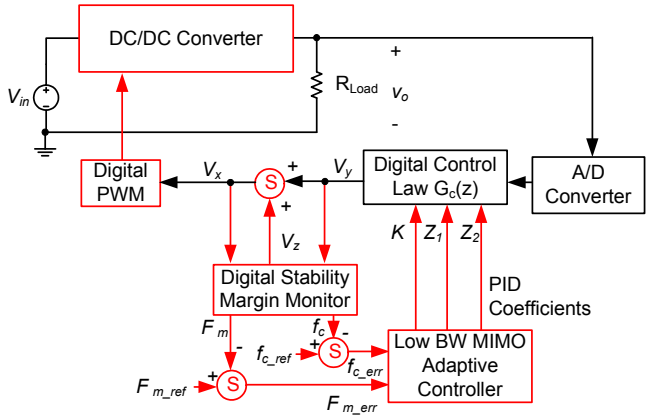

Fig. 8 Autotuning based on continuous phase margin measurement

B. *Capacitor Charge Balance Control*

A major application of dc-dc Buck converter is for powering modern processors in the computing industry. Due to the increasing load step/slew value and the stringent requirements of the regulated output voltage, the bandwidth barrier of the conventional linear mode controller needs to be

broken through. Although multiphase dc-dc buck converter with conventional controller solution is provided in the market, the incremental transferred cost on the output capacitors apparently limits the applicability of this solution for the future. Under such demands, many advanced control methods are proposed to minimize the concerns or modifications on the hardware design, but achieving optimal or suboptimal response, for example, V^2 control, sliding mode control and capacitor charge balance control.

Charge balance control (CBC, also known as time-optimal control) involves attempting to drive a converter to steady state in the theoretically minimum time and was introduced in [18] for load transient and [23] for input voltage transient. Charge balance controllers typically behave as a linear controller when the converter experiences steady-state conditions and as a nonlinear controller following a transient event. For example, as illustrated in Fig. 99, for a buck converter undergoing a load step transient, it involves a single switching transition at a precise moment. Due to the complex derivation involved, initially, this is well-suited for digital control and has received considerable research attention [14]-[23] and [24]-[27]. The concept involves determining the capacitor current zero-crossover point to estimate the output voltage peak/valley point [25] at t_1. Another key time point is to decide when the switching state of the main switch should be changed, as shown in Fig. 99, at t_2. Finally, the linear mode of controller will take over the regulation task after t_3.

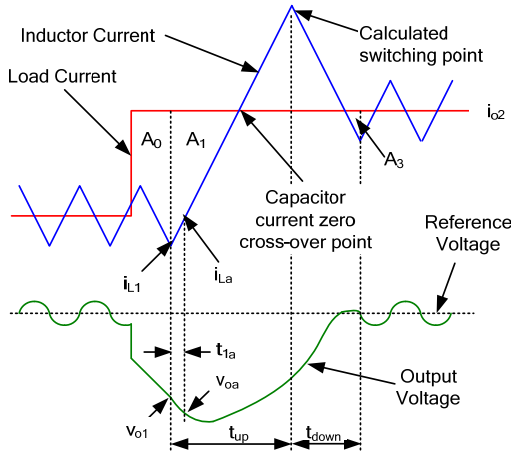

Fig. 9 CBC response under load step transient

In [23], shown in Fig. 1010, a new optimal two-switching cycle compensation algorithm is proposed to achieve optimal transient performance for DC-DC converters under an input voltage change. Using the principle of capacitor charge balance, the proposed algorithm predicts the optimized two-switching cycle duty cycle series to drive the output voltage back to the steady state when the input voltage changes. But the algorithm will lose capabilities for regulation ultrafast and large input voltage transient cases.

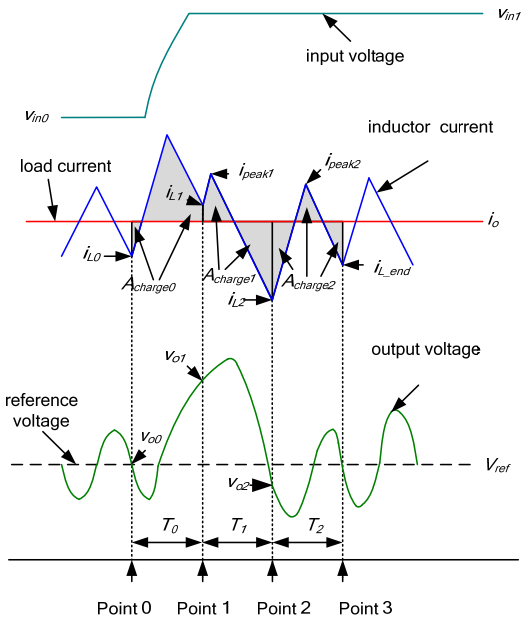

Fig. 10 Charge balance controller response to an input voltage transient

The controller proposed in [18] employs a asynchronous ADC to capture the time point t_1 based on the voltage valley/peak and uses this information to calculate the optimal switching time instants/intervals, while in [21] and [22], the information is used to calculate the correspondingly mapped output voltage at which the controller should alter its output (ON/OFF) state. An advantage of the controller presented in [21] and [22] is that the inductor and capacitor values are not required; however, it is assumed that the ESR of the capacitor is negligible. If not, the capacitor and ESR values would be required in order to compensate the lead time caused by ESR. From practical design point of view, a current limiting scheme is also concerned in [26], while, fast dynamic response performance can be achieved with proper modifications on original CBC algorithm.

A digital implementation of CBC concept is discussed in [25] based on its analog counterpart [24]. In [25], a current estimation algorithm is presented for predicting capacitor current zero-crossover at t_1. And a double accumulator is employed using FPGA to emulate the double integrator in analog domain [24] and enhance the previous controller performance for AVP extension. With the help of double accumulator/integrator, the algorithm dependence on inductance can be removed, however, for AVP applications the capacitance is still required to be known accurately for determining t_2 in the algorithm.

The above nonlinear controllers can be extended to multiphase operation [27] and [28]. In [27], rather than minimum recovery time, it compromises the aim only at achieving the minimum voltage deviations. Further, a smooth controller transition is realized by inserting specified ON/OFF sequences right after the capacitor current undergoes zero-crossover, shown in Fig. 111. However, under a negative load step transient, the improvement is

minor because the conventional linear mode compensator is still well-suited for regulating the low output ratio converters with sub-optimal voltage overshoot.

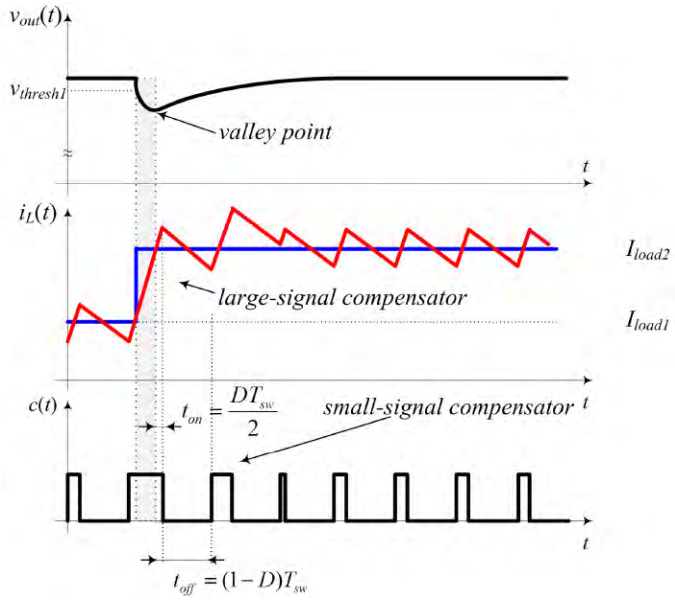

Fig. 11 Principle of operation of the "large-small" signal compensator during light-to-heavy with inserted control sequence

In [28], a current mode digital CBC controller is presented for multiphase Buck converters, which takes advantage of peak current control on the phase inductors to achieve minimum recovery time. During transients shown in Fig. 122, new steady-state current information can be collected at the voltage valley/peak point and the digital peak current reference can be calculated and set based on CBC principles. However, both of the methods [27] and [28] are still limited for low ESR Buck converters and sensitive for passive components' value. Also, the controllers will not work as well for example, if a negative load step occurs before the valley point resulted from a previous positive load step is approached.

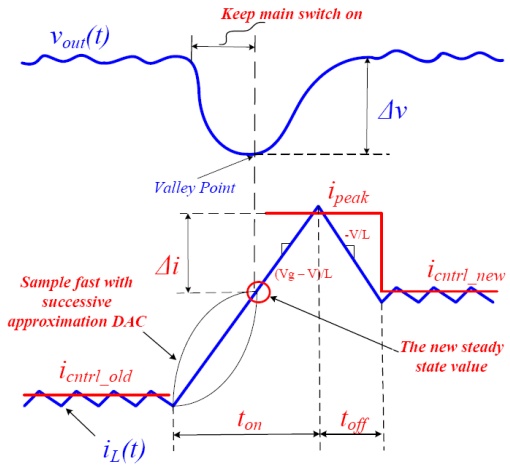

Fig. 12 The key waveforms of a single-phase power stage during a light-to heavy load transient. Top: output voltage; Bottom: the inductor current.

It is demonstrated in [24] shown in Fig. 133 that for low-duty-cycle conversion applications (e.g., 12 $V_{dc} \rightarrow$ 1.5 V_{dc}), the voltage overshoot caused by a step-down load current transient may be more than five times as large as the corresponding voltage undershoot caused by a positive current step of equal magnitude.

This is illustrated in Fig. 133. Therefore, to adhere to voltage specifications, capacitor selection must be based on the larger voltage overshoot condition. Numerous topology modifications to Buck and synchronous Buck converters have been proposed to address the aforementioned problem. Ideally, the steady-state duty cycle would be close to 50% in order to achieve a symmetrical transient response to positive and negative load current changes. One solution is to use two synchronous Buck converters in series in order to increase the duty cycle of the second stage. For example, the first stage could convert the voltages 12 $V_{dc} \rightarrow$ 5 V_{dc} and the second stage could convert the voltages 5 $V_{dc} \rightarrow$ 1.5 V_{dc}. Therefore, the second stage's steady-state duty cycle would be increased from 12.5% to 30%, yielding a much more symmetric transient response. This allows the use of a smaller inductor for a fixed inductor current ripple value. This concept is studied extensively

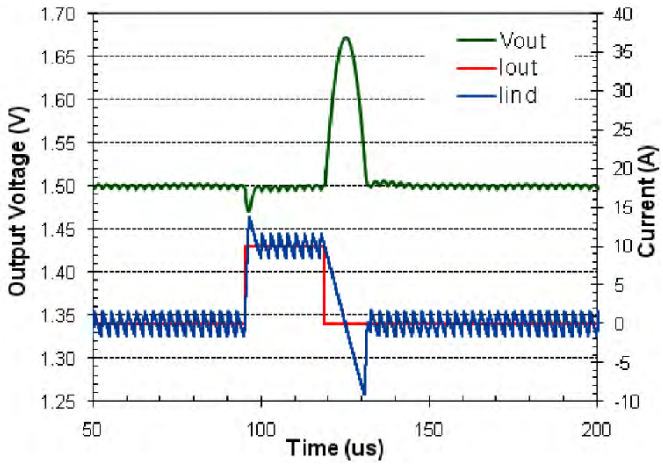

Fig. 13 Asymmetrical transient response to positive and negative load current step change

In [29] and [30]. Three obvious drawbacks of this method are an increase in cost, an increase in physical size, and a decrease in efficiency. However, it is argued in [30] that if a low-enough switching frequency was used in the first stage, then the overall efficiency would not suffer.

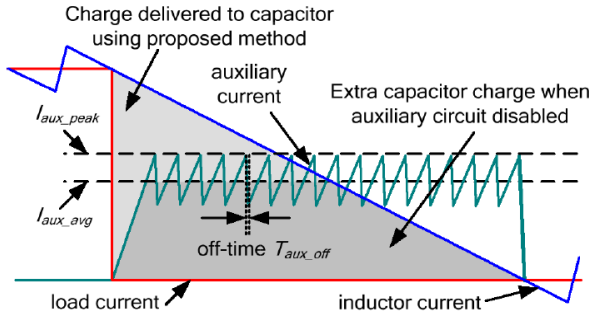

Fig. 14 Peak current mode, constant off-time operation of the proposed controller.

In the paper [31], a controlled auxiliary circuit (CAC) is presented to improve the transient response of a Buck converter. It is well established that for converter applications with a large input/ output voltage ratio, voltage overshoots (due to step-down load transients) are much larger than corresponding voltage undershoots (due to step-up load transients). Therefore, the goal of the proposed method is to reduce the overshoot. The control method only activates the auxiliary circuit during step-down load transients and operates by rapidly transferring excess load current from the output inductor of a Buck converter to the converter's input. The proposed method behaves as a controlled current source shown in Fig. 144 to remove a constant regulated current from the output of the Buck converter. The duration of activation of the auxiliary circuit is also regulated. The proposed circuit has the following advantages:

1) predictable behavior allowing for simplified design;

2) inherent over-current protection;

3) low peak current to average current ratio allowing for use of smaller components.

In addition, the proposed auxiliary controller estimates the magnitude of the unloading transient and sets the auxiliary current proportional to the transient magnitude. This allows for greater design flexibility and increases the auxiliary circuit efficiency for unloading transients of lesser magnitude. In this paper, it is shown through analysis, simulation, and experimental results that a large reduction of voltage overshoot and output capacitor requirements can be realized through the addition of a small MOSFET, diode, and inductor.

Capacitor charge balance control is a concept that has generated numerous digital controllers and subsequent analog designs [14]-[31]. The end result is a very fast reaction to transient events with minimal/reduced settling time. The main drawbacks of the existing CBC implementation methods are as follows:

(1) precise information of converter parameter information such as L and C is required;

(2) fast and accurate ADC for sensing is needed to detect the voltage peal/valley;

(3) complex computation is embedded in CBC algorithm formulas (i.e. division or square root)

(4) the ESR of the output capacitor is assumed to be negligible.

IV. Conclusions

This paper provided a brief review of the present-day topics in digital control of switching converters. As the cost of such controllers decrease and the controller requirements of switching converters become increasingly stringent, it is inevitable that digital controllers will become an integral part of the switching converter industry. Although there still exist some drawbacks to digital control, their unique capabilities such as efficiency optimization, autotuning, and nonlinear control will create a spot that cannot be filled by any analog controller.

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