A New Inductorless Bipolar Gate Driver for Control FET of High Frequency Buck Converters

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***Abstract*—A new inductorless bipolar gate driver for control FET of high frequency buck converters is proposed in this paper. Compared with the conventional unipolar gate driver, the most important advantage of the new gate driver presented in this paper is that it can turn off the power MOSFETs with a negative voltage, which will significantly reduce the turn off time and thus switching loss of the power MOSFETs. In addition, the proposed bipolar gate driver has no inductor in the driver circuit; therefore it can be fully integrated into a chip. Simulation results are provided to validate the benefits of the proposed inductorless bipolar gate driver compared with conventional voltage source driver. A prototype of synchronous buck converter driven by the proposed gate driver was built to verify its functionality and advantages. At 5V input, 1.3V/25A load, in 2 MHz switching frequency, the proposed gate driver increases the efficiency from 75.8% to 77.8%. At 5V input, 1.3V/25A load, in 2.5 MHz switching frequency, the efficiency is improved from 72.9% to 76.5% by the proposed driver. Therefore, the proposed bipolar gate driver is a better choice in high frequency and high current application.**

***Index Terms*— power MOSFET, buck converter, voltage regulator (VR), common source inductor, loss model, bipolar gate driver**

I. INTRODUCTION

Recently, there is a trend to increase the switching frequency of voltage regulators (VRs) above 1MHz [1] - [3]. The purposes for this trend are twofold: Firstly, the size of the passive components, especially the inductive components, is inversely proportional to the switching frequency [4]. As a result, with the switching frequency increasing, the size of the passive components that take up most of space of the VRs is shrinking, which increases the power density of the VRs [5]. Secondly, the dynamic response of the VRs will be better if they are operating in a higher frequency because the design of the wider bandwidth and control loops is more accessible in a higher frequency.

The primary barrier to increase switching frequency is the frequency-dependent losses, such as switching loss, gate drive loss and MOSFET output capacitance loss. In order to reduce the gate drive loss, resonant gate drivers (RGDs) were proposed to recover part of the gate drive loss [6] - [9]. However, RGDs cannot reduce the switching loss, which is the dominant part of the overall frequency-dependent loss.

Current source drivers (CSDs) were proposed to reduce the switching loss with a constant current to charge and discharge the power MOSEFT [10] - [15]. Particularly, it is noted that the major benefit of the CSDs during turn off transition is to turn off the power MOSFET with a negative voltage [16] - [17]. This is very beneficial during high frequency when the impact of the parasitic inductance becomes more significant. However, the inductor required in the CSDs is very hard to be integrated into the driver chip.

A novel inductorless bipolar gate driver is presented in this paper to reduce the turn off time and switching loss of the power MOSFETs. The proposed gate driver can turn off the power MOSFETs with a negative voltage, which will significantly increase the turn off speed and reduce the turn off loss. What is more, the proposed gate driver can be fully integrated into a chip since no inductor is needed in the driver circuit.

Section II presents the topology and main feature of the proposed inductorless bipolar gate driver compared with the conventional driver. The operation principle of the proposed inductorless bipolar gate diver is analyzed in Section III. Section IV illustrates the advantages of the proposed gate driver, which is validated by simulation result under SIMETRIX. Section V shows the experimental results and associated discussions that verify the advantages of the proposed gate driver over the conventional driver. Finally, the conclusions are drawn in Section VI

II. TOPOLOGY AND FEATURE OF PROPOSED INDUCTORLESS BIPOLAR GATE DRIVER

The conventional VSD is illustrated in Figure 1 to drive the power MOSFET, *M*, whose parasitics are shown in blue color: R_G is the gate resistance, C_{GS} is the gate-to-source capacitance, C_{GD} is the gate-to-drain capacitance, C_{DS} is the drain-to-source capacitance, L_S is the common source inductance including the bonding wire inside the MOSFET package and PCB trace inductance and L_D is the switching

loop inductance. The conventional VSD has a totem pole configuration, which turns on the MOSFET by turning on the top switch of VSD, S_P; while turns off the MOSFET by turning on the bottom switch of VSD, S_N.

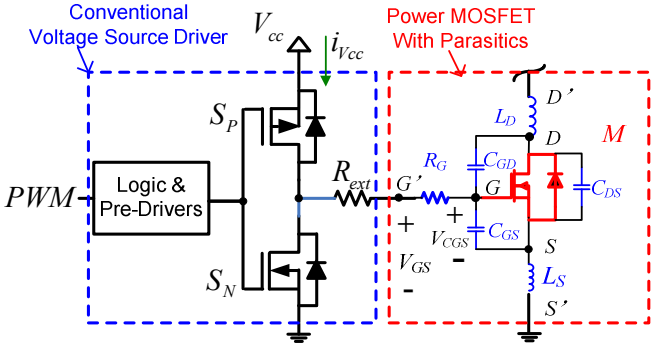


Figure 1 Conventional VSD with power MOSFET and its associated parasitics

The switching waveforms associated with Figure 1 are shown in Figure 2 ,where PWM is the PWM signal input of the VSD, V_{CGS} is the voltage across the C_{GS} of M, V_{DS} is the drain-to-source voltage across M, i_{DS} is the drain-to-source current flowing through the M, P_{on} is the turn on loss and P_{off} is the turn off loss. It is noted that turn off loss is the dominant loss of the total switching loss P_{switch}. It is also observed that, due to the effect of the parasitic inductance, V_{DS} reduces sharply when i_{DS} starts to increases at t_1 and then keeps at a plateau during (t_1 , t_2) since the rising rate of i_{DS} is almost constant in this interval.

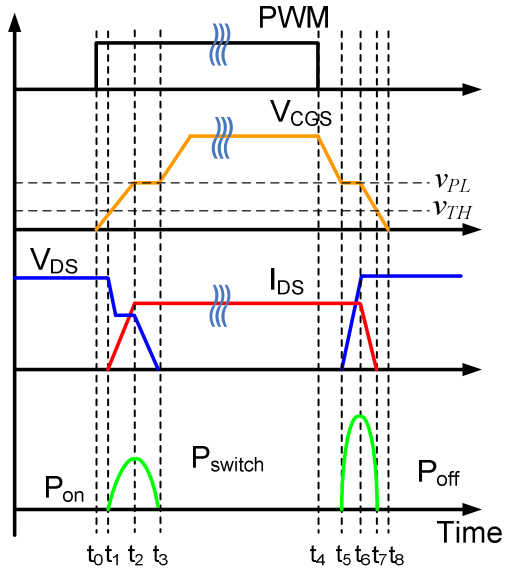


Figure 2 Switching waveforms of power MOSFET driven by the conventional VSD

The equivalent circuit of the MOSFET driven by the VSD during turn – off transition is given in Figure 3. When S_N in Figure 1 is turned on, because of the on resistance of S_N (larger than 0.5Ω), the voltage appearing across the gate-to-source of power MOSFET, V_{GS}, is around 0.5V. Therefore, the main drawback of VSD is that V_{GS} is unipolar, which means V_{GS} is always bigger than zero, even during turn–off transition. It seriously limits the turn – off speed, especially in the presence of the common source inductance in high frequency application as described below.

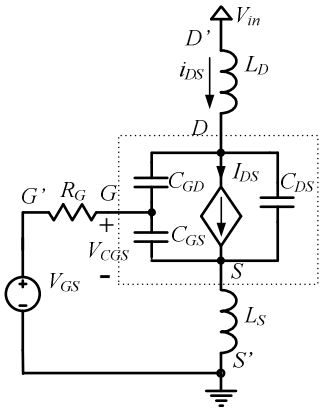


Figure 3 Equivalent circuit of the MOSFET driven by VSD during turn – off transition

An inductorless bipolar gate driver is proposed to drive the control FET of the synchronous buck converter as is shown in Figure 4. The synchronous rectifier is still driven by the conventional unipolar gate driver as its switching loss is very small. The proposed gate driver consists of two driver switches (S_1 and S_2), two capacitors (C_1 and C_2), and one schottky diode (D_1).

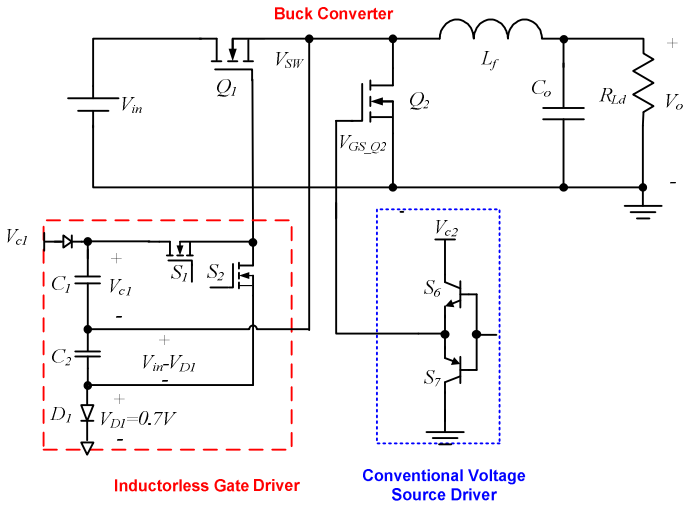


Figure 4 Topology of the proposed inductorless bipolar gate driver

The key waveforms of the proposed gate driver are shown in Figure 5. V_{GS_S1} and V_{GS_S2} are the driver signals for driver switches S_1 and S_2; V_{CGS_Q1} and V_{CGS_Q2} are the gate-source voltages of Q_1 and Q_2 respectively; V_{DS_Q1} is the drain-source voltage of Q_1; I_{DS_Q1} is drain-source current of Q_1; V_{SW} is the switching point of the synchronous buck converter.

The main feature of the proposed gate driver is that it can turn on Q_1 with a positive voltage, and turn it off with a negative voltage. As a result, it is termed as “bipolar gate driver”, which is opposed to the “unipolar gate driver”. The

detailed operations for C_1 and C_2 to build up voltage will be explained in Section III.

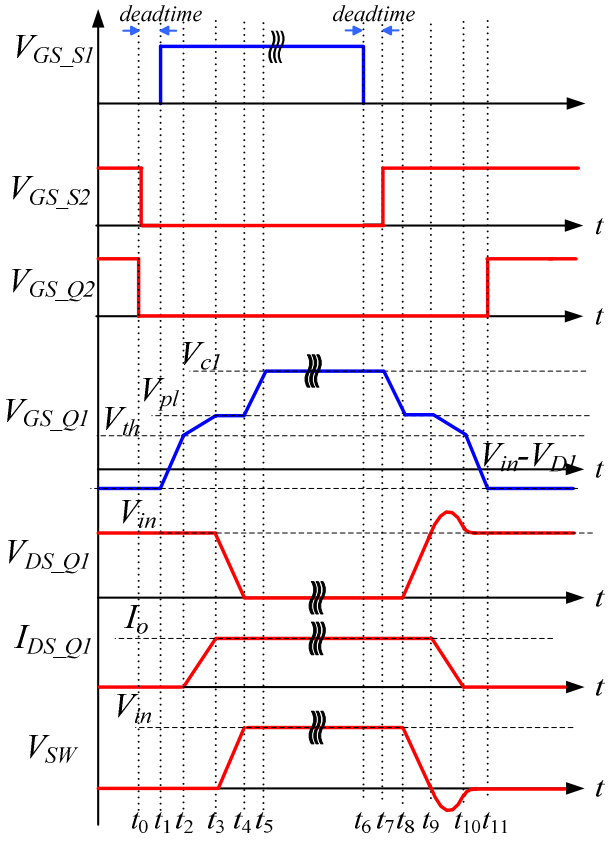


Figure 5 Driver signals and switching waveforms of Q_1

III. Analysis of Switching Intervals With Proposed Bipolar Gate Driver

In this section, the detailed operation of the proposed indutorless bipolar gate driver will be covered. In addition, the piecewise modeling is made to derive the equations for the V_{cgs}, I_{ds} and V_{ds}. Based on the modeling and equations, the calculated switching loss comparison between the proposed indutorless bipolar gate driver and conventional gate driver is made to validate the advantage of the proposed gate driver. Simulation results are also provided to support the advantage of the proposed gate driver. Time period [t_0, t_5] is the turn on transition of Q_1, while the turn off transition is the interval between [t_6, t_{11}].

Before t_0, assume Q_1 is in the OFF state and Q_2 is in the ON state. Therefore, V_{SW} is almost clamped to GND by Q_2. C_1 is charged to V_{C1} through the path shown in Figure 6 and the voltage across C2 keeps unchanged.

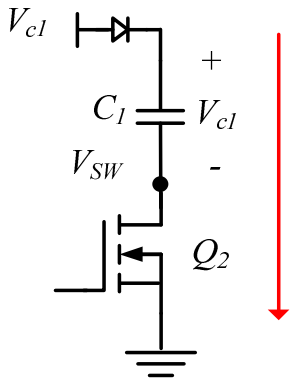


Figure 6 Equivalent circuit for C_1 being charged to V_{C1}

At t_0, S_2 is turned off. After a short period of dead time ([t_0, t_1]), the turn on transition of Q_1 begins at t_1. The turn on transition is made up of four intervals: turn on delay ([t_1, t_2]), current rising ([t_2, t_3]), Miller Plateau ([t_3, t_4]) and the remaining gate charge ([t_4, t_5]).

A. *Turn-ON Transition:*

(a) Turn-on Delay [t_1, t_2]: at t_1, S_1 is turned on, and gate drive voltage V_{C1} is applied across the gate and the source of the power MOSFET. The gate charge current i_G charges the input capacitance C_{ISS1} of the power MOSFET, which is the combination of the gate-to-source capacitance C_{GS1} and the gate-to-drain capacitance C_{GD1}. This interval ends when v_{CGS1}= V_{TH} at t_2.The equivalent circuit of this interval is shown in Figure 7 a.

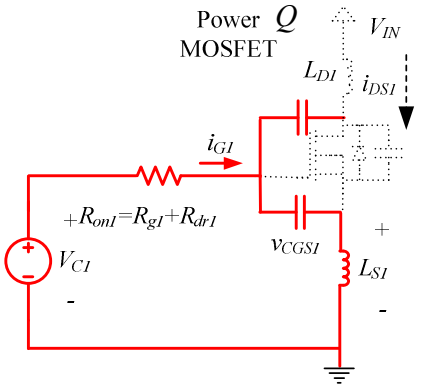
(b) Drain Current Rising [t_2, t_3]: At t_2, v_{CGS1}= V_{TH}. During this interval, v_{CGS1} keeps increasing, and the drain current i_{DS1} starts to rise according to the relationship in Equation (1). The equivalent circuit is shown in Figure 7 b. At this interval, i_{DS1} rises from 0 to I_o, the load current. Since i_{DS1} flows through L_{S1}, the large voltage is induced across L_{S1}, making i_{G1} drop sharply.

$$i_{DS} = g_{fs}(v_{CGS} - V_{TH}) \tag{1}$$

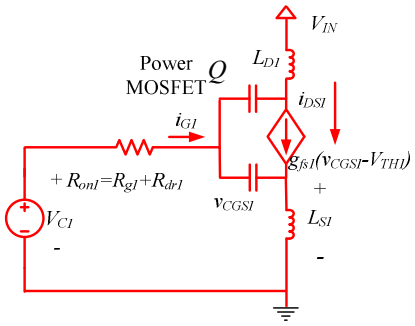
(c) Miller Plateau [t_3, t_4]: At t_3, $i_{DS1} = I_o$. During this interval, v_{CGS1} is held at the Miller Plateau voltage V_{PL1}=V_{TH}+I_o/g_{fs1}.i_{G1} mainly flows through the gate-to-drain capacitance of Q, and v_{DS1} decreases accordingly. It is noted that i_{G1} starts to rapid increase since the EMF across L_s falls sharply due to the unchanged i_{DS1}. The equivalent circuit is given in Figure 7 c.

(d) Remaining Gate Charging [t_4, t_5]: At t_4, V_{DS1} = 0 and V_{CGS1} starts to rise again until it reaches V_{c1}. Due to the rising of the v_{CGS1}, i_{G1} decreases gradually. The equivalent circuit is given in Figure 7 d .

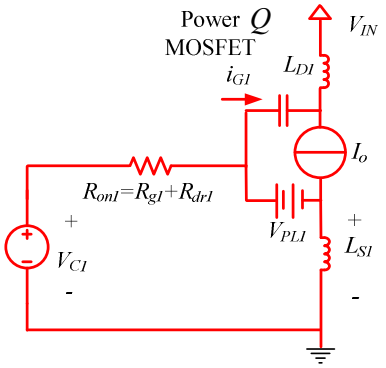
During [t_5, t_6], Q_1 is clamped to ON state by S_1. It is noted that V_{SW} equals V_{IN} during [t_4, t_8]. In this interval the voltage across C_2 is recharged to (V_{IN}-V_{D1}), where V_{D1} is forward voltage drop of the schottky diode D_1, while the voltage across C_1 keeps unchanged. The equivalent circuit for C_2 to be charged to (V_{IN}-V_{D1}) is shown in Figure 8.



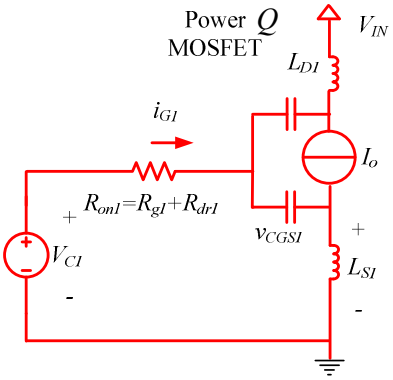
a. (t_1 ,t_2):Turn-on Delay



b. (t_2, t_3): Drain current Rising



c. (t_3, t_4): Miller Plateau



d. (t_4, t_5): Remaining Gate Charges

Figure 7 Turn on operation

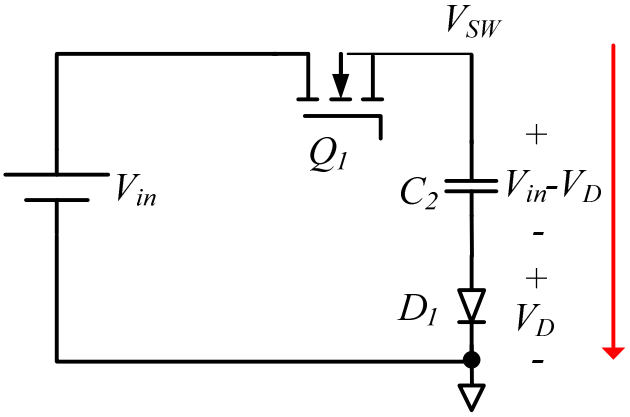


Figure 8 Equivalent circuit for C_2 being charged to (V_{IN}-V_{D1})

B. *Turn-off Transition*

At t_6, $S_1$is turned off. After a short period of deadtime ([t_6, t_7]), S_2 is turned on at t_7. It is noted that the voltage across C_2 is inversely applied to the gate-source capacitance of Q_1, which means Q_1 is turned off with a negative voltage -(V_{IN}-V_{D1}). By contrast, the conventional unipolar gate driver in Figure 1 only can turn off Q_2 with zero voltage. The turn off transition is also made up of four intervals: turn off delay ([t_7, t_8]), Miller Plateau ([t_8, t_9]), current dropping ([t_9, t_{10}]) and the remaining gate discharge ([t_{10}, t_{11}]).

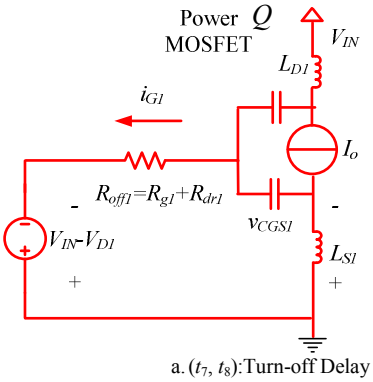
(a) Turn-off Delay [t_7, t_8]: at t_1, S_2 is turned on, and a negative voltage - (V_{IN}-V_{D1}) is applied across the gate and the source of the power MOSFET. The gate charge current i_G discharge the input capacitance C_{ISS1} of the power MOSFET. The initial condition is V_{CGS1_t7}=V_{C1}, i_{G1_t7}=0. This interval ends when v_{CGS1}= V_{TH}+I_o/g_{fs1} at t_8.The equivalent circuit of this interval is shown in Figure 9 a.

(b) Miller Plateau [t_8, t_9]: At t_8, V_{CGS1}= V_{TH}+I_o/g_{fs1}. During this interval, v_{CGS1} is held at the Miller Plateau voltage V_{PL1}=V_{TH}+I_o/g_{fs1}. i_{G1} mainly flows through the gate-to-drain capacitance of Q_1 and v_{DS1} increases accordingly. The equivalent circuit is given in Figure 9 b.

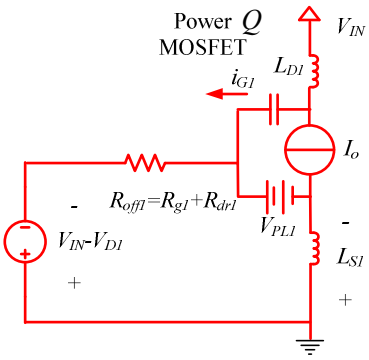
(c) Drain Current Drop [t_9, t_{10}]: At t_9, V_{DS1} = V_{IN}. During this interval, v_{CGS1} decreases, and the drain current i_{DS1} starts to drop according to the relationship in Equation (1).The equivalent circuit is shown in Figure 9 c. At this interval, i_{DS1} drops from I_o to 0. Since i_{DS1} flows through L_{S1}, the large voltage is induced across L_{S1}, making i_G drop sharply.

(d) Remaining Gate Charging [t_{10}, t_{11}]: At t_{10}, i_{DS1} = 0 and v_{CGS1} keeps decreasing until it reaches – (V_{IN}-V_{D1}). Due to the decreasing of the v_{CGS1}, i_{G1} decreases gradually to zero. The equivalent circuit is given in Figure 9 d.

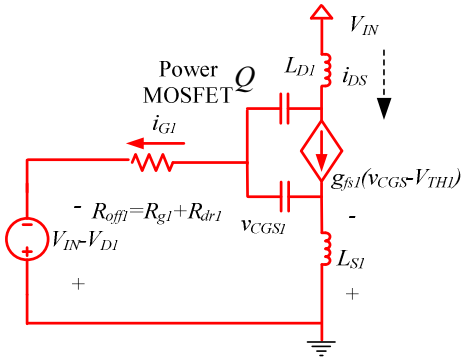
After t_{11}, $Q_1$is clamped to OFF state by S_2 until next switching cycle comes.



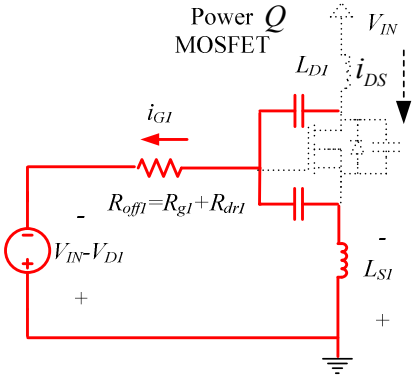
a. (t_7, t_8):Turn-off Delay



b.(t_8, t_9): Miller Plateau



c. (t_9, t_{10}): Drain current Rising



d.(t_{10}, t_{11}): Remaining Gate Discharges

Figure 9 Turn off operation

IV. Benefits Of The Proposed Inductorless Bipolar Gate Driver

The proposed inductorless bipolar gate driver has two main advantages compared with the previous gate drivers:

A. Much faster turn off speed and smaller turn off loss

In order to verify the function and advantage of the proposed bipolar gate driver, the simulation of the power MOSFET driven by the proposed driver is made in Simetrix. The condition for the modeling is: V_{DS}=12V, I_{DS}=25A, f_s=2MHz, L_s=2nH; the power MOSFET used for the simulation is Si7386DP. The performance of the conventional driver is also simulated for comparison. Figure 10 shows the turn off waveforms for conventional driver, while Figure 11 presents the turn off waveforms for the proposed driver. It is noted that the turn off time for conventional driver is 16ns, while for the proposed driver, the turn off time is 6ns, almost one third of the conventional driver, which means the proposed bipolar gate driver can turn off the power MOSFET much faster.

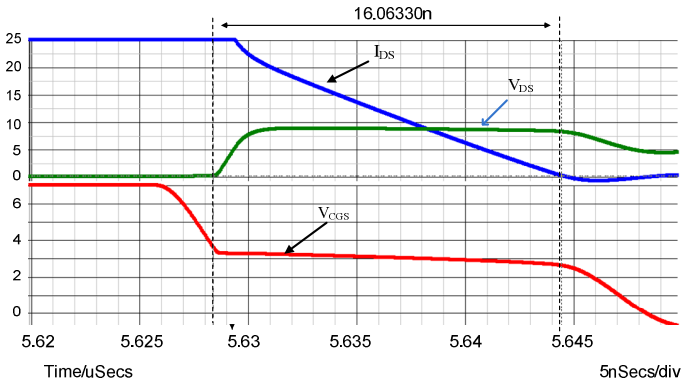


Figure 10 Simulated turn off waveforms of power MOSFET driven by conventional driver

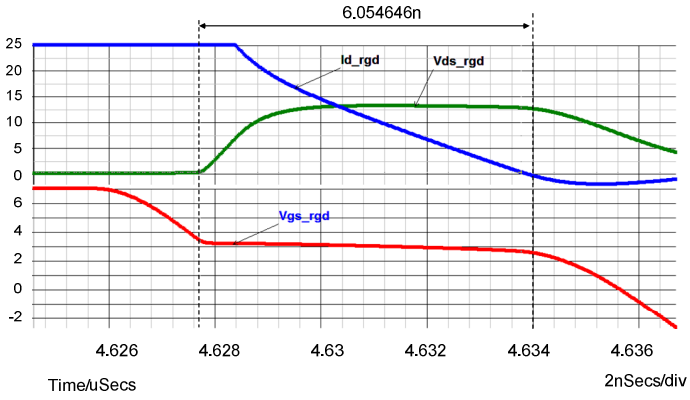


Figure 11 Simulated turn off waveforms of power MOSFET driven by proposed driver

Figure 12 shows the comparison of the simulated turn off loss between the proposed gate driver and conventional

driver at 12V input, 25A drain current in 2MHz switching frequency. It is observed that the turn off loss of the power MOSFET driven by proposed driver is reduced from 2.96W to 1.50W.

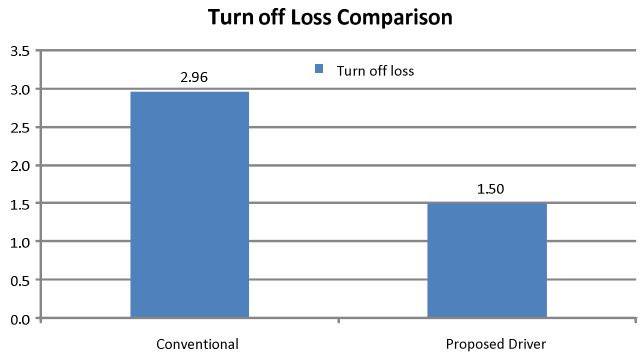


Figure 12 Comparison of the simulated turn-off loss between proposed driver and conventional driver

B. *Inductorless configuration and easiness to be fully integrated*

Since the proposed bipolar gate driver has no inductor in the driver circuits, therefore, it is much easier to be fully integrated into chips, which will further increase the power density of the VRMs.

V. Experimental Results And Discussions

A prototype of a synchronous buck converter was built to verify the feasibility of the proposed inductorless bipolar gate driver as well as the switching loss model. The control FET of the converter is driven with the proposed bipolar gate driver, while the SR is driven with a conventional unipolar gate driver since the switching loss for SR is very small. The picture of the prototype is shown in Figure 13. The operating conditions are: input voltage V_{IN}: 5V; output voltage V_O: 1.3V; switching frequency f_s: 2MHz~2.5MHz.

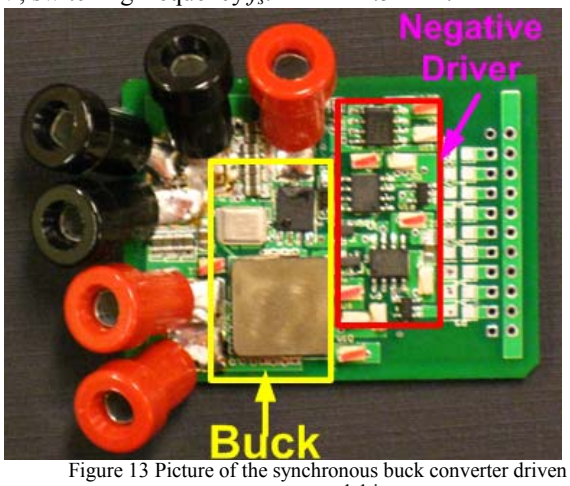


Figure 13 Picture of the synchronous buck converter driven with proposed driver

The PCB consists of 6 layer 4 oz copper. The components used in the circuit are: Q_1: SIR462DP; Q_2: IRF6691; output filter inductance: L_f=100nH; drive switches S_1-S_2: FDN359; D_1:MBR0520.Altera Max II EPM240 CPLD is used to generate the PWM signals with accurate delays since the CPLD can achieve time resolution as high as 1/3 ns per gate. The driver voltages for the control FET and SR are both set to be 7V, to make fair comparison with the conventional driver used in Figure 17.

Figure 14 shows the driving signals for switches S_1, S_2 and Q_2. It is observed that it is necessary to maintain enough deadtime between V_{GS_S1}, V_{GS_S2} to avoid shoot through problem of the driver switches, S_1, S_2.

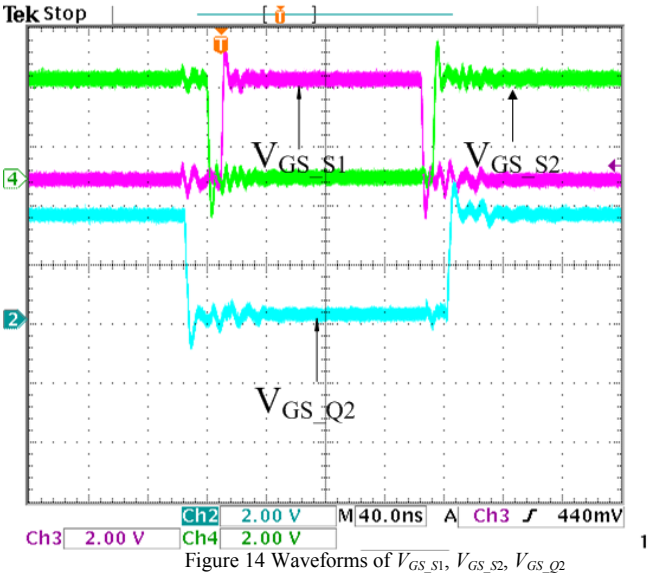


Figure 14 Waveforms of V_{GS_S1}, V_{GS_S2}, V_{GS_Q2}

As is shown in Figure 15, V_{GS_Q1} equals +7V during turn-on transition and is -5V during turn off transition, which validates the feasibility of the proposed inductorless bipolar gate driver.

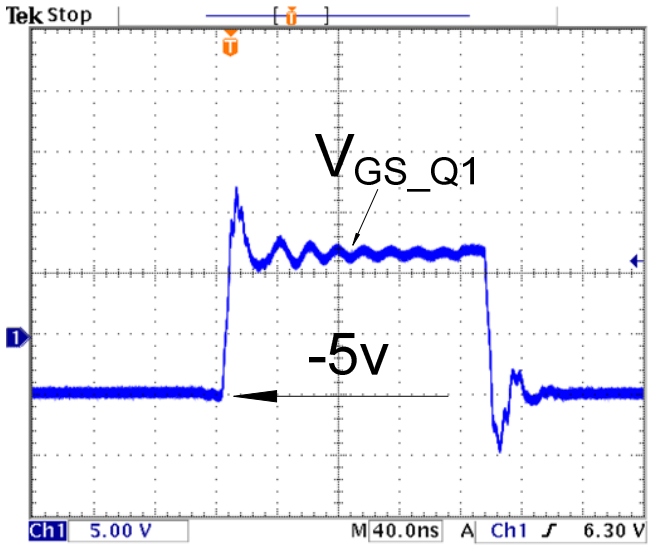


Figure 15 Bipolar Gate Driver signal for $Q1$: V_{GS_Q1}

Figure 16 illustrates the drain-source voltage across Q_2

at 1.3V/25A load under 2MHz operating frequency. It is noted that because the circuit works in 2MHz frequency, the impact of the parasitic inductance becomes more obvious, therefore there are some ringing during the turn on and turn off transitions.

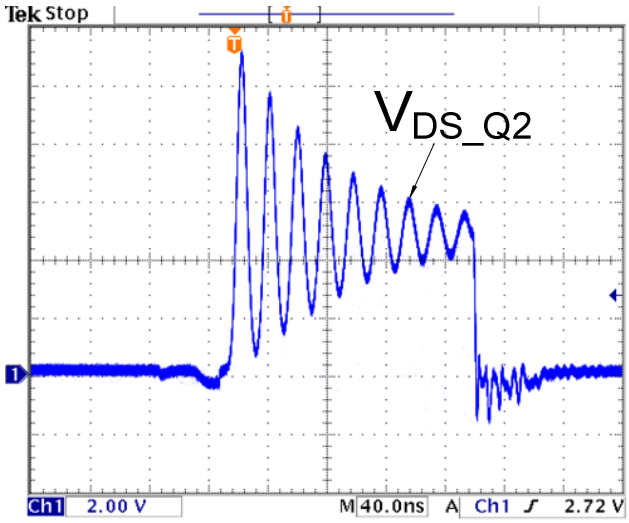


Figure 16 The drain-to-source voltage of $Q2$: V_{DS_Q2}

To make a fair comparison with the proposed gate driver, a benchmark of synchronous buck converter driven by conventional driver was built. In Figure 17, advanced synchronous rectified buck MOSFET drivers ISL6594D from Intersil is used to drive the synchronous buck converter. The driver voltage for control FET and SR are both set to be 7V since the minimum voltage for ISL6594D is 6.8V.

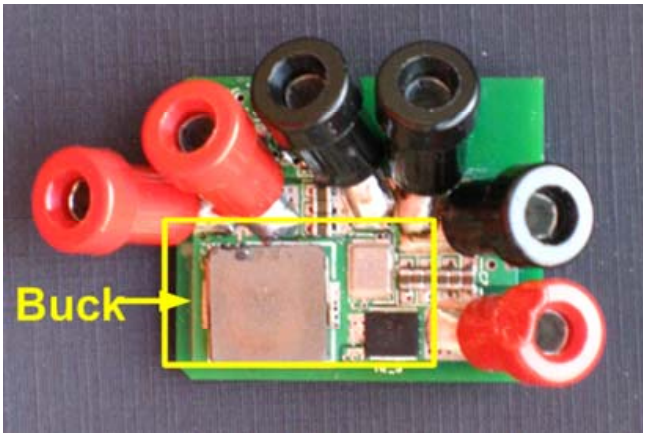


Figure 17 Picture of the buck converter driven with conventional driver

Figure 18 compares the efficiencies of the proposed scheme and conventional driver at 1.3V output in 2MHz operating frequency. It is observed that the efficiency improvement of the buck converter is achieved by the proposed bipolar gate driver; especially at 25A load, the proposed driver increases the efficiency from 75.8% to 77.8%.

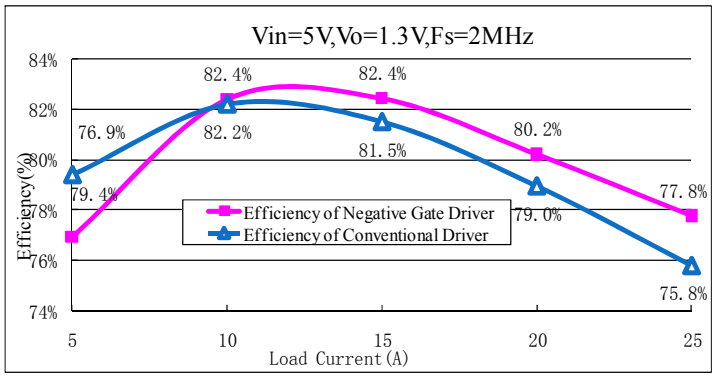


Figure 18 Efficiency comparison at 2MHz between proposed driver and conventional driver

Figure 19 illustrates the measure loss comparison between conventional driver and the proposed inductorless bipolar gate driver at 1.3V output in 2MHz switching frequency. It is observed that as the load increases, the proposed driver can achieve a higher loss reduction; specifically at 25A, the proposed driver can reduce the loss by 0.91W (10.46-9.55W).

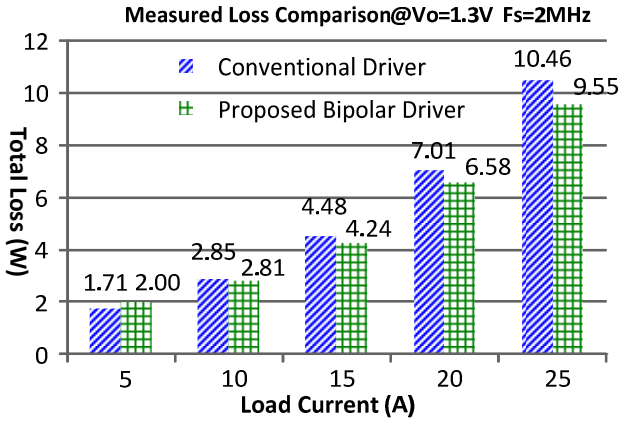


Figure 19 Measured loss comparison at 2MHz between proposed driver and conventional driver

Figure 20 illustrates the efficiencies comparison of the proposed scheme and conventional driver at 1.3V output in 2.5MHz operating frequency. It is noted that the proposed gate driver can achieve better performance than the conventional driver for all load levels. At 5V input, 1.3V/15A load, the efficiency is improved from 79.2% to 81.9%; while for 25A load, the efficiency is boosted from 72.9% to 76.5%.Therefore, as the load increases, the improvement becomes more obvious, which further proves that the proposed bipolar gate driver is a better choice in high frequency and high current application.

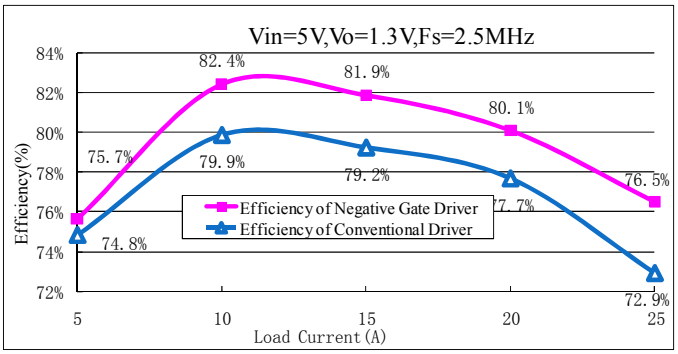


Figure 20 Efficiency comparison at 2.5MHz between proposed driver and conventional driver

Figure 21 shows the measure loss comparison between conventional driver and the proposed inductorless bipolar gate driver at 1.3V output in 2.5MHz switching frequency. It is observed that as the load increases, the proposed driver can achieve a higher loss reduction; specifically at 25A, the proposed driver can reduce the loss by 1.88W (11.95-10.07W).

It is also observed from Figure 19 and Figure 21that, the loss reduction achieved by the proposed driver becomes more significant when the switching frequency increases.

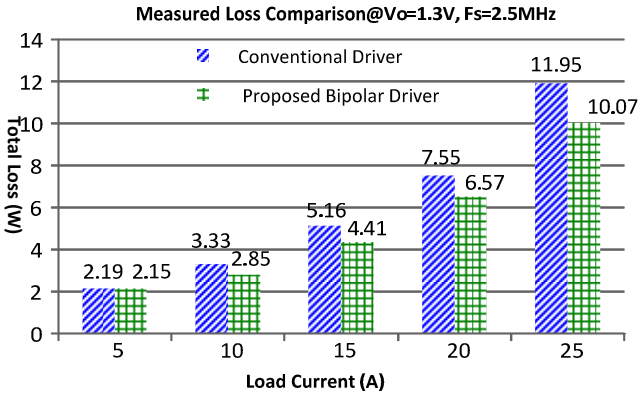


Figure 21 Measured loss comparison at 2.5MHz between proposed driver and conventional driver

VI. Conclusions

A new inductorless bipolar gate driver is proposed in this paper. In comparison with the conventional driver, the proposed driver can turn off the power MOSFET with a negative voltage, which could significantly reduce the turn off loss and thus the switching loss. Also the proposed driver could be fully integrated into a chip as it has no inductor in the circuit. Mathematical modeling and computer simulation are conducted to illustrate the advantages of the proposed gate driver over the conventional driver. The experimental results verify the functionality and advantage of the proposed driver. At 5V input, 1.3V/25A load, in 2 MHz switching frequency, the proposed driver increases the efficiency from 75.8% to 77.8%. At 5V input, 1.3V/25A load, in 2.5MHz switching frequency, the efficiency is boosted from 72.9% to 76.5% by the proposed driver. Therefore, the proposed bipolar gate driver is a better choice in high frequency and high current application.

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