A Nonisolated ZVS Self-Driven Current Tripler Topology for Low-Voltage and High-Current Applications

Zhiliang Zhang, *Member, IEEE*, Eric Meyer, *Member, IEEE*, Yan-Fei Liu, *Senior Member, IEEE*, and Paresh C. Sen, *Life Fellow, IEEE*

***Abstract*—A new nonisolated zero-voltage-switching (ZVS) current tripler topology is proposed in this paper. It is suitable to nonisolated low input voltage applications, especially 12 V input voltage regulator modules (VRMs). At the same time, due to high gate drive voltage using the input voltage, the conduction losses of the SRs can be reduced. The self-driven scheme can also achieve the reduced body diode conduction and gate energy recovery of the SRs so that no external drive IC with the dead time control is needed. More importantly, the existing multiphase buck controllers and buck drivers can be directly used in the proposed topology. Other benefits of the isolated current tripler are also maintained. The nonisolated self-driven current quadrupler and *N*-phase rectifier are also proposed. A 12-V input, 1.0-V/50-A output, 1-MHz prototype was built to verify the advantages of the proposed topology.**

***Index Terms*—Full bridge (FB), high current and low voltage, self-driven, synchronous rectifier (SR), voltage regulator module (VRM), zero-voltage switching (ZVS).**

I. Introduction

In high-performance computer and communication power systems, the output voltage of the voltage regulator modules (VRMs) keeps reducing while output currents are increasing. As an example, for dual-core Intel Xeon Processor 7000/7100 series processor, Intel VRM/EVRD 11.0 is required to support a maximum continuous load current of 130 A and a maximum load current of 150 A peak [1]. This high demanding current causes a serious challenge to rectifier circuits. Furthermore, in order to meet the strict dynamic requirement and achieve high power density, switching frequency of VRMs has increased to megahertz range in recent years [2]–[5].

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Z. Zhang is with the Aero-Power Sci-Tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, P. R. China (e-mail: zlzhang@nuaa.edu.cn).

E. Meyer was with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada. He is now with the Advanced Micro Devices (AMD), Toronoto, ON L3T 7X6, Canada (e-mail: eric.meyer@amd.com).

Y.-F. Liu and P. C. Sen are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: yanfei.liu@queensu.ca; senp@post.queensu.ca).

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Among different high-frequency dc–dc conversion solutions [6]–[8], multiphase buck converters are popular for 12 V VRMs in high-current and low-voltage applications presently due to the simplicity and low cost. However, the buck converter suffers from an extremely low duty cycle that increases the switching losses and the reverse recovery losses of the body diode significantly. More importantly, the parasitic inductance increases the switching losses even higher [9]–[11]. Another important frequency-dependent losses are the gate driver loss, especially synchronous rectifier (SR) MOSFETs with high total gate charge since more SRs are paralleled to reduce the conduction losses at high-current applications. Resonant gate driver technique has strong potential to achieve gate energy recovery [12]–[15]. However, external circuitry has to be required by this technique.

In order to extend the low duty cycle of the buck converter, several nonisolated topologies with the transformers were proposed for 12 V input voltage applications such as the nonisolated half-bridge converter(NHB) [16]–[18], nonisolated full-bridge converter (NFB) [19]–[21], and zero-voltage-switching (ZVS) phase-shift buck (PSB) converter [22]. A nonisolated ZVS self-driven converter was proposed in [23] and [24]. The driving loss and SR body diode loss are both reduced by using self-driven technique for the SRs. Its self-driven schemes were investigated thoroughly in [25] and [26]. Among these topologies, current doubler rectifier topology is used as a most efficient way to achieve low winding losses for low-voltage and high-current applications.

In order to reduce the current stress of the transformer windings with the current doubler rectifier, a new rectification topology for high-current isolated converters was proposed in [27] and [28]. The advantage of this rectification topology is to use an additional inductor to share the load currents other than two inductors in the current doubler structure. However, the concern of the rectification topology is that the current stress of the SRs is not reduced, and consequently, the high-current conduction losses of SRs are not reduced.

An isolated current tripler topology was proposed in [29], which can further reduce the current stress and conduction losses of the SRs and windings. The topology in [29] is optimized for 48 V isolated VRM applications. If this topology is applied to 12 V input nonisolated application, the primary ground and secondary ground need to be connected together. But the problem of not being able to achieve direct SR driving is a major issue of this topology. Actually, it needs three drive transformers for the

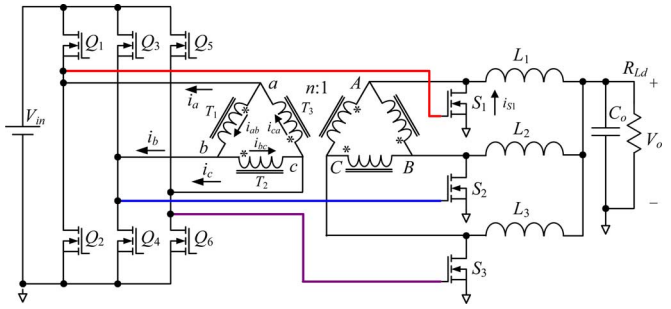

Fig. 1. Proposed nonisolated ZVS self-driven FB converters with current tripler rectifier topology.

SR MOSFETs. Furthermore, the control strategy of this topology is not able to achieve direct SR driving for the nonisolated applications.

The drawbacks of the drive transformers include:

1) the leakage inductance of the SR drive transformers can cause drive signal delay and increase the loss of the SR body diodes;
2) the leakage inductance can also oscillate with the SR gate capacitance and cause voltage spike over the gate terminal;
3) the drive transformers have additional high-frequency loss, especially at 1 MHz switching frequency, and reduce the SR gate energy recovery efficiency;
4) the SR drive transformers need additional board space and cost.

In order to solve the aforementioned problem, a new self-driven ZVS current tripler topology for nonisolated applications is proposed in this paper. The proposed topology is suitable to nonisolated low input voltage applications, especially 12 V input VRMs. For 12 V VRM applications, the variation of the input voltage is limited so that the input voltage can be used to drive the SRs. At the same time, due to high gate drive voltage, the conduction losses of the SRs can be reduced. The proposed converter can also achieve the reduced body diode conduction and gate energy recovery of the SRs. More importantly, the existing multiphase buck controllers and buck drivers can be directly used in the proposed topology. Other benefits of the isolated current tripler in [29] are also maintained, including: 1) the reduced current stress and conduction losses of the SRs and transformer windings; 2) ZVS of all the control MOSFETs; and 3) reduced reverse recovery loss and lower voltage rating SRs with lower $R_{\mathrm{DS(ON)}}$.

Section II presents the proposed nonisolated rectifier converter and its principle of operation. Section III presents the analysis of duty cycle loss, ZVS condition, and loss analysis. Section IV demonstrates the advantages of the proposed converter. Section V contains the experimental results and discussion. Section VI provides a conclusion.

II. Proposed Nonisolated ZVS Self-Driven Current Tripler Topology and Principle of Operation

A. Proposed Nonisolated ZVS Self-Driven Current Tripler Topology

Fig. 1 illustrates the proposed nonisolated ZVS self-driven current tripler converter. In Fig. 1, V_{in} is the input voltage source, $Q_1 - Q_6$ are the control MOSFETs, $S_1 - S_3$ are the SR MOSFETs, L_1, L_2, and L_3 are the output filter inductors, and C_o is the output filter capacitor. In this configuration, three transformers T_1, T_2, and T_3 (turn ratio n) are organized with a delta (Δ) connection. The midpoints (a, b, and c) of each bridge leg are connected to the gate terminals of $S_1 - S_3$ to drive the SRs, respectively.

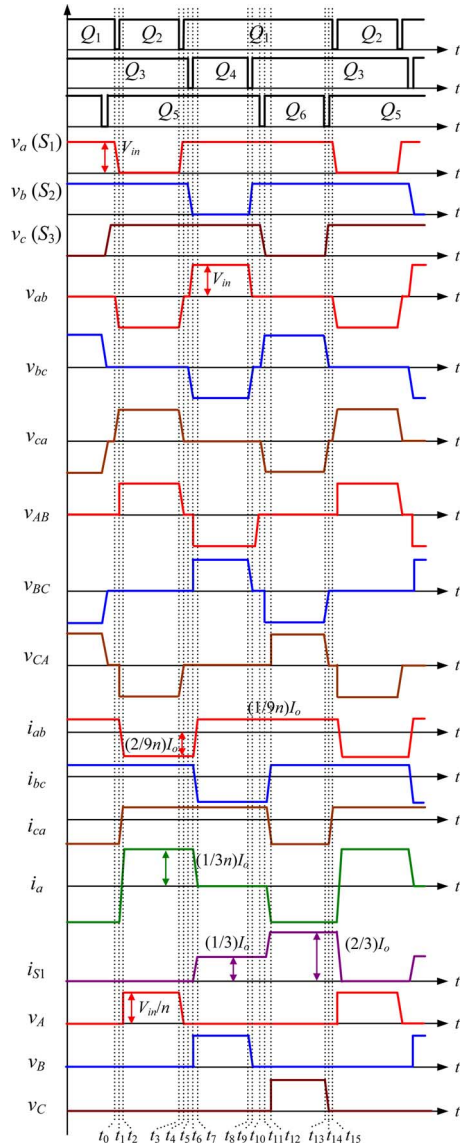

Fig. 2. Key waveforms of the proposed nonisolated current tripler converter.

Fig. 2 illustrates the key waveforms. As shown in Fig. 2, the control MOSFETs in each leg are with complimentarily control; and Q_2, Q_4, and Q_6 in each leg are with interleaving control of 120 degrees phase shifting. Therefore, the voltages applied to the primary sides of each transformer are phase-shifted with 120 degrees. In turn, the magnetic field in each core is also 120 degrees phase-shifted, which allows for a magnetic flux cancellation effect. So, the three transformers can be integrated into one magnetic core similar to an AC three-phase transformer. The connection points (A, B, and C, see Fig. 1) of the secondary sides of the transformers are applied to the output inductors to

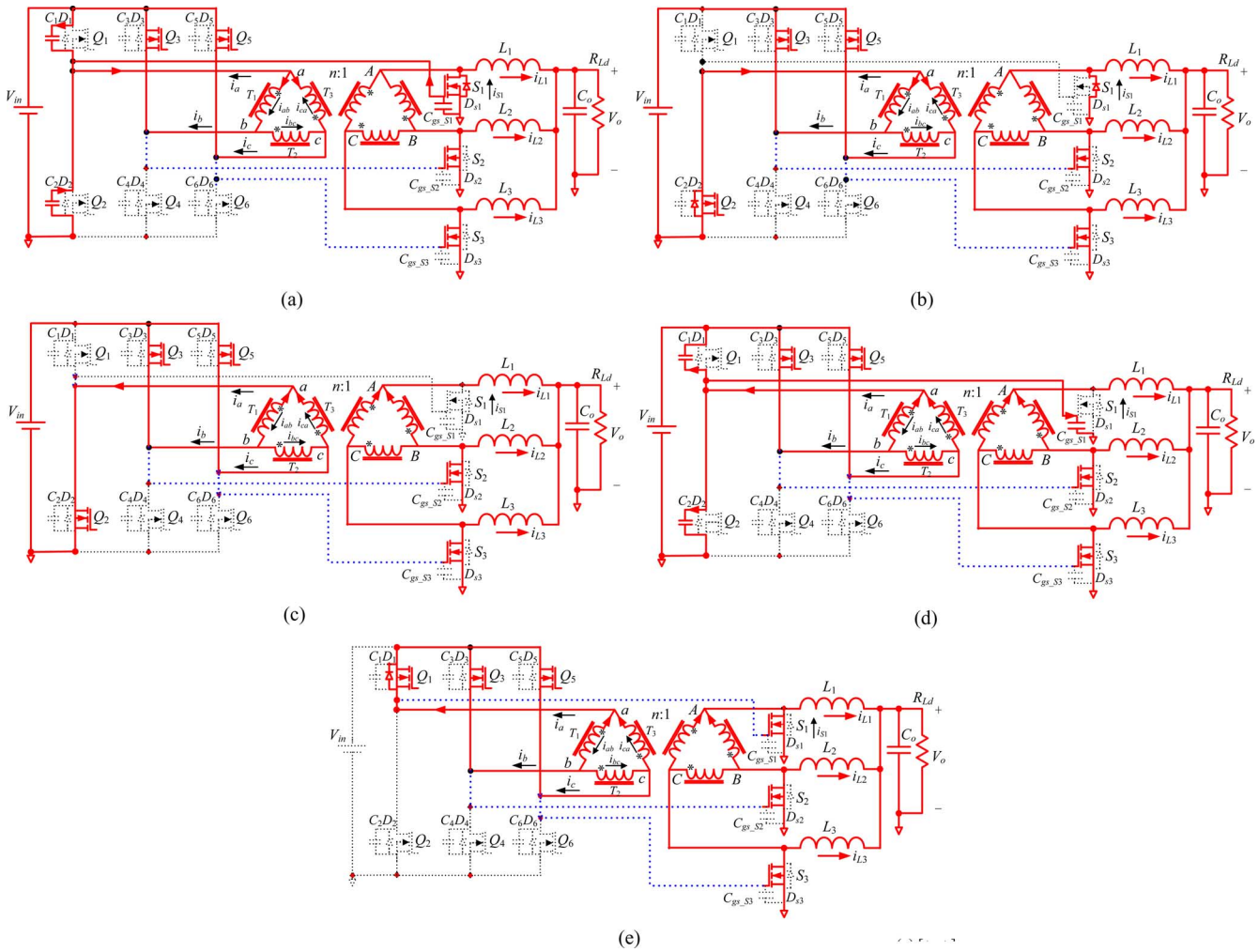

Fig. 3. Equivalent circuits of operation. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$. (c) $[t_2, t_3]$. (d) $[t_3, t_4]$. (e) $[t_4, t_5]$.

form a multiphase rectification structure. Compared to current doubler rectifier, the freewheeling load currents are shared by two SRs rather than one SR. Therefore, the rms currents of the SRs and transformer windings are significantly reduced. This leads to a significant reduction of the conduction losses of the SRs and transformer windings. This is beneficial since the high conduction losses are the dominant losses in low-voltage and high-current applications.

B. Principle of Operation

There are 15 switching modes in one switching period. Accordingly, the equivalent circuits in one-third of one switching cycle are shown in Fig. 3. D_1–D_6 are the body diodes and C_1–C_6 are the intrinsic output capacitors of Q_1–Q_6, respectively, assuming that $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_{\rm oss}$. D_{s1}–D_{S3} are the body diodes and C_{gs_S1}–C_{gs_S3} are the input capacitors of SRs S_1–S_3, respectively, assuming that $C_{gs\_S1} = C_{gs\_S2} = C_{gs\_S3} = C_{gs}$. The output inductors are large enough to be regarded as current sources. The inductor currents $i_{L1} = i_{L2} = i_{L3} = I_o/3$, where I_o is the total output current.

1) Mode 1 [t_0, t_1] [See Fig. 3(a)]: Prior to t_0, Q_1, Q_3, and Q_5 are ON, the voltages over the primary sides and the secondary sides of the transformers T_1, T_2, and T_3 are all zero, i.e., $v_{ab} = v_{bc} = v_{ca} = 0$. The gate drive voltages of the SRs S_1, S_2, and S_3 are all clamped high to the input voltage $V_{\rm in}$. At t_0, Q_1 turns off, and the primary current i_a charges C_1 and discharges C_2 and C_{gs_S1} at the same time. As C_1, C_2, and C_{gs_S1} limit the rising slew rate of the voltage of C_1, Q_1 is under zero-voltage turn-off condition.

During this stage, the energy to discharge C_2 and C_{gs_S1} is provided by the leakage inductance of the transformer. Here, i_a decreases resonantly as

$$i_a(t) = \frac{I_o}{3n} \times \cos\,\omega_r(t - t_0). \tag{1}$$

The voltage v_{C1} of C_1 and v_{C2} of C_2 are

$$v_{c1} = Z_r \times \frac{I_o}{3n} \times \sin\,\omega_r(t - t_0) \tag{2}$$

$$v_{c2} = v_{gs\_S1} = V_{\rm in} - Z_r \times \frac{I_o}{3n} \times \sin\,\omega_r(t - t_0) \tag{3}$$

where $\omega_r = 1/\sqrt{L_k(2C_{\rm oss} + C_{gs})}$ and $Z_r = \sqrt{L_k/(2C_{\rm oss} + C_{gs})}$.

2) Mode 2 [t_1, t_2] [See Fig. 3(b)]: At t_1, $v_{C1} = V_{\rm in}$, and $v_{C2} = 0$, D_2 conducts, which provides zero-voltage turn-on condition for Q_2. It should be noted that due to ZVS, C_{gs_S1} is discharged with i_a, which means that the gate drive energy of the SR is returned to the input voltage source so that the high gate drive losses of SRs can be reduced significantly.

The interval of $[t_0, t_1]$ and the value of i_a at t_1 are

$$t_{1,0} = \frac{1}{\omega_r} \times \sin^{-1}\left(\frac{3nV_{\rm in}}{Z_r \times I_o}\right) \tag{4}$$

$$I_a(t_1) = \frac{I_o}{3n} \times \sqrt{1 - \left(\frac{3nV_{\rm in}}{Z_r \times I_o}\right)^2}. \tag{5}$$

During this stage, i_a decreases and is not enough to power the load, i_{L1} freewheels through the body diode D_{s1} of S_1, i_{L2} freewheels through S_2, and i_{L3} freewheels through S_3, respectively. Then, i_a increases inversely but is still not large enough to power the load.

3) Mode 3 [t_2, t_3] [See Fig. 3(c)]: At t_2, i_a rises to the reflected load current causing D_{S1} to turn off. During this stage, the voltage over the transformer is the input voltage, i.e., $v_{ab} = -V_{\rm in}$, $v_{ca} = V_{\rm in}$. The energy transfers from the primary side of the transformer to the load. The voltage over the primary side of T_2 is zero, i.e., $v_{bc} = 0$. The inductor current i_{L2} freewheels through S_2 and i_{L3} freewheels through S_3, respectively.

4) Mode 4 [t_3, t_4] [See Fig. 3(d)]: At t_3, Q_2 turns off, and the primary current i_a charges C_2 and C_{gs_S1} and discharges C_1. As C_1, C_2, and C_{gs_S1} limit the rising slew rate of the voltage of C_2, Q_2 is under zero-voltage turn-off condition. During this stage, the energy to discharge C_1 is provided by the leakage inductance and L_1. Here, L_1 is large enough to be regarded as a constant current source so that the primary current i_p keeps the value $I_{a2} = I_{L1}/n$, where I_{L1} is the dc current of L_1. The voltage of C_2 rises linearly and the voltage of C_1 decays linearly.

The interval of $[t_3, t_4]$ is

$$t_{4,3} = \frac{3nV_{\rm in}(2C_{\rm oss} + C_{gs})}{I_o}. \tag{6}$$

5) Mode 5 [t_4, t_5] [See Fig. 3(e)]: At t_4, D_1 conducts, which provides zero-voltage turn-on condition for Q_1. The voltages over the primary sides of T_1, T_2, and T_3 are zero, i.e., $v_{ab} = v_{bc} = v_{ca} = 0$. The gate drive voltages of the SRs S_1, S_2, and S_3 are all clamped high to the input voltage again. The inductor currents i_{L1}, i_{L2}, and i_{L3} freewheel through S_1, S_2, and S_3, respectively. At t_5, Q_3 turns off and the other two-thirds of the switching cycle start. The principle of operation is similar to Mode 1–Mode 5 except for polarity changes.

III. Duty Cycle Loss, ZVS Condition, and Loss Analysis

A. Duty Cycle Loss

As shown in Fig. 2, during $[t_1, t_2]$ and $[t_6, t_7]$, the leakage inductance of the transformer limits the rise (or decay) slope of i_a. Transition time is required for i_a to travel from the positive direction to the negative direction (or vice versa). During this transition time, the primary voltage of the transformer v_{AB} is $+V_{\rm in}$ or $-V_{\rm in}$, i_p is lower than the reflected load current, and all the SR diodes conduct. This makes the secondary rectified voltage v_A and v_B zero; thus, v_{AB} loses the voltage in $[t_1, t_2]$ and $[t_6, t_7]$, respectively.

The duty cycle loss $D_{\rm loss}$ during $[t_1, t_2]$ and $[t_6, t_7]$ is

$$D_{\rm loss} = \frac{2I_o}{3n \times T_s} \times \frac{L_k}{V_{\rm in}} \tag{7}$$

where I_o is the output current, L_k is the leakage inductance, and n is the transformer turns ratio.

It is noted that the duty cycle loss should be minimized by reducing the leakage inductance of the transformer, especially under the low duty cycle condition. The leakage inductance can be minimized by interleaving the primary windings and secondary windings of a planar transformer. However, the lower leakage inductance will reduce the range of ZVS. Therefore, this is design tradeoff between the duty cycle loss and ZVS range.

The voltage gain of the proposed converter is

$$V_o = \frac{V_{\rm in}}{n} \times D \tag{8}$$

where $V_{\rm in}$ is the input voltage, D is the duty cycle, V_o is the output voltage, and n is the transformer turns ratio.

For $V_{\rm in} = 12$ V and $V_o = 1.0$ V, in order to make the converter work properly, the maximum duty cycle should be limited below 1/3 theoretically ($D_{\max} < 1/3$). In addition, the duty cycle loss has to be considered. Therefore, $n < V_{\rm in}/V_o \times D_{\max} = 12\ {\rm V}/1\ {\rm V} \times (1/3) = 4$, and the turns ratio is chosen as $n = 3$.

B. Condition of ZVS

In Fig. 3(d), for the upper control MOSFETs (Q_1, Q_3, and Q_5), the energy to achieve ZVS is provided by the output inductors, so (9) should be satisfied

$$\begin{aligned}\frac{1}{2} \times L_f \times I_o^2 &\geq \frac{1}{2} \times C_1 \times V_{\rm in}^2 + \frac{1}{2} \times (C_2 + C_{gs\_S1}) \times V_{\rm in}^2 \\ &= C_{\rm oss} \times V_{\rm in}^2 + \frac{1}{2} \times C_{gs\_S1} \times V_{\rm in}^2\end{aligned} \tag{9}$$

where L_f is one of the output filter inductors, $L_1 = L_2 = L_3 = L_f$; $C_1 = C_2 = C_{\rm oss}$ (output capacitances of Q_1 and Q_2), and C_{gs_S1} is the gate capacitance of S_1. Here, $C_{\rm oss}$ and C_{gs_S1} are not constant due to the nonlinear properties of the MOSFET parasitics. However, the values of $C_{\rm oss}$ and C_{gs_S1} can be obtained from the datasheets. Therefore, the energy stored in $C_{\rm oss}$ and C_{gs_S1} can still be calculated using $1/2CV^2$, even if the $C_{\rm oss}$ and C_{gs_S1} change when the voltage varies. As an example, for $V_{\rm in} = 12$ V, $V_o = 1.0$ V, $C_{\rm oss} = 0.65$ nF, and $C_{gs\_Q5} = 6.6$ nF, the energy needed to achieve ZVS from (9) is 569 nJ, while the energy of the output inductor is 2375 nJ at $I_o = 5$ A, which is much higher than the energy needed to achieve ZVS. Therefore, Q_1 and Q_3 can achieve ZVS in a wide load range.

In Fig. 3(a), for the lower control MOSFETs (Q_2, Q_4, and Q_6), the energy to realize ZVS is provided by the leakage

inductance of the transformer, so (10) should be satisfied

$$\frac{1}{2}\times L_k\times\left(\frac{I_o}{3\times n}\right)^2\geq\frac{1}{2}\times C_1\times V_{\rm in}^2+\frac{1}{2}\times(C_2+C_{gs\_S1})\times V_{\rm in}^2=C_{\rm oss}\times V_{\rm in}^2+\frac{1}{2}\times C_{gs\_S1}\times V_{\rm in}^2 \quad (10)$$

where L_k is the leakage inductance of the transformer. Note that the larger the leakage inductance, the easier to achieve ZVS. We can take advantage of the energy of the leakage inductance of the transformer that is very similar to the ZVS condition of the lagging leg of the traditional full-bridge converter [30].

However, the larger leakage inductance results in higher duty cycle loss. The leakage inductance L_k can be chosen based on (10), depending on ZVS range

$$L_k\geq\frac{2C_{\rm oss}\times V_{\rm in}^2+C_{gs\_Q5}\times V_{\rm in}^2}{(I_{o\_\rm ZVS}/3n)^2}. \quad (11)$$

As an example, for $V_{\rm in}=12$ V, $V_o=1.3$ V, $n=3$, $C_{\rm oss}=0.65$ nF, and $C_{gs\_Q5}=6.6$ nF, in order to achieve ZVS at $I_{o\_\rm ZVS}=40$ A, from (11), the leakage inductance can be calculated as 50 nH. With the transformer turn ratio $n=3$, this leakage inductance reflected to the secondary side is about 5.6 nH (50 nH/n^2). Compared with the output inductor $L_f=190$ nH, this value is small. The core of the transformer we used in the experiment is one-third of the EI32 core. The standard EI32 core is cut into one-third of the width. The output inductors are formed from ICE components and the part number is LP02-191-5. The size of the profile of the inductor is 13.5 mm $\times$ 13 mm $\times$ 8 mm [31].

C. Loss Analysis

1) Conduction Loss Comparison of SRs: From the waveform of i_{S1} in Fig. 2, the rms current of SR S_1 with current tripler is

$$I_{S1\_\rm rms}=\sqrt{\frac{1}{3}\times\left(\frac{I_o}{3}\right)^2+\frac{1}{3}\times\left(\frac{2I_o}{3}\right)^2}=\frac{\sqrt{15}}{9}I_o\approx 0.43I_o. \quad (12)$$

The rms current of SR MOSFET S_1 of the current doubler is

$$I_{S1\_\rm rms}=\sqrt{\frac{1}{2}}\times I_o\approx 0.71I_o. \quad (13)$$

For example, $V_{\rm in}=12$ V, $V_o=1.0$ V, and total load current 120 A, in order to do the fair comparison, each phase is assumed to proved 20 A. So, we can use three ZVS self-driven FB VR converters to parallel and each of them provides $I_o=40$ A. If the three-phase nonisolated ZVS self-driven FB converters with current tripler in Fig. 1 are used, we need two converters to parallel and each of them provides $I_o=60$ A. According to (12) and (13), Fig. 4 shows the SR rms current comparison between the conventional current doubler and the proposed self-driven converter. It can be seen that at the load current of 60 A, the rms current of each SR is reduced from 28.4 to 25.8 A.

In the experiment, 20 V IRF6691 from International Rectifier is chosen as the SR MOSFETs. The $R_{\rm DS(ON)}$ of each IRF6691 is 1.6 mΩ at $V_{GS}=12$ V and three SR MOSFETs are used

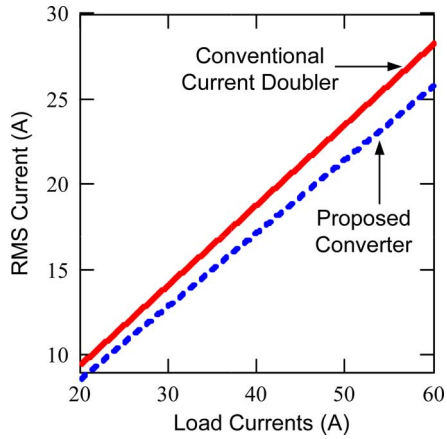

Fig. 4. RMS current comparison of SRs: Conventional current doubler versus proposed converter.

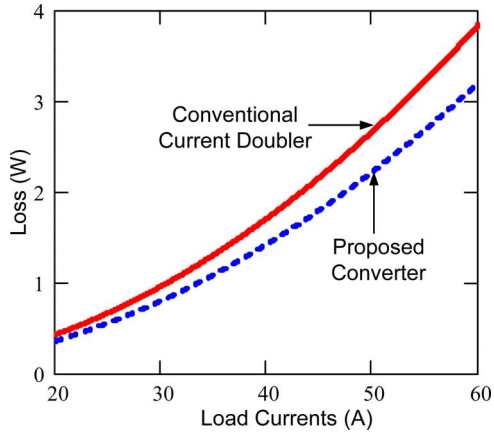

Fig. 5. Conduction loss comparison of SRs: Conventional current doubler versus proposed converter.

totally. Fig. 5 illustrates the total conduction loss comparison of the SRs. Note that at 60 A, the rms current reduction translates into the SR conduction loss reduction of 0.6 W (3.8 W $-$ 3.2 W), which is a reduction of 15.8% (0.6 W/3.8 W) of the total SR conduction loss. This is 1.0% of the output power, i.e., 0.6 W/(1.0 V $\times$ 60 A).

2) Conduction Loss Comparison of Transformer Windings: From the waveform of i_{ab} in Fig. 2, the current rms value of the primary windings with current tripler is

$$I_{\rm Sec\_rms}=\frac{1}{n}\times\sqrt{\frac{1}{3}\times\left(\frac{2I_o}{9}\right)^2+\frac{2}{3}\times\left(\frac{I_o}{9}\right)^2}=\frac{\sqrt{2}}{9n}I_o\approx 0.16\frac{I_o}{n}. \quad (14)$$

The current rms value of the primary windings with the current doubler is

$$I_{\rm Sec\_rms}=\frac{1}{n}\times\frac{I_o}{2}=0.5\frac{I_o}{n}. \quad (15)$$

According to (14) and (15), Fig. 6 shows the rms current comparison of the transformer primary windings between the conventional current doubler and the proposed self-driven

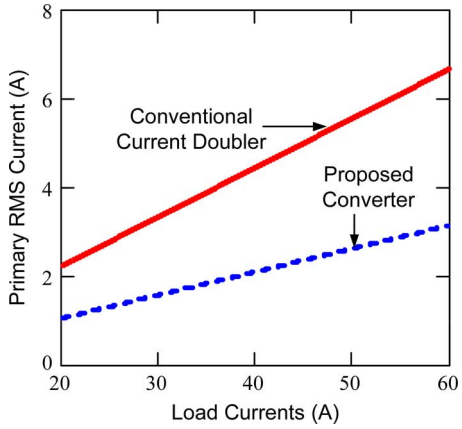

Fig. 6. RMS current comparison of primary windings: Conventional current doubler versus proposed converter.

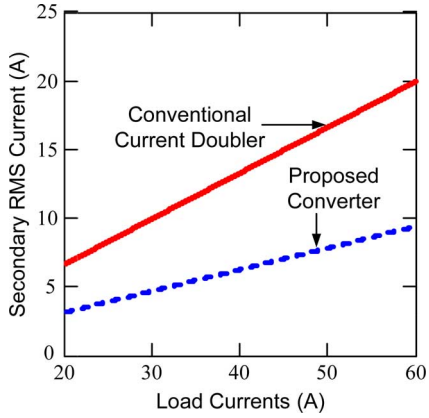

Fig. 7. RMS current comparison of secondary windings: Conventional current doubler versus proposed converter.

converter. It is seen that at 60 A, the rms current value is reduced from 6.7 to 3.1 A with the proposed converter. Assuming the same primary winding ac resistance $R_{\mathrm{ac\_pri}}$, the winding loss of the current tripler is $P_{\mathrm{pri\_tripler}} = 3.1^2 \times 6R_{\mathrm{ac\_pri}}$ since there are six secondary windings, while the winding loss of the current doubler is $P_{\mathrm{pri\_doubler}} = 6.7^2 \times 3R_{\mathrm{ac\_pri}}$ since there are three secondary windings. Therefore, the total secondary winding loss reduction is 57.2% $(1 - P_{\mathrm{pri\_triplerc}}/P_{\mathrm{pri\_doubler}})$.

Similarly, the rms value of the secondary winding current with current tripler is

$$I_{\mathrm{Sec\_rms}} = \sqrt{\frac{1}{3} \times \left(\frac{2I_o}{9}\right)^2 + \frac{2}{3} \times \left(\frac{I_o}{9}\right)^2} = \frac{\sqrt{2}}{9} I_o \approx 0.16 I_o. \tag{16}$$

The rms value of the secondary winding current with the current doubler is

$$I_{\mathrm{Sec\_rms}} = \frac{I_o}{2}. \tag{17}$$

According to (16) and (17), Fig. 7 shows the rms current comparison of the transformer secondary windings between the conventional current doubler and the proposed self-driven converter. As can be seen that at 60 A, for the high-current secondary winding loss, the rms current is reduced from 20 to 9.6 A with the proposed topology. Assuming the same secondary winding ac resistance $R_{\mathrm{ac\_sec}}$, the winding loss of the current tripler is $P_{\mathrm{sec\_tripler}} = 9.6^2 \times 6R_{\mathrm{ac\_sec}}$ since there are six secondary windings, while the winding loss of the current doubler is $P_{\mathrm{sec\_doubler}} = 20^2 \times 3R_{\mathrm{ac\_sec}}$ since there are three secondary windings. Therefore, the total secondary winding loss reduction is 53.9% $(1 - P_{\mathrm{sec\_tripler}}/P_{\mathrm{sec\_doubler}})$.

D. Topology Extension

Similarly, a four-phase nonisolated ZVS self-driven FB converter with current quadrupler rectifier can be obtained, as shown in Fig. 8, and the corresponding waveforms are given in Fig. 9. The four-transformer structure can use two magnetic cores using the magnetic integration due to the magnetic flux cancellation effect.

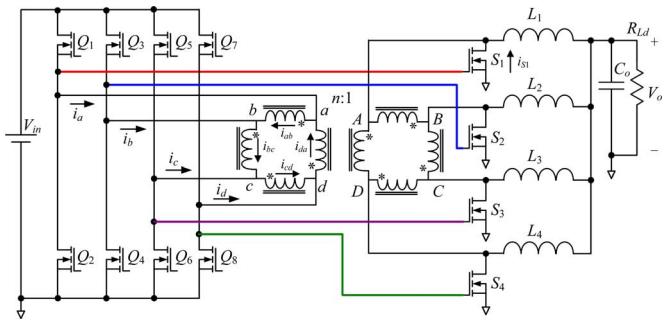

Fig. 8. Proposed four-phase nonisolated ZVS self-driven FB converters.

From the waveform of i_{S1} in Fig. 9, the rms current of SR MOSFET S_1 of the current quadrupler is

$$I_{S1\_\mathrm{rms}} = \sqrt{\frac{1}{4} \times \left(\frac{I_o}{8}\right)^2 + \frac{1}{4} \times \left(\frac{I_o}{4}\right)^2 + \frac{1}{4} \times \left(\frac{3I_o}{8}\right)^2} = \frac{\sqrt{14}}{16} I_o. \tag{18}$$

The rms value of the secondary winding current with current quadrupler is

$$I_{\mathrm{Sec\_rms}} = \sqrt{\frac{1}{4} \times \left(\frac{3I_o}{16}\right)^2 + \frac{3}{4} \times \left(\frac{I_o}{16}\right)^2} = \frac{\sqrt{3}}{16} I_o. \tag{19}$$

For the similar example, $V_o = 1.0$ V and $I_o = 100$ A; in order to do the fair comparison, each phase is assumedto be of 25 A. So, we need two ZVS self-driven FB VR converters with current doubler rectifier to parallel as a module. According to (13), the rms current of each SR MOSFET is 35.4 A. Assuming that the $R_{\mathrm{DS(ON)}}$ of the SR MOSFET is 1.6 mΩ, and the total SR conduction loss is 8.0 W ($I_{\mathrm{rms}}^2 R_{\mathrm{DS(ON)}} \times 4$). For the four-phase nonisolated ZVS self-driven FB converter with current quadrupler rectifier in Fig. 8, two of these converters need to be paralleled. According to (18), the rms current of each SR MOSFET is 23.4 A. So, the total conduction loss of SR MOSFETs is 3.5 W ($I_{\mathrm{rms}}^2 R_{\mathrm{DS(ON)}} \times 4$). This leads to a significant SR loss reduction of 4.5 W, which is a reduction of 56.3% (4.5 W/8.0 W)

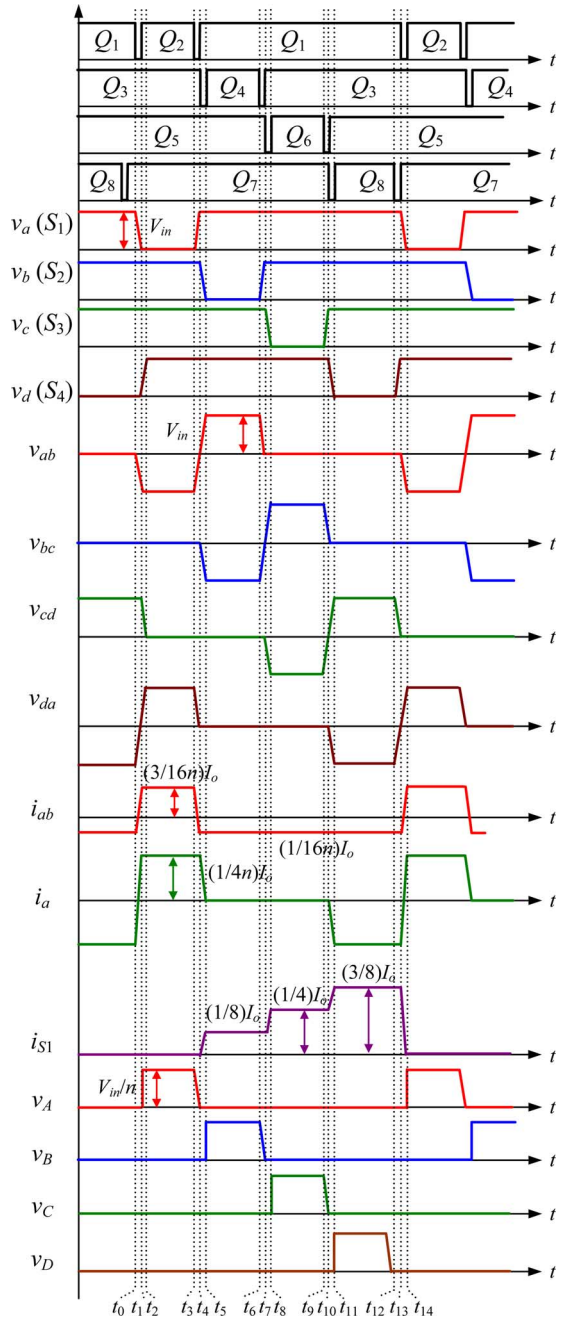

Fig. 9. Key waveforms of four-phase nonisolated ZVS self-driven FB converters with current quadrupler rectifier.

of the total SR loss and 4.5% of the output power (4.5 W/1.0 V/100 A).

For the high-current secondary winding loss, the rms current of the secondary winding with current quadrupler is 10.8 A from (19) and the rms current of the secondary winding with current doubler is 25 A from (17). This leads to the total secondary winding loss reduction of 62.7% $(1 - 10.8^2 \times 4R_{\rm ac}/25^2 \times 2R_{\rm ac})$, assuming the same secondary winding ac resistance $R_{\rm ac}$.

Fig. 10 shows the simulated waveforms of the self-driven quadrupler rectifier. Here, v_{ab}, v_{bc}, v_{cd}, and v_{da} are the primary-side voltages. The phase voltages are 90 degrees phase-shifted, which means that the magnetic flux cancellation is achieved. Here, i_{S1} is the drain-to-source current and v_a is the gate drive voltage of the SR MOSFET S_1. Note that when S_1 carries current, the phase voltage v_a is applied as the self-driven gate voltage to achieve the synchronous rectification.

In addition, *N*-phase nonisolated ZVS self-driven FB converters with multiple stages rectifier can also be extended from the same idea, as shown in Fig. 11, to provide more output currents.

IV. Advantages and Limitations of the Proposed Topology

A. Advantages of the Proposed Topology

The advantages of the proposed converter are highlighted as follows:

1) Extension of Duty Cycle: According to the voltage gain of $V_o = (V_{\rm in}/n)D$, in order to achieve $V_{\rm in} = 12\,{\rm V}$ and $V_o = 1.0\,{\rm V}$, with $n = 3$, the required duty cycle is $D = 0.25$. However, for the same output voltage and input voltage, the duty cycle of a buck converter is only 0.08. Therefore, the duty cycle is extended by three times.

2) ZVS of the Control MOSFET*s:* With the proposed control strategy, all the control MOSFETs can achieve ZVS and this will reduce the switching losses significantly at high frequency (>1 MHz).

3) Gate Energy Recovery of SR MOSFET*s and Reduced Body Diode Conduction:* One of the most important advantages of the proposed topology is the self-driven capability for the SRs and no external drive ICs are needed any more. Also, with the self-driven control, the dead time is minimized inherently to reduce the body diode conduction loss significantly. More importantly, the self-driven circuit actually forms a current-source driver by using the leakage inductance of the transformer to ensure the fast turn-on and turn-off transition of the SRs and recover gate energy at the same time, which is critical at switching frequency of megahertz. And it also provides high gate drive voltage (input voltage, usually 12 V) for SR MOSFETs with lower $R_{\rm DS(ON)}$ to reduce the conduction losses further.

4) Reduced Conduction Loss of SRs and Body Diode Reverse Recovery Loss: The most important advantage of this proposed topology is that the rms currents of the SRs and transformer windings are significantly reduced compared to nonisolated converters with current doubler rectifier. Compared to the current doubler rectifier, the freewheeling load currents are shared by two SRs rather than one SR that reduces the current rms value significantly. According to the loss analysis in Section III, the proposed topology achieves the SR conduction loss reduction of 17%, the primary winding conduction loss reduction of 57.2%, and the secondary winding conduction loss reduction of 53.9%.

B. Limitations of the Proposed Topology

Compared with the conventional current doubler rectifier, the proposed converter needs three transformers theoretically. However, owing to the magnetic integration technology, these three transformers can be integrated into one magnetic

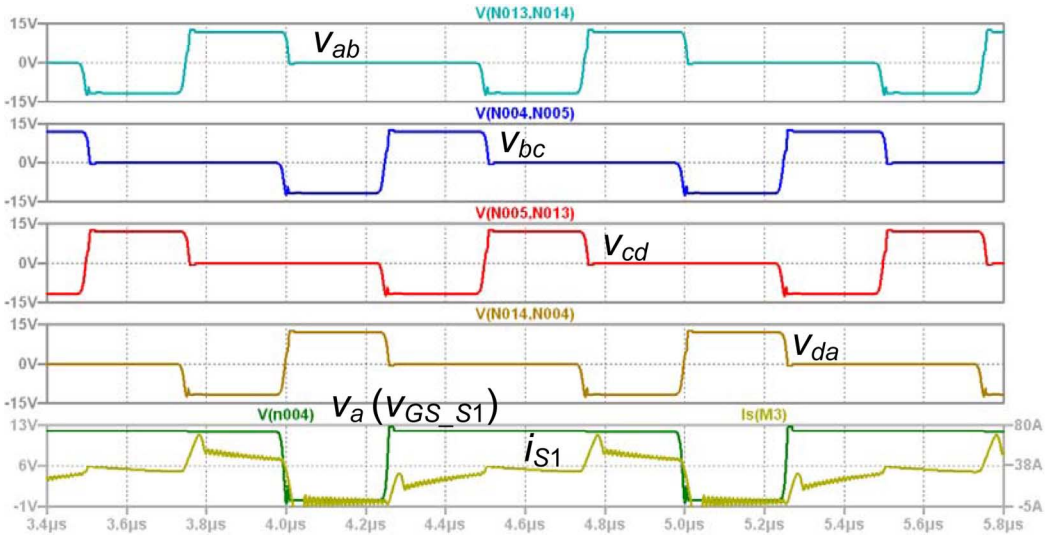

Fig. 10. Simulated waveforms of the self-driven quadrupler rectifier: $V_{\rm in} = 12$ V, $V_o = 1.0$ V, $I_o = 120$ A, $f_s = 1$ MHz, and $n = 2$.

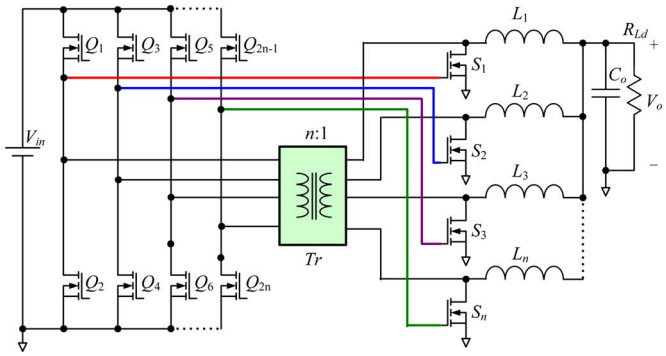

Fig. 11. *N*-phase nonisolated ZVS self-driven FB converters with multiple-stage rectifier.

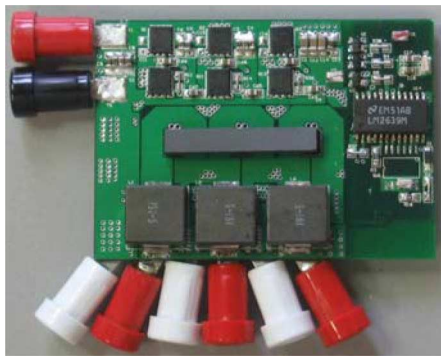

Fig. 12. Photograph of prototype.

component. We cut the standard EI32 core into one-third of the width as the integrated transformer. Its $\mathrm{Ae} = 20\ \mathrm{mm}^2$ and the space volume is $5.5\ \mathrm{mm} \times 32.0\ \mathrm{mm} \times 7.5\ \mathrm{mm} = 1320\ \mathrm{mm}^3$. For the same input voltage, the current doubler transformer can use RM5 core ($\mathrm{Ae} = 20\ \mathrm{mm}^2$) and the space volume is $14.9\ \mathrm{mm} \times 11.4\ \mathrm{mm} \times 8.0\ \mathrm{mm} = 1359\ \mathrm{mm}^3$. So, the size of these two magnetic components is similar. However, the problem of using the integrated transformers is to need custom-designed core. Therefore, the standard planar core cannot be

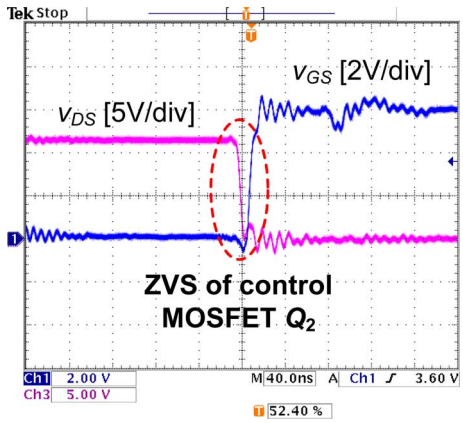

Fig. 13. v_{DS} and v_{GS} of Q_2 @ $I_o = 50$ A.

used directly. This results in additional design efforts and increases the cost of the magnetic component. So, this can be regarded as the drawback of the proposed approach.

As shown in Fig. 1, the voltage of the midpoint of each bridge leg is used to drive the SR MOSFET as the self-driven scheme. So, the input voltage is the gate drive voltage and this limits the application of this circuit to low input voltage applications with low variation.

V. Experimental Results and Discussion

A 1-MHz prototype was built to verify the operation principle of the proposed converter. The specifications are as follows: input voltage $V_{\rm in} = 12$ V; output voltage $V_o = 1.0$ V, and output current up to $I_o = 60$ A. The PCB uses six-layer 2 oz copper. The components used are listed as follows: Q_1: Si7860DP; Q_2: Si7336ADP; output filter inductance: $L_1 = L_2 = L_3 = 190$ nH; control MOSFETs driver: Intersil 6208 (buck driver). One custom-designed EE core (one-third of the EI20 core) is used as the integrate transformer. Fig. 12 illustrates the photograph of the prototype.

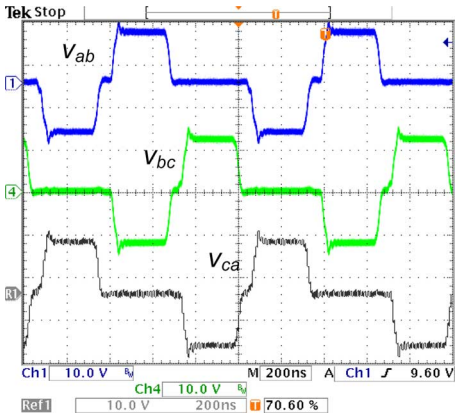

Fig. 14. Primary-side voltages of the transformer at $I_o = 50$ A.

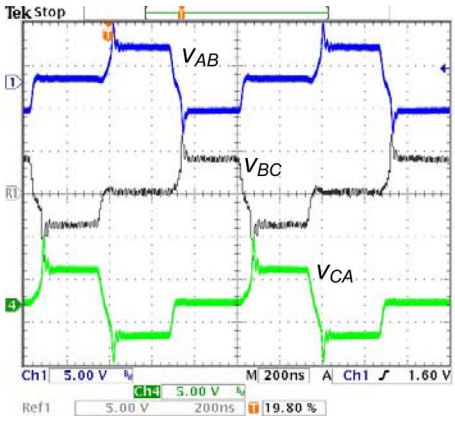

Fig. 15. Secondary-side voltages of transformer at $I_o = 50$ A.

Fig. 13 shows the gate signal v_{GS} and drain-to-source voltage v_{DS} of the control MOSFET Q_2, which indicates that ZVS has been achieved. This also means that the gate drive energy of SR S_1 has been recovered to the input voltage source $V_{\rm in}$ since the gate drive voltage v_a (i.e., drain voltage of Q_2) is fully discharged to zero.

Figs. 14 and 15 illustrate the primary-side voltages, i.e., v_{ab}, v_{bc}, and v_{cb}, and secondary-side voltages, i.e., v_{AB}, v_{BC}, and v_{CB} of the transformers, respectively. All waveforms agree with the theory in Fig. 2. Most notably, the phase voltages are 120 degrees phase-shifted, which means that the magnetic flux cancellation is achieved.

Fig. 16 illustrates the gate signal v_{GS} and drain-to-source voltage v_{DS} of the SR MOSFET S_1. Note that the gate drive voltage is 12 V, which means that the $R_{\rm DS(ON)}$ of SRs is only 1.6 mΩ (IRF 6691) compared to 2.2 mΩ with 5 V gate drive voltage (a reduction of 20%). Moreover, there is no body diode conduction time for the turn-on transition of the SRs since the gate voltage has been applied before v_{DS} reaches zero. Note that the peak voltage of v_{DS} is less than 10 V, which also means a significant reduction of reverse recovery losses. It should also be noted that the future low-voltage rating MOSFETs can be used to reduce the $R_{\rm DS(ON)}$ loss further.

Fig. 17 illustrates the rectified voltages across the output filters that are 120 degrees phase-shifted so that rippler cancellation can be achieved.

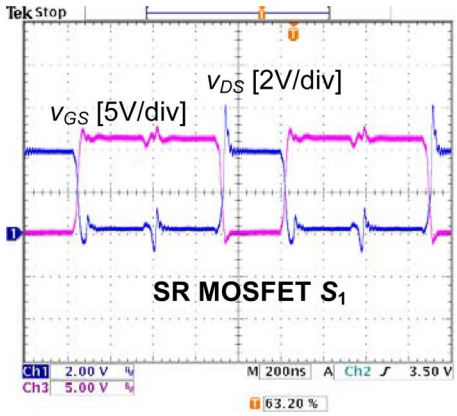

Fig. 16. Gate drive signal and v_{DS} of SR S_1 at $I_o = 50$ A.

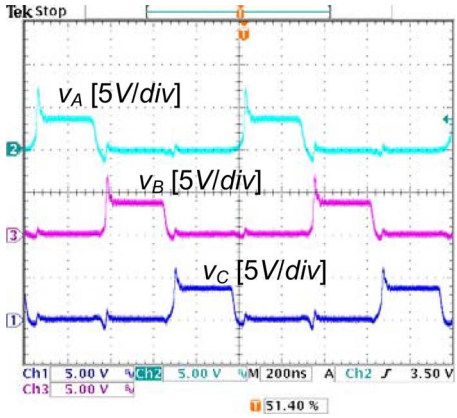

Fig. 17. Rectified voltages at $I_o = 50$ A.

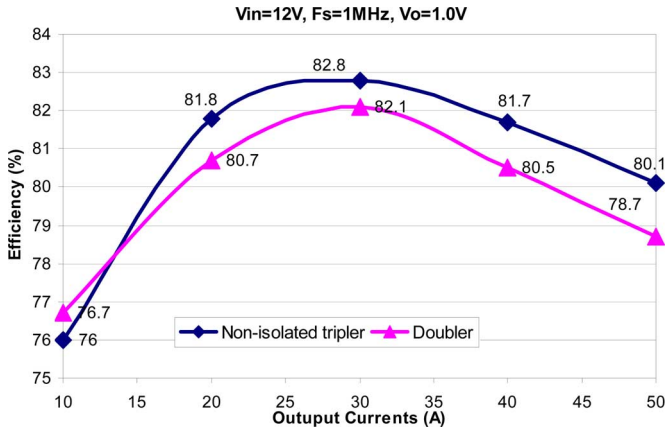

Fig. 18. Efficiency comparison with different load currents. (Top) Nonisolated current tripler. (Bottom) current doubler converter.

Fig. 18 gives the measured efficiency comparison between the proposed topology and the current doubler rectifier converter at 1.0 V output. It is observed that at 40 A, the efficiency is improved from 80.5% to 81.7% (an improvement of 1.2%), and at 50 A, the efficiency is improved from 78.7% to 80.1% (an improvement of 1.4%). As shown in Fig. 18, at 1.0 V/ 50 A, for the current doubler, the total input power is 63.5 W (50 W/ 78.7%); while for the proposed approach, the total input power is 62.4 W (50 W/80.1%). Therefore, the total power loss saving

is 1.1 W (63.5 W−62.4 W). As shown in Fig. 5, at the load currents of 50 A, the SR loss reduction is 0.5 W (2.7 W−2.2 W) and this is 45.5% (0.5 W/1.1 W) of the total loss reduction.

VI. Conclusion

In this paper, a new nonisolated ZVS current tripler topology is proposed. It is suitable to nonisolated low input voltage applications, especially 12 V input VRMs. At the same time, due to high gate drive voltage using the input voltage, the conduction losses of the SRs can be reduced. The self-driven scheme can also achieve the reduced body diode conduction and gate energy recovery of the SRs so that no external drive IC with the dead time control is needed. More importantly, the existing multiphase buck controllers and buck drivers can be directly used in the proposed topology. Other benefits of the isolated current tripler in [29] are also maintained. The nonisolated self-driven current quadrupler and *N*-phase rectifier are also proposed. A 12-V input, 1.0-V/50-A output, 1-MHz prototype was built to verify the advantages of the proposed topology.

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Zhiliang Zhang (S'03–M'09) received the B.Sc. and M.Sc. degrees in electrical and automation engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2002 and 2005, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University at Kingston, Kingston, ON, Canada, in 2009.

Since June 2009, he has been an Associate Professor with Aero-Power Sci-tech Center, College of Automation Engineering, NUAA. His current research interests include high-frequency dc/dc converters for microprocessors, novel soft-switching topologies, power integrated circuit, digital control techniques for power electronics, and current–source gate driver technique. From June 2007 to September 2007, he was a Design Engineering Intern at Burlington Design Center, VT, and Linear Technology Corporation, CA.

Dr. Zhang was a recipient of the Graduate Scholarship through Lite-On Technology Corporation in 2004 and a winner of United Technologies Corporation Rong Hong Endowment in 1999. He also won the award from the Power Source Manufacture's Association (PSMA) to present papers at Applied Power Electronics Conference (APEC 2009), Washington, DC.

Eric Meyer (S'05–M'10) received the B.Sc. and Ph.D. degrees from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2005 and 2009, respectively.

He is currently a Senior Engineer at Advanced Micro Devices (AMD), Toronto, ON, Canada. His current research interests include novel topologies and control methods to improve the dynamic response of voltage regulator module devices. He has one patent pending and has authored over ten technical papers in conferences and IEEE journals.

Dr. Meyer was the recipient of the Natural Sciences and Engineering Research Council (NSERC) Scholarship.

Yan-Fei Liu (M'94–SM'97) received the B.SC. and M.Sc. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1984 and 1987, respectively, and the Ph.D. degree in 1994 from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, where he is currently a Professor in the Department of Electrical and Computer Engineering.

From February 1994 to July 1999, he was a Technical Advisor with the Advanced Power System Division of Astec (formerly Nortel Networks), where he was responsible for high-quality design, new products, and technology development. His current research interests include digital control technologies for dc–dc switching converter and ac–dc converter with power factor correction, current–source MOSFET drive technology, topologies and control for voltage regulator application, electromagnetic interference (EMI) filter design methodologies for switching converters, topologies and controls for high switching frequency, low switching loss converters, modeling and analysis of core loss and copper loss for high-frequency planar magnetics, and large-signal modeling of switching converters.

Dr. Liu was the recipient of the Premiere's Research Excellent Award (PREA) in 2001, Golden Apple Teaching Award in 2000, 2008, and 2009, all in Queen's University, and the 1997 Award in Excellence in Technology in Nortel Networks.

Paresh C. Sen (M'67–SM'74–F'89–LF'04) was born in Chittagong, Bangladesh. He received the B.Sc. degree (with honors) in physics and the M.Sc. (Tech.) degree in applied physics from the University of Calcutta, Calcutta, India, in 1958 and 1961, respectively, and the M.A.Sc. and Ph.D. degrees in electrical engineering in 1965 and 1967, respectively, from the University of Toronto, Toronto, ON, Canada, where he is currently an Emeritus Professor of electrical and computer engineering and be active in research and several IEEE societies.

He was an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS (1975–1982) and the Chairman of the Technical Committees on Power Electronics (1979–1980) and Energy Systems (1980–1982) of the IEEE Industrial Electronics Society. From 1994 to 1999, he was a Natural Science and Engineering Research Council of Canada (NSERC) Scientific Liaison Officer, evaluating University–Industry coordinated projects. He has authored or coauthored more than 160 research papers in the area of power electronics and drives. He is the author of two internationally acclaimed textbooks: *Principles of Electric Machines and Power Electronics* (New York: Wiley, 1989, 2nd ed., 1997) and *Thyristor DC Drives* (New York: Wiley, 1981). His current research interests include power electronics, electric drive systems, switching power supplies, power factor correction circuits, modern control techniques for high-performance drive systems, and applications of fuzzy logic control in power electronics and drive systems.

Dr. Sen was the recipient of the IEEE Canada Outstanding Engineering Educator Award in 2006 for his outstanding contributions over four decades as an author, teacher, supervisor, researcher, and consultant; and the Prize Paper Award from the Industrial Drives Committee for technical excellence at the IEEE Industry Applications Society (IAS) Annual Meeting in 1986.