A Novel Analog Implementation of Capacitor Charge Balance Controller with a Practical Extreme Voltage Detector

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Abstract -- In this paper, a practical analog implementation of capacitor charge balance controller is presented, which is capable of achieving the optimal response for dc-dc Buck converters without relying on the knowledge of the nominal passive component (output inductor and capacitor) value. This ready-for-integration analog controller applies the output voltage curve analysis for deriving the formulas to optimize the response under the load transients. A simple extension is also offered for adaptive voltage positioning (AVP) application to power the modern processors. Furthermore, an operational amplifier (OPAMP) based peak/valley voltage detector is presented in place of using a fast or asynchronous ADC, as a result, lower cost, lower operating power consumption and fully analog implementation can be expected. Finally, simulation and experimental results are provided to validate the proposed schemes.

***Index Terms*—Capacitor Charge Balance Control, Voltage Regulators (VRs), Robust Control, Optimal Control, Analog VR Controller, Fast Dynamic Performance**

I. INTRODUCTION

The voltage regulator (VR) requirements for modern processor power supplies become more and more stringent, that is, low output overshoot/undershoot and short settling time under increasingly large and ultrafast CPU load transient. Although couples of analog controllers and digital control algorithms have been introduced in some previous literatures [1]-[11] to achieve better response performance than conventional schemes such as voltage and current mode controllers, unfortunately, all of them cannot address all the limitations. Also, there are several drawbacks in digital control that hinder its use in VR applications, so most of the existing laptop/notebook computer VR controllers are analog ICs. The digital controller may suffer from one or more limitations:

1. High power consumption of DSP or FPGA type of digital controllers is the main bottleneck against their wide use for VRs, especially, during standby mode operation of VR. Although the ASIC type of controller is an existing digital controller candidate for VR, the power consumption is still much higher than its analog counterparts. Therefore, the existing digital controllers are only used in higher power VRs for servers.
2. The propagation delay, calculation delay, sampling delay and aliasing effect in the digital compensation loop make the (linear mode) digital controller impossibly faster than analog controller. Therefore, for VR applications, the digital (linear mode) controller is not that attractive.
3 Digital controller has several applicability issues, such as the limit-cycle oscillation caused by analog-digital converter (ADC) and DPWM resolution mismatching, as well as the high ADC power consumption and relatively complex structure of the DPWM generator.
4 Hardware multipliers are required for implementing the control law and specific software and interface are needed for programming the arithmetic core, resulting in high cost of the digital controller.

For the analog controllers based on sliding mode control (SMC) [1], [2] or capacitor charge balance control (CBC) principles [3], either complex calculation blocks or design parameters matching adjustment [4] is required to realize the proposed implementations. On the other hand, latest existing digital schemes [6]-[11], though removing most of the algorithm barriers, for example, the requirement of accurate current sensing for estimation, the need of real time complex calculations (square root/division) and the dependence on the design parameters (L_o, C_o and ESR) [10], as previously discussed, they are still not the best solutions for efficient industrial IC design and fabrication.

To address the aforementioned drawbacks, an analog CBC controller is presented, combining the advantages of fast dynamic performance, enhanced robustness, design simplicity, easy fabrication of analog IC and low power consumption. In lieu of ADC and capacitor current sensor, an analog extreme voltage detector is used to detect the capacitor current zero crossing moment. And an analog circuitry based on OPAMP and comparator (OP-COM) circuitry is proposed to carry out the digital function for achieving charge balance concept [11]. When a low voltage Buck converter for VR is well-designed with negligibly low ESR by using ceramic output capacitors, the proposed implementation is parameter-independent, robust and simply extendable for AVP applications [11].

This paper is organized as follows. In Section II, the principles of the proposed analog controller for load transients are introduced and the critical mathematical expressions of the proposed scheme are derived. In Section

III, the operations of the proposed control under positive load transients and adaptive voltage positioning are outlined. Following the hardware implementation and design guidelines in Section IV, finally, the simulation and experimental results are demonstrated in Section V to validate the proposed analog CBC controller. The conclusion is made in Section VI.

II. Charge Balance Control Based on Output Voltage Sensing Information

Charge balance principle is a practical solution for achieving minimal settling time [3]. For all the CBC based controllers [3]-[11], the time instants t_1 (capacitor current undergoing zero-crossing) and t_2 (PWM changing ON/OFF state) are very important to arrange the desired ON/OFF control actions (in Figure 1), accordingly. In this paper, a practical extreme voltage detector is presented to find t_1. And in place of calculating interval T_2 in [3]-[6], the time information t_2 is mapped to the switching point voltage (SPV) V_{SW}, which provides a output voltage sensing based parameter-independent formula set under load transient cases. Also an extension can be made for AVP application based on this SPV information. And an OP-COM circuitry is used in place of digital functions to achieve the time detection of t_2. The operations of the proposed controller to minimize the output deviations are discussed in this section.

Following the load current step transient, the proposed analog CBC (ACBC) controller will firstly sample and hold (S/H) the maximum/minimum output voltage at t_1 and convert this information into SPV V_{SW} to detect t_2. The main waveforms of the control scheme under negative load step transient (in CCM mode with synchronous rectifier, SR) are shown below with reference to Figure 1:

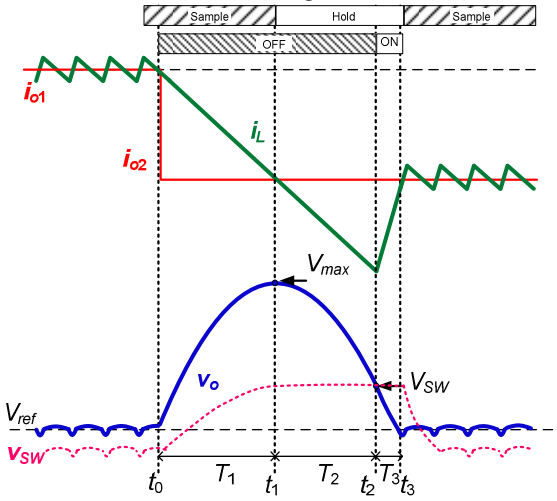

Figure 1 Typical waveforms of VR using the proposed CBC controller under negative load step transient

A. Charge Balance Principles for a Buck Converter Undergoing a Negative Load Step Change

The analog CBC (ACBC) controller is designed for applications in which the load current slew rate is significantly larger than the inductor current slew rate. Therefore, in this analysis, it is assumed that the load current steps instantaneously from I_{o1} to I_{o2} and that the controller is able to react to the step with negligible delay. It is also assumed that the load current remains constant for the duration of the transient period. For the computer CPU VRs, sufficiently large output capacitance is required to suppress the output voltage deviation. And also for the low voltage rating, often, the selected ceramic output capacitors could provide very low *ESR* (<1mΩ). So in the following discussion, an ideal dc-dc Buck converter model is used. And the starting time t_0 is set to be 0 in the analysis for discussion simplification in Figure 1.

Step 1: Time Interval T_1 ($t_0 \le t < t_1$) for a Negative Load Step

For negative current step change, during the time period 0-t_1 capacitor current i_c can be approximated as a linear function in (1), where m_2 is the falling slew rate of the inductor current, v_o is the output voltage and L_o is the output inductance.

$$i_C(t)\big|_{0\sim t_1} = -m_2(t-t_1) = -\frac{V_o}{L_o}(t-t_1) = C_o\frac{dv_o}{dt} \tag{1}$$

As an alternative approach for solving differential equations, the capacitor/output voltage v_o can be approximated with a parabola based on its current i_c in the equation (2).

$$v_o(t) = V_{ref} + \frac{1}{C_o}\int_0^t i_c dt = V_{ref} + \frac{m_2}{2C_o}t_1^2 - \frac{m_2}{2C_o}(t-t_1)^2 \tag{2}$$

Step 2: Time Interval T_2 ($t_1 \le t < t_2$) for Negative Load Step

When the inductor current i_L reaches the new steady-state load current I_{o2} at t_1, the output voltage v_o will reach its peak value, $V_{\max}$. Similarly, the capacitor current i_c can be expressed in (3), and the instantaneous output voltage v_o will be able to be computed in (4) based on the voltage $V_{\max}$ at t_1.

$$i_C(t)\big|_{t_1\sim t_2} = -m_2(t-t_1) = -\frac{V_o}{L_o}(t-t_1) \tag{3}$$

$$v_o(t) = V_{\max} + \frac{1}{C_o}\int_{t_1}^t i_c dt = V_{\max} - \frac{m_2}{2C_o}(t-t_1)^2 \tag{4}$$

Step 3: Balancing Capacitor Charge Regions $A_{discharge}$ and A_{charge}, T_3 ($t_2 \le t \le t_3$)

According to (4), the output voltage at t_2, called switching point voltage (SPV, V_{SW}) in this paper, is expressed in (5).

$$V_{SW} = V_{\max} - \frac{m_2}{2C_o}T_2^2 \tag{5}$$

Referring to the rising slope of the inductor current m_1 in this interval, the capacitor current can be written as (6) and the time intervals T_2 and T_3 will follow the relationship expressed in (7).

$$i_C(t)\big|_{t_2\sim t_3} = m_1(t-t_3) = \frac{V_{in}-V_o}{L_o}(t-t_3) \tag{6}$$

$$\frac{T_2}{T_3} = \frac{m_1}{m_2} = \frac{V_{in}-V_o}{V_o} \tag{7}$$

The instantaneous output voltage v_o can be calculated in (8) based on the capacitor current i_c information in (6).

$$v_o(t) = V_{SW} + \frac{1}{C_o}\int_{t_2}^t i_c(t)dt \tag{8}$$

So the SPV voltage V_{SW} can be calculated using (9), where the symbol T_s represents the switching period and the V_{ref} is the output voltage reference.

$$V_{SW} = \frac{1}{2C_o} m_1 \left[T_3^2 - \left(\frac{1}{2} DT_s \right)^2 \right] + V_{ref} \quad (9)$$

Without sacrificing the accuracy of the algorithm a lot, especially when the switched-mode power supply operates at a high frequency (>100kHz) and narrow duty ratio (12 V-1.5 V), the item $(1/2DT_s)^2$ can be neglected in the equation (9). Therefore, the voltage V_{SW} can be fitted as (10) combining the other two known data points (t_1, V_{max}) and (t_3, V_{ref},) in (5) and (9).

$$V_{SW} = \frac{m_2 (V_{\max} - V_{SW})}{m_1} + V_{ref} = DV_{\max} + (1-D)V_{ref} \quad (10)$$

The peak voltage information V_{max} in the equation (10) can be sampled and held at time instant t_1, so the t_1 detection is important in this analog implementation.

Using equation (10), it is clear that OPAMP and comparator can be used to determine the time instant t_2. The OPAMP serves as an amplifier with constant gain for $V_{\max}$ and V_{ref} and an adder to sum up the information at the non-inverting port, shown in Figure 2. As shown in Figure 1, the voltage v_{sw} is lower than the output voltage during steady-state and before t_2 during negative load step transient. So the comparator with hysteresis configuration will capture the crossover point of v_o and v_{sw} at t_2 and avoid comparison ringing.

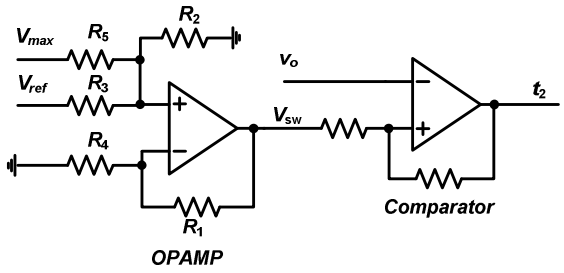

Figure 2 Analog Implementation for calculating V_{sw} and t_2 determination.

The guidelines of circuit design and parameter calculation will be presented in the Section IV, *B*.

B. An Analog Extreme Voltage Detector for Locating the Voltage Peak V_{max} at t_1

In order to implement the equation (10), the peak voltage V_{max} is needed. If the *ESR* is ignored, the output voltage peak appears at time instant t_1. Because of the current sensor mismatching [4], cost and accuracy issue [7], a practical extreme voltage detector is used in this paper to detect t_1 and locate the voltage information $V_{\max}$ [11]. Also, compared to a fast ADC, the proposed analog voltage detector can significantly reduce the power consumption. In Figure 3, as an instance, during negative current step, the output voltage overshoot is delayed with a period of time t_{delay}, and represented as v_{o_delay}. This delay can be equalized with a first-order OPAMP circuit based on *Padė* Approximation (11) [11]. Then, the voltages v_o and v_{o_delay} will be fed to the input ports of the output comparator. And at a certain voltage error v_{err}, the comparator output signal begins rising to this upper limit, such that time point t_1 can be detected for control logic. And the inserted delay time t_{delay} can be compensated to a certain acceptable degree, with the help of the lead time (provided by *ESR*) and comparator hysteresis configuration (which can adjust the v_{err} band in Figure 3) [11].

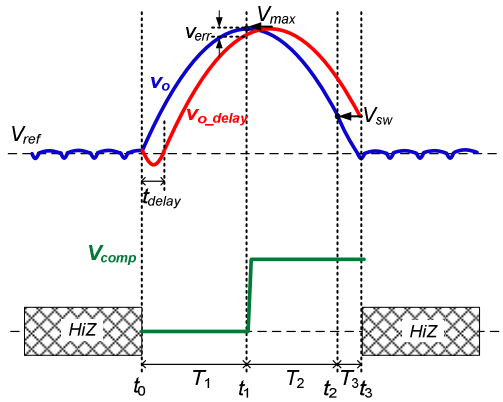

Figure 3 Illustration of the analog extreme voltage detector under negative load transient

In Figure 4, an adjustable delay circuit is synthesized based on the *Padė* approximation (11).

$$\frac{v_{c\_delay}}{v_c} = e^{-\tau s} \approx \frac{1-\tau s/2}{1+\tau s/2} = \frac{1-R_T C_T s}{1+R_T C_T s} \quad (11)$$

In this circuit, the delay time constant τ can be adjusted by the product of R_T and C_T (i.e. τ=2R_T·C_T). And the inverting section is added to the output end to implement two-fold functions: 1) inverting the delayed signal and 2) tuning the output voltage offset level. The output comparator is connected with a hysteresis configuration and the one with latched output function is more preferred for blanking steady-state comparison "noise", such as TL3016 (TI Company) [12]. Also, in the experiments, the aforementioned delay can be also compensated by using a trim resistor as the feedback resistor R_{k2}' to tune the gain of the delayed voltage v_{o_delay} such that the crossover of the two voltage waveforms (v_o and v_{o_delay}, Figure 3) will appear right at t_1.

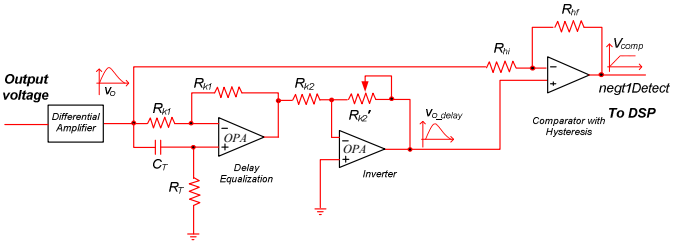

Figure 4 Hardware implementation of the detector based on the adjustable delay circuit

C. Regarding Assumptions Involving m_1 and m_2

It is noted that m_1 and m_2 will not remain constant in actuality during a load transient due to the varying output voltage. This simplification was made in order to allow for a practical implementation of a charge balance controller. For this reason, it is claimed that the controller can only yield a "near-optimal" transient response. However, the

simplification does not degrade the performance significantly due to the following reasons:

i) for a low duty ratio Buck (e.g. 12V-1.5V), the undershoot (due to a positive load current step) will be much smaller than the overshoot (due to a negative load current step). Thus, for a properly designed Buck, the output voltage deviation during a positive load transient would be very small.

ii) for a negative load transient, the output voltage can vary significantly (typically 10% of the steady-state voltage). However, for example, a single phase 12V-1.5V VR with 1μH output inductance and 200μF output capacitance, under 10A step-down load transient the overshoot will be about 0.2V, and the exact SPV V_{SW} is 1.528V, however, using constant duty ratio D, the calculated V_{SW} is 1.525V, causing a very small error of 3mV. Therefore, the controller's gain of OP-COM can be determined by the steady-state D and (1-D) in (10).

III. Operations of the Proposed Controller under Positive Step Load Transients and Adaptive Voltage Positioning Extension

A. Charge Balance Equation for a Buck Converter Undergoing a Positive Load Step Change

A similar analysis as performed in Section II. *A* can be carried out for a positive load current step change.

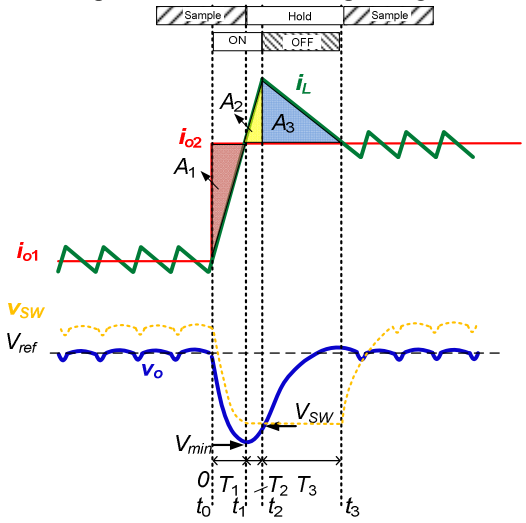

Figure 5 Capacitor charge integral areas during a positive load step change

During the time intervals t_0-t_2 and t_2-t_3, the capacitor current can be expressed as a linear function in (12) and (13), respectively.

$$i_C(t)\big|_{t_0-t_2} = m_1(t-t_1) \tag{12}$$

$$i_C(t)\big|_{t_2-t_3} = -m_2(t-t_3) \tag{13}$$

So the voltage V_{SW} can be calculated using (14), where the symbol T_s represents the sampling period and the V_{ref} is the output voltage reference, while the equation (15) provides the formula for voltage V_{min}.

$$V_{SW} = V_{ref} - \frac{1}{2C_o} m_2 \left[T_3^2 - \left(\frac{1}{2} D' T_s \right)^2 \right] \tag{14}$$

$$V_{\min} = V_{SW} - \frac{1}{2C_o} m_1 T_2^2 \tag{15}$$

Similarly, the item $(1/2D'T_s)2$ can be ignored in the equation (14). Therefore, the voltage V_{SW} can be derived as (16), where $m_1/m_2 = (V_{in}\text{-}V_o)/V_o = T_3/T_2$. According to the voltage V_{SW}, we can change the main switch from on-state to off-state. By combining (14) and (15), the SPV can be expressed in (16), in which neither inductor nor capacitor value is explicit.

$$V_{SW} = V_{ref} + \frac{m_2 (V_{\max} - V_{SW})}{m_1} = DV_{ref} + (1-D)V_{\min} \tag{16}$$

B. Adaptive Voltage Positioning/Load Line Regulation Extension

Load-line regulation (a.k.a. adaptive voltage positioning) has increasingly become a requirement in many Buck converter applications, for example, Intel's CPU VRs. Load-line regulation essentially involves outputting lower voltages during higher load current conditions. This assists in improving the overall transient performance of the converter along while decreasing power consumption of the load device.

Due to several factors (e.g. complexity, mode transitioning), it is difficult to achieve load-line regulation through analog charge balance control. However, the proposed ACBC controller can be applied to AVP operation with only simple modifications, i.e. adding inductor current sensor and one more connection to the inverting input port of the OPAMP.

It is observed in Figure 6, for AVP application, the difference of operation is in the interval t_1-t_3. At time instant t_3, instead of recovering the output voltage to V_{ref}, the AVP controller maintains the new steady-state output voltage V_{ref}-$\Delta I \cdot R_{droop}$, referring to the load line.

Similarly, the switching point voltage V_{sw} can be calculated in (17) by referring the parabolic curve during t_1-t_2.

$$V_{SW} = V_{\max} - \frac{m_2}{2C_o} T_2^2 \tag{17}$$

Considering the new adaptive voltage positioning level, the switching point voltage V_{SW} can also be expressed during t_2-t_3. And, as previously discussed, the term $(1/2DT_s)^2$ can be ignored in (18) when the VR is operated at high switching frequency and narrow output duty ratio.

$$V_{SW} = \frac{1}{2C_o} m_1 \left[T_3^2 - \left(\frac{1}{2} D T_s \right)^2 \right] + \left(V_{ref} - R_{droop} \cdot \Delta I \right) \tag{18}$$

By substituting (17) into (18), the switching point voltage V_{SW} can be calculated in (19) for AVP application.

$$V_{SW} = DV_{\max} + (1-D)\left(V_{ref} - R_{droop} \cdot \Delta I \right) \tag{19}$$

From the equation (19), it is noted that, compared with (10), we can simply replace the voltage V_{ref} with the new load line voltage at V_{ref}-$\Delta I \cdot R_{droop}$. In the same way, the switching point voltage under positive load step transient is able to be expressed in (20).

$$V_{SW} = D\left(V_{ref} - R_{droop} \cdot \Delta I \right) + (1-D)V_{\min} \tag{20}$$

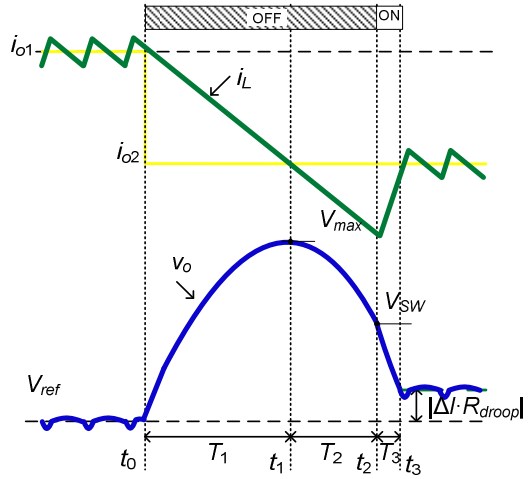

Figure 6 Inductor current and capacitor voltage waveforms for AVP applications under negative current step change case (R_{droop}: droop resistance)

And the hardware modification for AVP operation is also minor, shown in Figure 7, the inductor current sensor is required to feed the load line information to the inverting port of the OPAMP to implement the equations (19) and (20). And the detailed implementation is discussed in Section IV. *B*.

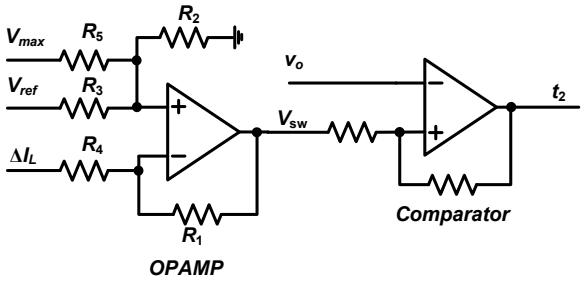

Figure 7 Analog Implementation modification for calculating V_{sw} and t_2 determination in AVP applications.

IV. Implementation of the Proposed Analog Capacitor Charge Balance Controller

The implementation and design of the proposed analog charge balance controller will be discussed in this section. The three main components of the proposed analog charge balance controller are: a) an extreme voltage detector to determine t_1 (when the inductor current reaches the new load current level); b) an analog circuitry consisting of OPAMP and comparator to determine the switching instant t_2; and c) associated logic to control the components a) and b) and the converter's PWM signal. Figure 8 shows the block diagram of the charge balance control method. In addition, a particular Type III compensator is designed for steady-state or near steady-state regulation purposes as well as the smooth transition between linear mode and CBC controllers.

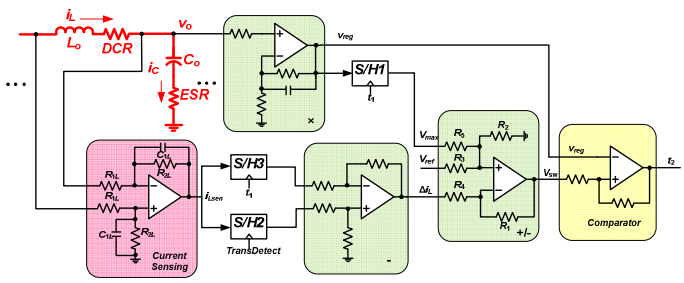

Figure 8 Simplified schematic of the proposed analog CBC controller implementation for computing V_{sw} and detecting t_2

In Figure 8, the inductor current measurement information is merely used to implement AVP or load-line regulation, as discussed in Section III. *B*.

A. *Extreme Voltage Detector Design (For t_1 Detection)*

As discussed in Section II. B, the adjustable delay t_{delay} can be tuned by selecting different value of C_T and R_T. The proper delay should be selected to compromise two factors: 1) good time detection accuracy; and 2) sufficient voltage error for generating comparator output (rising/falling edge). Using the equation (11), the values of C_T and R_T can be calculated.

The experimental result shown in Figure 9 demonstrates the aforementioned delay based extreme voltage detector to detect time t_1. The pink waveform is the input sinusoidal signal at 100kHz with $1.5V_{pp}$ and the blue waveform is the output signal of extreme voltage detector. The delay time t_{delay} is set to be 330ns by selecting C_T as 330pF and R_T as 500Ω.

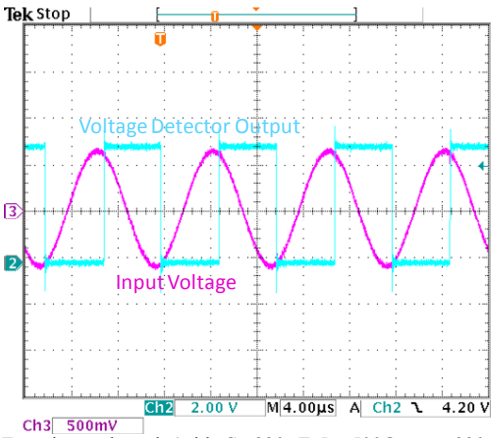

Figure 9 Experimental result (with C_T=330*pF*, R_T=500Ω, t_{delay}=330ns)

B. *Analog Circuitry Design for t_2 Detection*

The design of the analog circuitry for t_2 detection is presented in this section and the hardware schematic is shown in Figure 7, for AVP application. And for non-AVP operation, the inverting port of the OPAMP will be tied to GND in Figure 2.

In this analog implementation, the critical time point t_2 can be determined by comparing instant output voltage (v_o) with switching point voltage (V_{SW}). And the analog extreme voltage detector is used to decide time t_1, and the controller logic will feed the proper logic signal to S/H1 for collecting V_{max}, shown in Figure 8. For computing the load step value

Δi_L, two S/Hs (S/H2 and S/H3) are used and the S/H timing is controlled by the controller logic according to t_0 (from transient detector) and t_1 (from extreme voltage detector output) in Figure 7. Then Δi_L is obtained by subtracting $i_L(t_1)$ from $i_L(t_0)$. To implement the equations (19) and (20), an analog OPAMP adder/subtractor is employed following the formula in (21). And the design parameters can be selected using (22)-(24), referring to (19) and (21).

$$V_{SW}=\left(1+\frac{R_1}{R_4}\right)\left(\frac{R_2}{R_5+R_2}V_{\max}+\frac{R_2}{R_3+R_2}V_{ref}\right)-\frac{R_1}{R_4}\cdot\Delta i_L \quad (21)$$

$$D=\left(1+\frac{R_1}{R_4}\right)\frac{R_2}{R_5+R_2} \quad (22)$$

$$1-D=\left(1+\frac{R_1}{R_4}\right)\frac{R_2}{R_3+R_2} \quad (23)$$

$$(1-D)\cdot R_{droop}=\frac{R_1}{R_4} \quad (24)$$

C. Associated Charge Balance Controller Logic

The controller logic block is responsible for: a) registering a load current transient, b) switching control from the linear controller to the charge balance controller during the transient interval and providing PWM control signals, c) providing control signals to the extreme voltage detector, linear mode controller, and S/Hs during the transient interval, d) registering time instants (at t_1 and t_2), and e) reactivating the linear controller at the end of the transient interval (at t_3).

The controller logic using only logic gates is shown in Figure 10, which is very convenient to implement using CPLD or FPGA at the cost of only 20 logic elements.

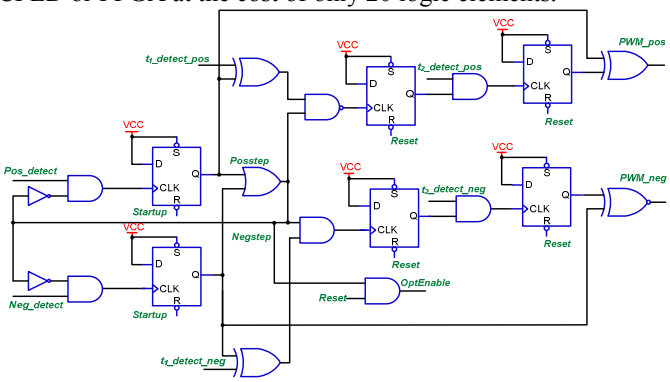

Figure 10 Simplified schematic of the proposed analog CBC controller logic circuit

V. Simulation and Experimental Verifications

A. Simulation Results

In order to verify the functionality of the proposed analog controller, a Buck converter undergoing different transient conditions is simulated. And the simulation results are shown in Figure 11 and Figure 12 for comparison between the proposed analog CBC controller and the conventional voltage mode controller. The nominal design parameters are listed as follows: V_{in}=12 V, V_o=V_{ref}=1.5 V, f_s=450 *k*Hz, L=1 μH, R_L=1 *m*Ω, C=200 μF, ESR=0.1 *m*Ω, ESL=100 *p*H. The Type III compensator is well-designed with 75 kHz bandwidth and 60° phase margin in the following simulations.

Under 12A positive load step transient, compared to voltage mode controller, the voltage overshoot is reduced by 66.7% and the settling time is shortened by 93.3%. Although, under the negative 12A step load transients, the voltage undershoot is only reduced by 19.0% due to the narrow operating duty ratio, the settling time is still significantly reduced by about 76.7%.

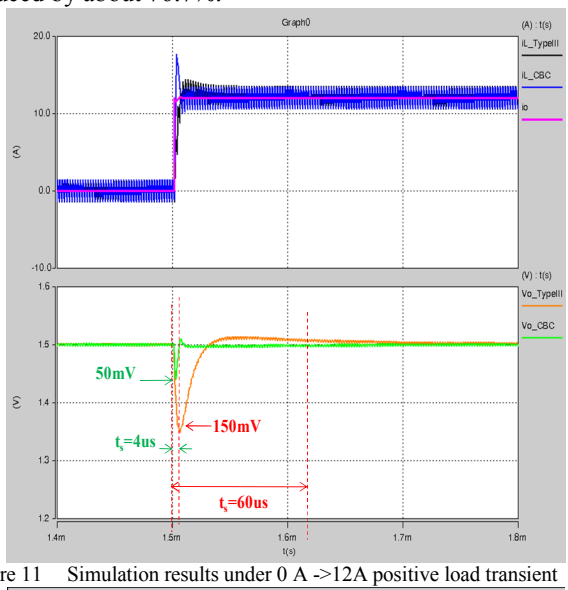

Figure 11 Simulation results under 0 A ->12A positive load transient

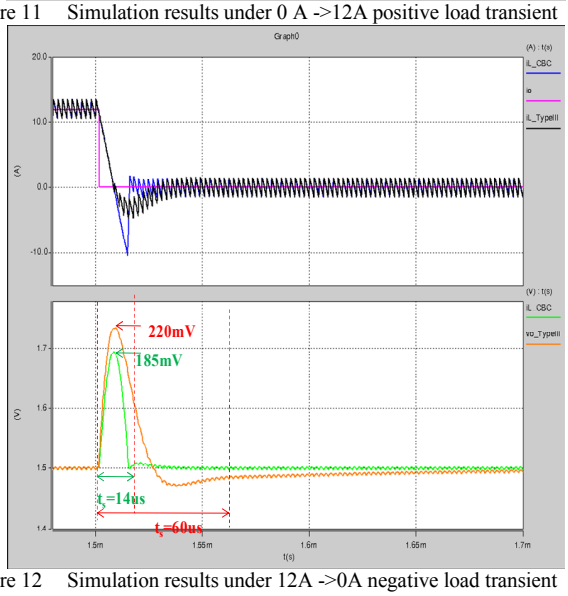

Figure 12 Simulation results under 12A ->0A negative load transient

B. Design Prototype and Experimental Results

A 12 V-1.5 V prototype is designed using the same nominal parameters in the simulation and a FPGA (EP2C70F896C6, Cyclone II, Altera) is employed to implement the proposed CBC controller logic (in Figure 9). The analog linear mode controller is implemented by using ISL6559 controller (Intersil Co.) [13]. Experimental results are shown in Figure 13-Figure 16, under the load current step changes between no load (0A) and full load (12A). The

proposed analog CBC controller demonstrates quite similar enhanced performance as its digital counterpart [11] but facilitating the integration and fabrication of the industrial controller IC products with reduced power consumption.

Figure 13 and Figure 14 show comparative results for a VR undergoing a 0A-> 12A positive load step transient using proposed ACBC controller and conventional voltage mode controller. The voltage detector signal is shown for time detection of t_1. In order to illustrate the operation of the ACBC controller, the charge balance control intervals have been shown in the figures.

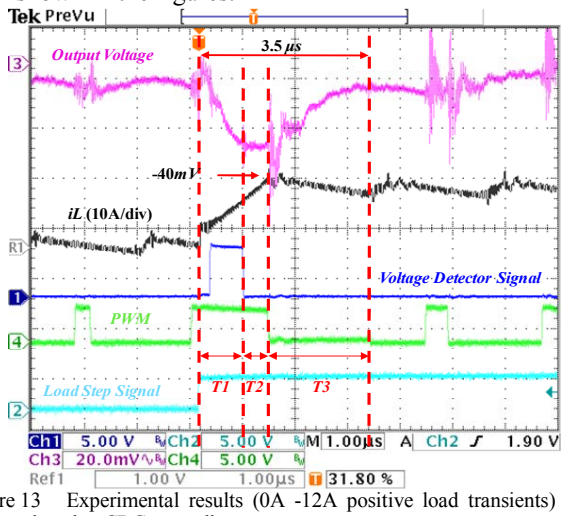

Figure 13 Experimental results (0A -12A positive load transients) using proposed analog CBC controller

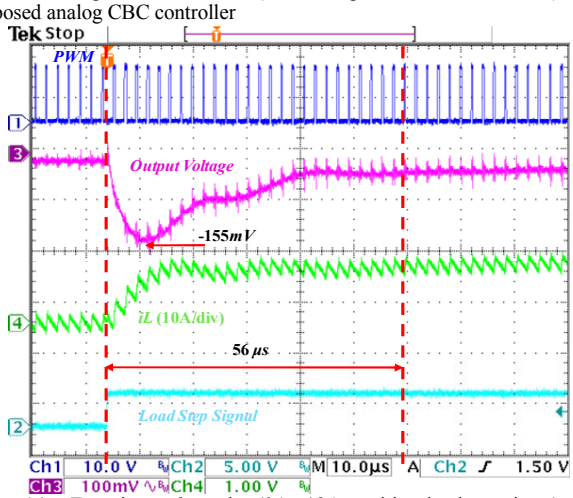

Figure 14 Experimental results (0A -12A positive load transients) using Type III compensator

It is demonstrated, under a positive 12A load current step transient, the settling time is reduced from 56us (using voltage mode controller) to 3.5us (using ACBC). In other words, the settling time of the VR with ACBC is shorten by 93%, compared to that of the voltage mode controlled VR. And the experimental result is in close correspondence of the simulation result (4us).

Also, it is shown that voltage undershoot is reduced from -155mV (using the linear controller) to -40mV (using ACBC). The undershoot of the VR with ACBC controller is reduced by 74% compared to that of the voltage mode controller VR. And the -40mV undershoot is accordance with the simulated result (-50mV).

Figure 15 and Figure 16 show a voltage mode controlled VR and the ACBC controlled VR undergoing a 12A->0A load step change, separately.

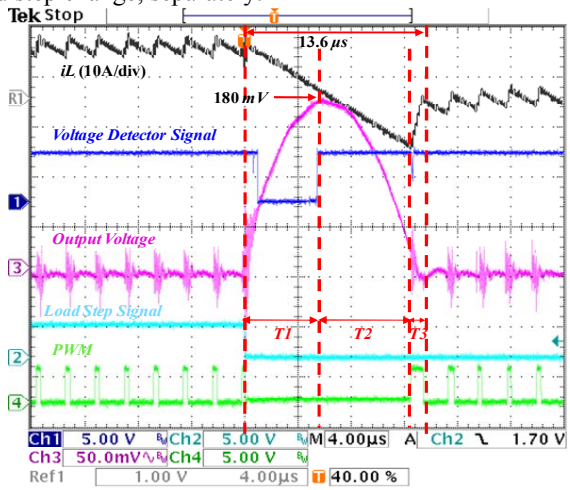

Figure 15 Experimental results (12A-0A negative load transients) using proposed analog CBC controller

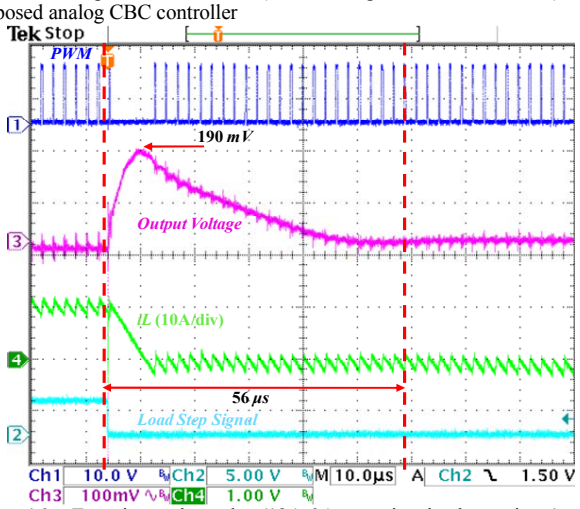

Figure 16 Experimental results (12A-0A negative load transients) using Type III compensator

It is demonstrated, under a 12A load negative current step transient, the settling time is reduced from 56us (using voltage mode controller) to 13.6us (using ACBC). In other words, the settling time of the VR with ACBC is shorten by 75%, compared to that of the voltage mode controlled VR. And the experimental result is in close correspondence of the simulation result (14us).

Also, it is shown that voltage overshoot is only reduced from 190mV (using the linear controller) to 180mV (using ACBC) based of the narrow operating output ratio at 12V-1.5V. But the 180mV overshoot is accordance with the simulated result (185mV).

The adaptive voltage positioning technique is applied to the ACBC controller with simple modification on top of the non-AVP ACBC scheme. And in the experimental results

shown in Figure 17 and Figure 18, the droop resistance is selected to be 5mΩ.

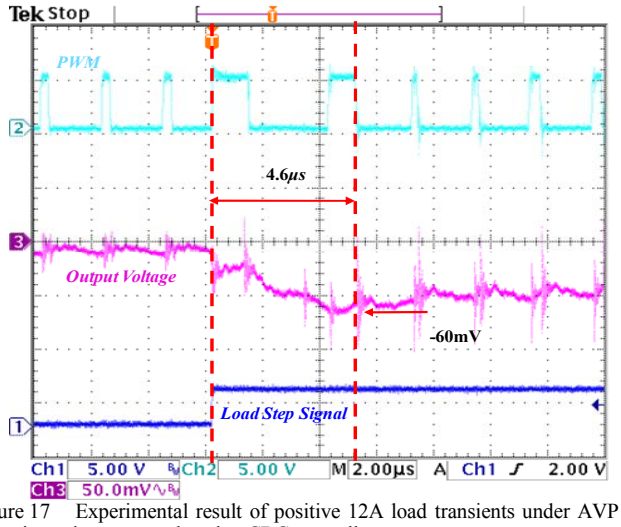

Figure 17 Experimental result of positive 12A load transients under AVP operation using proposed analog CBC controller

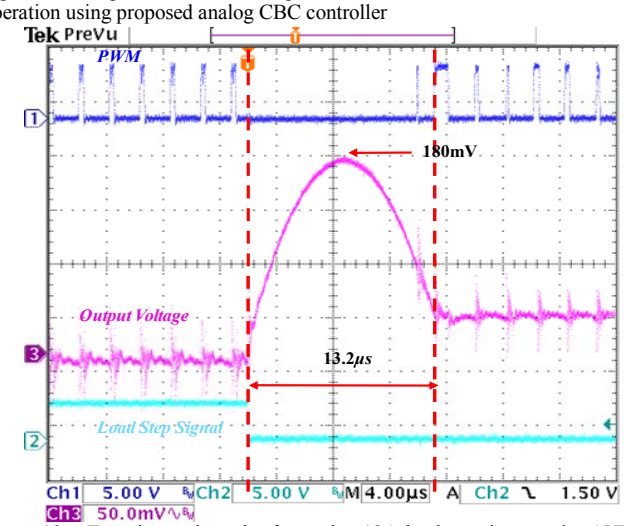

Figure 18 Experimental result of negative 12A load transients under AVP operation using proposed analog CBC controller

It is demonstrated that, for a 12A positive load step transient, the undershoot is 0mV at -60mV AVP regulation in Figure 17. And the settling time is 4.6us. The experimental result in Figure 18 demonstrates that the overshoot is 120mV above the AVP regulation level of 60mV (180mV in total) with13.2us settling time under a 12A negative step load transient.

VI. CONCLUSIONS

In this paper, a fully analog CBC controller based on parameter-independent algorithm [11] is presented. This proposed analog implementation facilitates analog controller IC fabrication to the next-generation VRs. Also, the power consumption of proposed controller can be significantly reduced compared to a DSP or FPGA type of digital controller. It is demonstrated through simulations and experimental results, that the proposed ACBC controller can be implemented for low-*ESR* designed Buck converter to optimize the transient response performance and enhance the robustness against the tolerance and variation of the passive components (output inductance L_o and output capacitance C_o). Also a capability is shown for AVP applications using this scheme without increasing design complexity. Compared with a well-designed analog voltage mode Type III controller, under a 12A positive current step, the settling time and undershoot are improved by 93 % and 74 %, respectively. For a 12A negative current step, although the overshoot is not improved because of the narrow duty ratio, the settling time is still shortened by 75 % using the proposed controller.

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