High-accuracy Digital Controlled Isolated Power Supply with Low Data Transfer Requirements

Zhiyuan Hu Yan-Fei Liu
Department of Electrical and Computer Engineering
Queen's University
Kingston, Canada
zhiyuan.hu@queensu.ca yanfei.liu@queensu.ca

Tet Hin Yeap
School of Information Technology and Engineering
University of Ottawa
Ottawa, Canada
tet@site.uottawa.ca

***Abstract*— In this paper, a digital controlled isolated power supply system is developed combing an 8B/10B-based protocol and a Multi-Resolution Feedback (MRF) method to achieve optimized communication. It features 4 times higher output accuracy and averagely consumes less than a half bandwidth than existing systems, and transmits all data using a single pulse-transformer, which saves substantial cost of high-speed isolators. Experimental results demonstrate the feasibility of the proposed system.**

I. INTRODUCTION

The data communication in digital controlled isolated power supplies must be high-speed in order to achieve fast response and high output accuracy. The required data transfer rate is determined by three factors: the sampling frequency, the number of ADC bits, and the protocol efficiency. In general, high sampling frequency is preferred to improve the dynamic response; high resolution ADC is also preferred to improve the output accuracy; and existing protocols used in isolated digital power supplies are inefficient [1-3]. Therefore, the data transfer rate across the isolation boundary has to be inevitably high to achieve satisfactory performance, which leads to high system cost. Otherwise, compromises must be made in order to use slower and cheaper logic isolators. The undesired power consumption and the design difficulties due to the high-speed circuitry also rise as the data transfer rate increases.

In [1], although a very fast 150 MHz isolator [4] is used, the duty-cycle resolution is only $400\text{KHz}/150\text{MHz} \times 100\% = 0.267\%$. As a result, the ADC resolution is limited to 6-bit, otherwise limit cycle oscillation will occur [5].

In [2] , the protocol efficiency is only 25%: a 12-bit frame contains only 4-bit data, thus only the 4 LSBs of an 8-bit ADC can be transmitted. Higher resolution ADCs cannot be used, otherwise 4 LSB are too few to cover the output regulation range.

In [3], 8 MSB of a 10-bit ADC are transmitted. The UART (Universal Asynchronous Receiver/ Transmitter) standard used in this application was not designed for real-time communications, or increased software and processing effort are needed to overcome problems such as clock drift, send jitter, and so on [6].

Furthermore, the cost of the logic isolators will quickly add up when a system contains multiple isolated power supply modules, such as Plasma TVs, LCD TVs, medical equipment, bench top power supplies, and so on. Depending on the protocol used [7, 8], each module may use several logic isolators for data line, clock line, and frame synchronization line, shown in

Figure 1. The logic isolators are hundreds of times more expensive than traditional analog isolators, and thus the high cost may prevent isolated digital power supplies from market success.

In this paper, an isolated digital power supply with systematic optimization in data communication will be presented. The system uses only one low-cost pulse-transformer to transfer all data for all power supply modules, which saves significant cost. The protocol designed for this system is more efficient than existing protocols, while providing beneficial features such as DC-balance and clock recovery to reduce the system cost. A Multi-Resolution Feedback (MRF) method is used to compress ADC data by 60%. Together the proposed system provides 4 times higher output accuracy than existing designs, with averagely less than a half

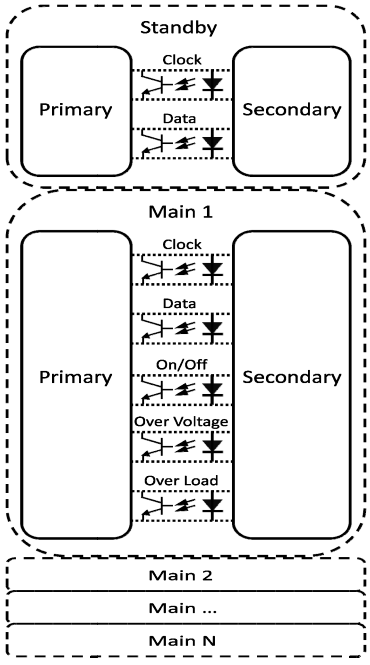


Figure 1. High-speed opto-couplers used in a traditional system

of the data rate. A prototype is built to demonstrate the feasibility of the proposed system.

II. The Proposed System

The proposed system is shown in Figure 2, where one set of controllers is used to control multiple power stages. A communication protocol is developed for this application. The proposed system takes six measures to optimise the data communication: (1) Use the Multi-Resolution Feedback (MRF) method to compress 10-bit ADC samples into 4 bits, providing higher output accuracy while lowering the data transfer rate; (2) Multiplex all digital feedback loops into one data bus to reduce the number of digital isolators; (3) Integrate control functions such as on/off, over voltage protection, over temperature protection, etc., into the data bus to reduce the required isolators; (4) Use a highly efficient 8B/10B-based protocol to improve the protocol efficiency; (5) Use clock recovery to eliminate the clock line isolator; (6) Use a low-cost pulse-transformer, which is much cheaper than other types of isolators, and can deliver power to the secondary digital circuits while transmitting data, if properly arranged [9].

III. The Multi-Resolution Feedback Method

Two facts are considered for data compression in digital power supplies. The first, the output voltage will never go beyond the Output Regulation Range, which is defined in the design specification, usually less than ±5% of the output voltage. If the required output accuracy is 0.1%, then there are 100 possible quantization levels within the output regulation range, versus the full 1023 quantization levels of a 10-bit ADC. The second, the power controller does not require accurate sample voltage for feedback control when the output voltage is far from the reference voltage. Only after the output voltage is recovered near the reference voltage level, high resolution samples are needed to finely adjust the duty cycle. Taking advantage of these two facts, much information can be taken out from sample data without impacting the system performance, and thus the sample length can be shortened.

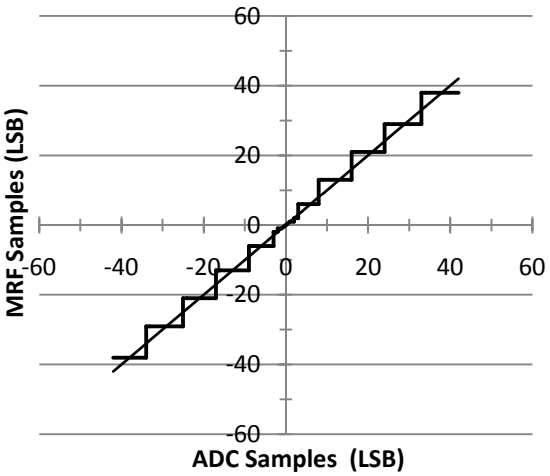


Figure 3. Concept map of MRF levels

The multi-resolution feedback (MRF) method is a lookup table which unevenly divides the power supply's output regulation range into several levels. The highest resolution is provided near the reference voltage, and becomes coarser and coarser as the sample value deviates away from the reference voltage. The number of MRF levels is much less than the ADC quantization levels thus the sample data can be encoded into a much shorter length. The concept map of MRF levels is shown in Figure 3.

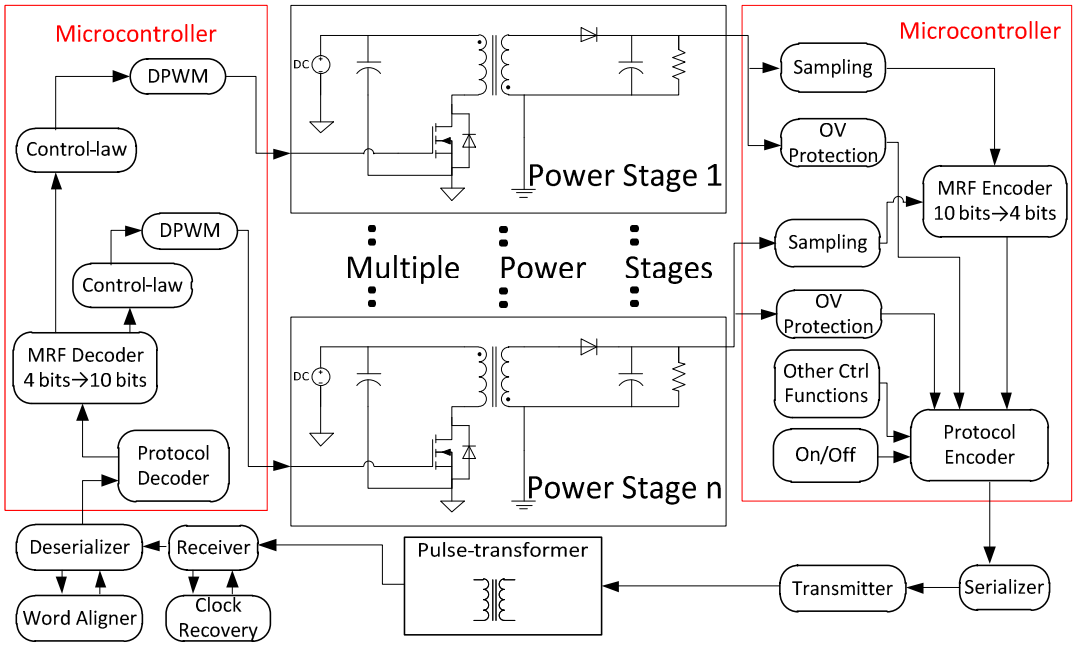


Figure 2. The proposed system

The error introduced by MRF can be considered as round-off error in quantization effect due to the finite ADC resolution, which does not affect the system stability [10]. Its effect can be considered a variable gain, which is the ratio between the MRF sample value and the real sample value. The system open-loop transfer function can be written as:

$$\widehat{H}(s) = M(V_{error}) \cdot H(s)$$

where $H(s)$ is the original open-loop transfer function, and $M(V_{error})$ is the variable gain.

$$M(V_{error}) = V_{MRF} / V_{error}$$

where V_{MRF} is the decoded voltage value corresponding to the MRF level, and $V_{error} = V_{ref} - V_{ADC}$.

In the steady state, the highest resolution is provided, thus there is no MRF error, and $M(V_{error}) = 1$. Therefore, the MRF variable gain does not change the system transfer function in steady state.

An example MRF look-up table is shown in Table 1. A 5V output is regulated within 5±0.25V. The output regulation range (equivalent to ±42 LSBs) is divided into 15 levels, which are represented by 15 MRF codes. These 4-bit MRF codes are sent through the digital isolator to the primary side, and are then decoded back to LSB value for control law calculation. While decoding, each MRF code has a corresponding LSB value, which may be different than the original sample, so the MRF error is introduced. This error is zero at 0 LSB (the reference voltage), ±1 LSB, and ±2 LSB, providing accurate feedback and unity extra gain. This MRF error is the largest at ±42 LSB, nevertheless, the extra gain introduced in here is not the largest because the real sample value is also larger, and their ratio becomes small.

The MRF variable gain across the output regulation range is plotted in Figure 4. It shows that the maximum extra gain in this MRF look-up table is 1.5, which is rather insignificant comparing to the total loop gain.

Table 1. MRF Look-up Table Design Example

Verror (V)	Verror (LSB)	MRF Value (LSB)	MRF Code
-0.2632 to -0.2131	-42 to -34	-38	1111
-0.2068 to -0.1567	-33 to -25	-29	1110
-0.1504 to -0.1066	-24 to -17	-21	1101
-0.1003 to -0.0564	-16 to -9	-13	1100
-0.0501 to -0.0251	-8 to -4	-6	1011
-0.0188 to -0.0125	-3 to -2	-2	1010
-0.0063	-1	-1	1001
0	0	0	1000
0.0063	1	1	0111
0.0125 to 0.0188	2 to 3	2	0110
0.0251 to 0.0501	4 to 8	6	0101
0.0564 to 0.1003	9 to 16	13	0100
0.1066 to 0.1504	17 to 24	21	0011
0.1567 to 0.2068	25 to 33	29	0010
0.2131 to 0.2632	34 to 42	38	0001

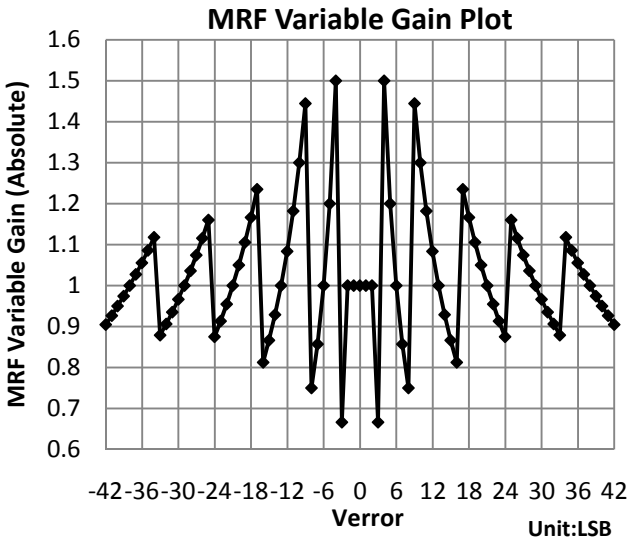
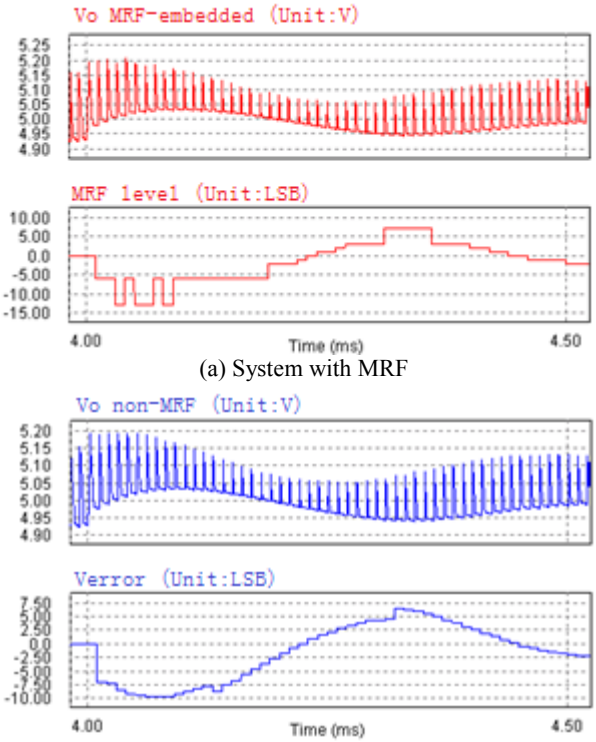


Figure 4. MRF Variable Gain Plot

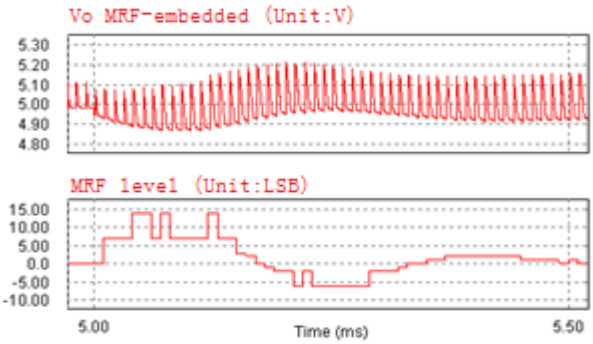
Figure 5 and Figure 6 show the simulation result of a Flyback converter with and without the MRF. It is demonstrated that although the MRF-embedded system has coarse resolution on error signal (MRF level) at large values, the output voltage waveforms from the two systems are



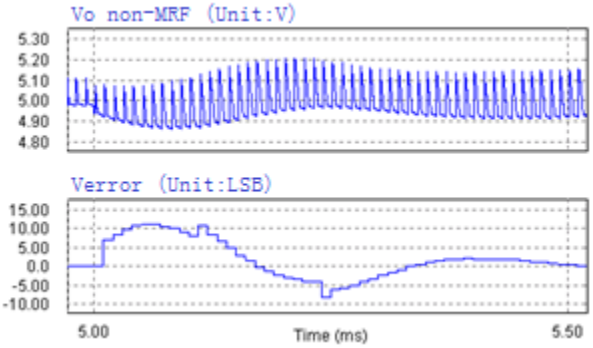
(a) System with MRF

(b) System without MRF

Figure 5. Simulation results (75% to 25% load step)



(a) System with MRF



(b) System without MRF

Figure 6. Simulation results (25% to 75% load step)

almost identical. Therefore the MRF method has no visible influence on the system's dynamic response.

Nevertheless, there are a few design considerations:

If steady state error exists, the output voltage in steady state may vary, therefore the highest resolution must be provided by the MRF levels throughout this range, which significantly increases the amount of MRF levels. Therefore the steady-state error must be eliminated to minimize the total MRF levels.

The ripple voltage should be averaged out before encoding, because the highest resolution is only provided within a few LSB of the objective voltage point, and the ripple voltage is likely to exceed this range.

IV. THE 8B/10B-BASED PROTOCOL

A desired protocol should be DC-balanced, where the transmitted 1s and 0s should be equal within a period of time to prevent the pulse-transformer from core saturation. Also, the protocol must ensure enough signal state changes to support clock recovery in order to eliminate the clock line to reduce a digital isolator. Furthermore, the protocol must have means to detect errors with ideally no bandwidth consumption. Traditionally used Manchester code [11] uses a "10" pair to represent a "1", and a "01" pair to represent a "0", thus it consumes two times the bandwidth to achieve DC-balance. 8B/10B line-code [12] is found to have above features and efficient. It converts every 8-bit code into two complementary 10-bit codes to achieve DC-balance.

The mechanism of 8B/10B code is briefly described below: each 8-bit code is mapped into two 10-bit codes, which are complement codes of each other. All 10-bit codes consist of five 0s and five 1s, or four 0s and six 1s, or six 0s and four 1s. Therefore the disparity of a 10B code is either neutral (five 0s and five 1s) or ±2 (four 0s and six 1s, or six 0s and four 1s). The system's Running Disparity (RD) is monitored by the encoder: if a 10B code is neutral, the system RD does not change; if a 10B code is non-neutral, +2 and -2 disparity codes are selected alternatively to balance the system RD.

The 8B/10B code has three "comma" codes, which are distinguishable anywhere in a data stream and thus can be used for frame synchronization. Whenever the receiver "sees" a "comma", it resets its counter and a frame starts from there. The "comma" codes can be used to replace a separate frame synchronization line, and along with 9 other special codes, can be used as control symbols to integrate all control functions into the data bus.

The proposed MRF method can fit into the 8B/10B line-code very well, as two 4-bit MRF code can form an 8-bit code for 8B/10B encoding.

The 8B/10B-based protocol is described as below.

1. For two-module systems

An application usually has at least a standby power stage and a main power stage. Each output voltage is sampled by a 10-bit ADC. The MRF compresses each sample into 4 bits, and the two 4-bit samples compose an 8-bit code for 8B/10B encoding. In this system, the frame length is one 10B code. A "comma" code is repeatedly sent to initialize the clock recovery and frame synchronization at start up. The 8B/10B decoder detects/corrects illegal codes if the receiver receives wrong bits or loses frame synchronization.

2. For multi-module systems

In multi-module mode, a system has several power stages. The frame length is several 10B codes, starting with a symbol code as a frame header, followed by several MRF-8B/10B-encoded samples. The frame header identifies the beginning of a frame. In the simplest case, each frame carries samples of all power stages in a fixed order: the first 10B code following the frame header is for Power Stages 1 and 2; the second 10B code is for Power Stages 3 and 4, and so on. Therefore the address bits are omitted.

In the case that a system contains several power stages of different sampling frequency, the above method may not be optimized and result in higher bandwidth requirement. For example, for a system that consists of 8 power stages where the sampling frequencies are: CH1 (Power Stage 1/2): 100 KHz, CH2 (Power Stage 3/4): 50 KHz, CH3 (Power Stage 5/6): 25 KHz, CH4 (Power Stage 7/8): 25 KHz, the frame length will be five 10B codes (1 frame header+4 data bytes), and the required communication bandwidth will be

50bit/frame*100K frames/sec=5Mbit/sec, where only 60% of the bits carry useful information.

In order to use the communication bandwidth efficiently when the sampling frequencies of the power stages are different, several types of frames are used. The types of the frames are indicated by the different control symbols which are used as frame headers. Therefore no extra bits are needed to identify the frame type. Using the above case as an example, the frame types are defined in Figure 7: the frame length is only three 10B codes (1 frame header +2 date bytes) instead of five. The required communication bandwidth will be 30bit/frame*100K frames/sec=3Mbit/sec, where 100% of the bits carry useful information.

The frame types are arranged in a sequence shown in Figure 8 which optimizes the bandwidth usage: CH1 takes all Byte 1 positions, CH2 takes 50% of the Byte 2 positions, and CH3 and CH4 take 25% of Byte 2 positions, respectively. All channels communicate at their own frequencies and no bandwidth is wasted.

The rest control symbols can be used for On/Off command, Over Voltage/Load/Temperature Protection commands, and so on. The 3 "comma" codes are recommended to be used as frame headers in order to regain frame synchronization in case it is lost. This way, the frame synchronization line is eliminated and a digital isolator is saved.

The only restriction of the proposed arrangement is that each sampling frequency must be integral times lower than the highest one in a system. For example, if a sampling frequency is 100 KHz, and another sampling frequency is 70 Khz, the two channels cannot be multiplexed together in one frame for communication.

A comparison of existing systems and the proposed system is shown in Table 2, which shows the proposed system has the highest output accuracy and the lowest data transfer requirements with various features to reduce the system cost.

Frame Type	Header	Byte 1	Byte 2
Type 1	Symbol 1	CH1	CH2
Type 2	Symbol 2	CH1	CH3
Type 3	Symbol 3	CH1	CH4

Figure 7. Example Frame Types

Frame Type	Byte 1	Byte 2
Type 1	CH1	CH2
Type 2	CH1	CH3
Type 1	CH1	CH2
Type 3	CH1	CH4
Type 1	CH1	CH2
Type 2	CH1	CH3
Type 1	CH1	CH2
Type 3	CH1	CH4
Type 1	CH1	CH2
Type 2	CH1	CH3
Type 1	CH1	CH2
Type 3	CH1	CH4

t

Figure 8. Example Frame Sequence

V. Experimental Results

The prototype consists of two identical 100 KHz digital Flyback power stages. Vin= 48± 5VDC, and Vo=5V/25W. Two dsPIC30F2020 microcontrollers are used for implementing ADC, controller and codec. The serializer, de-serializer, and word aligner are built with logic gates. The secondary-side On/Off and Over Voltage Protection commands are integrated into the data bus. A pulse-transformer is used and is driven by discrete VLDS

Table 2. System Comparison

Author	**The Proposed System**	**Ka Leung**[1]	**Aleksandar Prodic**[2]	**Microchip** [3]
Method	MRF using the 8B/10B-based protocol	Direct duty cycle transmission	4 LSB using a customized protocol	8 MSB using UART standard
DC-Balance	Yes	No	No	No
Multiplexed	Yes	No	No	No
Isolators needed	1 pulse-transformer for all power modules	1 expensive logic isolator for 1 PWM	2 logic opto-couplers for 1 power stage	1 logic opto-coupler for 1 power stage
Accuracy	0.098% (10-bit ADC)	1.563% (6-bit ADC)	0.392% (8-bit ADC)	0.392% (8-bit ADC)
Control Func.	Yes	No	No	No
Clock Recovery	Support	N/A	Do not support	Do not support
Error Detection	Yes (with no bit cost)	N/A	Yes (with large cost)	Yes (with bit cost)
Bandwidth Consumption	5 bits per sample for 2 modules (theoretical maximum) to $5 + \frac{10}{4} = 7.5$ bits per sample for 4 modules (worst case scenario).	N/A	16 bits per sample for 1 power stage.	12 bits per sample for 1 power stage.

transceivers. Since researches [12] and FPGA manufacturers provide mature technology to use 8B/10B code to support clock recovery, a separate clock line instead of a clock recovery block is used in this prototype for simplicity. The data rate of the communication bus is 8 Mbps, which is capable of transmitting data for 14 power stages at 100 KHz sampling frequency (eight 10B codes per frame, 100K frames per second). In this prototype, only the frame header and Byte 1 are used, and the rest 6 10B codes are filled with "01100 01011" (corresponding to "0000 0000" in MRF code).

The MRF look-up table shown in Table 1 is used in the prototype. The output regulation range is 5V±5%. A 10-bit ADC is used and 1 LSB represents 6.3mV.

Figure 9 and Figure 10 shows the load transient responses. The waveforms do not show any nonlinear behavior, which is consistent with the simulation results. Ch1 (yellow): Vout of Power Stage 1; Ch2 (red): Vout of Power Stage 2; Ch3 (blue): Vout of Power Stage 1, AC coupled; Ch4 (green): Iout of Power Stage 1.

Figure 11 shows the excellent output accuracy of the prototype system. Figure 12 shows a data stream in nine successive frames, captured in a single waveform, and then zoomed in at each frame. This test examines output accuracy (the ADC samples) in steady state, and also verifies the DC-balance. The extracted data are in Table 3. The Disparity column shows that the ±2 disparity 10B codes are chosen alternately to balance the system RD. The MRF Code column shows that the output voltages of both power stages are regulated within 1 LSB of the reference level (1000).

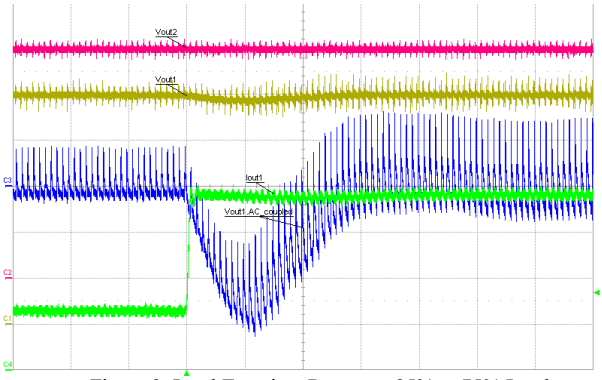


Figure 9. Load Transient Response 25% to 75% Load

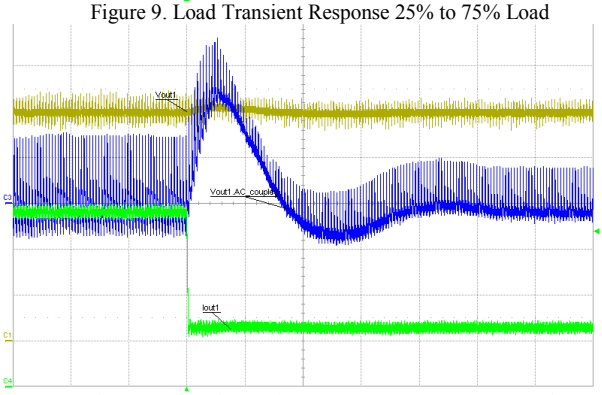


Figure 10. Load Transient Response 75% to 25% Load

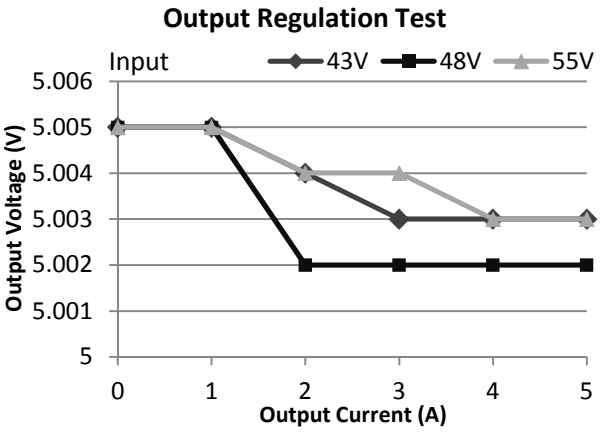
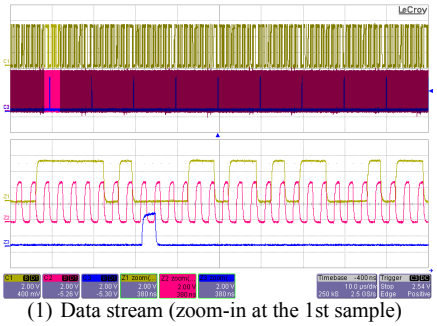
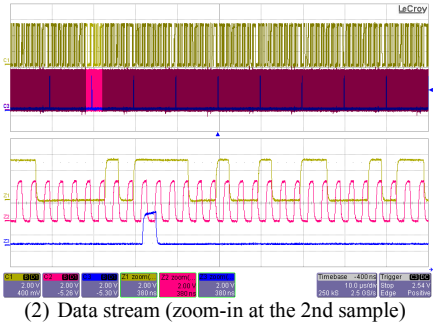


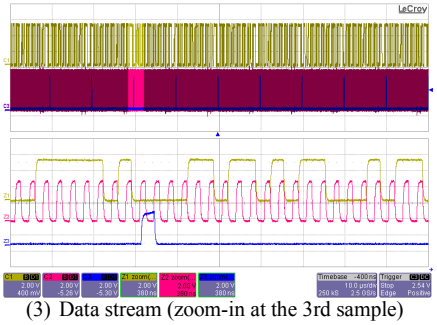
Figure 11. Output Regulation Test



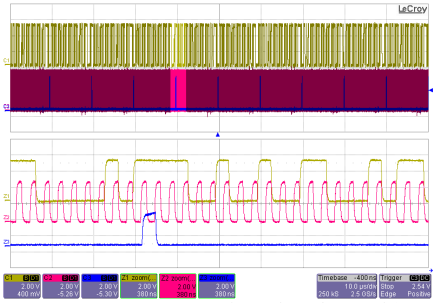
(1) Data stream (zoom-in at the 1st sample)



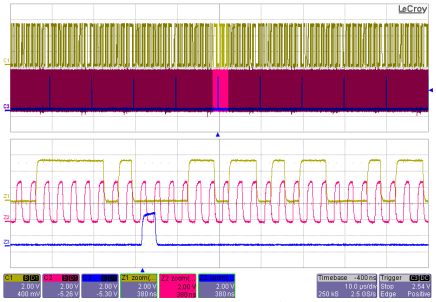
(2) Data stream (zoom-in at the 2nd sample)



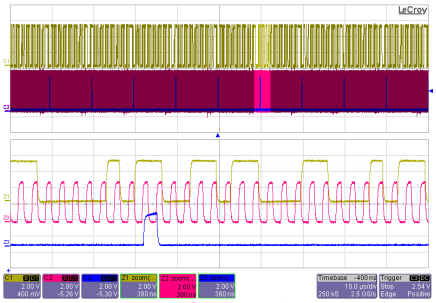
(3) Data stream (zoom-in at the 3rd sample)



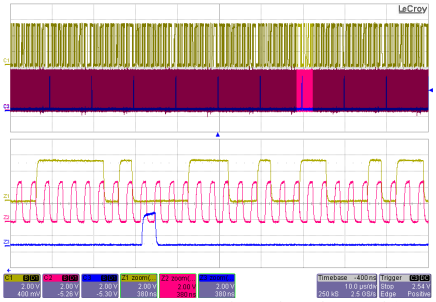
(4) Data stream (zoom-in at the 4th sample)



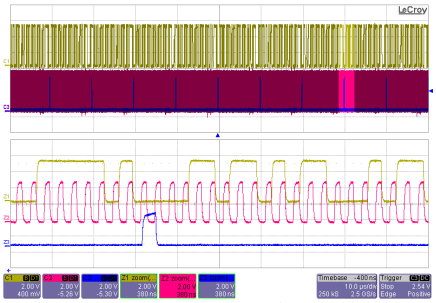
(5) Data stream (zoom-in at the 5th sample)



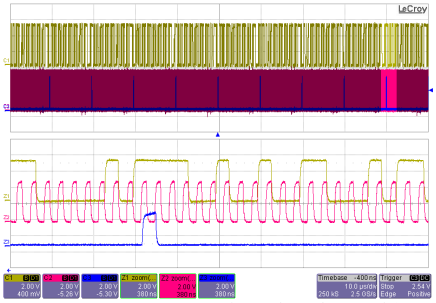
(6) Data stream (zoom-in at the 6th sample)



(7) Data stream (zoom-in at the 7th sample)



(8) Data stream (zoom-in at the 8th sample)



(9) Data stream (zoom-in at the 9th sample)

Figure 12. Data stream in 9 successive frames. Ch1 (yellow): Data, Ch2 (red): Clock, Ch3 (blue): Frame Header.

Table 3 Extracted data from 9 successive frames

Frame #	Byte #	10B Code	8B Code		Disparity
			CH1	CH2	
1	header	0011111010	Comma		+2
	1	0001101101	1000	1000	0
2	header	1100000101	Comma		-2
	1	1110010010	1000	1000	0
3	header	0011111010	Comma		+2
	1	0001101101	1000	1000	0
4	header	1100000101	Comma		-2
	1	1110010010	1000	1000	0
5	header	0011111010	Comma		+2
	1	0001101101	1000	1000	0
6	header	1100000101	Comma		-2
	1	1001101100	0111	1001	0
7	header	0011111010	Comma		+2
	1	0001110010	1000	0111	-2
8	header	0011111010	Comma		+2
	1	0001101101	1000	1000	0
9	header	1100000101	Comma		-2
	1	1110010010	1000	1000	0

VI. CONCLUSION

A multiplexed power supply system with high-accuracy and low data transfer requirement is proposed. The system combines an efficient 8B/10B-based protocol and a MRF method to compress ADC sample length by 60% in order to optimize the data communication, and improve the output accuracy at the same time. The system consumes less bandwidth than existing systems and features much lower cost by replacing all high-speed opto-couplers by a single pulse-transformer. The advantages of the proposed system over the existing systems are demonstrated. The feasibility is proved by the prototype.

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