A Practical Control Strategy to Improve Unloading Transient Response Performance for Buck Converters

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***Abstract*— In this paper, a practical control strategy is presented which is capable of controlling a 12V-1.5V Buck converter and an auxiliary converter to achieve significantly improved unloading response performance. The auxiliary circuit is controlled by peak current mode method for a predictable number of auxiliary switching, while the charge balance controller minimizes the settling time of the Buck converter. In the proposed strategy, a good tradeoff has been made (between the trends to further suppress the voltage overshoot and reduce the power loss). Furthermore, analysis of the auxiliary circuit power loss and the improved output voltage overshoot has been conducted as a design guideline. Finally, simulation and experimental results are provided to verify the proposed scheme on a 12V-1.5V 10A Buck converter prototype.**

***Index Terms*—Capacitor charge balance controller, Buck converter, fast transient response, controlled auxiliary current**

I. INTRODUCTION

As the computing capabilities of high-performance digital devices continue to expand, the demand on the power supplies for powering such devices becomes increasingly stringent. Thus, extensive research has been conducted to develop advanced controllers to improve the transient performance of Buck converters to their physical limits. In [1]-[14], controllers have been presented which apply second-order sliding surfaces, pre-calculated switching time intervals or capacitor charge balance methodologies to reduce the voltage deviation and settling time of a Buck converter, undergoing a load transient, to its virtually optimal level. But, in [1],[6], it is demonstrated that for a commonly used 12V-1.5V Buck converter even under optimal control, the undesired large output voltage overshoot still dominates the output capacitance requirement, because of the much worse and marginally improved unloading response performance. To address the asymmetrical response, a two-stagy power conversion scheme is presented in [12], which creates a 5V intermediate dc bus voltage to balance the stage conversion ratio close to 50% but adds more power loss, cost and board space to the entire system. Many auxiliary circuitries are reviewed in [14] to reduce the output voltage overshoot, and the one shown in Figure 1 coupled with its control law has the following advantages: 1) predictable behavior allowing for simplified design; 2) inherent over-current protection; and 3) low peak current to average current ratio allowing for use of smaller components. However, the auxiliary converter operates for very high switching frequency (>MHz) during activation under a relatively complex current mode control law, which downgrades the enhancement if applied to a multiphase Buck converter. In [15], another overshoot reduction solution using the aforementioned auxiliary circuit with an external energy storage capacitor and synchronous rectifier (SR) implementation is provided; however, the practicality is limited due to the additional linear compensator, the subsequent high frequency switching of the auxiliary converter and the unimproved settling time.

In this paper, a practical auxiliary current control strategy is presented to improve unloading transient performance, which has the following unique advantages: 1) the auxiliary circuit operating at relatively low frequency to reduce the switching loss; 2) further voltage overshoot reduction; 3) predictable auxiliary switching based on the main to auxiliary inductance ratio; and 4) minimizing the settling time of unloading response based on charge balance principles.

This paper is organized as follows. In Section II, the operating principles of the proposed scheme are presented. The analysis of voltage overshoot and power loss is made in Section III, followed by hardware implementation in Section IV. The simulation and experimental results are shown in Section V. The conclusions are drawn in Section VI.

II. OPERATING PRINCIPLES OF THE PROPOSED CONTROL SCHEME

When a Buck converter follows an unloading transient response, it is important to reduce the current conducting through the output capacitor. As stated in [5], the load current falls at a much higher slew rate than the inductor current, the capacitor must absorb charge (and thus increase voltage). The voltage overshoot may be reduced by modifying the output filter parameters, that is, by decreasing the size of the output inductor (resulting in decreased efficiency due to larger peak and thus RMS MOSFET current levels and/or increased switching frequency) or by increasing the size of the output capacitor (resulting in a significantly higher cost of the Buck converter).

Alternatively, the amount of charge absorbed by the capacitor can be reduced by diverting excess current from the output inductor of the Buck converter to the converter's input

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through operation of the proposed controlled auxiliary circuit. As will be shown, a large reduction in the output voltage overshoot can be realized by the addition of a small inductor, MOSFET, and diode. The auxiliary circuit can be modeled as a controlled current source, drawing current from the output capacitor of the Buck converter and transferring it to the input of the Buck converter. Figure 1 shows the model of such method when used with a synchronous Buck converter. The auxiliary current is only active during step-down load current transients (i.e., before and after an unloading transient, the circuit operates as a conventional Buck or synchronous Buck converter).

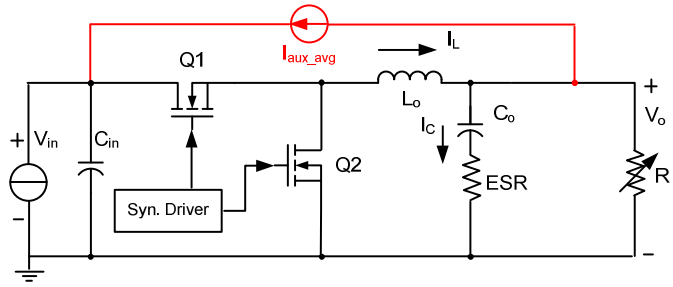

Figure 1 Simplified model of the proposed CAC

Figure 2 shows one possible implementation of the auxiliary circuit used in this paper. An alternate implementation would involve using a second MOSFET (in lieu of D_{aux}) for synchronous rectification. As is shown, the auxiliary circuit resembles a small boost converter connected in antiparallel with the Buck converter.

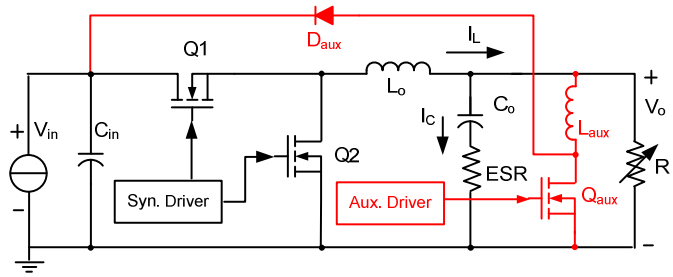

Figure 2 MOSFET-diode implementation of the CAC

In [14], a controlled auxiliary current (CAC) is presented to improve the transient response of a Buck converter as shown in Figure 3. The duration of activation of the auxiliary current is regulated. That method has the following advantages:

1) predictable behavior allowing for simplified design; 2) inherent over-current protection; 3) low peak current to average current ratio allowing for use of smaller components.

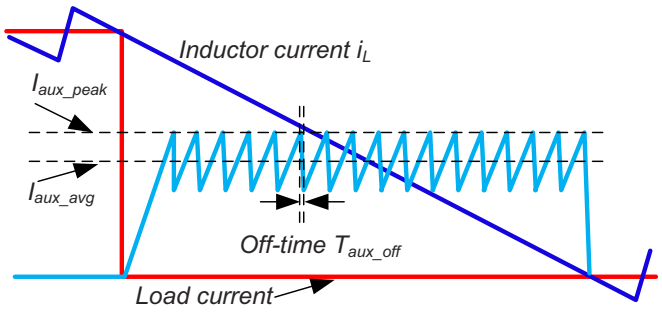

Figure 3 Peak current mode, constant off-time operation of the proposed controller

This method also estimates the magnitude of the unloading transient and sets the auxiliary current proportional to the transient magnitude. This allows for greater design flexibility and increases the auxiliary circuit efficiency for unloading transients of lower magnitude. The auxiliary is controlled by using constant off time peak current control scheme.

However, this controller is not suitable for multiphase Buck converters due to the high switching frequency of the auxiliary circuit. For example, in order to maintain the average value of the auxiliary current for a two phase Buck converter with 360nH per phase output inductance, the switching frequency of the auxiliary switch will be reaching above 5MHz, resulting in highly increased switching losses, gate drive losses and auxiliary MOSFET driver cost. Also, the controller design is relatively complex with constant T_{aux_off} delay time injection, load current estimation, and filtered current sensing. Above all, because of the low initial auxiliary current peak, the overshoot of this control scheme is not optimal/near-optimal, even though the current level is adjustable.

Although a similarly designed auxiliary circuit is employed for improving the unloading transient performance (see Figure 2), several unique merits of the proposed control strategy will be discussed in this paper (through details in Section III). The proposed BCM peak current mode (PCM) controlled auxiliary current (CAC) is shown in Figure 4. During steady state operation or step-up loading transient, the CAC is deactivated and the main Buck converter is regulated by an analog charge balance controller (discussed in [17], but other CBC controllers/schemes are also applicable) [16]. When the unloading transient happens, the CAC will be operated for rapidly removing the extra capacitor charge energy back to the input source through the Schottky diode D_{aux}. The operations of the CAC and the proposed control strategy are described as follows (see Figure 4):

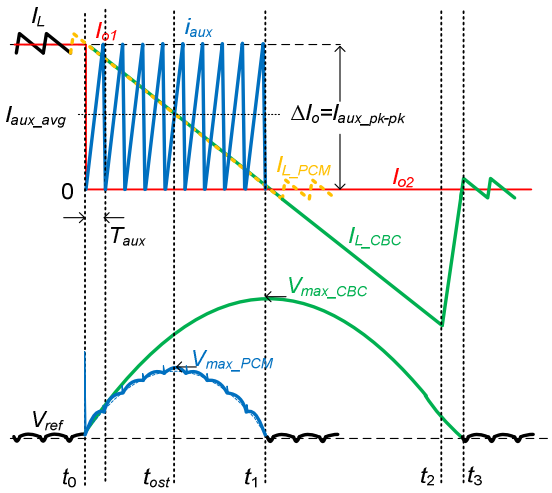

Figure 4 BCM Peak current mode (PCM) CAC and normal CBC operation waveforms

1. It is assumed that the unloading transient happens at t_0, triggering the proposed control scheme to minimize the output voltage overshoot;
2. The main switch $Q1$ will immediately turn off to reduce the additional capacitor charge at t_0, while, the S/H circuit sets the peak current reference value $I_{aux\_pk\text{-}pk}$ by holding the output of the capacitor current sensing circuit (see Figure 13);
3. The auxiliary circuit will be controlled using peak current (at $I_{aux\_pk\text{-}pk}$) mode method in BCM (see Figure 4), which can be approximately modeled as a current source connected between output capacitor and input voltage source to minimize the output voltage overshoot (see Figure 1).
4. After a predictable n (to be calculated later in Section III, A) cycles of auxiliary switching, the output voltage will recover to the reference voltage V_{ref} at t_1 and the normal CBC controller will take over the regulation such that the settling time can be optimized.

From the settling time point of view, when we set the BCM peak current at $I_{aux\_pk\text{-}pk}$, equivalently, the average auxiliary current I_{aux_avg} will be half of the transient load current step value ΔI_o, that is, I_{aux_avg}=1/2 ΔI_o. Therefore, the auxiliary current can rapidly balance the capacitor charge at t_1.

On the contrary, without the help of CAC, the output capacitor will be charged by the current of (I_L-I_{o2}) until t_1. Therefore, the CBC controller requires the negative portion of inductor current to discharge the capacitor. As soon as the capacitor charge is balanced and the output voltage will recover to V_{ref} at t_3 for normal CBC controller [5][17]. In conclusion, the CAC coupled with CBC controller can significantly reduce the settling time.

Furthermore, in Figure 5, it reveals that in order to meet the overshoot requirement at 50mV under 10A step-down load transient, 630μF output capacitance is required for CBC controlled Buck converter without CAC, while, by using the proposed BCM PCM controlled CAC, the required output capacitance can be reduced by 73.0% to 170μF. As a result, the output capacitance can be implemented with ceramic capacitors, resulting in reduced motherboard area and improved output voltage ripple.

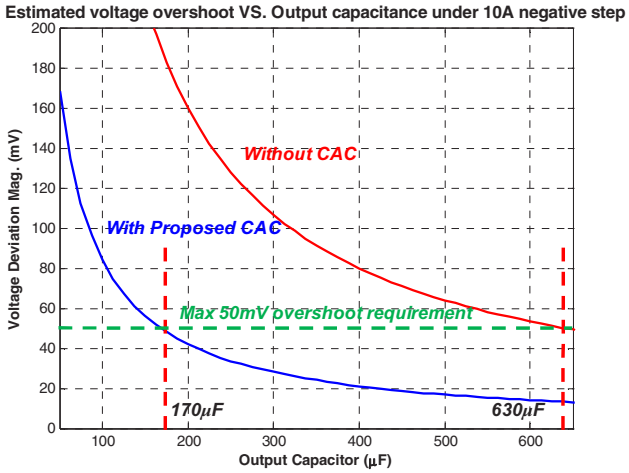

Figure 5 Estimated voltage overshoot for various output capacitance with and without BCM PCM CAC for an unloading transient of 10A (V_{in}=12V, V_o=1.5V, L_o=1uH, L_{aux}=100nH)

Several unique advantages of the proposed control strategy will be discussed in this paper (through details in Section III). Firstly, the auxiliary current (CAC) will be operated in the boundary condition mode (BCM) at reduced switching frequency (the CAC falls to zero at the end of each switching cycle), such that the switching power loss can be decreased and a commonly used PWM driver can be used to drive the auxiliary switch $Q1$. Also, because of the higher initial peak current of the auxiliary inductor, the output voltage overshoot will be lower compared to the previous scheme in [14]. Furthermore, according to the design ratio between main output inductance (L_o) and the auxiliary inductance (L_{aux}), the number of auxiliary switching cycles is predictable, which enhances the reliability of the proposed control scheme. For example, if the output inductance L_o=1μH and the auxiliary induction L_{aux}≈100nH, the number of auxiliary switching cycles will be n=9. And the proposed scheme can be simply scaled and extended to multiphase Buck converter with much lower equivalent output inductance. But on the other hand, in this circumstance, previous schemes may badly suffer from the impossibly high frequency switching or low auxiliary inductance for maintaining the average auxiliary current level.

III. Voltage Overshoot Estimation and Auxiliary Circuit Power Loss Analysis

A. Overshoot Estimation with the Proposed Strategy of Controlled Auxiliary Current

Without loss of generality, it is assumed that the auxiliary circuit is switched for n times under BCM PCM control, where integer n is the number of auxiliary switching cycles. The instantaneous output voltage variation can be expressed as (1) for two intervals depending on the ON/OFF state of the auxiliary circuit and the N^{th} time of switching, where T_{aux} is the switching period of the auxiliary current and d_{aux} is the duty cycle of the auxiliary converter.

$$\Delta v_o(t)=\begin{cases}\dfrac{1}{C_o}\left[\Delta I_o\cdot t-\dfrac{V_o}{2L_o}t^2-\dfrac{N\cdot\Delta I_o\cdot T_{aux}}{2}-\int_0^{(t-N\cdot T_{aux})}\dfrac{V_o}{L_{aux}}t\cdot dt\right] \\ \left(NT_{aux}\le t<NT_{aux}+d_{aux}T_{aux}\right)\left(N=0,\ 1,\ 2\ ...,n\right) \\ \dfrac{1}{C_o}\left[\Delta I_o\cdot t-\dfrac{V_o}{2L_o}t^2-\dfrac{N\cdot\Delta I_o\cdot T_{aux}}{2}-\dfrac{V_{in}-V_o}{2V_{in}}T_{aux}\Delta I_o\right. \\ \left.-\int_{(t-N\cdot T_{aux}-d_{aux}T_{aux})}^{T_{aux}}\dfrac{(V_{in}-V_o)(T_{aux}-t)}{L_{aux}}dt\right] \\ \left(NT_{aux}+d_{aux}T_{aux}\le t<(N+1)T_{aux}\right)\left(N=0,\ 1,\ 2\ ...,n\right)\end{cases} \quad (1)$$

The output overshoot/maximum voltage will occur at the time t_{ost} in (2), when the derivative of the equation (1) is zero during the (N'+1)th switching, where N' is calculated in the equation (3) depending on the parity of n.

$$t_{ost}=\frac{D_{aux}+N'}{D_{aux}+n}\cdot nT_{aux} \quad (2)$$

$$N'=\begin{cases}\dfrac{n-1}{2} & (\text{when } n \text{ is odd}) \\ \dfrac{n}{2}-1 & (\text{when } n \text{ is even})\end{cases} \quad (3)$$

Based on the average auxiliary current L_{aux_avg} without considering the auxiliary inductor current ripple under the BCM peak current control, a simplified equation is provided as practical method to calculate the overshoot in the equation (4). The symbols L_o, C_o, ESR, ΔI_o, V_o and L_{aux} represent the output inductance, output capacitance, equivalent series resistance, load step value, output voltage and the auxiliary inductance, respectively.

$$\Delta V_o\approx\frac{ESR\cdot C_o^{\,2}\cdot V_o^{\,2}+\left(\dfrac{\Delta I_o}{2}\right)^2\cdot L_o^{\,2}}{2V_o\cdot L_o\cdot C_o}+\frac{\left(\dfrac{\Delta I_o}{2}\right)^2\cdot L_{aux}^{\,2}}{2V_o\cdot C_o} \quad (4)$$

Another advantage of the proposed scheme is that under a certain value of step-down load transient, the number n of auxiliary switching can be predicted using the input and output voltage information as well as the inductance ratio of L_o and L_{aux}. The number of switching n can be estimated using the equation (5), where $[]_{\text{int}}$ indicates the rounding down operation. It is noted that n is independent on the load transient step value ΔI_o.

$$n=\left[\frac{(V_{in}-V_o)L_o}{L_{aux}\cdot V_{in}}+0.5\right]_{\text{int}} \quad (5)$$

Figure 6 shows the relationship between the number of auxiliary switching cycles n (as well as the ratio of L_o/L_{aux}) and the auxiliary inductance value under different output voltages V_o. So based on the power circuit design parameters (V_{in}, V_o. L_o, and L_{aux}), the necessary cycles of auxiliary switching for fast recovering the overshoot can be counted by a counter for n. By this means, it becomes very straight forward for the CBC controller to deactivate the CAC (as soon as the count reaches n).

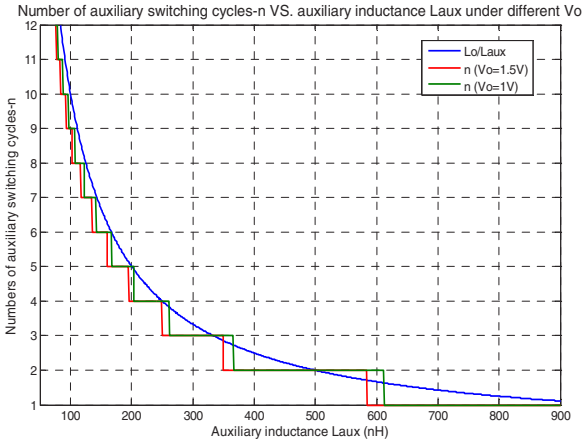

Figure 6 Number of auxiliary switching cycles n (as well as the ratio of L_o/L_{aux}) and the auxiliary inductance value under different output voltages V_o

Figure 7 illustrates the impact of rounding down operation of n on the settling time. In Figure 7(a) the CAC will be deactivated before the inductor current reaches the new load level I_{o2}. A second overshoot occurs and the settling time is longer than the ideal case shown in Figure 4. On the contrary, as shown in Figure 7(b), the CAC activates longer than required, so that a voltage undershoot appears and increases the settling time, too. However, it is noted that the output overshoot equations in (1) are still valid because they are actually not dependent on the number of n. And the time instant t_{ost} can be expressed more generally in (6).

$$t_{ost}=\frac{\Delta I_o+\dfrac{V_o}{L_{aux}}NT_{aux}}{\dfrac{V_o}{L_o}+\dfrac{V_o}{L_{aux}}}=\frac{\Delta I_o\cdot L_{aux}L_o+V_o\cdot NT_{aux}\cdot L_o}{V_o\left(L_{aux}+L_o\right)} \quad (6)$$

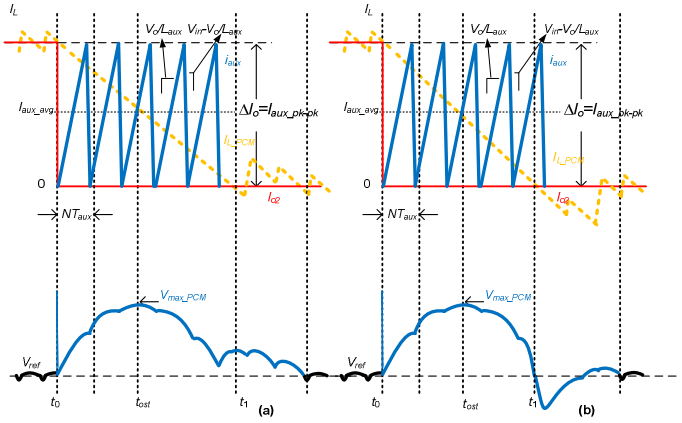

Figure 7 The effect of rounding down operation of n on the settling time, (a) $[(V_{in}\text{-}V_o)/V_{in}*L_o/L_{aux}]\text{-}n<0.5$;(b) $[(V_{in}\text{-}V_o)/V_{in}*L_o/L_{aux}]\text{-n}\ge0.5$

Figure 8 gives the overshoot voltage for various numbers of auxiliary switching cycles using the proposed BCM PCM controlled auxiliary current. By choosing proper auxiliary inductance L_{aux}, the number of auxiliary switching n can be controlled according to the equation (5).

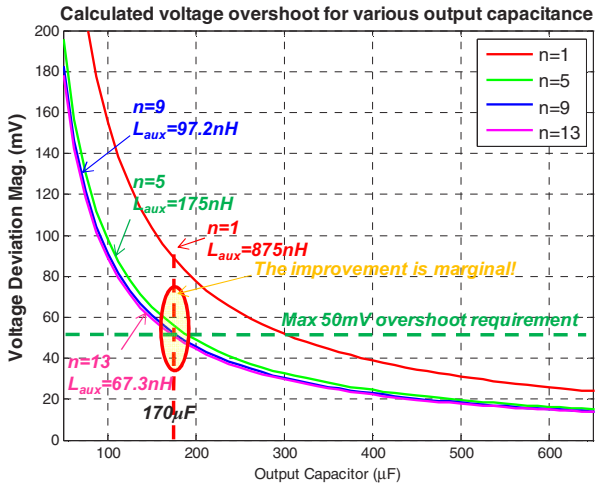

Figure 8 Estimated voltage overshoot for various times of CAC switching and different output capacitance for an unloading transient of 10A (V_{in}=12V, V_o=1.5V, L_o=1uH)

For example, as shown in Figure 9, n=1 means that in order to meet the overshoot requirement, the auxiliary circuit will be activated for one switching cycle during the unloading transient which can be achieved by selecting L_{aux}=875nH and output capacitance C_o=300μF, as shown in Figure 9(a). And for n=5, the auxiliary circuit will be activated for 5 switching cycles with selecting L_{aux}=175nH and C_o=185μF as shown in Figure 9 (b).

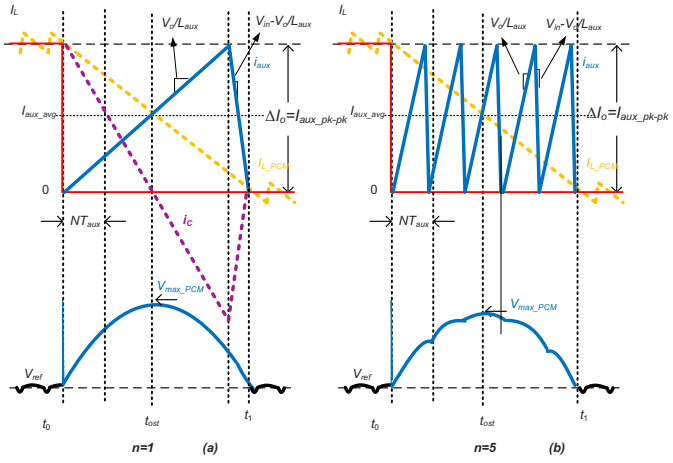

Figure 9 Controlled auxiliary current switching for n cycles by selecting different L_{aux} (a)n=1, L_{aux}=875nH; (b)n=5, L_{aux}=175nH (V_{in}=12V, V_o=1.5V, L_o=1uH)

It is also noted from Figure 8 that the lower the auxiliary inductance L_{aux} is, the more the number n of auxiliary switching cycles and the better the unloading transient performance will be. However, from the simulation result shown in Figure 6, the improvement is marginal when the auxiliary inductance L_{aux} becomes too small (i.e. L_{aux}<100nH, n>9) but on the contrary, low L_{aux} will increase the auxiliary switching frequency f_{aux} and harm the overall efficiency due to the more cycles of auxiliary switching.

In Figure 10, it shows that the switching frequency of the auxiliary FET f_{aux} increases linearly with the number of switching n. When the switching frequency f_{aux} is much higher than 1MHz, the cost of the auxiliary MOSFET driver will increase dramatically, resulting in extra/high cost of the CAC implementation. Therefore, design compromise should be made for output voltage overshoot and switching frequency/switching loss the auxiliary circuit.

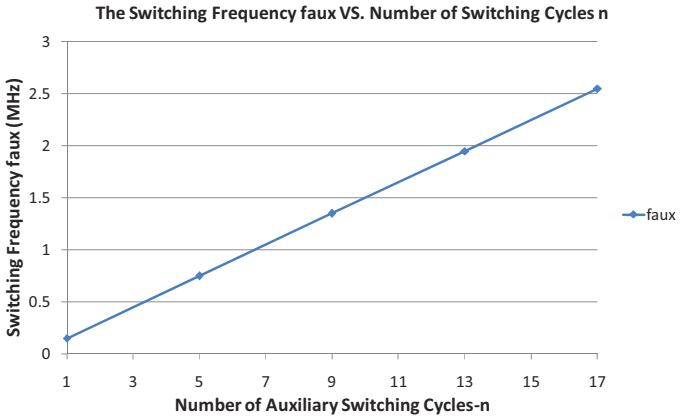

Figure 10 The plot of switching frequency f_{aux} versus the number n of switching cycles

B. *Auxiliary Circuit Power Loss Analysis*

There are three main sources of conduction loss pertaining to the proposed circuit [14]: the auxiliary inductor L_{aux}, the auxiliary FET Q_{aux} and the auxiliary diode D_{aux}.

By calculating the RMS auxiliary current in (7), the inductor conduction loss can be calculated but in the loss analysis due to the very low DCR and sensing resistance R_{Laux} of the auxiliary inductor L_{aux} (about 0.2mΩ in total). The auxiliary inductor conduction loss is in 10mW order and ignored.

$$I_{aux(rms)} = I_{aux\_avg}\sqrt{1+\frac{1}{3}\left(\frac{I_{aux\_pk-pk}}{2I_{aux\_avg}}\right)^2} \tag{7}$$

The RMS current of the auxiliary FET and the average current of the auxiliary diode can be calculated using (8) and (9).

$$I_{Qaux(rms)} = I_{aux\_avg}\cdot\sqrt{\frac{V_{in}-V_o}{V_{in}}}\sqrt{1+\frac{1}{3}\left(\frac{I_{aux\_pk-pk}}{2I_{aux\_avg}}\right)^2} \tag{8}$$

$$I_{Daux(avg)} = I_{aux\_avg}\left(1-\frac{V_{in}-V_o}{V_{in}}\right) \tag{9}$$

The conduction loss for the auxiliary FET and auxiliary diode can be calculated using (10) and (11).

$$P_{con\_Qaux} = I^2_{Qaux(rms)}\cdot R_{Qaux} \tag{10}$$

$$P_{con\_Daux} = I_{Daux(rms)}\cdot V_{diode} \tag{11}$$

Since a Schottky diode is utilized, it is assumed that the switching loss of the diode is negligibly small compared to the FET switching loss and the total conduction loss. Generally, the switching loss for the auxiliary FET can be

calculated using (12), where, T_{rise} is the rise time of the auxiliary FET and Ion is the instantaneous auxiliary current when Q_{aux} is turned on, respectively. T_{fall} equals the typical fall time of the auxiliary FET. I_{off} equals the instantaneous auxiliary current when Q_{aux} is turned off, which is equal to the peak auxiliary current.

$$P_{sw\_Qaux} = \frac{1}{2} f_{aux} \cdot V_{in} \cdot \left(T_{rise} \cdot I_{on} + T_{fall} \cdot I_{off} \right) \quad (12)$$

Because of the zero turn-on current under BCM operation of the CAC, the switching loss of the auxiliary FET can be simplified in (13).

$$P_{sw\_Qaux} = \frac{1}{2} f_{aux} \cdot V_{in} \cdot T_{fall} \cdot I_{off} \quad (13)$$

In Figure 11, according to the previous equations, the power loss analysis is shown for comparison between the proposed control strategy (BCM) and the existing control scheme (CCM). The conduction loss of auxiliary MOSFET and the Schottky diode, MOSFET switching loss and total losses are represented as Pcon_Qaux, Pcon_Daux, Psw_Qsw and Total_PCM for the proposed control strategy, while, Pcon_Qaux', Pcon_Daux', Psw_Qsw' and Total_CCM for the existing control scheme [14]. It is noted that the conduction loss of the auxiliary diode is unchanged (Pcon_Daux and Pcon_Daux' coincide in the figure) using the proposed scheme because of the same average current. The conduction loss of the auxiliary MOSFET using proposed BCM PCM controller is higher than that of the auxiliary MOSFET controlled by existing scheme [14] due to the larger inductor current ripple, thus, the RMS current value. However, compared to the existing scheme, the switching loss of the auxiliary MOSFET and the total losses are reduced using the BCM PCM controlled CAC. It is also worth noting that the auxiliary FET switching loss is independent on the load current level.

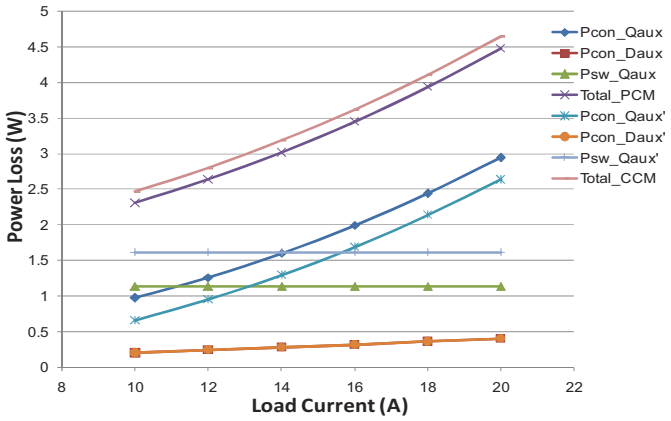

Figure 11 Comparison results of loss breakdown based on different control schemes (the power circuit design parameters: V_o=1.5V, f_s=450kHz, L_o=1μH, R_L=1mΩ, L_{aux}=100nH, RL_{aux}=0.2mΩ, RQ_{aux}=30mΩ, V_{diode}=0.32V, T_{fall}=2ns)

Although the total loss of the CAC is around 4.5W under 20A load current, the activation interval is only under unloading transient condition for couples of micro-seconds. As a result, the thermal issue will not be a big problem for this implementation.

The switching losses are simulated under different values of step unloading transients (from 10A to 20A) as shown in Figure 12. Compared to n=13 case, when the number of auxiliary switching cycles n equals 9, the overshoot is only higher by 1mV (see Figure 6) but the switching frequency f_{aux} and loss Psw_Qaux are lower by 1/3. So finally, the auxiliary inductance L_{aux} is chosen to be 100nH to achieve a good design, considering the trade-off between overshoot improvement and power losses.

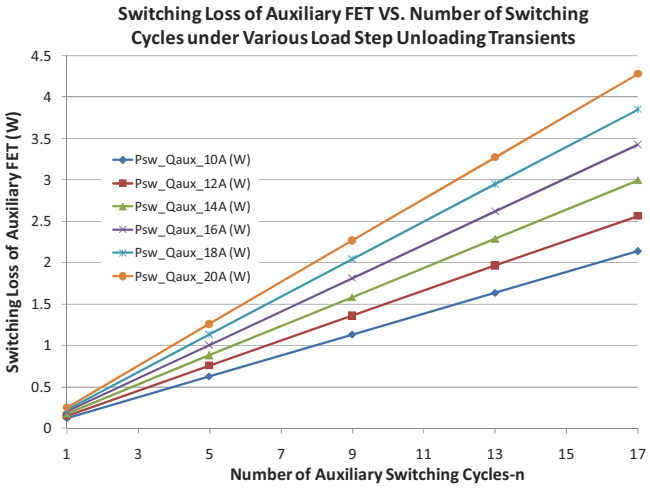

Figure 12 The plot of switching loss of the auxiliary FET versus the number n of auxiliary switching cycles under various load step unloading transients (the power circuit design parameters: V_o=V_{ref}=1.5V, f_s=450kHz, T_{fall}=2ns)

IV. Implementation of the Proposed Strategy Controlled Auxiliary Current

The diagram of the proposed BCM PCM strategy to control the CAC is shown in Figure 13. To set the peak current level of the auxiliary current, the load step value is required to be sensed/calculated. The ac component of the capacitor current during load transient is an alternative representation of the load step ΔI_o. So the capacitor current can be rebuilt by active filtering the output voltage (considering ESR in (14)) with an extra pole provided by C_f to attenuate the switching noise.

$$C_{1C} \cdot R_{1C} = \left(\frac{C_o}{k} \right) \cdot \left(ESR \cdot k \right) = C_o \cdot ESR \quad (14)$$

The output of the capacitor current sensor i_{Csen}, in relation to the actual capacitor current i_C is equated in (15).

$$i_{Csen} = \frac{R_{2C}}{k} i_C \quad (15)$$

Also, an improved capacitor current sensing circuit [14] can be applied in this implementation.

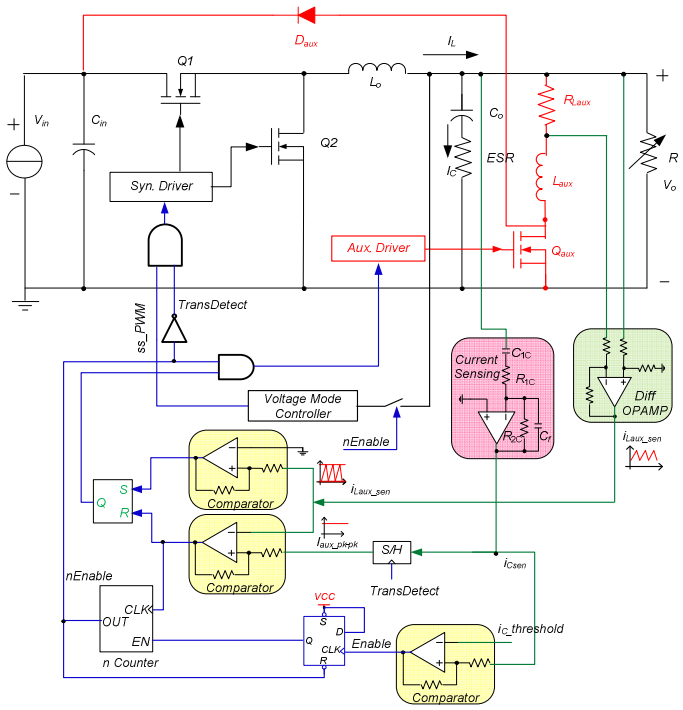

Figure 13 Hardware implementation of the proposed BCM PCM CAC

The *nCounter* (for counting the cycles of switching) generates the *TransDetect* signal to hold the $I_{aux\_pk\text{-}pk}$ value. A differential OPAMP amplifies the voltage across the current sensing resistor R_{Laux} to equalize the auxiliary current i_{aux}, which is compared with $I_{aux\_pk\text{-}pk}$ and *GND*. And an SR flip-flop is used to create the PWM signal to the auxiliary driver for switching Q_{aux} and implement the BCM operation. When the *nCounter* reaches *n* (that is, the desired number of auxiliary switching cycles), the *nEnable* (*OUT*) signal of *nCounter* will 1) deactivate the auxiliary current; 2)reset the *EN* signal; and 3)generate the CBC PWM signal for Buck converter.

V. Simulation and Experimental Verifications

In order to verify the functionalities of the proposed control strategy, a Buck converter with/without CAC undergoing unloading transient condition is simulated. And the simulation results are shown in Figure 14 and Figure 15 for comparison between the normal CBC controller in [14] and the proposed control scheme with BCM PCM CAC during 10A unloading transient. The design parameters are listed as follows: V_{in}=12V, V_o=V_{ref}=1.5V, f_s=450kHz, L_o=1μH, R_L=1mΩ, C_o=200μF, *ESR*=0.1mΩ, *ESL*=100pH, L_{aux}=100nH, R_{Laux}=0.2mΩ, R_{Qaux}=30mΩ, V_{diode}=0.32V, T_{fall}=2ns and *n*=9 (using equation (5), V_{in}-V_o/V_{in}*L_o/L_{aux}=8.75). And the Type III compensator in the CBC controller is well-designed with 75 kHz bandwidth and 60° phase margin in [14].

In Figure 14, the previously discussed CBC control technology is employed for optimal response of the single phase Buck converter. The overshoot is 175mV with 13.6μs settling time under a 10A step-down load transient case.

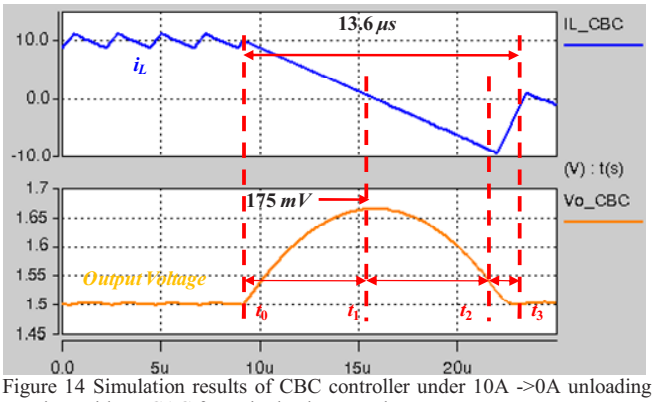

Figure 14 Simulation results of CBC controller under 10A ->0A unloading transient without CAC for a single phase Buck converter

Applying the proposed BCM PCM controlled CAC, the output voltage overshoot is reduced to 45mV and the settling time is reduced to 6.6μs, compared to the CBC controlled Buck converter without CAC. In other words, the overshoot and the settling time are improved by 74.2% and 51.5%, separately.

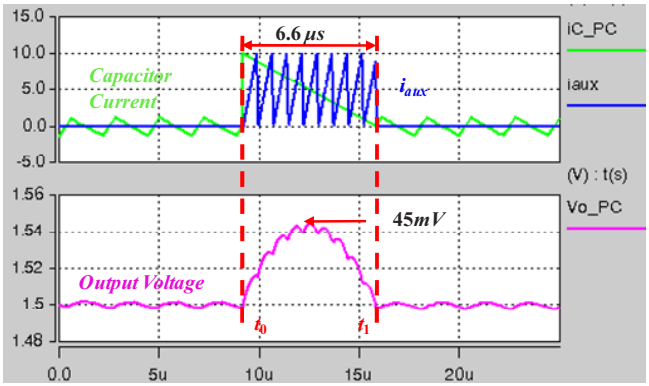

Figure 15 Simulation results of CBC controller under 10 A ->0 A unloading transient with proposed CAC for a single phase Buck converter

A Buck converter with 12V input and 1.5V output prototype is built with CAC using the same parameters in the simulation. Experimental results are shown in Figure 16 and Figure 17, under the unloading transient between full load (10A) and no load. Using the proposed BCM PCM CAC, the overshoot is decreased from 180mV to 45mV (a reduction by 75.0%) and the settling time is shortened from 13.6μs to 6.3μs (a reduction of 54%), compared with the optimal response provided by an analog CBC controller without CAC (discussed in [14]). And the number of switching is predictable using (11) and in the experiment the rounded off number *n* is 9.

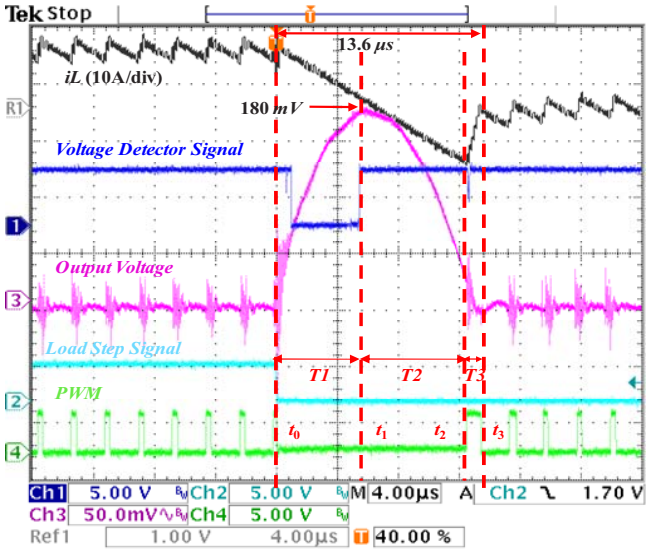

Figure 16 Experimental results of analog CBC controller under 10A ->0A unloading transient without CAC

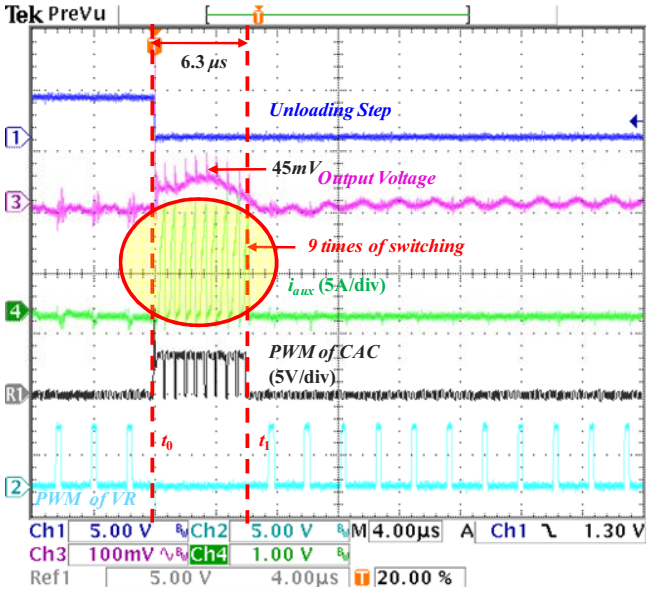

Figure 17 Experimental results of the proposed BCM PCM controller under 10A ->0A unloading transient with CAC

VI. Conclusions

In this paper, a practical auxiliary circuit control strategy is presented to improve unloading transient performance, which has the following unique advantages: 1) further voltage overshoot reduction; 2) predictable auxiliary switching based on the main-auxiliary inductance ratio; 3) the auxiliary circuit operating at relatively low frequency to reduce the switching loss and 4) minimizing the settling time of unloading response based on charge balance principles. The power loss analysis and output voltage overshoot estimation are made in this digest as design guidelines. To meet the maximum overshoot requirement, the output capacitance can be decreased from 630μF to 170μF. Through simulation and experimental results, under 10A unloading transient, it demonstrates that the proposed control strategy reduces the overshoot by 75% and shortens the settling time by 54%.

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