Adaptive Discontinuous Current Source Driver to Achieve Switching Loss Reduction for MHz PFC Boost Converters*

Pengcheng Xu, Zhiliang Zhang, *Member*, *IEEE*
Jiangsu Key Laboratory of New Energy Generation and Power Conversion
Nanjing University of Aeronautics and Astronautics
Nanjing, Jiangsu, P.R.China
{xupengcheng, zlzhang}@nuaa.edu.cn

Yan-Fei Liu, *Senior, Member IEEE* and P.C. Sen, *Life Fellow IEEE*
Department of Electrical and Computer Engineering
Queen's University, Kingston, Ontario, Canada, K7L 3N6
yanfei.liu@queensu.ca and senp@post.queensu.ca

***Abstract* – Adaptive control concept for the discontinuous Current Source Drivers (CSDs) is proposed for MHz Power Factor Correction (PFC) boost converters. Compared to the continuous CSDs, the discontinuous CSDs have lower circulating current and less conduction loss. Therefore, the discontinuous CSDs are able to use higher gate drive current to reduce the switching loss further. Using different pre-charge time to build Current Source (CS) inductor currents based on different load conditions, the gate drive currents can be achieved adaptively to the load currents, so that the efficiency of the PFC converter can be improved in a wide operation range. The CS inductor of the discontinuous CSD is as low as 120nH. This reduces the board space of the main MOSFET driver part. An 110V input, 380V/ 200W output, 1MHz PFC boost converter with the proposed adaptive discontinuous CSD was built to verify the advantages. With the discontinuous CSD, at 50% load, an efficiency improvement of 5.1% is achieved over the conventional voltage source driver (VSD), and at full load, an efficiency improvement of 4.8% is achieved. The measured PF values are all above 99% and complying with the industrial requirements.**

***Index Terms*: Current Source Driver (CSD), Switching Loss, Power Factor Correction (PFC), Adaptive Control**

I. INTRODUCTION

With the development of the information technologies, the distributed power system (DPS) requires higher power density in the future. As the first stage of the DPS, in order to improve the power density of power factor correction (PFC) converters, pushing the switching frequency higher is the most direct method [1]-[2]. For a Continuous Conduction Mode (CCM) PFC converter, increasing the switching frequency can dramatically reduce the volume of the boost inductor, while the EMI filter size can be reduced if the switching frequency is higher than 400kHz.

Since the switching loss is proportional to the switching frequency, higher switching frequency means higher switching loss. Loss breakdown of the MHz PFC shows that the major loss of the PFC converter is the high frequency switching loss [3]. Limited by the switching loss, most of today's PFC converters are running at about 100KHz switching frequency. Therefore, for high frequency PFC converter, how to reduce the switching loss and improve the efficiency is an interesting topic.

Recently, Current Source Drivers (CSDs) have been proposed to reduce the switching loss and gate drive loss in MHz switching frequency in DC-DC converters [4]-[8]. The basic idea of the CSD circuits is to build constant current sources to charge and discharge the power MOSFET gate capacitance so that the fast switching speed and the reduced switching loss can be achieved [9]-[11].

With certain load, when the input line voltage is low, the continuous CSD solution for the boost PFC converters proposed in [8] can achieve adaptive drive current inherently in some range of the operation of the converter. But, essentially, the gate drive current of the continuous CSD is adaptive to the duty cycle *D*, which is changed with the sine input line voltage. If the load changes, the input current increases, and the switching loss increases accordingly, however, the continuous CSD can not achieve adaptive current to different load conditions.

In this paper, in order to reduce the switching loss of the high frequency PFC converter, the discontinuous CSD is investigated for MHz switching frequency PFC. The key to this type of CSD is to control of the drive switches to generate discontinuous inductor current waveforms enabling the peak portion of the current to be used to charge/discharge the power MOSFET as a nearly constant current source. Compared to the continuous CSD, the CS inductor value of the discontinuous CSD is reduced much, which is only about 100nH. Therefore, an air core inductor can be used in the drive circuit.

* This work was supported by Natural Science Foundation of China (51007036), Delta Power Electronics Science and Education Development Fund, Aviation Science Fund, The Project of University Excellent Discipline, Jiangsu Province and NUAA Research Funding, No. NS2010087 and NJ2010016.

Generally speaking, when a switching power converter is in full load condition, the switching loss and the conduction loss of the MOSFET become the dominant losses. On the contrary, the drive loss weighs a big proportion of the total loss when the converter is in light load condition. Both of these situations will lead to the lower efficiency. Therefore it is important to find an optimized trade-off point among the switching loss, the conduction loss and the driver loss. However, for the traditional CSD technology, the optimal drive current is fixed and may not be able to achieve optimal loss reduction effect in different load conditions. In this paper, using different pre-charge time over the CS inductor, the discontinuous CSD can achieve adaptive gate drive current in different load conditions, and the efficiency of the MHz PFC can be improved in a wide load range.

II. Proposed Adaptive Control for Discontinuous Current Source Drivers

A. Description of the discontinuous CSD circuit

The topology of the discontinuous CSD is illustrated in Fig.1. It consists of four drive switches, S_1-S_4 and a small resonant inductor L_r. S_1-S_4 are controlled to allow the inductor current to be discontinuous and the MOSFET M can be turned on or off beginning by nearly constant drive current.

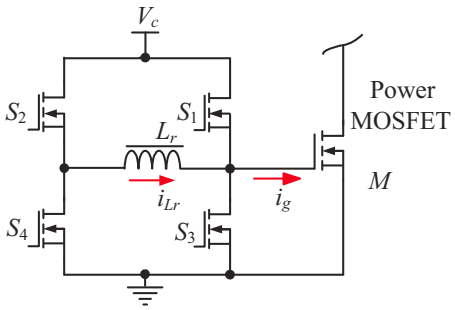


Fig.1 Proposed CSD Solution for PFC applications

The key waveforms are illustrated in Fig.2. The inductor current i_{Lr} is discontinuous to minimize conduction loss compared to the continuous circulating current, where t_{10} is the pre-charge time and t_{21} is the turn on time.

According to Fig.2, the gate drive current I_{G_on} is approximated as:

$$I_{G\_on} = I_{G\_off} = i_{Lr}(t_1) = \frac{V_c T_{pre}}{L_r} \qquad (1)$$

The control sequence of the four drive switches S_1-S_2-S_3-S_4, along with the CS inductor current i_{Lr}, gate drive current i_g and the gate-to-source voltage of the power MOSFET M are illustrated in Fig.3. The key waveforms to note are: 1) the CS inductor current i_{Lr} is discontinuous to minimize the conduction loss of the CSD; 2) the gate drive current i_g is nearly constant (in comparison to the conventional voltage source drivers) to reduce the turn on and off switching time significantly. The *TD*1 and *TD*2 are the two delayed waveforms of the input *PWM*. In order to achieve discontinuous inductor current, the key to this CSD is to control of the driver switches to generate discontinuous inductor current waveforms enabling the peak portion of the inductor current to be used to charge and discharge the power MOSFET gate capacitance as a nearly constant current source.

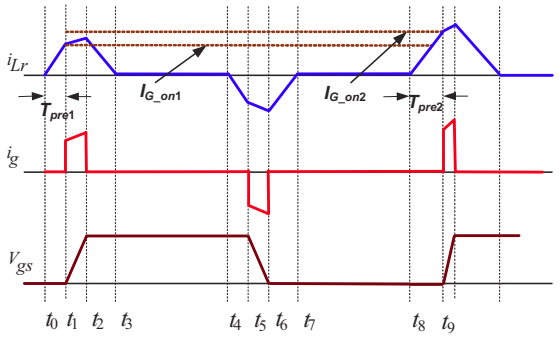


Fig.2 Key waveforms of the discontinuous CSD

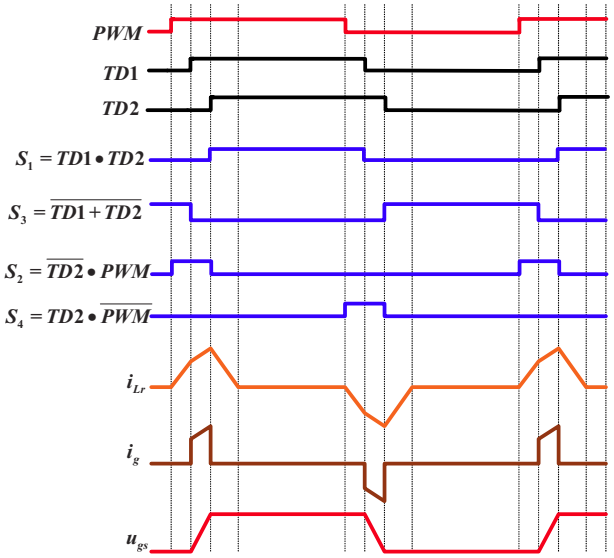


Fig.3 The control sequence of the four drive switches S_1-S_4, the CS inductor current i_{Lr}, gate drive current i_g and gate-to-source voltage of the power MOSFET

The CSD has two drive switches to ensure low impedance path through the gate terminal to the drive voltage or the ground, which provides good noise immunity of the power MOSFET against *Cdv*/*dt* problem, and the four drive switches of the discontinuous CSD can operate correctly for duty cycle from 0%-100%, which is suitable for the PFC applications.

B. Adaptive control concept for the discontinuous CSD

There is a design tradeoff for the discontinuous CSD between speed and driver loss. Faster switching speed requires higher driver current, which increases the conduction loss in the driver. In order to find the optimized gate drive current, the objective function of the gate drive current I_{G_on} is established by adding the switching loss and the CSD circuit loss together as:

$$P\left(I_{G\_on}\right)=P_{CSD\_sw}\left(I_{G\_on}\right)+P_{CSD}\left(I_{G\_on}\right) \qquad (2)$$

where $P_{CSD\_sw}(I_{G\_on})$ is the switching loss, and $P_{CSD}(I_{G\_on})$ is the CSD circuit loss. Compared to the continuous CSD solutions [12], the discontinuous CSD has smaller conduction and no circulating current, so the gate drive current of the discontinuous CSDs can be chosen higher to further reduce the switching loss.

1) Fixed load current conditions

With certain load, when the input line voltage is low, the continuous CSD solution for the boost PFC converters proposed in [12] can achieve adaptive drive current inherently in some range of the operation of the converter. Fig.4 shows that, from t_0 to t_1, the gate drive current of the continuous CSD is adaptive to the switching current.

When the input voltage increase, the input current becomes higher accordingly, the switching loss of the power MOSFET becomes more. From Fig.4, it can be seen that the continuous CSD can achieve adaptive drive current to the input current, but when the load current changes after t_1, the average of the input line current increased, the gate drive current of the continuous CSD is kept constant and is not depending on the load current any more,

In addition, the major concern is that the continuous current operation results in high circulating loss in the drive circuit. This actually makes stronger drive current difficult to be chosen to reduce the switching loss further.

.2) Different load current conditions

From (1) and Fig.2, it is interesting to notice that the drive current of the discontinuous CSD is proportional to the pre-charge time, which is normally fixed when the control circuit is designed. So the idea is that if the pre-charge time can be varied according to different conditions, then adaptive drive current can be realized. The benefit is that the switching time and the switching loss can be optimized with different load condition, while the drive circuit circulating loss is also minimized at the same time.

Fig.4 shows that when during t_1 and t_2, the load current increases, the peak current of the boost inductor will also increase, the dotted line shows that the peak gate drive current of the continuous CSD keeps unchanged, which is not able to be adaptive to load current. Fig.5 illustrated the adaptive solution of the discontinuous CSD for PFC applications.

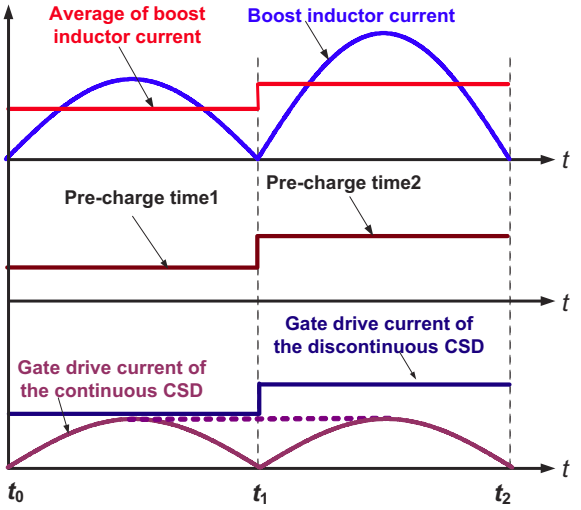


Fig.4 Key waveforms of the adaptive solution for PFC applications

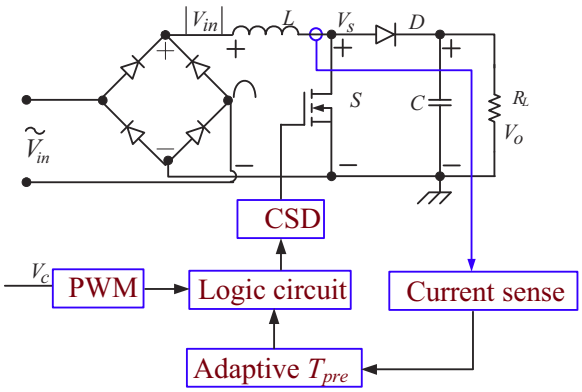


Fig.5 The proposed adaptive solutions for PFC boost converter

By sensing average of the boost inductor current, we can adjust the pre-charge time to change the gate drive current of the discontinuous CSD, so that the drive current can be adaptive to the load current. Fig.4 show that when the load current increases between t_1 and t_2, the pre-charge time increased to be adaptive to the load current, so the discontinuous CSD could provide high gate current to further reduce the switching loss. By using the discontinuous CSD, the efficiency of the PFC converter can keep on high at different load conditions.

III. Benefits Of Adaptive Discontinuous Current Source Driver For PFC

A. *Adaptive gate drive current for MHz PFC converters*

For the CSD technology, high drive currents lead to lower switching loss. Strong drive current is desired to reduce the switching loss further when the power MOSFET carries higher current. Nevertheless, higher drive currents also result

in higher circulating loss. However, the present CSD circuits normally use constant drive currents and voltages. For the power MOSFETs, stronger drive currents means fast switching speed and lower switching loss, but results in higher drive circuit loss. High gate drive currents and voltages are beneficial to the normal load conditions, but hurt light load efficiency. This leads to a tradeoff between the switching loss reduction and gate drive loss. The constant drive currents and voltages limit the optimal operating conditions of the loss reduction. To achieve high efficiency curves in a wide load range becomes an interesting topic for the MHz converters.

The linear regulator was proposed for continuous CSD to achieve adaptive voltage in different load conditions [13]. Fig.6 gives the basic circuit diagram. However, adding the linear regulator to continuous CSD, which increased the complexity of the circuit, also will introduce the additional loss of the linear regulator.

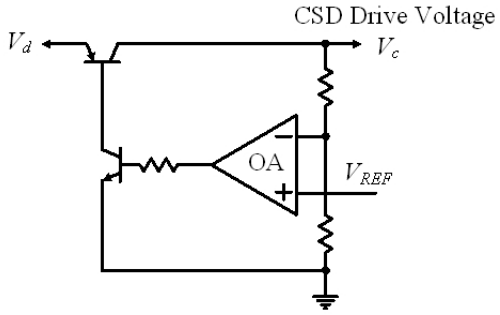


Fig.6 Linear regulator achieving adaptive voltage in different load conditions

In this paper, by sensing the average value of the boost inductor current to change the pre-charge time, the adaptive drive current solutions are proposed for the discontinuous CSDs, so the efficiency of the MHz PFC converter can be improved at different load conditions.

The proposed method to achieve adaptive current using the pre-charge time for discontinuous CSD has the advantages is that no additional loss involved and easy to be implemented with digital control method. Another advantage the pre-charge time for the turn on transition and turn off transition could be chosen respectively since the turn off loss is usually higher than the turn on loss as far as the parasitic inductances are concerned.

B. Reduction of the drive circuit loss

Both the continuous CSDs and discontinuous CSDs use the inductor as a current source. The drive energy stored in the inductance can be recovered to the driver supply voltage rail.

The drive loss of the CSD includes: 1) the resistive loss caused by the impedance of the driver switches, P_{cond}, 2) the loss of the current source inductor L_r, P_{ind}; 3) the resistive loss caused by the internal gate mesh resistance of the power MOSFETs, P_{RG}; 4) gate drive loss of drive switches, P_{gate}.

Therefore, the total loss CSD is

$$P_{Drive} = P_{cond} + P_{ind} + P_{RG} + P_{gate} \tag{3}$$

Fig.7 shows the drive loss comparison between the continuous and discontinuous at the switching frequency of 1 MHz. The components used are as follows: drive switches S_1-S_4: FDN335N; CS inductors: L_r=100nH (1812SMS) for the discontinuous, and L_r=1μH (DO3316P) for the continuous.

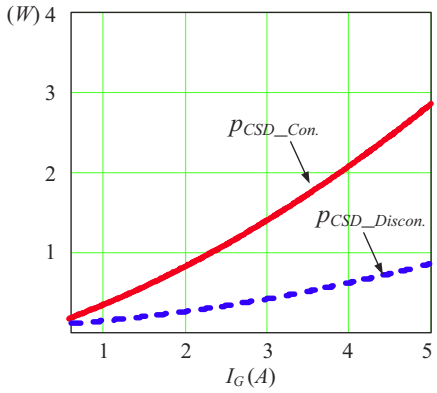


Fig.7 Drive loss comparison between the continuous CSD and discontinuous CSD at 1MHz with different gate currents

It is observed that for the same gate drive current I_G, the discontinuous CSD has much lower drive loss than the continuous one, since the continuous current is a triangle waveform with larger RMS value and thus higher conduction loss. So, compared to the continuous CSD, the gate drive current of the discontinuous CSD can be designed higher to reduce the switching loss more.

C. High power density and high efficiency of the MHz PFC stage

Compared with traditional 100KHz PFC converters, the 1MHz PFC with the adaptive CSD will leads to the 90% reduction of the inductor. Owing to the constant drive current of the proposed CSD solution, the switching loss of the MHz PFC converter can be greatly reduced, so the MHz PFC with the CSD can achieve high efficiency over the conventional VSD, which leads to the MHz operation of the PFC.

More importantly, the MHz PFC can also achieve great size reduction of the EMI filter. Therefore, with the discontinuous CSD, the MHz PFC converter can achieve much higher power density.

IV. Experimental Results and Discussion

An 110V input, 380V/200W output and 1MHz boost PFC

converter was built to verify the advantages. Fig.8 gives the photo of the prototype. The specifications are as follows: boost inductor L=100μH; output capacitance C=220μF; the CS inductor L_r=120nH; the gate driver voltage V_c=12V.

The adaptive discontinuous CSD was built using discrete components. FDN335N n-channel MOSFETs were used for the four switches S_1-S_4. A Coilcraft 1812SMS air core inductor (120nH) was used for the CS inductor, L_r. The Fairchild NC7S series logic ICs are used for the timing logic implementation.

Fig.9 shows the input line voltage and current of the power stage. It is observed that the input line current is the sinusoidal waveform, which is able to catch up with the input line voltage.

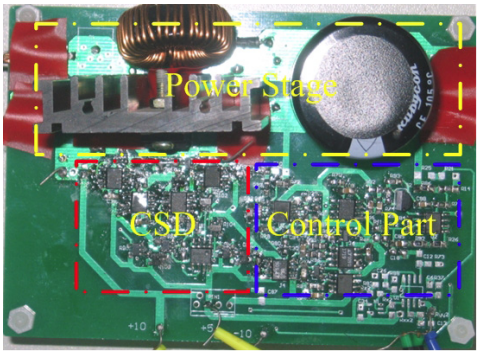


Fig.8 Photo of the power stage and CSD

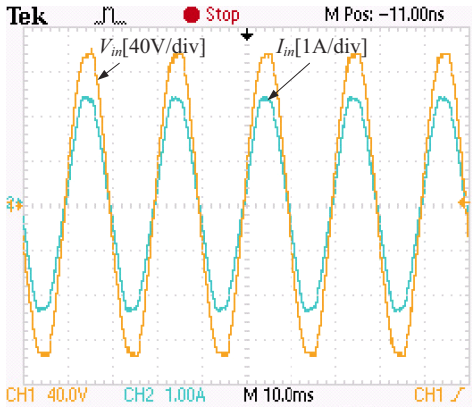


Fig.9 The input line voltage and current of the power stage

The measured PF values are given in Table I according to different loads. It is observed that the PF values are all above 0.99, which are compatible to the industrial standards. The functionality of the power factor correction is realized with the discontinuous CSD.

Fig.10 shows the CS inductor current i_{Lr} and the gate-to-source voltage u_{GS} to demonstrate the fast switching speed. It is observed that the gate drive current i_{Lr} is constant in each switching cycle.

TABLE Ⅰ
MEASURED PF VALUES AT DIFFERENT LOADS UNDER 100VAC.

Load Conditions (W)	25% (50W)	50% (100W)	75% (150W)	100% (200W)
PF	0.992	0.994	0.998	0.999

To demonstrate the proposed adaptive current function, the detailed waveforms of turn on transition with different pre-charge time are provided in Fig.11. The two control signal for S_3 and S_2 are at the top, and the bottom waveform is the CS inductor current i_{Lr}. The turn on of the switch S_2 initiates to pre-charge the CS inductor as labeled as pre-charge interval, during which, the CS inductor current ramps up. After the pre-charge time, the CS current is nearly constant to drive the power MOSFET. It is observed from Fig.11 (a), the pre-charge time is 12ns, and the peak drive current is 1.2A. Fig.11 (b) show that when the pre-charge time increased to 25ns, the peak drive current also increased to 2.5A adaptively.

For the turn off transition, the detailed waveforms with different pre-charge time are provided in Fig.12, which is similar to the situation of turn on transition.

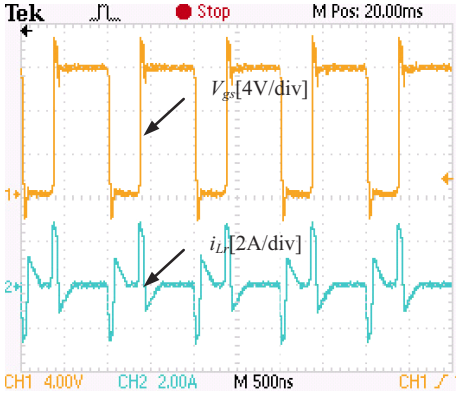
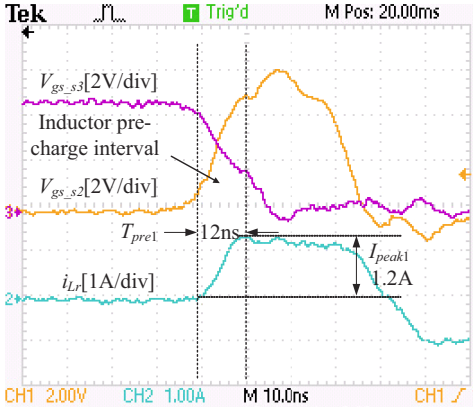
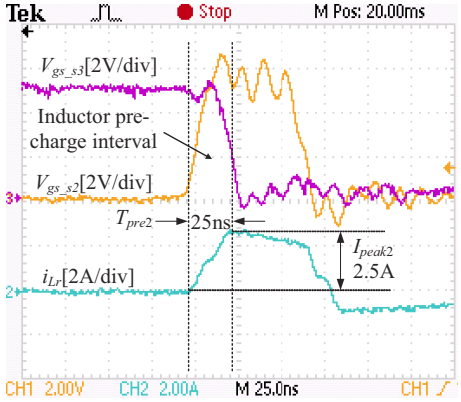


Fig.10 Gate drive voltage and CS inductor current

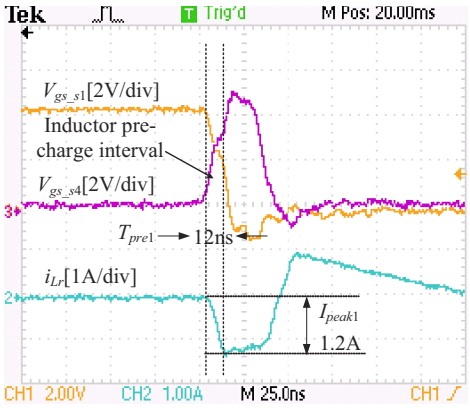


(a) Turn on transition with pre-charge time1

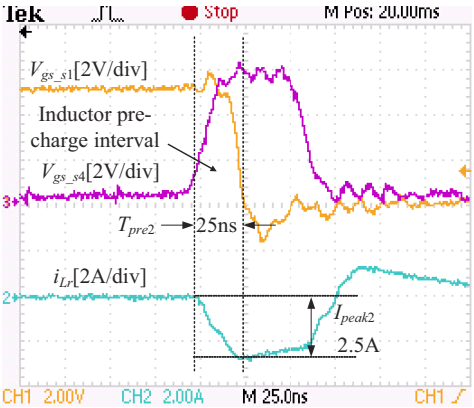


(b) Turn on transition with pre-charge time2

Fig.11 Detailed turn on waveforms with different pre-charge time, top: gate drive signals for S_3 and S_2, bottom: CS inductor current i_{Lr}.



(a) Turn off transition with pre-charge time1



(b) Turn off transition with pre-charge time2

Fig.12 Detailed turn off waveforms with different pre-charge time, top: gate drive signals for S_3 and S_2, bottom: CS inductor current i_{Lr}.

Fig.13 shows the measured efficiency comparison of the conventional VSD and CSD with different loads. The efficiencies at 25%, 50%, 75%, and 100% loads for 100VAC are provided. It is noted that the discontinuous CSD can improve the efficiency of the boost PFC converter over the conventional VSD in all load range. At 50% of the load, an efficiency improvement of 5.1% is achieved, and at full load, an efficiency improvement of 4.8% is achieved over the VSD.

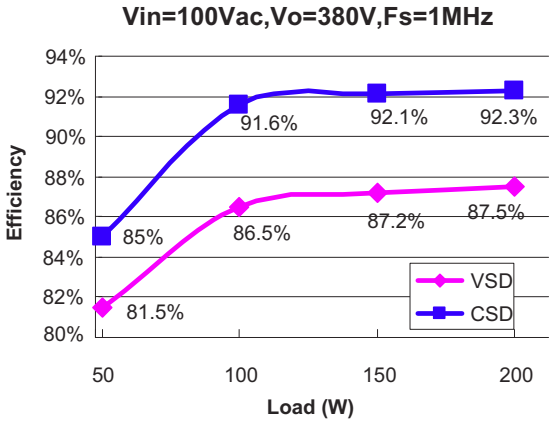


Fig.13 Efficiency comparison between the VSD and CSD with different loads (V_{in}=100VAC, V_o=380V, f_s=1MHz)

V. Conclusion

The discontinuous CSD is investigated for the MHz PFC boost converter in this paper. Using the pre-charge time, the adaptive drive current can be achieved in a wide line input voltage and load current. This helps to improve the PFC stage efficiency in a wide operation condition. In addition, this proposed adaptive control method is well compatible with the digital control, while no additional circuitry is needed to implement the adaptive drive current compared to the continuous CSDs. The experimental results verified the proposed solution. With 100VAC input, with the discontinuous CSD, at 50% load, an efficiency improvement of 5.1% can be achieved over the VSD, and at full load, an efficiency improvement of 4.8% can be achieved over VSD. The measured PF values are all above 99% and are complying with the industrial requirements.

References

[1] C. Wang, M. Xu, B. Lu and F. C. Lee, "New architecture for MHz switching frequency PFC," in Proc. IEEE APEC, 2007, pp. 179-185.

[2] Nishimura. K, Yokoyama. N, Hirachi. K, Soon-Kurl. Kwon and Nakaoka. M, "Dual high-frequency chopper-based single stage PFC converter with output DC high quality," in Proc. IEEE ECCE, 2009.

[3] P. O. Jeannin, D. Frey, J.C. Podvin, J. P. Ferrieux, J. Barbaroux, J. L. Schanen, B. Rivet, "1 MHz power factor correction boost converter with SiC Schottky diode," in Proc. IEEE IAS, 2004, pp. 1267-1272.

[4] W. Eberle, Z. Zhang, Y. F. Liu and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz," IEEE Trans. on Power Electronics, Vol. 23, No. 2, pp. 678 - 691, Mar. 2008.

[5] Z. Zhang, J. Zhen, Y. F. Liu and P. C. Sen, "Discontinuous current source drivers for high frequency power MOSFETs," IEEE Trans. Power Electron., Vol. 25, No. 7, Jul. 2010, pp. 1863-1876.

[6] X. Zhou, Z. Liang and A. Huang, "A new resonant gate driver for switching loss reduction o f high side switch in buck converter," in Proc. IEEE APEC, 2010, pp. 1477-1481.

[7] Q. Li and P. Wolfs, "The power loss optimization of a current fed

ZVS two-inductor boost converter with a resonant transition gate drive," IEEE Trans. Power Electron., Vol. 21, No. 5, Sep. 2006, pp. 1253 -1263.

[8] Y. Ren, M. Xu, Y. Meng and F. C. Lee, "12V VR efficiency improvement based on two-stage approach and a novel gate driver," in Proc. IEEE PESC, 2005, pp. 2635-2641.

[9] Z. Yang, S. Ye, and Y. F. Liu, "New dual channel resonant gate drive circuit for low gate drive loss and low switching loss", IEEE Trans. on Power Electron, Vol. 23, No. 3, pp. 1574-1583, May 2008.

[10] Z. Zhang, J. Fu, Y. F. Liu and P. C. Sen, "A new discontinuous current-source driver for high frequency power MOSFETs," in Proc. IEEE ECCE 2009, pp. 1655-1662.

[11] Z. Zhang, W. Eberle, P. Lin, Y. F. Liu and P. C. Sen, "A 1-MHz high efficiency 12V buck voltage regulator with a new current-source gate driver," IEEE Trans. Power Electron., Vol. 23, No. 6, Nov. 2008, pp. 2817-2827.

[12] Z. Z. Zhang, P. C. Xu, and Y. F. Liu, "Adaptive current source drivers for MHz power factor correction", in Proc. IEEE APEC, 2011.

[13] Z. Z. Zhang, P. C. Xu, Y. F. Liu and P. C. Sen, "Adaptive Current Source Drivers for Efficiency Optimization of High Frequency Synchronous Buck Converters" in Proc. IEEE ECCE, 2011.