MHz Power Factor Correction with Adaptive Current Source Drivers*

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***Abstract*— Adaptive Current Source Drivers (CSDs) are proposed for MHz Power Factor Correction (PFC) applications. Due to the fast duty cycle change, the half-bridge (HB) CSD topology can hardly be accepted for high frequency PFC Applications. To solve the problem, the full-bridge (FB) CSD topology is used instead. It is interesting to note that the FB CSD with the continuous inductor current can actually achieve adaptive drive currents inherently depending on the drain currents in the main power MOSFETs to achieve optimal design. The loss analysis and design procedure are also presented for the FB CSD for the boot PFC converter. Due to the fast switching speed and the switching loss reduction, an efficiency improvement of 3.2% can be achieved to a 1MHz/ 300W boost PFC converter with the line input voltage of 110VAC. The analysis and experimental results verified the conclusion.**

Index Terms: Current Source Driver (CSD), power MOSFET, MHz switching frequency, Power Factor Correct (PFC), Boost converter.

I. INTRODUCTION

With the development of the information technologies, the distributed power system (DPS) requires higher power density in the future. As the first stage of the DPS, in order to improve the power density of power factor correction (PFC) converters, pushing the switching frequency higher is the most direct method. Recently, Current Source Drivers (CSDs) have been proposed to reduce the switching losses and gate drive loss in MHz switching frequency Voltage Regulators (VRs) for microprocessors. The idea of the CSD circuits is to build current sources to charge and discharge the power MOSFET gate capacitance so that the fast switching speed and the reduced switching loss can be achieved. At the same time, the energy stored in the gate capacitance of the MOSFETs can be recovered, similarly to the Resonant Gate Drivers (RGDs) [1]-[3].

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Presently, most of the work done with the CSDs is to investigate their applications in DC-DC converters [5]-[9], where the duty cycle normally has a steady state value. In the AC-DC applications, Power Factor Correction (PFC) technique is widely used. Different from DC-DC converters, the duty cycle of the PFC converters has wide operation range and fast change. In order to achieve high power density, the passive components of capacitors and inductors need to be shrunk. In the PFC stage, the inductance can be reduced when the switching frequency increases. Furthermore, the EMI filter stage can also be further reduced when the switching frequency increases over 400kHz [10]-[11]. However, today's PFC stage is still running at 100-200kHz. The major concern of increasing the switching frequency in PFC is the excessive frequency-dependent losses, including the switching loss, the gate drive loss and the reverse recovery loss of the diode, where the switching loss is the major loss in MHz PFC converter.

In this paper, the CSDs for MHz PFC applications are investigated. Normally, high gate drive currents lead to faster switching speed and thus lower switching loss. It would be of great benefit if the drive current could be adaptive to the switching current, so that when the switch carries more current, the driver would provide stronger gate drive current to reduce the switching loss. Compared to the previous CSDs, the proposed solution can actually achieve adaptive drive currents inherently depending on the drain currents in the main power MOSFETs to achieve optimal design.

II. ANALYSIS OF CSD CIRUCITS AND THE PROPOSED ADAPTIVE CSD FOR MHZ PFC

A. Analysis of the Half-Bridge CSD Crcuits

The basic CSD with the continuous inductor current is half-bridge (HB) structure as shown in Fig. 1

It consists of two drive MOSFETs S_1 and S_2. V_c is the drive voltage, L_r is the current source (CS) inductor and C_b is the

blocking capacitor. The voltage across the blocking capacitor C_b equals $v_{Cb} = (1-D)\cdot V_c$, which changes with the duty cycle D. This drawback limits the HB CSD application in the PFC converters when the duty cycle is modulated with the line voltage. Fig. 2 shows the simulated waveforms when this CSD is used in the boost PFC converter. It is observed that the voltage over the blocking capacitor v_{cb} changes with the duty cycle and this also leads to the drive current i_{Lr} oscillation.

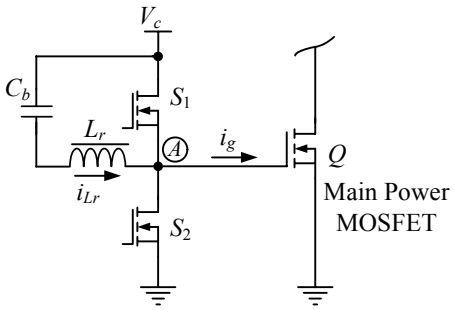

Fig. 1 HB CSD topology

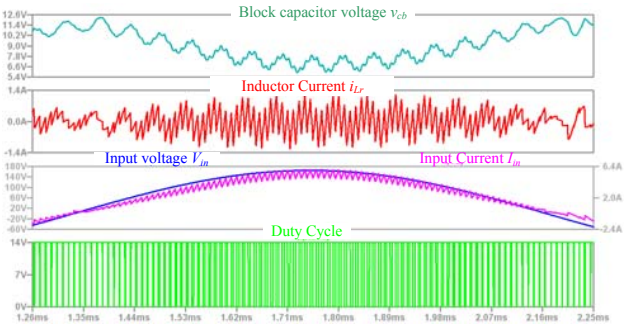

Fig. 2 Key waveforms of the boost PFC converter with the HB CSD

Therefore, the CSD solution for the PFC converters should have no blocking capacitor.

B. The Proposed CSD Circuit for Boost PFC Converter

Fig. 3 shows the proposed CSD solution for the PFC application. Fig. 4 shows the key waveforms. Fig. 5 shows the single phase boost PFC stage with the CSD. Compared to Fig. 1, S_2 and S_4 are used to remove the blocking capacitor, which forms a full bridge CSD topology. Since there is no blocking capacitor, the proposed CSD can be suitable for the PFC application, where the duty cycle keeps changing.

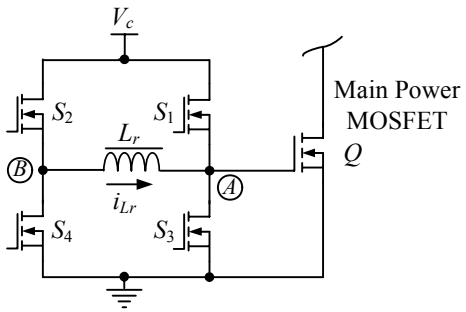

Fig. 3 Proposed CSD Solution for PFC applications

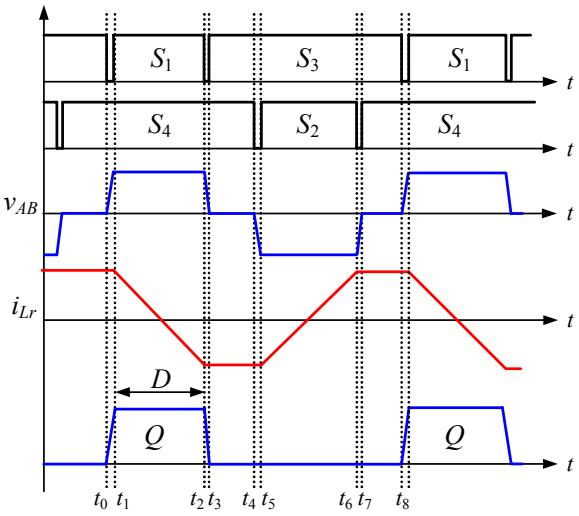

Fig. 4 Key waveforms

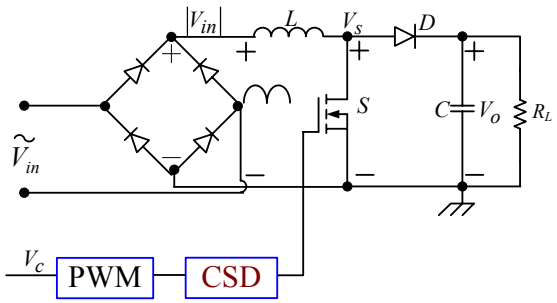

Fig. 5 Proposed CSD solution for the boost PFC converter

According to the voltage applied to the CS inductor, the peak inductor current I_{Lr_pk} is:

$$I_{Lr\_pk} = \frac{V_c \cdot D}{2 \cdot L_r \cdot f_s} \tag{1}$$

$$I_{Lr\_pk} = \frac{V_c \cdot (1-D)}{2 \cdot L_r \cdot f_s} \tag{2}$$

Fig. 6 shows the peak current value of the CS inductor, which is used to drive the main power MOSFET. It is observed that the drive current changes with the duty cycle and the value can be chosen when the CS inductor value is decided. It should be also noted that the operation region of adaptive drive current is limited by the duty cycle range.

For a boost PFC converter with 120V input and 380V output, the minimum modulated duty cycle is 0.55. According to Fig. 6, when D>0.5, when with duty cycle decrease, the drive current begins to increase adaptively and this will drive the MOSFET faster and achieve lower switching loss. This means the drive current is able to behavior adaptively according to the MOSFET switching current.

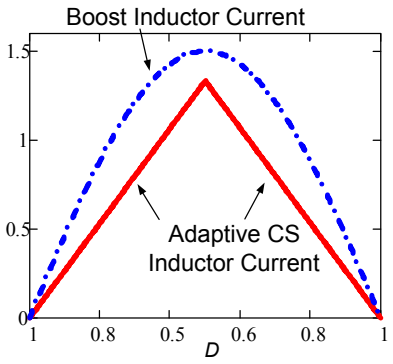

Fig. 6 Inductor current with the duty cycle

As seen from Fig. 4, S_1&S_3 and S_2&S_4 are complementarily controlled, which is similar to the control of the synchronous buck converters. Therefore, anther advantage of this solution is that the commercial off shelf components can be directly used instead of using discrete ones in other CSD circuits [12]-[13].

III. Loss Analysis Of The Proposed Adaptive CSD For Boost PFC Converter

The efficiency of the PFC stage is determined by the power losses of the input diode bridge, the boost inductor, the main switch, and the rectifier diode. The active switch and boost diode are under hard switching conditions with the fixed switching frequency operation. Therefore, the dominant losses are caused by the switching losses in the active switch and boost diode. The loss analysis of a boost PFC converter with the proposed CSD is presented as follows:

1) *The loss of the power MOSFET*

The losses of the power switch include the conduction loss and switching loss. For a single phase PFC converter, the current which flows through the main switch has a half sinusoidal shape. The switching loss P_{sw} and conduction loss P_{cond} are (3) and (4) respectively.

$$P_{sw} = \frac{2\int_0^{\frac{T_{line}}{2}} Kf_s V_o I_{L-pk} \sin(\omega_L t)(T_r + T_f)dt}{T_{line}} \quad (3)$$

$$P_{cond} = \frac{2\int_0^{\frac{T_{line}}{2}} (I_{L-peak} \sin(\omega_L t))^2 R_{ds-on} D(t)dt}{T_{line}} \quad (4)$$

where $\omega_L = 2\pi \cdot f_L$, T_r and T_f are the rising time and the falling time of MOSFET respectively. I_{L_pk} is the peak of input boost inductor current. The constant K is typically between 1/6 and 1/2. T_{line} is line period and f_s is the switching frequency.

2) *The conduction loss of the boost diode*

The power losses of the boost diode include the forward conduction loss and the reverse recovery related switching loss. With the SiC diode, the reverse recovery is low, so the power loss of the diode is

$$P_{fd} = \frac{2\int_0^{\frac{T_{line}}{2}} I_{L-peak} \sin(\omega_L t) V_{f-fd}\left[1-d(t)\right]dt}{T_{line}} \quad (5)$$

where V_{f_fd} is the forward voltage drop of the boost diode.

3) *The conduction loss of the rectifier bridge*

The rectifier bridge has four rectifier diodes, the conduction loss of the rectifier bridge is

$$P_{rd} = \frac{4}{T_{line}} \int_0^{\frac{T_{line}}{2}} I_{L-peak} \sin(\omega_L t) V_{f-rd} dt \quad (6)$$

where V_{f_rd} is the forward voltage drop of the rectifier diodes.

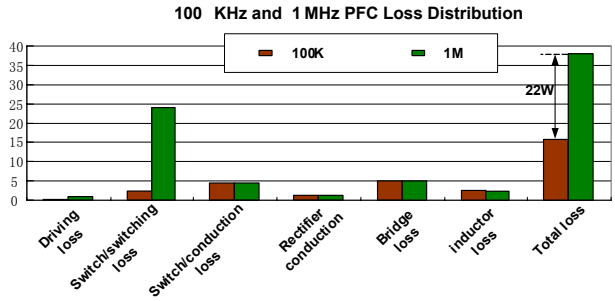

Fig. 7 Loss distribution of the boost PFC converter with 100KHz and 1MHz: V_{in}=110VAC, V_o=380V and P_o=300W

Fig. 7 shows the loss breakdown of the 300W boost PFC converter with 100kHz and 1MHz. For the boost converter, the 600V/11A CoolMOS™ SPA11N60 from Infineon and the SiC Schottky diode CSD06060 from CREE are used. The input line voltage is 110VAC and the output voltage is 380V.

From Fig. 7, it is observed that the switching loss is the dominant loss of the PFC while the switching frequency becomes 1MHz, which is as much as ten times of the switching loss in 100KHz. This results in poor efficiency when the boost PFC converter runs at 1MHz. The predicted efficiency of the 100KHz converter is 94.5%, while the efficiency of the 1MHz converter is only 89% in comparison.

In order to improve the efficiency, the proposed CSD is employed to reduce the switching loss of the converter. The total power losses of the CSD circuit are listed as below:

1) *The CS inductor loss*

$$P_{copper} = R_{ac} \cdot I_{LRMS}^2 \quad (7)$$

$$P_{ind} = P_{copper} + P_{core} \quad (8)$$

where I_{LRMS} is the RMS value of the CS inductor current, R_{ac} is the AC resistance of the inductor winding, P_{copper} is the copper loss and P_{core} is the core loss.

2) *The mesh resistance loss of the power MOSFET*

$$P_{RG} = 2 \cdot R_G \cdot I_{Lpeak}^2 \cdot t_{sw} \cdot f_s \quad (9)$$

where R_G is the internal gate mesh resistance, t_{sw} is the switching time and I_{Lpeak} is the peak value of the CS inductor current.

3) *The total conduction loss of S_1-S_4*

$$P_{cond} = 2 \cdot R_{DS(on)} \cdot I_{Lpeak}{}^2 \cdot \frac{4D-1}{3} \tag{10}$$

where $R_{DS(on)}$ is the on-resistor of the four switches.

4) The total gate drive loss of four switches

$$P_{Gate} = 4 \cdot Q_{g-s} \cdot V_{gs-s} \cdot f_s \tag{11}$$

where Q_{g_s} is the total gate charge of switch and V_{g_s} is the drive voltage of the switch.

From (8), (9), (10) and (11), the total loss of the CSD is

$$P_{drv} = P_{ind} + P_{RG} + P_{cond} + P_{Gate} \tag{12}$$

A. Loss Comparison with 110V Input

With the input voltage V_{in}=110V, output voltage V_o=380V, 1MHz/300W PFC converter, the drive voltage V_c is 12V, DS3316P-1uH is chosen for the CS inductor and the power MOSFET is SPA11N60.

With input voltage V_{in}=110V, output voltage V_o=380V, the duty cycle of the boost PFC converter is:

$$D(t) = 1 - \frac{V_{in}\left|\sin \omega_L t\right|}{V_o} \tag{13}$$

From (2), the gate drive current is given by:

$$i_g(t) = \frac{V_{CC}\left[1-D(t)\right]}{2 f_s L_r} = \frac{V_{CC} V_{in}\left|\sin \omega_L t\right|}{2 f_s L_r V_o} \tag{14}$$

As an ideal current source driver, the switching loss of the power MOSFET with CSD is

$$p_{sw-csd}(t) = \frac{1}{2} f_s V_o I_L(t)\left[T_{rcsd}(t) + T_{fcsd}(t)\right] \tag{15}$$

$$T_{rcsd}(t) = \frac{Q_{pl} - Q_{th} + Q_{gd}}{I_g(t)} \tag{16}$$

$$T_{fcsd}(t) = \frac{Q_{pl} - Q_{th} + Q_{gd}}{\left|I_g(t)\right|} \tag{17}$$

where Q_{pl} is the MOSFET total gate charge at the beginning of the plateau; Q_{th}, the total gate charge at the threshold and Q_{gd}, the gate-to-drain charge. T_{rcsd} is the rising time and T_{fcsd} is the falling time with CSD.

Fig. 8 illustrates the switching time comparison with the CSD and conventional driver, and the CSD gate drive current i_g. Between t_1 and t_2, in half of line period, the switching time with the CSD is much reduced over the voltage driver. At the same time, it is observed that when i_g increases, the switching time of the CSD drops rapidly, which means significant switching loss reduction.

During [0, t_1] and [t_1, T_{line}/2], it is also noted that the switching time with the CSD is longer than that with the voltage driver. This is because during these intervals, the gate drive current is not large enough to turn on the power MOSFET completely. However, what happens is that during the dead time of two drive switches, the CSD behaviors as a voltage driver with an effective drive current of 0.8A.

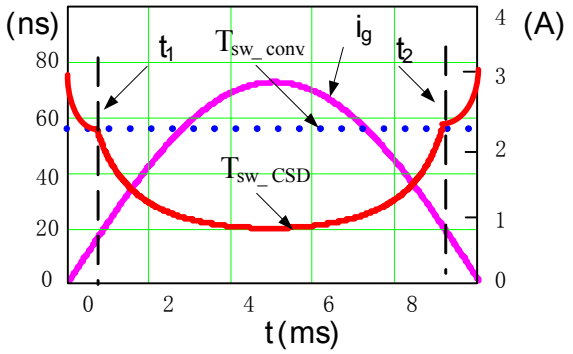

Fig. 8 The switching time with the CSD with the low line voltage in half of line period (V_{in}=110V, V_o=380V, V_c=15V, P_o=300W and L_r=1uH)

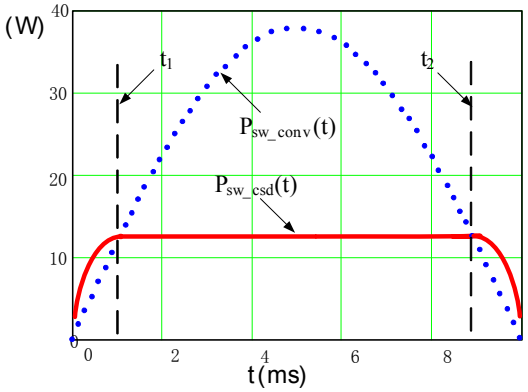

Fig. 9 The actual switching loss with the CSD compared with the conventional gate driver in half of line period (V_{in}=110V, V_o=380V, V_c=15V, P_o=300W and L_r=1uH)

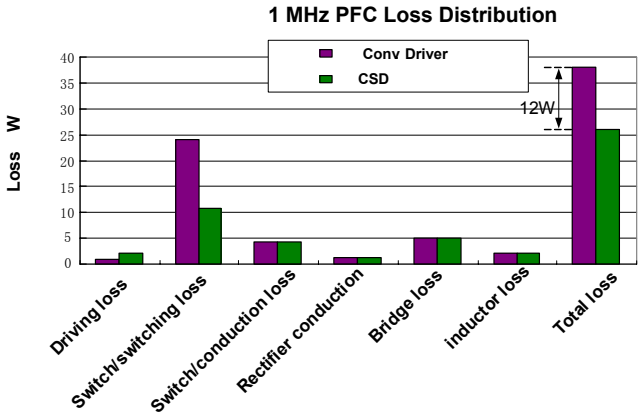

Fig. 10 Loss breakdown between the CSD and the conventional driver at 1MHz (V_{in}=110V, V_o=380V, V_c=15V, P_o=300W and L_r=1uH)

Based on Fig. 8, the switching loss comparison is shown in Fig. 9. However, it should be noted that at low line voltage, the input current is low and the switching current is also low. Therefore, the switching loss happens at the low line voltage is limited among the line period. Overall, the CSD can reduce the switching loss much over the conventional voltage driver.

Fig. 10 shows comparison of the 1MHz PFC loss distribution. At 110V input, 380V output voltage, the CSD reduces the total loss of 12W, which translates into an efficiency improvement of 3.2% (from 89% to 92.2%).

B. Loss Comparison of 220V Input

With V_{in}=110V and V_o=380V, during half of line period, the duty cycle of the boost PFC converter is always above 0.5. From (4), the current of the CS inductor is proportional to (1-*D*). Therefore, the curve of the CS gate drive current can be adaptive to the switching current of the power MOSFET in half of line period.

If the input voltage increases to 220V, compared to the 110V condition, the duty cycle of the power MOSFET is not always above 0.5. In order to understand this mode, the detailed analysis is given as follows.

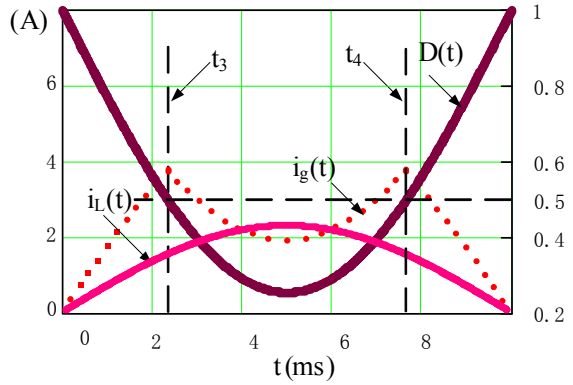

Fig. 11 Duty cycle *D*, gate drive current I_g and boost inductor current i_L in half of line period (V_{in}=220V, V_o=380V, V_c=15V, P_o=300W and L_r=1uH)

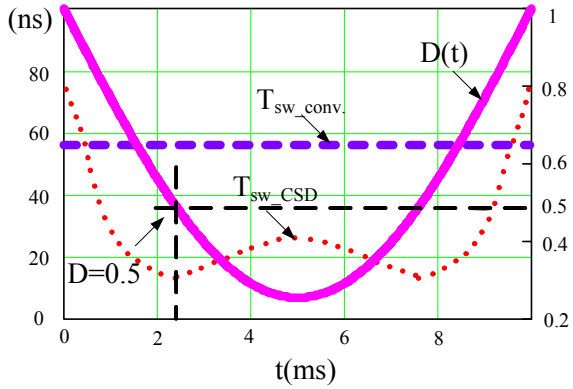

Fig. 12 The switching time with the CSD compared with the conventional driver in half of line period (V_{in}=220V, V_o=380V, V_c=15V, P_o=300W and L_r=1uH)

Fig. 11 shows the duty cycle $D(t)$, the CS gate drive current $i_g(t)$ and boost inductor current $i_L(t)$ during the half of line period. As seen from Fig. 11, between t_3 and t_4, the gate drive current i_g drops, and as a result, the switching time of the power MOSFET increases. This is because when D<0.5, the CS current will be governed by (3). Fig. 12 shows the switching time with the CSD compared with the conventional driver. According to Fig. 11, although the gate drive current drops during [t_3, t_4], and is not adaptive to the switching current, but compared with conventional drivers, the switching time T_{sw_CSD} with CSD is still reduced signicantly (see Fig. 12).

Based on Fig. 12, Fig. 13 gives the associated switching loss comparison with V_{in}=220VAC. As from Fig. 13, the switching loss reduction with the CSD is less compared to the value with 110V input (see Fig. 9). Fig. 14 shows the loss breakdown between the CSD and the conventional driver with 220V input. The CSD improves the 1MHz PFC efficiency from 93.8% to 95.6% with 220V input.

Fig. 21 gives the efficiency of 1MHz/300W PFC in comparison with different input voltages. At the same time, it is noted that the CSD achieve higher efficiency improvement with lower input line voltage.

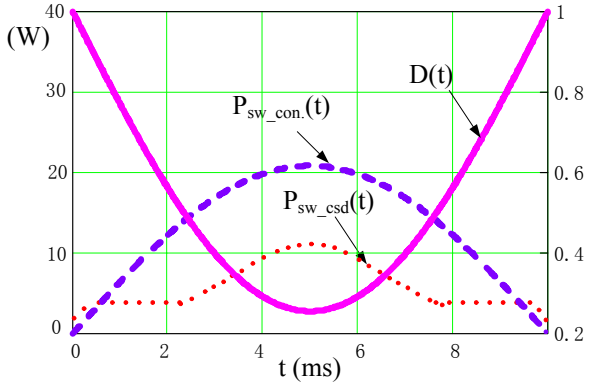

Fig. 13 The actual switching loss with the CSD compared with conventional gate driver in half of line period (V_{in}=220V, V_o=380V, V_c=15V, P_o=300W and L_r=1uH)

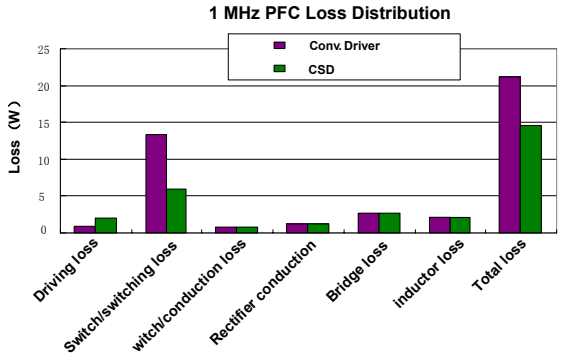

Fig. 14 1MHz PFC loss breakdown between the CSD and the conventional driver with 220V input voltage

IV. Experimental Results And Discussion

To verify the proposed solution, an 110VAC input, the PCB board of 380V/300W output and 1MHz boost PFC converter was built. Fig. 15 gives the photo of the prototype. The specifications are: boost inductor L=100μH; output capacitance C=220μF; the CS inductor L_r=1μH; the gate driver voltage V_c=12V. It should be noted that no commercial PFC IC chip is available for 1 MHz switching frequency PFC application. The discrete components were used to build the controller and saw tooth generator, etc.

Fig. 16 shows the input voltage and current of the power stage, it is observed that the input line current is the sinusoidal waveform, which is able to catch up with the input line voltage. Fig. 17 shows the input line voltage and the CS inductor current. As the duty cycle changes with the input line voltage, the CS inductor current is able to change simultaneously with fast dynamic response. When the input

voltage and current reach its peak value as shown in the dotted line, which means the main MOSFET carries the peak current, the CS inductor current also reaches its peak value adaptively.

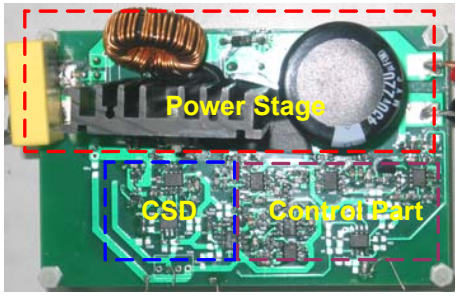

Fig. 15 Photo of power stage and CSD on PCB board

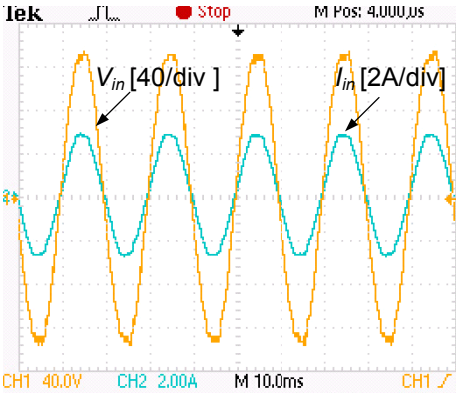

Fig. 16 The input voltage and current of the power stage

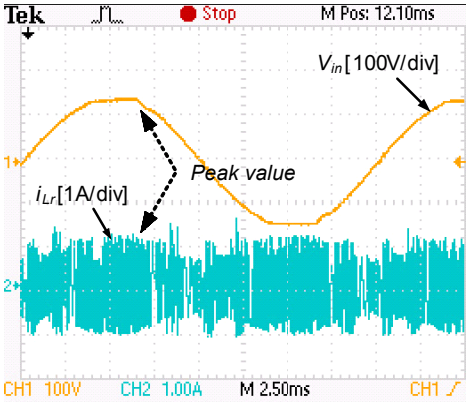

Fig. 17 Waveforms of input voltage and CS inductor current

Fig. 18 shows the drive signals of S_1 and S_2, and the voltage between A and B, u_{AB}, which agrees with the theoretic waveforms in Fig. 4.

Fig. 19 illustrates the CS inductor current, and the voltage between A and B, u_{AB}. During the interval t_1-t_2, the inductor current declines from positive peak value to the negative peak value. From t_2 to t_3, the CS inductor current is circulating through S_1 and S_2 and remains constant in this interval, so the main MOSFET can be switched off by a nearly constant drive current. During interval t_3-t_4, the inductor current increases from the negative peak value to the positive peak current. At t_4, the MOSFET can be switched on by a nearly constant current. Fig. 20 shows the CS inductor current and the gate-to-source voltage u_{GS} to demonstrate the fast switching speed.

Fig. 21 gives the measured efficiency comparison between the CSD and the conventional voltage driver with different line voltages. Due to the fast switching speed and the switching loss reduction, when 110VAC input line voltage, an efficiency improvement of 3.2% can be achieved to a 1MHz/ 300W boost PFC converter. When 220VAC input line voltage, an efficiency improvement of 1.5% can be achieved over the conventional voltage driver.

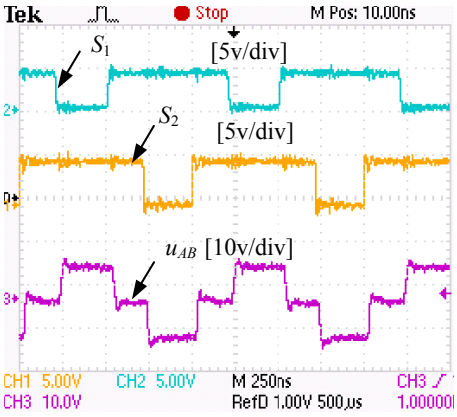

Fig. 18 Key waveforms of drive signals and u_{AB}

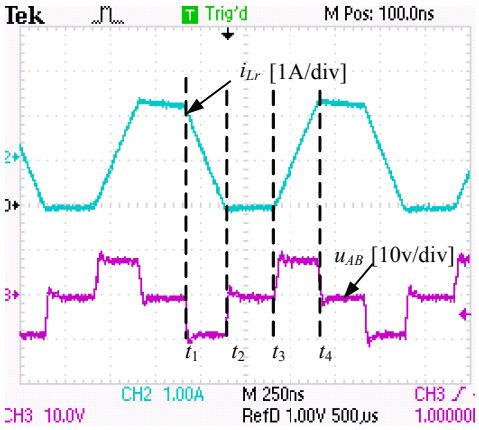

Fig. 19 CS inductor current and the voltage between A and B, u_{AB}

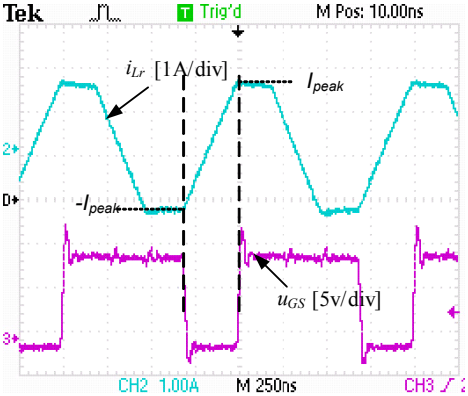

Fig. 20 Zoomed CS current and gate drive voltage

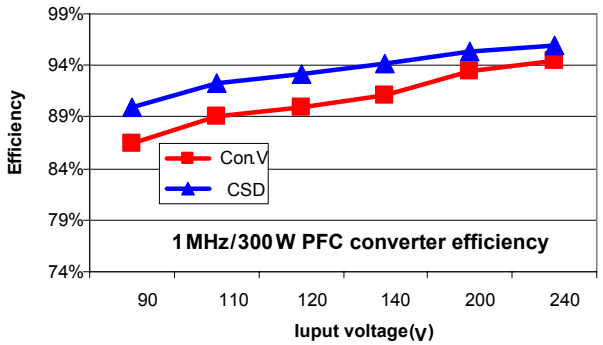

Fig. 21 Measured efficiency comparison with different line voltages: top: CSD; bottom: conventional voltage driver

V. CONCLUSION

In this paper, the CSD technique is investigated for MHz PFC applications. The proposed CSD solution for the boost PFC converter can achieve fast switching speed and switching loss reduction, and the proposed CSD with the continuous inductor current can actually achieve adaptive drive currents to the input line voltage and current. These benefits help to improve the switching frequency of the boost PFC converter to MHz over the conventional several kHz PFC converters. This will leads to significantly reduction of the inductors and the size of the EMI filter. From the experimental results, when 110VAC input, 380V output voltage, the CSD reduces the total loss of 12W, which translates into an efficiency improvement of 3.2% (from 89% to 92.2%), when 220VAC input, an efficiency improvement of 1.5% can be achieved over the conventional voltage driver.

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