Digital Charge Balance Controller to Improve the Loading/Unloading Transient Response of Buck Converters

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***Abstract*—A linear/nonlinear digital controller is presented that allows a Buck converter to recover from a load transient event with near-optimal voltage deviation and recovery time. A novel digital double accumulator calculation block is used to calculate the appropriate pulse width modulation switching time instants. The proposed controller possesses many advantages not demonstrated by a single controller in the previous literature. For example, unlike many previously proposed time-optimal digital controllers, the proposed controller provides an excellent transient response as it is capable of reacting asynchronously to a load transient event. In addition, it is demonstrated that the proposed controller can operate without requiring information pertaining to the Buck converter's output inductor. Furthermore, the proposed controller can be extended to applications that require load-line regulation. Lastly, unlike all previous digital time-optimal controllers, the proposed controller does not require digital multiplier or divider blocks nor does it require 2-D lookup tables. Thus, the controller can be implemented through the use of low-cost field programmable gate arrays or complex programmable logic devices.**

***Index Terms*—Buck converter, capacitor current estimator, charge balance control, DC-DC converter, digital control, optimal dynamic performance.**

I. Introduction

CONSIDERABLE research has been conducted in nonlinear and linear/nonlinear controllers that are capable of minimizing the voltage deviation and recovery time of a dc–dc converter undergoing a load transient event. Such control methods are often referred to as "optimal control."

In [1] and [2], a nonlinear analog controller is presented that employs a second-order curved switching surface to control the switching action of a Buck converter. While a near-optimal transient response is observed, the use of an analog multiplier/divider circuit significantly increases the cost and decreases the maximum switching frequency of the controller. In [3], a linear/nonlinear analog controller is presented that drives a Buck converter to recover in near-minimum time through determination of capacitor charge regions during a load transient event. The controller employs only simple mathematical functions (integration, subtraction, and addition) to determine optimal switching times; however, it requires a high-speed quasi-differentiator to detect the capacitor current zero crossover point. Furthermore, the control method is not compatible with high-performance digital features.

Digital control has gained popularity due to its unique characteristics such as robustness and reprogrammability along with its ability to employ features such as parameter auto-tuning and online efficiency optimization. Thus, a vast amount of investigation was conducted in the late 1990s in an attempt to design linear digital controllers that performed as well as their analog counterparts.

In [4]–[7], various methodologies of digital compensator design were investigated while in [8]–[13] research was focused on the quantization effects of digital controllers and effective digital pulse width modulation (DPWM) techniques. While early research laid the stepping stones for further digital control development, it did not capitalize on the truly unique abilities that digital control is able to offer such as the implementation of advanced control laws to improve the transient performance of Buck converters beyond the abilities of their analog counterparts.

It is known that nonlinear control is capable of improving the dynamic response of a converter since it is able to react to transient conditions at a faster rate. However, many nonlinear controllers tend to possess undesirable characteristics such as nonzero steady-state error and variable switching frequency.

Thus, several dual mode digital controllers have been proposed that exhibit separate behaviors depending on whether the converter is operating under steady-state conditions or not.

For example, in [14] two digital linear control loops are utilized: a compensator with high dc gain and lower bandwidth for steady-state conditions and a high-bandwidth compensator for transient conditions. A digital gain scheduler oversees the transition between loops. While this method improves dynamic performance, the controller still suffers from traditional bandwidth limitations.

In [15] and [16], digital controllers are presented that behave as a linear controller for conditions when the output voltage error is small and behave as a nonlinear controller when the output voltage error is large. This is accomplished in [15] by the use of

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a PI-like fuzzy logic controller and nonuniform fuzzy sets. The controller mimics a PI controller during steady-state conditions; however, when either the output voltage error or derivative of the output voltage is relatively high, the duty cycle varies at a faster nonlinear rate. In [16], a nonuniform A/D converter is used to acquire the output voltage. This nonlinear control method is powerful yet very simple as it does not require any multiplier or division blocks to implement.

In [17], a digital controller is presented that employs a linear PID scheme during steady-state conditions and uses a nonlinear sliding-mode like controller during large output voltage deviations. The controller was further improved in [18] by employing a digital algorithm to estimate the load current transient magnitude and selecting an appropriate switching law from a bank of digitally stored switching surfaces.

In [19], a digital controller is proposed that also employs a linear PID scheme during steady-state conditions and employs a nonlinear algorithm to effectively minimize the voltage deviation caused by a load transient event. The controller is capable of doing such with only a 4-comparator analog to digital converter (ADC).

While the aforementioned digital control methods improve the transient response of Buck converters (while not sacrificing zero steady-state error and fixed switching frequency), they do not attempt to minimize the converter's voltage deviation and settling time during a transient event.

Thus, numerous digital linear/nonlinear optimal control methods have been researched [20]–[24]. In [20], the concept of optimal control is demonstrated experimentally by calculating the optimal switching paths for a variety of transient conditions and programming them into a digital controller. However, the controller functions only in open-loop configuration; thus, the magnitude and time instant of a transient event must be predefined. In [21]–[24], digital optimal control schemes are discussed that are able to drive a Buck converter to recovery in near-optimal time "on-the-fly." The controllers in [21]–[24] suffer from at least one of the following drawbacks.

1) Delayed reaction to load transient events (either due to synchronous sampling delay or loose transient detection thresholds) [21]–[23].
2) Complex mathematical functions (e.g., multiplication/division/square root) are performed requiring either slow digital multipliers or numerous large 2-D lookup tables (LUTs) [21]–[24].
3) Nominal inductor value must be known to perform switching interval calculations [21]–[23].
4) No extension for load-line regulation (a.k.a. adaptive voltage positioning AVP) applications has been presented [22], [23].

In this paper, a digital charge balance controller is presented that addresses and corrects the aforesaid drawbacks. The proposed controller uses an analog asynchronous detection method to determine the beginning of a load transient and is therefore not impeded by digital sampling delays. The proposed controller uses only simple digital mathematical blocks such as accumulation, addition, subtraction, and comparison and does not require any 2-variable multiplication or division (removing the large gate count requirement of said functions). The controller operates without knowledge of the nominal inductor value. Finally, the proposed controller can be extended to cases that require load-line regulation (such as CPU voltage regulators).

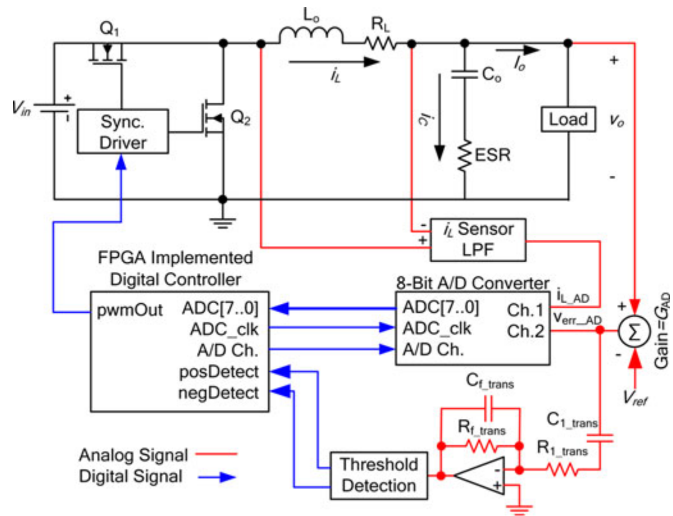

Fig. 1. Block diagram of the Buck converter and proposed controller.

In this paper, the core control elements (both during steady-state and transient conditions) are being implemented through complex digital algorithms. The proposed controller possesses all the described advantages of digital control such as reprogrammability and component tolerance immunity. However, an analog circuit is utilized in order to improve the effect of one of digital control's major drawbacks: discrete sampling. Thus, the controller could be considered a "hybrid" A/D controller.

Section II outlines the basic operation of the proposed controller. Section III demonstrates how capacitor charge balance integral regions can be calculated using a digital double accumulator. Section IV provides detailed operation of the controller following a load transient. Experimental results demonstrating the effectiveness of the controller are presented in Section V.

II. Basic Concept of Operation

This section will describe the high-level operation of the proposed digital charge balance controller. Fig. 1 illustrates the block diagram of a single-phase synchronous Buck converter and the proposed controller.

The block diagram consists of three major components.

An analog summer is used to subtract the reference voltage V_{ref} from the output voltage v_o to obtain the analog error voltage $v_{\text{err\_AD}}$. $v_{\text{err\_AD}}$ is fed to an analog/digital converter (ADC) and the analog load transient detector.

The 2-channel ADC samples the output voltage error along with the inductor current (used for load-line regulation). The output of the ADC is fed to the main controller block which is implemented using a field programmable gate array (FPGA).

The analog error voltage is also fed to the load transient detector. The transient detector consists of a high-pass filter and a window comparator. When the absolute value of the high-pass filter exceeds a predetermined threshold, it is determined that a

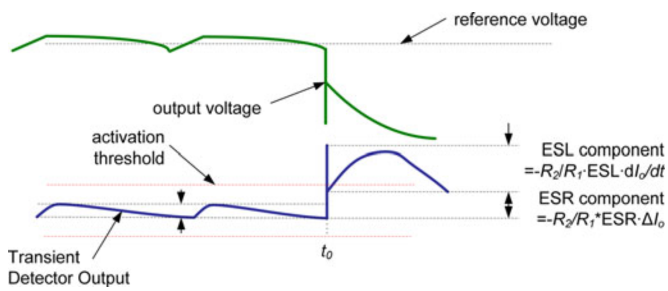

Fig. 2. Activation of a controller using high-pass filter.

load transient has occurred, and a "start" signal is sent to the controller to indicate the beginning of a load transient (along with the polarity of the load transient).

The output of the analog transient detector can be very noisy if it is not designed correctly. However, for this application, the transient detector can be designed such that it does not significantly amplify high-frequency noise.

In previous works [3] and [20], such a circuit was either designed as a pure differentiator or such that the time constant equaled the Buck converter's output capacitor [C_o and equivalent series resistance (ESR)]. A pure differentiator amplifies high-frequency noise to infinity and is practically infeasible. However, even in the latter case, the effective ESR of most low-voltage/high-current Buck converter applications is so low that the circuit still amplifies high-frequency noise.

In the previous works, the purpose of designing such a fast circuit is to continuously track the capacitor current. Therefore, the transfer function of the circuit must be tuned precisely in order to estimate the capacitor current without delay while ensuring that high-frequency noise does not significantly pollute the output.

However, in this paper, the analog transient detector is only used as a means to detect the beginning of a load transient. Therefore, a high-pass filter with a relatively low gain and corner frequency may be used with acceptable results.

In order to attenuate very high-frequency noise, a small capacitor can be added in parallel with $R_{\mathrm{f\_trans}}$, effectively creating a simple bandpass filter. By increasing $C_{\mathrm{f\_trans}}$, better noise immunity can be achieved at the cost of potentially increasing the activation delay.

The activation threshold should be set larger than half the steady-state output voltage ripple, multiplied by $R_{\mathrm{f\_trans}}/R_{1\mathrm{\_trans}}$, to ensure that only load transients trip the threshold. However, it should be noted that if the switching frequency is below the corner frequency of the transient detected, tighter thresholds may be used. When a load transient occurs, the high-frequency output voltage components, caused by the ESR and ESL of the capacitor, pass through the high-pass filter, as shown in Fig. 2. This allows for very fast detection of the load transient.

The use of an analog transient detector removes the inherent delay typical of digital controllers. Fig. 3 illustrates the proposed controller's transient response in comparison to that of [22].

The gray areas in Fig. 3 represent the charge being removed from the output capacitor. As shown, asynchronous transient

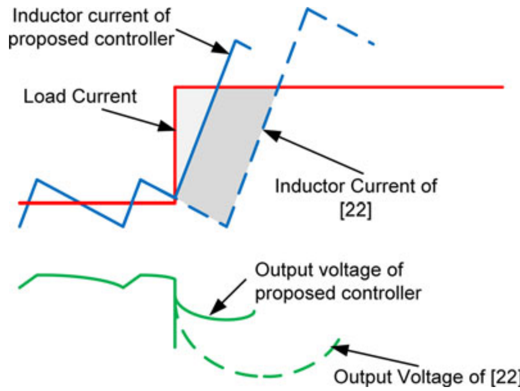

Fig. 3. Transient response improvement using asynchronous transient detection.

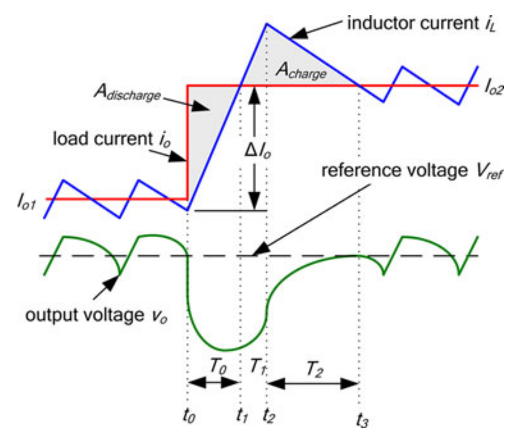

Fig. 4. Proposed controller operation following a positive load step .

detection significantly improves the output voltage deviation by decreasing the amount of charge removed from the output capacitor.

The controller's transient response will be described without and with load-line regulation.

A. Without Load-Line Regulation

Figs. 4 and 5 show the transient reaction of a Buck converter, controlled by the proposed method, undergoing a positive and negative load step, respectively.

The key points of the controller can be summarized in three steps.

1) The converter is controlled by a linear voltage-mode control scheme during steady-state conditions.
2) Immediately following a load step change, the controller sets the PWM control high (for a positive load step change) or low (for a negative load step change).
3) The controller will set the PWM low (for a positive load step) or high (for a negative load step) at a determined switching time instant t_2. t_2 should be such that the net capacitor charge over the transient period is zero (i.e., $A_{\mathrm{charge}} = A_{\mathrm{discharge}}$). This will cause the output voltage to equal the reference voltage at the exact moment that the

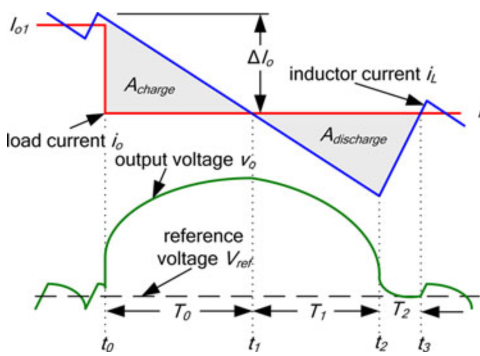

Fig. 5. Proposed controller operation following a negative load step.

inductor current equals the load current. Determination of t_2 will be discussed in Section III.

Following the recovery from the load transient, the controller will return to its linear voltage-mode operation.

B. With Load-Line Regulation

Load-line regulation (a.k.a. AVP) has increasingly become a requirement in many Buck converter applications. Load-line regulation essentially involves outputting lower voltages during higher load current conditions. This assists in improving the overall transient performance of the converter along with decreasing power consumption of the load device. As will be demonstrated, the proposed controller is capable of smoothly transitioning between two steady-state voltages in order to facilitate load-line regulation. In order to describe the operation of the digital charge balance controller with load-line regulation, two separate cases must be taken into consideration.

1) Case #1: As illustrated in Fig. 6, Case #1 occurs when the voltage deviation magnitude is larger than the allowed steady-state voltage change (determined by the droop resistance $|v_{o2}-v_{o1}|$), as expressed in the following relation:

$$\frac{|\int_{t_0}^{t_1}(i_L - i_o)dt|}{C_o} \geq |\Delta I_o| \cdot R_{\text{droop}} \tag{1}$$

where t_1 represents the first instance that the inductor current i_L equals the new load current I_{o2}.The constant R_{droop} represents the Buck converter's desired output impedance. ΔI_o represents the difference between the final load current I_{o2} and the initial load current I_{o1}. C_o equals the Buck converter's output capacitance. For a negative load step, under Case #1 conditions, the PWM signal will be kept low from t_0 to t_2. t_2 is such that (2) is true. For a positive load step, under Case #1 conditions, the PWM signal will be kept high from t_0 to t_2. t_2 is such that (3) is true. Determination of t_2 will be discussed in Section III

$$A_{\text{discharge}} - A_{\text{charge}} = \Delta I_o \cdot R_{\text{droop}} \cdot C_o \tag{2}$$

$$A_{\text{charge}} - A_{\text{discharge}} = -\Delta I_o \cdot R_{\text{droop}} \cdot C_o. \tag{3}$$

It is important to note that for low duty-cycle applications (e.g., 12 $V_{\text{dc}} \rightarrow 1.5$ V_{dc} conversion), Case #1 will likely occur for negative load current step changes since it is common practice to allow the output voltage to overshoot the load-line regulation window for a short period of time.

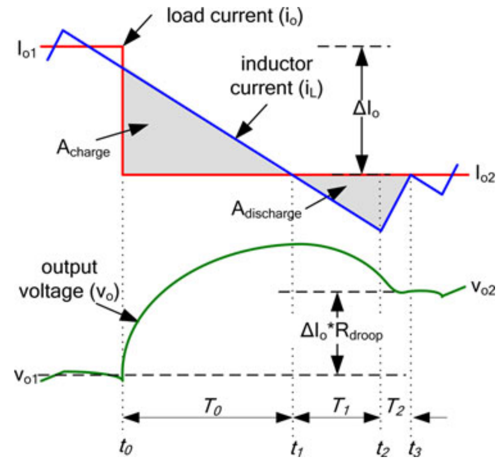

Fig. 6. Proposed controller operation following a negative load step (with load-line regulation Case #1).

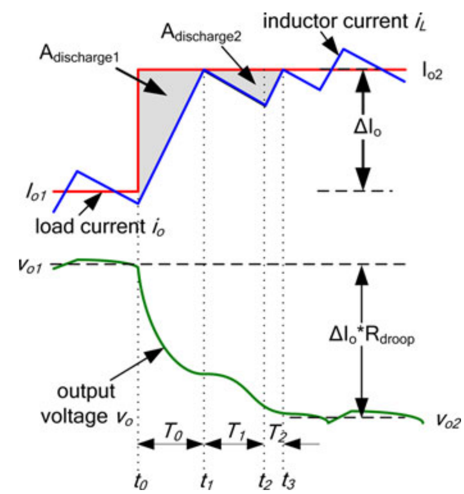

Fig. 7. Proposed controller operation following a positive load step (with load-line regulation Case #2).

2) Case #2: Case #2 occurs when the output voltage deviation magnitude (at t_1) is less than the allowed steady-state voltage change (determined by droop resistance $|v_{o1}-v_{o2}|$) as shown in Fig. 7 for a positive load current step change.

It is observed that an additional switching instant must occur in order to allow the output voltage to reach the new steady state-state value with minimal settling time. At time instant t_1 (the moment that the inductor current first equals the new load current), the PWM signal is set low in order to remove additional charge from the capacitor. At time instant t_2, the PWM signal is set high such that at t_3, the inductor current equals the new load current and (4) is true

$$A_{\text{discharge1}} + A_{\text{discharge2}} = \Delta I_o \cdot R_{\text{droop}} \cdot C_o. \tag{4}$$

For low duty-cycle applications (e.g., 12 $V_{\text{dc}} \rightarrow 1.5$ V_{dc} conversion), Case #2 will likely occur for positive load step changes since it is common practice to design the load-line

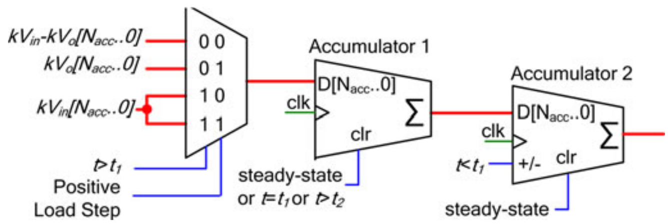

Fig. 8. Simplified diagram of digital double accumulator.

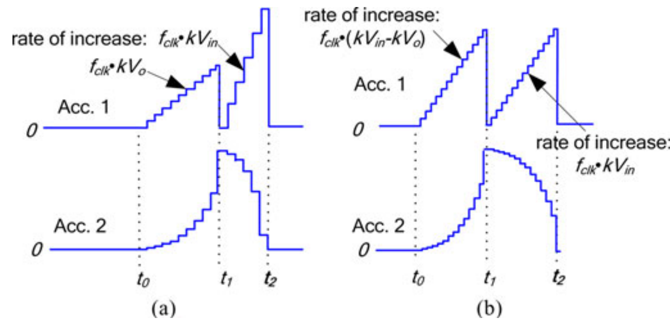

Fig. 9. Double accumulator operation: (a) during positive load step, (b) during negative load step.

regulation voltage window based on the worst case transient conditions (i.e., unloading transient events). Determination of t_2 will be discussed in Section III.

III. Calculation of Switching Intervals Based on a Digital Double Accumulator

This section will highlight the use of a digital double accumulator to determine the switching instant t_2 required such that $A_{\rm charge}$ and $A_{\rm discharge}$ are balanced appropriately. In order to simplify the derivation of the control method, there are three key assumptions regarding the load current and input voltage behavior.

1) The slew rate of the load variation is very large compared to the slew rate of the output inductor. In other words, the load variation can be viewed as an abrupt "step."
2) The load current remains constant for the duration of the operation of the nonlinear control loop.
3) The input voltage remains relatively constant for the duration of the operation of the nonlinear control loop.

In most microprocessor applications, applications 1 and 2 are typically valid.

A. Without Load-Line Regulation

Referring to Figs. 4–7, it is the calculation of the switching point t_2 that typically requires complex mathematical computation in [20]–[24]. However, it is demonstrated in [3] that through the use of a double integrator, the switching point t_2 may be determined in real time without the use of multiplication/division. The charge balance equations, previously derived in [3], are expressed in (5) and (6) for a positive and negative load step, respectively

$$V_o \iint_{t_0}^{t_1} dt\,dt - V_{\rm in} \iint_{t_1}^{t_2} dt\,dt = 0 \tag{5}$$

$$(V_{\rm in} - V_o) \iint_{t_0}^{t_1} dt\,dt - V_{\rm in} \iint_{t_1}^{t_2} dt\,dt = 0. \tag{6}$$

Thus, a digital double accumulator (see Fig. 8) may be employed (in lieu of an analog double integrator) to calculate the optimal switching moment t_2, as illustrated in Fig. 9.

$kV_{\rm in}$ and kV_o are digital variables representing the input and output voltages of the Buck converter. $f_{\rm clk}$ represents the clock frequency of the double accumulator. The input voltage of the converter may be preprogrammed or sensed using a slow ADC. As illustrated, the switching moment t_2 is determined when the double accumulator output returns to zero. However, modifications must be made to this method for applications that require load-line regulation.

B. With Load-Line Regulation

This analysis will be separated into Case #1 and Case #2, as defined in Section II.

1) Case #1: Referring to Fig. 6, the controller's goal is to drive the converter such that the inductor current reaches the new load current at the exact moment t_3 that the output voltage reaches its new steady state voltage v_{o2}.

In order to achieve this, (3) is modified such that $A_{\rm charge}$ and $A_{\rm discharge}$ are expressed in terms of the positive and negative slew rates of the inductor current, as shown in

$$\iint_{t_0}^{t_1} m_2\,dt\,dt - \iint_{t_1}^{t_2} \frac{m_1 \cdot m_2 + m_2^2}{m_1} dt\,dt = -\Delta I \cdot R_{\rm droop} \cdot C_o \tag{7}$$

where m_1 represents the rising slew rate of the inductor current when the converter's PWM signal is high. m_2 represents the falling slew rate of the inductor current when the converter's PWM signal is low.

It is assumed that m_1 and m_2 are relatively constant for the duration of the transient event (neglecting inductor DCR and MOSFET $R_{\rm ds\_on}$). This assumption holds true for low-voltage, high-current designs where components are chosen with very low dc resistances.

By assuming that the load current step magnitude is large compared to the magnitude of the steady-state capacitor ripple current, ΔI_o can be estimated by integrating the negative inductor current slew rate m_2 over the time period T_0 (from t_0 to t_1), as shown in

$$\iint_{t_0}^{t_1} m_2\,dt\,dt - \iint_{t_1}^{t_2} \frac{m_1 \cdot m_2 + m_2^2}{m_1} dt\,dt = R_{\rm droop} \cdot C_o \int_{t0}^{t1} m_2 dt \tag{8}$$

where m_2 can be divided from all terms of (8). The approximations $m_1 = (V_{\rm in} - V_o)/L_o$ and $m_2 = -V_o/L_o$ are then substituted

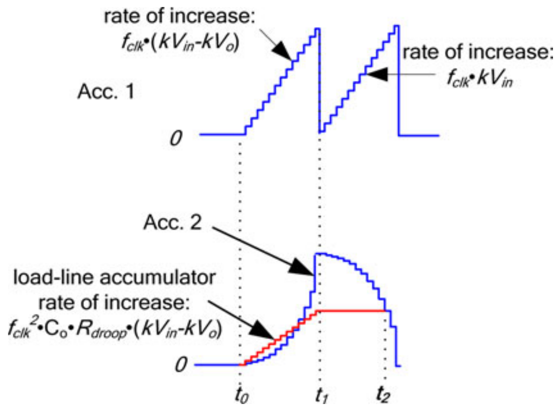

Fig. 10. Digital double accumulator operation for negative load current step with load-line regulation (Case #1).

into (8) to produce

$$\iint_{t_0}^{t_1} dt\,dt - \iint_{t_1}^{t_2} \frac{(V_{\text{in}} - V_o/L) + (V_o/L)}{(V_{\text{in}} - V_o/L)} dt\,dt = R_{\text{droop}} \cdot C_o \int_{t_0}^{t_1} dt. \quad (9)$$

By simplifying (9) and multiplying both sides of the equation by $(V_{\text{in}} - V_o)$, the final equation is presented in

$$(V_{\text{in}} - V_o) \iint_{t_0}^{t_1} dt\,dt - V_{\text{in}} \iint_{t_1}^{t_2} dt\,dt = R_{\text{droop}} \cdot C_o \cdot (V_{\text{in}} - V_o) \int_{t_0}^{t_1} dt. \quad (10)$$

Thus, t_2 can be determined for a negative load current step change, with load-line regulation implemented, by using the digital accumulator operation illustrated in Fig. 10.

It is observed that an additional digital accumulator (*load-line accumulator*) is required when load-line regulation is enabled. For a negative load step, $C_o \cdot R_{\text{droop}} \cdot f_{\text{clk}} \cdot (kV_{\text{in}} - kV_o)$ is applied to input of the *load-line accumulator* for the interval T_0 (from t_0 to t_1), according to (10).

Essentially, the charge balance "zero" of the second accumulator is shifted to compensate for load-line regulation. It should be noted that the output of a single accumulator is being compared to the output of two accumulators in series; therefore, the input constant $(R_{\text{droop}} \cdot C_o)$ of the load-line accumulator must be multiplied by f_{clk}.

If at t_1, the value of the load-line accumulator is greater than that of *accumulator 2*, (1) is not satisfied, and Case #2 is detected.

2) Case #2: Referring to Fig. 7, the positive load step change will be used as an example since Case #2 is not as likely to occur for a negative load step. The charge balance formula can be calculated using

$$A_{\text{discharge1}} + A_{\text{discharge2}} = \Delta I \cdot R_{\text{droop}} \cdot C_o. \quad (11)$$

Through similar derivation as presented earlier, (11) can be modified to

$$\iint_{t_0}^{t_1} m_2\,dt\,dt + \iint_{t_1}^{t_2} \frac{m_1 \cdot m_2 + m_2^2}{m_1} dt\,dt = R_{\text{droop}} \cdot C_o \int_{t_0}^{t_1} m_1 dt. \quad (12)$$

Equation (12) can be simplified by first multiplying both sides of the equation by (m_2/m_1), as expressed in

$$\iint_{t_0}^{t_1} m_2\,dt\,dt + \iint_{t_1}^{t_2} \frac{m_2^2}{m_1^2} \cdot (m_1 + m_2) dt\,dt = R_{\text{droop}} \cdot C_o \int_{t_0}^{t_1} m_2 dt. \quad (13)$$

Since m_2 and m_1 are assumed to be constant, the second double integration term can be simplified by modifying the period of integration, as expressed in

$$\iint_{t_1}^{t_2} (m_1 + m_2) \frac{m_2}{m_1} dt \frac{m_2}{m_1} dt = \iint_{t_1}^{t_{1a}} (m_1 + m_2) dt\,dt. \quad (14)$$

As shown in (14), the time interval of the second integration term is modified to $t_1 - t_{1a}$. t_{1a} is defined in

$$t_{1a} = t_1 + \frac{m_2}{m_1} \cdot T_1 \quad (15)$$

where T_1 equals the time interval between the capacitor current zero crossover point t_1 and the switching point t_2 (see Fig. 7). By substituting (14) into (13), (18) is created

$$\iint_{t_0}^{t_1} m_2 dtdt + \iint_{t_1}^{t_{1a}} (m_1 + m_2) dtdt = R_{\text{droop}} \cdot C_o \int_{t_0}^{t_1} m_2 dt. \quad (16)$$

Equation (18) implies that at the moment that the output of *accumulator 2* equals that of the load-line accumulator, the time interval is $|m_2/m_1| * T_1$. It is now necessary to determine time interval T_1 (and thus switching time instant t_2). Using the mathematical relationship (19), an additional accumulator (*Case 2 accumulator*) can be used to determine T_1

$$\int_{t_1}^{t_{1a}} m_1 dt - \int_{t_1}^{t_2} m_2 dt = 0. \quad (17)$$

By simplifying (17), substituting in for m_1 and m_2, and multiplying both sides by L_o, (18) is created

$$\int_{t_1}^{t_{1a}} (V_{\text{in}} - 2 \cdot V_o) dt - \int_{t_{1a}}^{t_2} V_o dt = 0. \quad (18)$$

Therefore, through use of an additional accumulator and (18), it is possible to determine t_2, as illustrated in Fig. 11. It is noted that no multipliers or 2-D LUTs were required to calculate t_2.

IV. Detailed Operation of Digital Charge Balance Controller

During steady-state conditions, the converter is controlled by a digital linear voltage-mode compensator. In order to

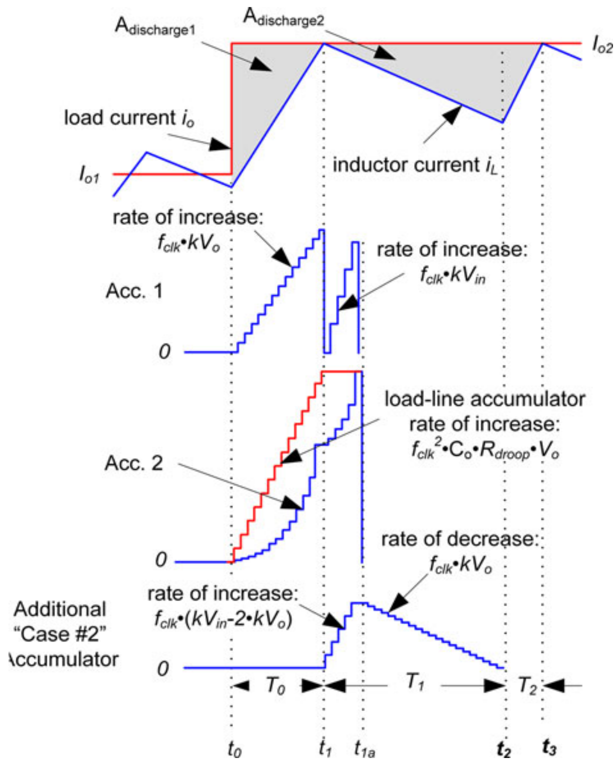

Fig. 11. Digital double accumulator operation for positive load step with load-line regulation (Case #2).

implement steady-state load-line regulation, the compensator's digital error input is shifted based on measured inductor current values. In order to prevent significant loop interaction between the voltage loop and the load-line loop, the steady-state controller calculates the load current by averaging the inductor current of four successive switching periods.

As shown in Fig. 1, the analog voltage error is fed to the ADC and to a quasi-differentiator (with roughly the same time constant as the C_o/ESR combination of the converter's output capacitor). Following a load transient, the output of the quasi-differentiator will rapidly exceed a predetermined threshold causing either the *posDetect* or *negDetect* signal to go high. The predetermined threshold should be such that it is only exceeded during large load transients. The detection of either signal will cause the controller to immediately enter transient mode. At this point, the linear controller integration will be frozen and the charge balance controller will retain control of the converter. The operation of the charge balance controller can be described in four steps.

A. Step 1: Detect Load Transient and React

Following the detection of a load transient (at t_0), the converter's PWM signal will be controlled by the charge balance controller. For a positive load step, the PWM control of the converter will be initially set high. For a negative load step, the PWM control will be initially set low.

The 4:1 input multiplexor (MUX) (see Fig. 8) will select either kV_o (for a positive load step) or $kV_{\mathrm{in}} - kV_o$ (for a negative

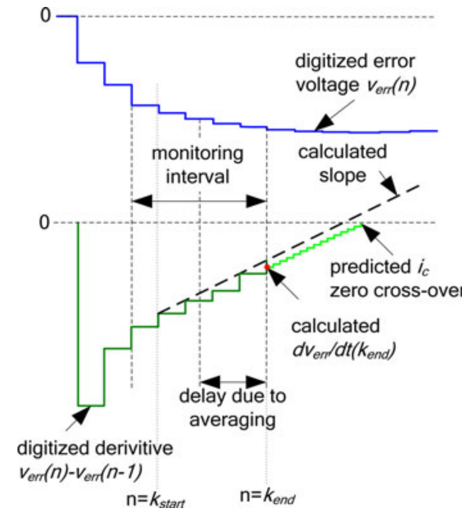

Fig. 12. Concept of capacitor current zero crossover point prediction.

load step). The output of *accumulator 1* will begin to increase linearly and the output of *accumulator 2* will begin to increase exponentially. If load-line regulation is enabled, the *load-line accumulator*'s output will be begin to increase linearly at a rate of $f_{\mathrm{clk}}^2 \cdot R_{\mathrm{droop}} \cdot C_o \cdot (kV_{\mathrm{in}} - kV_o)$ (for a negative load current step) or $f_{\mathrm{clk}}^2 \cdot R_{\mathrm{droop}} \cdot C_o \cdot kV_o$ (for a positive load current step).

B. Step 2: Predict Capacitor Current Zero Crossover Point

It is crucial to precisely determine the capacitor current zero crossover point t_1. In order to estimate the capacitor current, it is possible to approximate the output voltage derivative by oversampling ($f_{\mathrm{samp}} \gg f_{\mathrm{sw}}$) the voltage error and measuring the difference between successive samples. However, since it is important to determine the precise time instant t_1, it is necessary to detect t_1 with fine resolution. By increasing the sampling frequency, the time resolution of t_1 can be improved; however, quantization noise will be increased. In addition, since the output voltage is relatively flat for a substantial period before and after the capacitor current zero crossover point, it is difficult to accurately determine the precise moment that the output voltage derivative changes signs through direct digital sampling.

Thus, in order to improve the effective resolution and accuracy of t_1 while not excessively increasing the sampling frequency, a zero crossover point predictor is proposed, as shown in Fig. 12. The predictor is based on the hybrid capacitor current estimator presented in [18]; however in the proposed method, the inductor value is not required, which is a significant improvement. As shown in Fig. 12, the voltage error derivative is monitored for a set interval following the load step. The concept of the i_c zero crossover predictor consists of two points: 1) calculate the absolute value of the slope of the voltage error derivative over the monitoring period; and 2) calculate the magnitude of the voltage error derivative at $n = k_{\mathrm{end}}$.

The absolute value of the slope is calculated by comparing the voltage error derivative at the end of the monitoring period to the voltage error derivative at the beginning of the monitoring

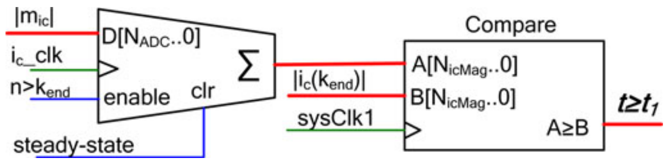

Fig. 13. Accumulator setup to predict capacitor zero crossover point t_1.

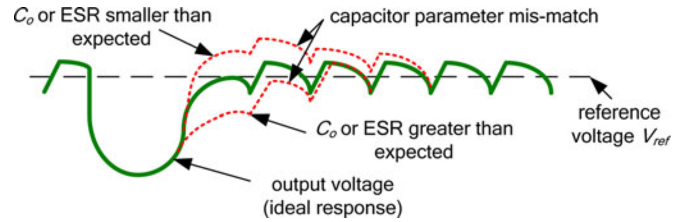

Fig. 14. Output voltage response due to capacitor parameter mismatch.

period, as equated in

$$|m_{ic}| = \left|\frac{dv_{\text{err}}}{dt}(k_{\text{start}}) - \frac{dv_{\text{err}}}{dt}(k_{\text{end}})\right|. \tag{19}$$

The magnitude of the output voltage derivative at k_{end} can be estimated by calculating the average of successive derivative samples and then adding a term to compensate for the averaging and ADC acquisition delay, as equated in

$$|i_c(k_{\text{end}})| = \frac{T_{ic\_\text{acq}}}{T_{ic\_\text{clk}}}\left[\left|\sum_{n=k_{\text{start}}+1}^{n=k_{\text{end}}} \frac{dv_{\text{err}}}{dt}(n)\right| + \frac{|m_{ic}|}{2} \cdot (N_{\text{samp}}+1) + \frac{T_{\text{AD\_del}}}{T_{ic\_\text{acq}}}|m_{ic}|\right] \tag{20}$$

where T_{ic_clk} equals the effective timing resolution of the i_c zero crossover predictor which is determined by the system clock frequency. T_{ic_acq} is equal to the period at which the voltage error derivative is being calculated. N_{samp} equals the number of T_{ic_acq} periods that occur in the monitoring period (e.g., in the case of Fig. 12, $N_{\text{samp}} = 4$). $T_{\text{AD\_del}}$ equals the ADC delay. For relatively simple digital calculation, N_{samp} and $T_{ic\_\text{acq}}/T_{ic\_\text{clk}}$ should be chosen to be 2^x. In this manner, multiplication can be carried out by simply shifting register bits. Using the capacitor current slope and magnitude calculated in (19) and (20) respectively, it is possible to predict t_1, by use of an accumulator as illustrated in Fig. 13.

After the monitoring interval, the accumulator output will increase linearly with a slope proportional to the capacitor current slew rate. When the output of the accumulator equals the calculated magnitude of the capacitor current $|i_c(k_{\text{end}})|$, it is determined that the capacitor current has crossed zero. If the ESR of the output capacitor is significant, a constant digital delay (of $T_{\text{del\_ESR}} = C_o{\cdot}\text{ESR}$) may be added to the detection of t_1 to compensate. In order to improve accuracy and mitigate quantization noise effects, each output voltage sample can be composed of a sum of successive output voltage samples acquired at a period $1/2^x$ of T_{ic_acq}.

Since the calculation of $|m_{ic}|$ and $|i_c(k_{\text{end}})|$ is unit less and proportional to each other, the aforementioned method is capable of predicting the i_c zero crossover point without knowledge of the input voltage, output voltage, nominal inductor value, or the output voltage error sensor gain.

Immediately following the prediction of t_1, the controller will send a pulse to the *clr* input of *accumulator 1* to reset its output (as shown in Figs. 9–11). The input of *accumulator 1* will then be set to kV_{in}.

If load-line regulation is enabled, the controller will also:

1) sample the inductor current at t_1. At this point, the inductor current will equal the new load current; therefore, the sample point can be used in the linear compensator, for load-line regulation, following the transient;
2) freeze the output of the load-line accumulator, as described by (10) and (16);
3) determine if Case #1 or Case #2 is occurring by comparing the output of accumulator 2 with the output of the load-line accumulator (see Figs. 10 and 11).

If Case #1 is detected or load-line regulation is not enabled, *accumulator 2* will be set to decrement (see Figs. 9 and 10).

If Case #2 is detected, the converter's PWM signal will be set low (for a positive load step), as shown in Fig. 7. The *Case 2 Accumulator* will be activated and will increase linearly at a rate of $kV_{\text{in}} - 2{\cdot}kV_o$, as shown in Fig. 11.

It is noted that the capacitor parameters (C_o, ESR) must be known in order to obtain an accurate detection of the capacitor zero crossover point (t_1). Due to tolerance, the exact parameters of the output capacitors may not be known. This will affect the timing of t_1, t_2, and t_3. A capacitor parameter mismatch will not affect the voltage deviation but will affect the settling time, as shown in Fig. 14.

It should also be noted that the accuracy of the digital calculation of the slope and prediction of capacitor zero current crossover point are related to the ADC's resolution. In this paper, the ADC resolution is relatively fine; however, if the ADC resolution were coarse, the miscalculation of switching instances may be larger than that implied in Fig. 14.

C. Step 3: Determine Switching Point t_2

If Case #1 is detected or load-line regulation is not enabled, the converter's PWM switch state will change at the moment that *accumulator 2*'s output is less than that of the *load-line accumulator* (see Figs. 9 and 10). This will cause the inductor current i_L to slew toward the new load current I_{o2} (see Figs. 4–6).

If Case #2 is detected, the *Case 2 accumulator* will begin to decrease linearly at a rate of kV_o (for a positive load step) when the output of *accumulator 2* exceeds that of the *load-line accumulator*. As shown in Fig. 11, when the *Case 2 accumulator* returns to zero, t_2 is detected and the PWM state is altered. As shown in Fig. 7, the inductor current will begin to slew toward the new load current I_{o2}.

D. Step 4: Determine End of Transient and Return Control to Linear Compensator

As illustrated in Figs. 4–7, the end of the transient occurs when the inductor current i_L equals the new load current I_{o2} for a second instance at t_3 (i.e., the moment that i_c equals zero for a second time). This can be detected by emulating the capacitor current following t_1. A digital accumulator (*accumulator 3*) is used to emulate the magnitude of i_c. The accumulator increments during time interval T_1 and decrements during time increment T_2. The input of *accumulator 3* is $kV_{\rm in} - kV_o$ when the converter's PWM signal is high and is kV_o when the output of the PWM signal is low. In other words, the output of *accumulator 3* is proportional to the absolute value of the capacitor current i_c during T_1 and T_2. Therefore, when the output of *accumulator 3* returns to zero, t_3 is detected and transient is over.

When t_3 is determined, the controller disables the transient controller and unfreezes the linear controller. The linear controller DPWM timer will be synchronized such that the mode transition occurs midway during the switching "off" period; this will facilitate a smoother transition.

It is important to note that the linear controller has already received the new load current I_{o2} (measured at t_1) for load-line regulation use. This operation will mitigate switchover effects that may occur following the transient-to-steady-state mode change.

V. Experimental Results

In order to demonstrate the proposed controller's effectiveness, a Buck converter prototype was built with the following parameters: $V_{\rm in} = 12$ V, $V_o = 1.5$ V, $f_{sw} = 400$ kHz, $L_o = 1\ \mu$H, $C_o = 180\ \mu$F, ESR $= 0.5$ mΩ, ESL $= 100$ pH. The output impedance $R_{\rm droop}$ was set to 5 mΩ.

The high-pass filter corner frequency of the analog transient detector was set to approximately 600 kHz, and the gain was set to 5. Therefore, the parameters were $C_{1\_{\rm trans}} = 1$ nF, $R_{1\_{\rm trans}} = 300\ \Omega$, $R_{\rm f\_trans} = 1.5$ kΩ. $C_{\rm f\_trans}$ was equal to 10 pF.

The voltage error ADC and the inductor current ADC each used 8-bit conversion; the ADC conversion range was 1 V. The voltage error sensor gain $G_{\rm AD}$ was equal to 5.

The i_c zero crossover predictor calculated the derivative every $T_{ic\_{\rm acq}} = 160$ ns (averaged using a finite impulse response filter from v_o samples acquired every 40 ns) and was capable of producing an effective resolution of $T_{ic\_{\rm clk}} = 10$ ns. The monitoring period of the i_c zero crossover predictor was dynamic based on the direction of the load current transient. For positive load transients, the monitoring period was 320 ns (i.e., $N_{\rm samp} = 2$). For negative load transients, the monitoring period was 1.92 μs (i.e., $N_{\rm samp} = 12$). It is important that the monitoring conclude before the inductor current equals I_{o2}.

The controller was implemented on an Altera Cyclone II FPGA chip. The chip is capable of utilizing over 70 000 logic elements; however, the combination of the i_c zero crossover predictor and the double accumulator blocks requires only a total of 450 logic elements. It is important to note that no multiplier, divider, square root, or 2-D LUTs were required to implement the digital charge balance controller.

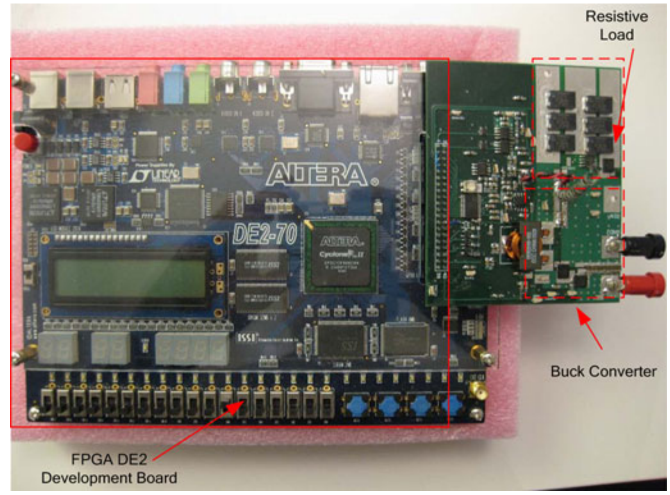

Fig. 15. Experimental setup: "Daughter card" Buck converter used with DE2 development board.

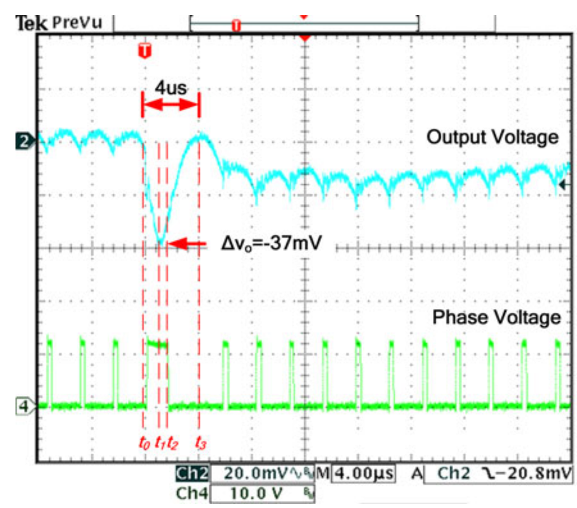

Fig. 16. Digital charge balance controller's response to a 0 A → 11.5 A load step without load-line regulation (output voltage and phase voltage).

To support the Altera FPGA, a Terasic DE2 development board was used, as shown in Fig. 15. In order to improve signal integrity, the Buck converter was designed as a "daughter card" that plugs directly into the DE2 expansion slot.

During startup, the controller exclusively relies on the linear PID controller to perform a digital "soft-start" response. The reference voltage of the PID controller is increased at a controlled rate until the output voltage has reached the target reference voltage. Until this moment, the nonlinear control loop is deactivated.

The previously defined converter and controller are subjected to rapid load current transients to demonstrate the effectiveness of the proposed controller. Fig. 16 illustrates the controller's reaction to a 0 A → 11.5 A load step (without load-line regulation). For reference, the time instants t_0–t_3 were superimposed on the scope display to better illustrate the controller's behavior.

Fig. 17 illustrates the inductor current (measured from the analog inductor current sensor shown in Fig. 1). For reference,

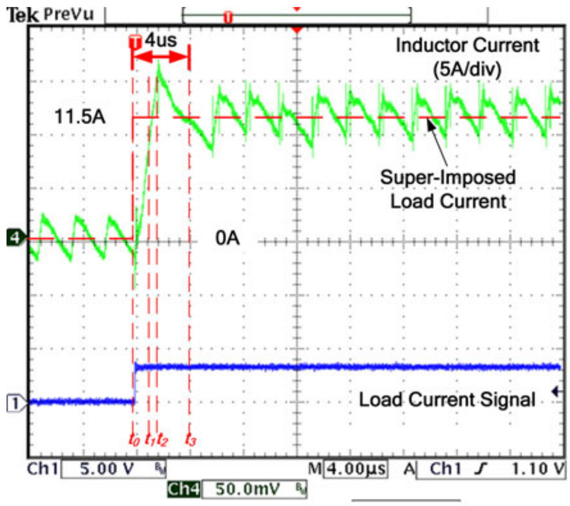

Fig. 17. Digital charge balance controller's response to a 0 A → 11.5 A load step without load-line regulation (inductor current and load current).

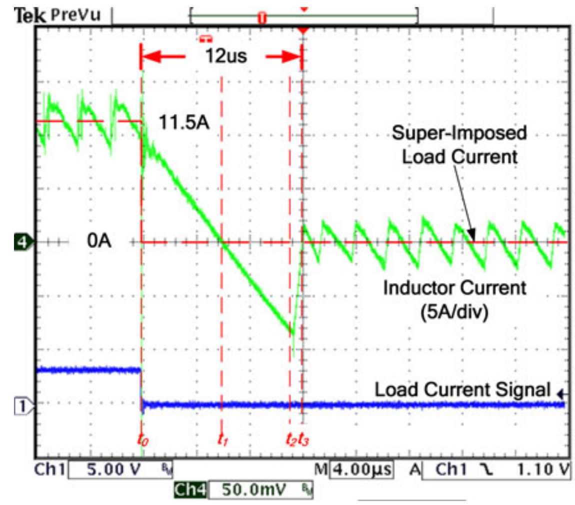

Fig. 19. Digital charge balance controller's response to an 11.5 A → 0 A load step without load-line regulation (inductor current and load current).

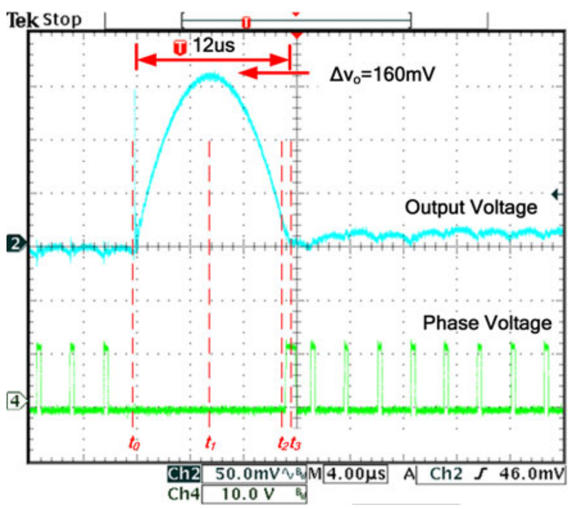

Fig. 18. Digital charge balance controller's response to a 0 A → 11.5 A load step without load-line regulation (output voltage and phase voltage).

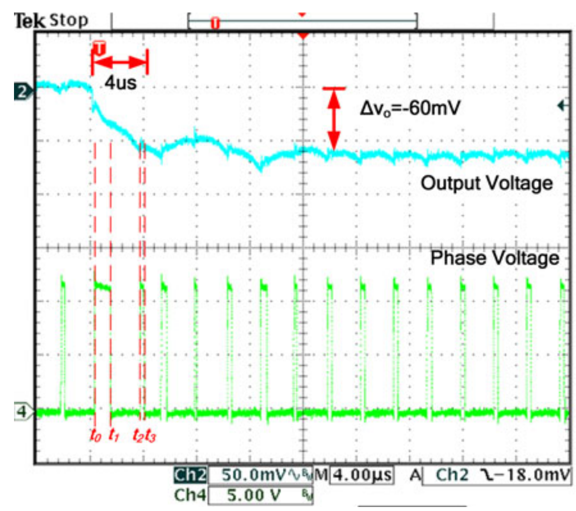

Fig. 20. Digital charge balance controller's response to a 0 A → 11.5 A load step (with load-line regulation).

the load current and time instants t_0–t_3 were superimposed on the graph.

As illustrated, the controller reacts to the load current transient with minimal delay by setting the PWM signal high at time t_0. The recovery time of the converter is only 4 μs.

It is noted that following the initial recovery time of 4 μs, the linear PID controller requires some additional time to fully recover. This is primarily due to a variation of the input voltage while the PID controller is frozen. Additional input capacitors or a wider PID controller bandwidth can mitigate this undesirable behavior.

Fig. 18 shows the controller's reaction to an 11.5 A → 0 A load current step change (without the use of load-line regulation). Fig. 19 illustrates the inductor current (measured from the analog inductor current filter).

The converter is capable of recovering from the load current transient within 12 μs with a voltage deviation of 160 mV.

Fig. 20 illustrates the controller's reaction to a 0 A → 11.5 A load step (with load-line regulation). In other words, the steady-state output voltage will transition from 1.5 V (at $I_{o1} = 0$ A) to approximately 1.44 V (at $I_{o2} = 11.5$ A). Fig. 21 illustrates the inductor current (measured from the analog inductor current sensor).

As is observed in Fig. 20, Case #2 occurs for a 0 A → 11.5 A load step. As shown, the controller reacts to the positive load step by immediately setting the PWM signal high; however, when the inductor current equals the new load current (at t_1), additional charge must be removed from the output capacitor in order for the output voltage to decrease to its new steady-state value. Thus, the PWM signal is set low until time instant t_2 in order to remove additional charge from the output capacitor in the fastest manner possible.

It is shown that the transition between the charge balance controller and the linear controller is relatively smooth. This is

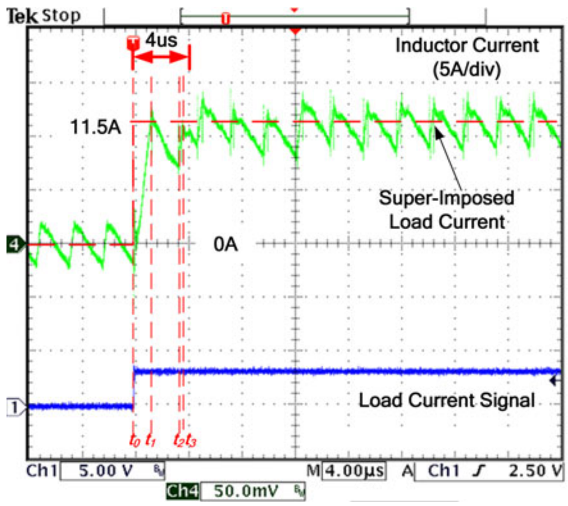

Fig. 21. Digital charge balance controller's response to a 0 A → 11.5 A load step with load line-regulation (inductor current and load current).

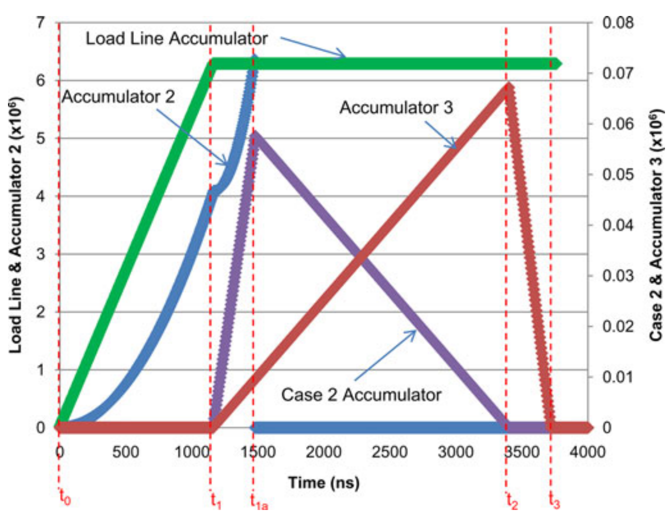

Fig. 22. Digital control signals of charge balance controller during 0 A → 11.5 A load current transient with load-line regulation (Case #2).

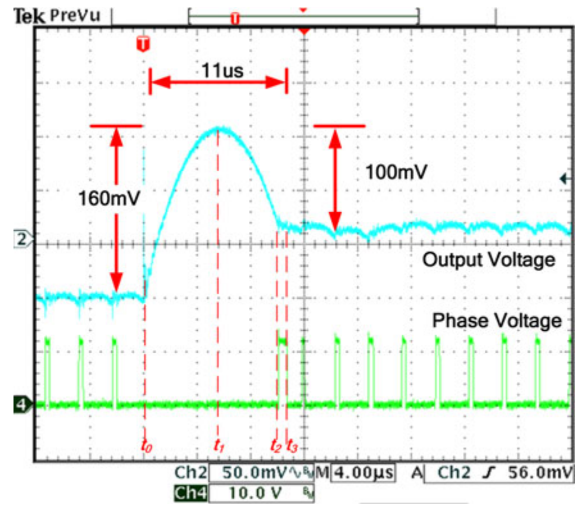

Fig. 23. Digital charge balance controller's response to an 11.5 A → 0 A load step (with load-line regulation).

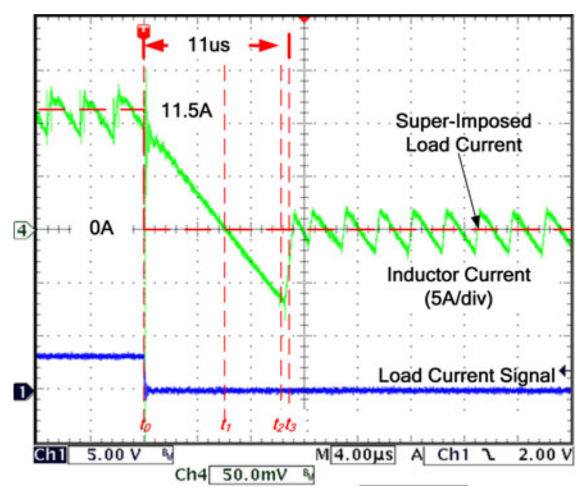

Fig. 24. Digital charge balance controller's response to an 11.5 A → 0 A load step with load-line regulation (inductor current and load current).

facilitated by the load current information (measured at time instant t_1) being passed directly to the linear controller.

For clearer understanding of the operation of the controller, the digital signals of the controller during the positive load current step transient are shown in Fig. 22. The digital signals were extracted during experimental tests using an embedded logic analyser. For reference, the time instants t_0–t_3 were superimposed on the graph.

Since the output of *accumulator 2* is less than that of the *load-line accumulator* at time instant t_1, Case #2 is detected. Thus, additional charge must be removed from the capacitor and the condition for Case #2 exists. The *case 2 accumulator* is used to determine the switching moment t_2. As shown, all time instants are consistent with the expected values according to Figs. 20 and 21.

Fig. 23 illustrates the controller's reaction to an 11.5 A → 0 A load step (with load-line regulation). Fig. 24 illustrates the inductor current (measured from the analog inductor current sensor).

As illustrated, the converter is capable of recovering from the unloading transient within 11 μs.

Fig. 25 shows the experimentally obtained digital signals of the controller during the negative load current step transient with load-line regulation.

Since the output of *accumulator 2* is greater than that of the *load-line accumulator* at time instant t_1, Case #1 is detected. The PWM signal is set low until the output of *accumulator 2* is less than the output of the *load-line accumulator* (at t_2). As shown, all time instants are consistent with the expected values according to Figs. 23 and 24.

It is shown that the transition between the charge balance controller and the linear controller is relatively smooth in Figs. 20 and 23. This is facilitated by the previously measured load current information being passed to the linear controller.

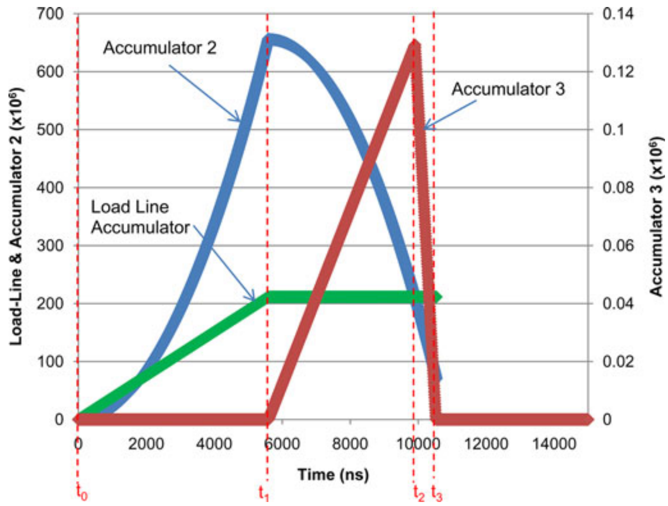

Fig. 25. Digital control signals of charge balance controller during 11.5 A → 0 A load current transient with load-line regulation (Case #1).

VI. Conclusion

A digitally implemented charge balance controller was presented in this paper.

It is demonstrate that the proposed controller possesses the following advantages over previously proposed controllers.

1) The proposed method uses an analog transient detector and an asynchronous "interrupt" in order to react to a load step virtually instantaneously, significantly improving the transient response.
2) The proposed controller does not require 2-D LUTs or multipliers to calculate optimal switching intervals, thereby decreasing the number of gates and chip real-estate required.
3) Unlike previous methods, the proposed controller does not require the nominal value of the output inductor to estimate the capacitor current zero crossover point and calculate the appropriate switching intervals,
4) Through the addition of a couple of digital accumulators, the proposed method can be extended to load-line regulation applications, which is an important criterion in modern voltage regulators.

Experimental results were presented, which demonstrate the feasibility and effectiveness of the proposed controller. As demonstrated, the controller is capable of driving a Buck converter to recovery in a very short time period (≤ 4 μs for a loading transient and ≤ 12 μs for an unloading transient). These results are equivalent to previous results demonstrated by the previously presented analog controller [3], and are superior to the results demonstrated by the digital controller [22].

It is also shown that, even with load-line regulation, the switch-over between transient and steady-state modes is relatively smooth. Since the proposed digital charge balance controller does not utilize digital multipliers, dividers, or 2-D LUTs, the addition of the nonlinear algorithm consumes a modest 450 Altera logic elements and can be transferred to low-cost ASIC or Complex Programmable Logic Device (CPLD) implementations.

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