An Interleaved LLC Resonant Converter Operating at Constant Switching Frequency

Zhiyuan Hu, Yajie Qiu, Laili Wang, Yan-Fei Liu
Department of Electrical and Computer Engineering
Queen's University, Kingston, Canada
zhiyuan.hu@queensu.ca, yajie.qiu@queensu.ca, l.l.wang@queensu.ca, yanfei.liu@queensu.ca

Abstract— **The interleaving and phase shedding techniques on LLC resonant converters will increase the load capacity, reduce the output current ripple and improve the efficiency. However, conventional frequency-controlled LLCs will lose regulation in individual phases if all phases are synchronized for interleaving, causing current imbalance. Existing load-sharing solutions for multiphase LLCs cannot achieve voltage regulation, phase shedding, and expandable load capacity all at the same time. In this paper, a switch-controlled capacitor (SCC) modulated LLC converter (SCC-LLC) is presented for multiphase paralleling. It features constant switching frequency, which results in a simple structure for paralleling and the ability for phase shedding to improve light-load efficiency. In the proposed structure, a SCC unit is used in each individual LLC stage to regulate the output gain, thereby inherently solves the conflict between the interleaving and the load sharing.**

I. INTRODUCTION

The LLC resonant converter has been found advantageous in front-end DC/DC conversions [1-4]. It is adopted in many applications such as flat-panel TVs, laptop adapters, and servers, etc. The main advantages of LLC resonant converters include primary-side zero-voltage switching (ZVS), secondary-side zero-current switching (ZCS), narrow frequency variation range, integrated magnetic components, and so on.

In order to further improve the efficiency and the load capacity of LLC converters, the interleaving technique must be used for the following reasons:

1. The load capacity is limited by the trade-offs of the resonant tank design. Higher output gain can be reached at the expense of increased circulating energy, resulting in lower efficiency[4]. The interleaving technique will solve this problem by adding parallel LLC stages to multiply the load capacity, while each stage remains the optimized design.

2. In high-current applications, the transformer becomes a major source of power loss because of the eddy current and the associated effects (AC loss) and the copper resistance of the transformer windings (DC loss). By splitting the current with multiple phases, both AC and DC losses can be mitigated.

3. The discontinuous nature of the output current imposes high RMS current on the output capacitors. Interleaving the paralleled LLC stages will cancel the current ripple and therefore reduce the required capacitor size and also lower the power loss on ESR.

4. The phase shedding technique has been successfully used in multiphase point-of-load converters to improve light-load efficiency. Multiphase LLC converters can also take advantage of this technique to obtain a relatively flat load-efficiency curve.

Among the efforts to parallel conventional frequency-controlled LLCs, load sharing is the key problem. This is because all the stages must operate at the same switching frequency for current ripple cancellation, whereas due to the components' tolerances, individual LLC stages may have different resonant frequencies, resulting in unequal output gains. For example, the commonly seen ±10% tolerances of resonant capacitors can cause drastic current imbalance [5].

Previous studies on multiphase LLCs provided several load-sharing solutions but all had limitations. The work in [6] revealed that a hot-plugged LLC stage automatically shares the load current within a few switching cycles, proving that phase shedding in multiphase LLCs is easy to achieve. Nevertheless the paper did not address the current imbalance problem due to the component tolerances. The work in [7] dealt with the aforementioned load sharing problem by tracking the switching frequency point at which current balance is reached between the two non-identical LLC stages. However it then loses the freedom for voltage regulation and therefore needs an additional power stage to control the output voltage, which degrades the efficiency. And also, this solution cannot work for more than two paralleled LLC stages. The work in [8] proposed a series-input structure that automatically achieves load sharing between two non-identical LLC stages. However the input voltage is divided by the two phases, so for the same output power, the total primary current will double; thus in each phase, the primary current remains approximately the same as the single-phase LLC. Therefore, the resonant tank design trade-offs still limits the load capacity. Further, phase shedding in this configuration is difficult, which is deemed an important feature for improving light-load efficiency. Similarly, the Y-LLC proposed in [5] also has difficulties realizing phase shedding.

In this paper, a switch-controlled capacitor (SCC) [9] is used to regulate each LLC stage (SCC-LLC), thus the

978-1-4673-0803-8/12/$31.00 ©2012 IEEE

resonant frequency becomes the control variable instead of the switching frequency. As a result, the regulation is done in individual phases while the switching frequencies of all phases are constant and identical. This advantage enables a simple interleaving structure, thus load sharing and phase shedding are easy to implement. The system's load capacity can be expanded by paralleling an arbitrary number of phases. Also, the constant switching frequency is favorable for higher level integration. In the following sections, Section II describes the operation of the switch-controlled capacitor, Section III discusses the analysis and the design procedure of SCC-LLC, and Section IV shows the experimental results of a 600W prototype.

II. Operation of Switch-Controlled Capacitor

The concept of switch-controlled capacitor (SCC) is introduced in 1980s [9]. The driving scheme for SCC is further improved in this paper to prevent the MOSFET body diodes from carrying current, and the resulting SCC is applied in LLC converters to obtain the benefits that were discussed in the introduction.

The structure of SCC is shown in Fig. 1, which consists of two drain-to-drain connected MOSFETs, S_1 and S_2, and a parallel capacitor, C_a. The charge of C_a can be controlled by S_1 and S_2 therefore the equivalent capacitance can be modulated. The operation waveforms are in Fig. 2 and are described as follows.

When a sinusoidal current, I_{AB}, is applied to the SCC unit, the current zero-crossing points are at angle *0, π, 2π* …etc. For a positive half-cycle where the current flows from A to B, the gating signal of S_1 is synchronized at $2n\pi$ ($n \in N$), and turns off S_1 at angle $2n\pi+\alpha$, where $\pi/2<\alpha<\pi$.

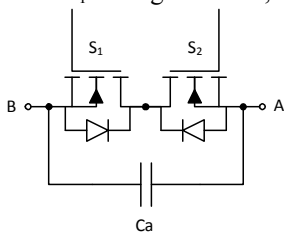

Figure 1 Structure of SCC.

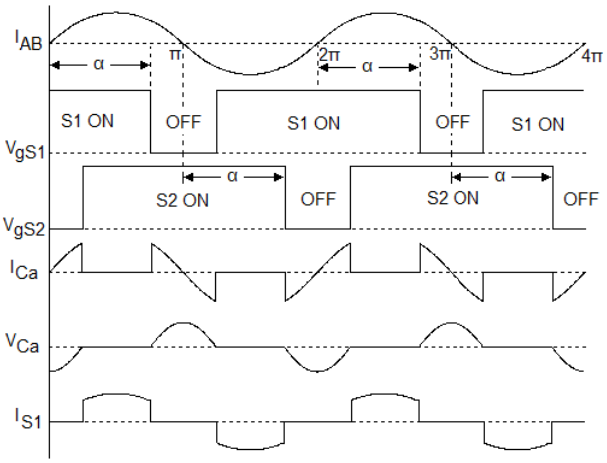

Figure 2 Waveforms of SCC.

The current then flows from A to B via C_a and charges up the C_a voltage until the angle $(2n+1)\ \pi$. At the angle $(2n+1)\ \pi$, the current reverses the direction, and begins to discharge C_a. After C_a is fully discharged, and the negative current is about to flow from B to A via S_1's body diode, S_1 is turned on again to prevent the body diode from carrying current. Then S_1 remains on for the rest of the cycle and turns off again at angle $(2n+2)\ \pi + \alpha$, which is α angle past the next sync point $(2n+2)\ \pi$. S_2 controls the negative half-cycle and has the same procedure, except the sync point is at $(2n+1)\ \pi$. It is observed in Fig. 2 that S_1 and S_2 are switched both on and off at ZVS conditions. The voltage amplitude of C_a can be designed to be below 100V thus low on-resistance MOSFETs can be used and the power loss in the SCC unit is minimum.

The equivalent capacitance of SCC, C_{SC}, is modulated by the turn-off angle α, given in (1) [9].

$$C_{SC} = \frac{C_a}{2-(2\alpha-\sin 2\alpha)/\pi} \qquad (1)$$

III. Analysis and Design of SCC-LLC

The proposed half-bridge SCC-LLC is shown in Fig. 3. The SCC unit is connected in series with the resonant tank in order to modulate the equivalent resonant capacitance, C_r, and thus to control the resonant frequency. As it is derived in many literatures [2-4], the gain of LLC converters is modulated by the ratio of the switching frequency and the resonant frequency. Likewise, with constant switching frequency, varying the resonant frequency can also modulate the gain, which is accomplished by controlling the switching angle α in the SCC. The analysis and the design procedures are described below.

A. Constant Switching Frequency LLC Design

The properties of the constant switching frequency LLCs are different than that of variable switching frequency LLCs: 1. the peak gain is solely determined by the magnetizing or parallel inductance, which will be discussed further below in this section; 2. the worst-case magnetizing current for ZVS happens at the full-load condition, because in constant switching frequency LLCs, the resonant frequency is the highest at full load while the switching period does not change; consequently the resonance time is the shortest, resulting in the smallest magnetizing current at the switching point. For above reasons, the design considerations of constant switching frequency LLCs are different than that of variable switching frequency LLCs, and are given as follows.

Firstly determine the switching frequency, ω_s, in radians, and the transformer turns ratio, N. The turns ratio is selected such that the required gain of the LLC resonant tank is slightly above unity during normal operation. And thus, the nominal gain required for the nominal input voltage scenario is calculated in (2), where η is the efficiency, $E_{i,nom}$ is the nominal input voltage , and E_o is the output voltage.

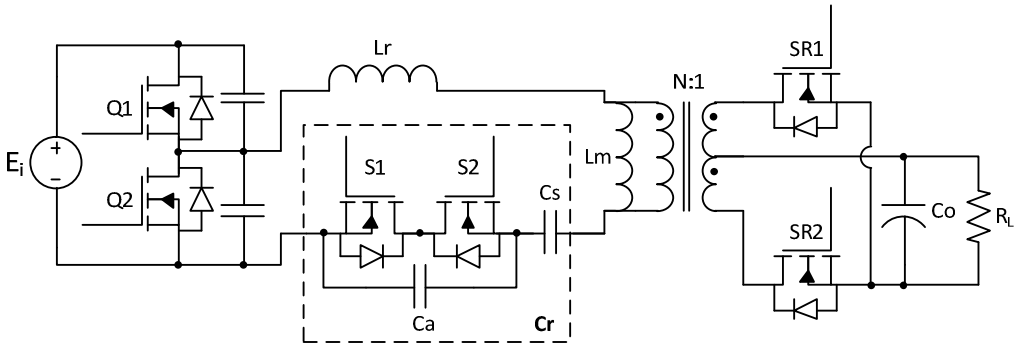

Figure 3 Topology of the proposed SCC-LLC.

$$M_{nom} = \frac{NE_o}{\eta E_{i,nom}/2} \tag{2}$$

Similarly, the peak gain required for the minimum input voltage scenario is:

$$M_{pk} = \frac{NE_o}{\eta E_{i,\min}/2} \tag{3}$$

The next step is to determine the parallel inductance, L_p, which can be implemented using the magnetizing inductance of the transformer. There are two constraints for the design of L_p: full-load ZVS condition and the peak gain requirement. Usually the peak gain requirement is more restrictive, but for applications that require a low peak gain, the full-load ZVS condition can be dominant. The designer must calculate L_p for both constraints, and select the value that can fulfill both.

The derivation for the full-load ZVS constraint is as follows: Let I_{ZVS} be the magnetizing current at the switching point and ω_{FL} be the resonant frequency at full load. Assuming the magnetizing current rises from $-I_{ZVS}$ to I_{ZVS} linearly within the resonance time π/ω_{FL}, and remains approximately unchanged until the switching point, we can get:

$$I_{ZVS} = \frac{NE_o\pi}{2L_p\omega_{FL}} \tag{4}$$

At nominal input voltage, I_{ZVS} must be sufficient to charge and discharge the MOSFET junction capacitance C_j within the dead time t_d, thus:

$$I_{ZVS} \geq \frac{2E_{i,nom}C_j}{t_d} \tag{5}$$

Combine (4) and (5) and get:

$$L_p \leq \frac{t_d\pi NE_o}{4\omega_{FL}E_{i,nom}C_j} \tag{6}$$

Equation (6) defines the required L_p for the full-load ZVS condition. The ω_{FL} will be calculated later in this section.

The derivation for the peak gain constraint is as follows: Use Fundamental Harmonic Approximation (FHA) approach, starting from basic LLC equations in [2] but derived in a different way, and get the gain expression of the LLC resonant tank, in (7):

$$M(\omega_i) = \frac{1}{\sqrt{\left(\frac{\omega_i^2-1}{K}-1\right)^2 + \frac{\pi^4\omega_s^2L_p^2}{64N^4R_L^2}\left(\frac{\omega_i^2-1}{K}\right)^2}} = \frac{1}{\sqrt{\left(\frac{\omega_i^2-1}{K}-1\right)^2 + Q^2\left(\frac{\omega_i^2-1}{K}\right)^2}} \tag{7}$$

where K is the inductance ratio, L_p/L_r; R_L is the load resistance, and ω_i is the resonant frequency normalized at the switching frequency, ω_r/ω_s. The notation "i" stands for inverse normalization as oppose to that in variable switching frequency LLC analysis where switching frequency often be normalized at the resonant frequency. Q is the factor defined in (8), where R_{ac} is the load resistance reflected to the primary side.

$$Q = \frac{L_p\omega_s}{R_{ac}} = \frac{\pi^2L_p\omega_s}{8N^2R_L} \tag{8}$$

Let $X = \frac{\omega_i^2-1}{K}$, Equation (7) can be rewritten as:

$$M(X) = \frac{1}{\sqrt{(X-1)^2+Q^2X^2}} = \frac{1}{\sqrt{(1+Q^2)X^2-2X+1}} \tag{9}$$

The denominator in (9) is a parabolic function; therefore the peak gain, M_{pk}, can be solved in (10).

Equation (10) reveals that the peak gain of the SCC-LLC is determined by Q and is independent from K. Recall (8), since the switching frequency ω_s, the transformer turns

ratio N and the load resistance R_L are determined beforehand, the peak gain M_{pk} is solely determined by the parallel inductance L_p.

$$M_{pk} = \sqrt{\frac{1}{Q^2}+1} \quad \text{at} \quad X = \frac{1}{1+Q^2} \tag{10}$$

Further derivation from (10) yields the following relations:

$$\omega_{iPK} = \sqrt{K+1-\frac{K}{M_{pk}^2}} \tag{11}$$

$$L_p = \frac{8N^2 R_{L,FL}}{\pi^2 \omega_s \sqrt{M_{pk}^2-1}} \tag{12}$$

where ω_{iPK} is the normalized resonant frequency at which the peak gain occurs; $R_{L,FL}$ is the load resistance at full load.

Equation (11) reveals that the K only determines the frequency at which the peak gain occurs. The properties that are revealed by (10) and (11) can be observed from the gain plots drawn using (7), in Fig. 4. In which, Q is given,

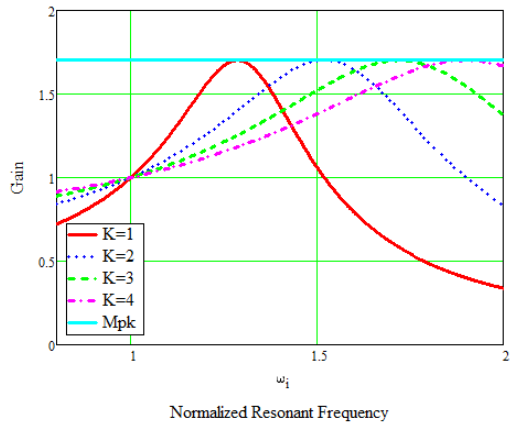

Figure 4 Gain plot, varying K.

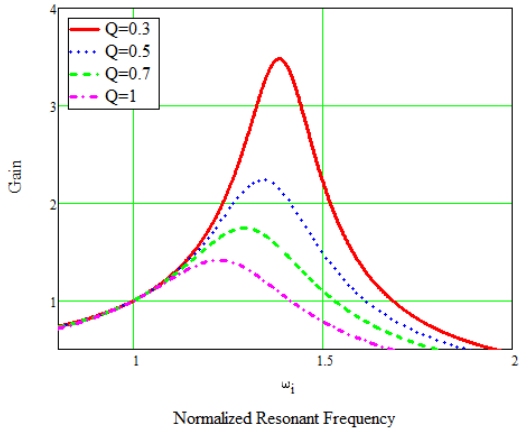

Figure 5 Gain plot, varying Q.

and varying K only changes the slope of the gain curves, whereas the peak gain amplitude remains the same. Fig. 5 illustrates how the peak gain changes with Q. Since ω_s, $R_{L,FL}$ and N are determined already, (12) is used to calculate L_p according to the peak gain requirement.

The next step is to determine the inductance ratio, K. The selection of K is discussed below.

From Fig. 4, it is observed that, the smaller the K, the steeper the gain slope, thus the less the operating resonant frequency deviates from the switching frequency. However, in contrast with that in variable switching frequency LLCs, a small K in the constant switching frequency LLC does not result in less circulating energy. In fact, the magnetizing current even decreases slightly with a larger K. This is because the switching period is fixed, and with a larger K, the resonant frequency needs to be higher to achieve the same gain, which yields shorter resonance time for the magnetizing current to build up linearly. Nevertheless, a higher resonant frequency will cause the secondary RMS current to be higher. So from the RMS current point of view, there are still advantages of using a small K value.

However, the selection of K should also take into account the magnetic design and the resonant capacitor voltage. A small K indicates a large resonant inductor, which may be difficult to implement using the transformer's leakage inductance. Also, a large resonant inductor indicates small resonant capacitance being used to achieve the same resonant frequency; therefore, the capacitor voltage will be high, thus high voltage-rating MOSFETs will be used in the SCC unit accordingly. Because high-voltage MOSFETs have high on-resistance, the primary-side conduction loss will increase.

With above considerations in mind, different K values can be tested in the following steps to find the trade-off:

From (9), with a given gain M, the X can be solved as:

$$X = \frac{1 \pm \sqrt{\frac{1+Q^2}{M^2}-Q^2}}{1+Q^2} \tag{13}$$

Then ω_i can be solved from the definition of X:

$$\omega_i = \sqrt{KX+1} = \sqrt{\frac{K \pm K\sqrt{\frac{1+Q^2}{M^2}-Q^2}}{1+Q^2}+1} \tag{14}$$

The ω_i has two roots for a given gain M, as can be observed in Fig. 5. The smaller root is chosen because it is in the ZVS region; the larger root is in the ZCS region, which is undesired. Thus, the normalized resonant frequency at full load, ω_{iFL}, can be calculated in (15), where Q_{FL} is the Q value corresponding to the full-load output resistance, $R_{L,FL}$.

Then the peak capacitor voltage can be estimated using (16). Plug in $E_i=E_{i.nom}$, $\omega_i=\omega_{iFL}$ and $E_i=E_{i.min}$, $\omega_i=\omega_{iPK}$ to calculate the peak resonant capacitor voltage, respectively, as both cases can be the worst case.

$$\omega_{iFL}=\sqrt{\frac{K-K\sqrt{\frac{1+{Q_{FL}}^2}{M_{nom}^2}-{Q_{FL}}^2}}{1+{Q_{FL}}^2}+1} \tag{15}$$

$$v_{Cr,\max}=\left[\frac{E_o\pi}{R_L N\omega_s}+\frac{NE_o}{2L_p}\cdot\frac{\pi}{\omega_i\omega_s}\left(\frac{\pi}{\omega_s}-\frac{3\pi}{4\omega_i\omega_s}\right)\right]\cdot\frac{(\omega_i\omega_s)^2 L_p}{2K}+\frac{E_i}{2} \tag{16}$$

It is found that K=*5~7* is a reasonable trade-off. Smaller K value can only slightly reduce the secondary RMS current at the expense of significantly increased resonant capacitor voltage, which results in high on-resistance MOSFET to be used in the SCC unit.

The last step is to check the full-load ZVS constraint: convert the full-load resonant frequency ω_{iFL} obtained from (15) into the absolute resonant frequency ω_{FL}, and then substitute into (16) to get the L_p value that fulfills the full-load ZVS constraint. Compare the L_p values obtained from (6) and the one from (12), and choose the smaller L_p value which will fulfill both constraints. Once L_p and K are chosen, L_r is determined at the same time.

Note that the equations derived from FHA are less accurate when the resonant frequency is further deviated from the switching frequency, because the resonant current is no longer sinusoidal. As a result, the L_p calculated from (12) tend to provide a higher peak gain than needed, hence the actual peak resonant frequency and the peak resonant capacitor voltage will be lower than those calculated from (11) and (16). This inaccuracy results in a tendency of over-design, but nevertheless provides some useful margins to take into account the component tolerances.

B. SCC Design

The SCC unit is connected in series with a series capacitor, C_s, in order to modulate the resonant capacitance C_r. The SCC equivalent capacitance, C_{SC}, is given in (1). The total equivalent resonant capacitance, C_r, can be calculated using (17).

$$C_r=\frac{C_{SC}C_s}{C_{SC}+C_s}=\frac{\pi C_a C_s}{\pi C_a+2\pi C_s-2\alpha C_s+C_s\sin(2\alpha)} \tag{17}$$

where $\frac{\pi}{2}\le\alpha\le\pi$.

By substituting (17) into (7), the SCC-LLC's gain expression as a function of the control angle α is derived in (18).

$$M(\alpha)=\frac{K}{\sqrt{\left(\frac{\pi C_a+2\pi C_s-2\alpha C_s+C_s\sin(2\alpha)}{\omega_s^2 L_r\pi C_a C_s}-K-1\right)^2+Q^2\left(\frac{\pi C_a+2\pi C_s-2\alpha C_s+C_s\sin(2\alpha)}{\omega_s^2 L_r\pi C_a C_s}-1\right)^2}} \tag{18}$$

The first step in SCC design is to determine the objective minimum and maximum equivalent capacitance. The minimum equivalent capacitance is determined by the resonant frequency at which the peak gain is achieved:

$$C_{r,\min}=\frac{1}{(\omega_s\omega_{iPK})^2 L_r} \tag{19}$$

The maximum equivalent capacitance is determined by the resonant frequency at which the burst mode will be triggered. The burst-mode resonant frequency can be calculated in (20).

$$\omega_{i,burst}=\sqrt{\frac{K-K\sqrt{\frac{1+Q_{burst}^2}{M_{nom}^2}-Q_{burst}^2}}{1+Q_{burst}^2}+1} \tag{20}$$

where $Q_{burst}=\frac{\pi^2 L_p\omega_s}{8N^2 R_{L,burst}}$

Then the maximum equivalent capacitance can be calculated in (21).

$$C_{r,\max}=\frac{1}{(\omega_s\omega_{i,burst})^2 L_r} \tag{21}$$

The next step is to determine the maximum and the minimum control angle of the SCC. Theoretically, the angle α is from 0.5π to π. However, in order to ensure the reliability of the driving scheme, it is better to make α_{max} slightly below π and make α_{min} slightly above 0.5π.

A plot of the control angle α versus the equivalent resonant capacitance C_r that is described in (17) is illustrated in Fig. 6, in which the C_r curve becomes flat when α is beyond 0.9π. This characteristic holds true for most reasonably designed C_s and C_a values. Because the flat α versus C_r curve indicates a reduction of the loop gain, it is suggested to place α_{max} below 0.9π in order to ensure the dynamic performance.

The last step of SCC design is to solve for C_s and C_a. By substituting two sets of values, $C_{r,max}$, α_{max} and $C_{r,min}$, α_{min}, into (17), respectively, C_s and C_a can be solved, in (22) and (23).

Finally, an example of the SCC control angle versus the SCC-LLC gain is plotted in Fig. 7 using (18).

It is desired to have the peak SCC voltage less than 100V due to the fact that the MOSFETs rated below 100V have significantly lower $R_{ds(on)}$ than those above 100V. The

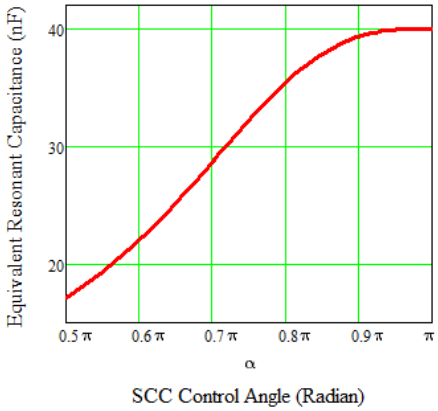

Figure 6 SCC Control Angle VS. Equivalent Resonant Capacitance.

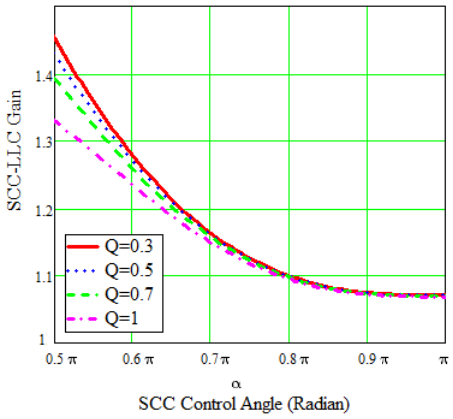

Figure 7 SCC Control Angle VS. SCC-LLC Gain.

maximum C_a voltage occurs at $\alpha=0.5\pi$ in which case C_a is always connected in series with C_s; therefore its peak voltage is estimated by C_a and C_s proportionally dividing the peak C_r voltage that is calculated in (16), given in (24).

$$C_a = \frac{[\sin(2\alpha_{\min}) - \sin(2\alpha_{\max}) + 2\alpha_{\max} - 2\alpha_{\min}]}{(C_{r,\max} - C_{r,\min})\pi} C_{r,\min} C_{r,\max} \tag{22}$$

$$C_s = \frac{[\sin(2\alpha_{\min}) - \sin(2\alpha_{\max}) + 2\alpha_{\max} - 2\alpha_{\min}]}{(2\alpha_{\max} - \sin(2\alpha_{\max}) - 2\pi)C_{r,\max} + (\sin(2\alpha_{\min}) - 2\alpha_{\min} + 2\pi)C_{r,\min}} C_{r,\min} C_{r,\max} \tag{23}$$

$$v_{Ca,\max} = \frac{C_s}{C_s + C_a} v_{Cr,\max} \tag{24}$$

IV. Experimental Results

A 600W two-phase interleaved SCC-LLC is implemented to verify the effectiveness of the proposed method. The diagram of the prototype is shown in Fig. 8, and the parameters are in Table 1.

Table 1 Prototype parameters

Switching frequency	200kHz
Input Voltage	400V nominal/300V minimum
Output Voltage	12V
Output Power	300W × 2
Transformer Turns Ratio	20:1, Center tapped
Magnetizing Inductance	87μH(Phase1) 85μH(Phase2)
Resonant Inductance	12μH(Phase1) 14μH(Phase2)
Series Capacitance	36nF±5%
SCC Capacitance	30nF±3%
Output Capacitance	1790μF (100μF× 8, 330μF× 3)
Half-bridge MOSFET	Infineon IPB60R190C6
SCC MOSFET	Infineon BSC060N10NS3 G
SR MOSFET	Infineon BSC011N03LS

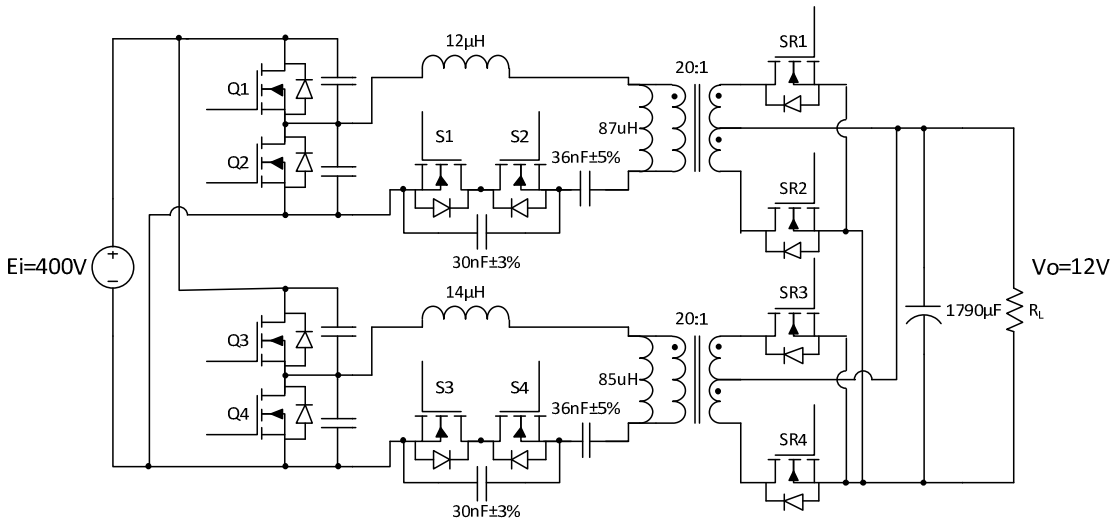

Figure 8 The implemented two-phase interleaved SCC-LLC.

The resonant inductors of the two phases are utilizing the transformers' leakage and are intentionally made non-identical in order to test the proposed method. The resonant capacitors also have tolerances. Phase 2 (lower) has 90˚ phase shift with respect to Phase 1 (upper).

A Microchip DSC dsPIC33FJ32GS606 is used to implement the digital controller. The SCC PWM is synchronized with the primary current zero-crossing points using the External PWM Reset (XPRES) function, which allows current transformers to send a signal to reset the PWM every time when the current crosses zero.

The load sensing circuitry is adopted from [10]. A slow load sharing loop is implemented digitally.

Fig. 9 and Fig. 10 demonstrate the effectiveness of SCC modulation. V_{ca} is the voltage of C_a; V_{gs_S1} is the gating signal of S_1; V_{gs_S2} is the gating signal of S_2; I_{pri} is the primary current. Fig. 9 shows the 20A output current scenario; the control angle α is 131˚. Fig. 10 shows the 10A output current scenario; the control angle α is 136˚.

Fig. 11 and Fig. 12 show the effectiveness of the current ripple cancellation and the load sharing. $V_{o,p-p}$ is the output ripple voltage, AC coupled; I_{pri} is the primary current of a single-phase LLC; I_{pri_ph1} is the primary current of Phase 1; I_{pri_ph2} is the primary current of Phase 2. Both Fig. 11 and Fig. 12 show 50A output current scenario. Fig. 11 shows a comparable 600W single-phase LLC converter, with identical output capacitance that is used in the prototype SCC-LLC. The output voltage ripple is measured 500mV peak to peak. Fig. 12 shows the proposed two-phase interleaved SCC-LLC converter. The output voltage ripple is reduced to 180mV peak to peak. The ripple cancellation can perform even better if external resonant inductors are used, which will make the resonant inductance of the two half-switching cycles better symmetrical. Fig. 12 also proves that the output current of the two phases are very well balanced.

Fig. 13 shows the efficiency curves of the two-phase interleaved SCC-LLC with and without phase shedding. It is shown that the heavy load efficiency approaches 96%; and with phase shedding, the efficiency at 5A load is improved from 81% to 90%.

Fig. 14 shows a photo of the prototype board.

V. Conclusion

In this paper, an interleaved SCC-LLC resonant converter is proposed to expand load capacity, reduce output current ripple, and improve light-load efficiency with phase shedding. It solves the load sharing problem by using SCC (switch-controlled capacitor) to modulate the voltage gain of individual LLC stages while all LLC stages are operating at a constant switching frequency. Detailed analysis and design procedure are presented in this paper. The two-phase 600W prototype proves the feasibility of the proposed method, and shows good load sharing performance and light-load efficiency improvements.

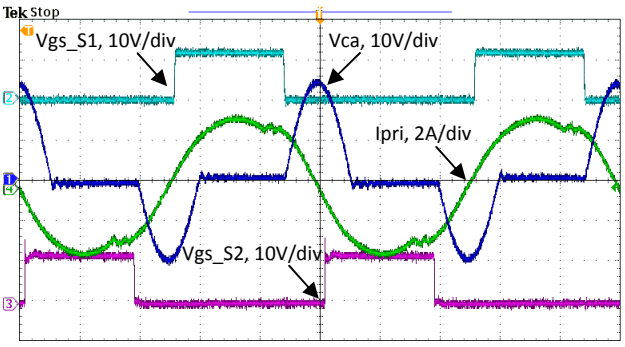

Figure 9 SCC operation, I_o=20A, α=131˚.

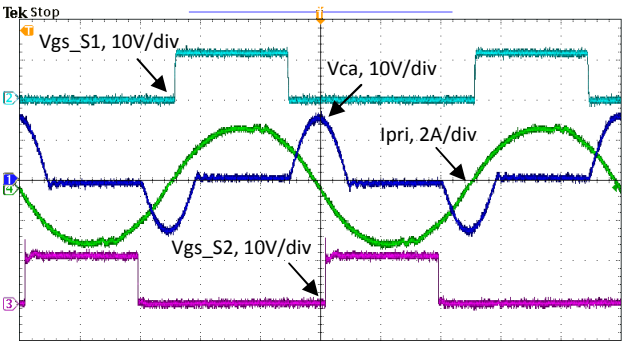

Figure 10 SCC operation, I_o=10A, α=136˚.

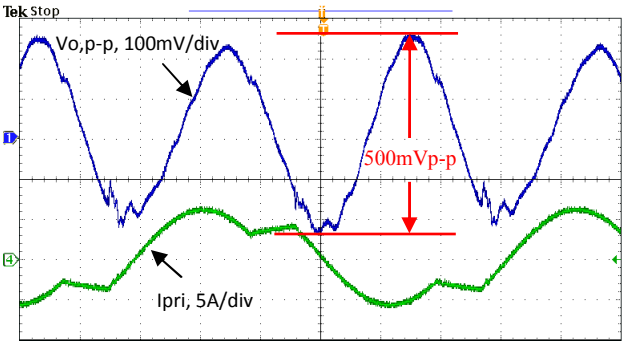

Figure 11 Output voltage ripple, I_o=50A, single phase LLC.

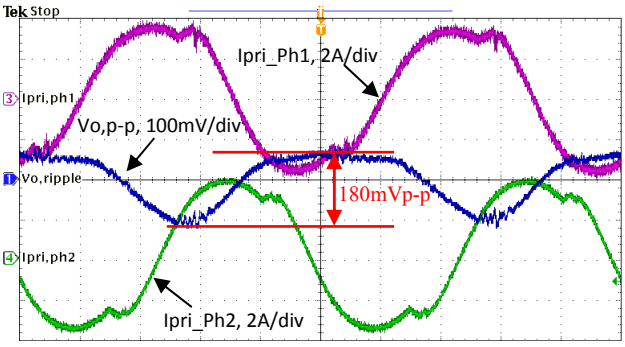

Figure 12 Output voltage ripple, I_o=50A, two-phase interleaved SCC-LLC.

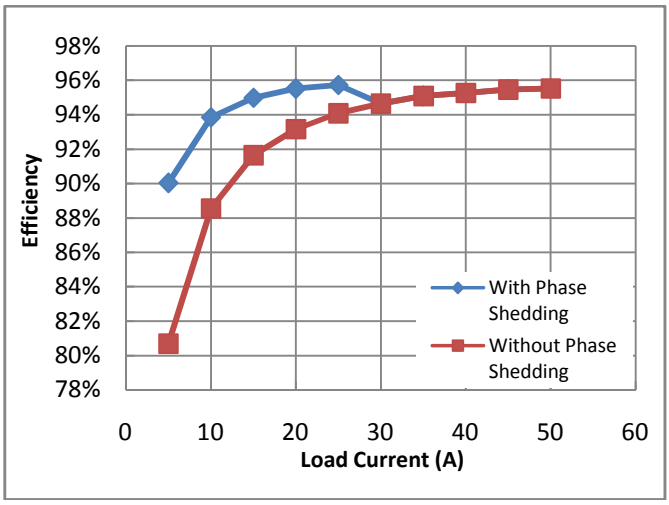

Figure 13 Efficiency comparison.

Figure 14 Prototype photo.

REFERENCE

[1] B. Yang, F. C. Lee, A. J. Zhang and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. Appl. Power Electron. Conf. and Expo. (APEC)*, Dallas, TX, 2002, vol. 2, pp. 1108-1112.

[2] Y. Zhang, D. Xu, M. Chen, Y. Han and Z. Du, "LLC resonant converter for 48 V to 0.9 V VRM," in *Proc. Power Electron. Specialists Conf. (PESC)*, Aachen, Germany, 2004, Vol. 3, pp. 1848-1854.

[3] S. De Simone, C. Adragna, C. Spini and G. Gattavari, "Design-oriented steady-state analysis of LLC resonant converters based on FHA," in *Proc. Int. Symposium on Power Electron., Electrical Drives, Automation and Motion (SPEEDAM),* Taormina, Italy, 2006, pp. 200-207.

[4] B. Lu, W. Liu, Y. Liang, F. C. Lee and J. D. van Wyk, "Optimal design methodology for LLC resonant converter," in *Proc. Appl. Power Electron. Conf. and Expo. (APEC)*, Dallas, TX, 2006, pp 533-538.

[5] E. Orietti, P. Mattavelli, G. Spiazzi, C. Adragna and G. Gattavari, "Current sharing in three-phase LLC interleaved resonant converter," in *Proc. Energy Conversion Congr. and Expo. (ECCE)*, San Jose, CA, 2009, pp. 1145-1152.

[6] T. Jin and K. Smedley, "Multiphase LLC Series Resonant Converter for Microprocessor Voltage Regulation," in *Conf. Rec. of. 2006 Ind. Applicat. Conf., 41st Ind. Applict. Soc. (IAS) Annu. Meeting.*, Tampa, FL, 2006, pp. 2136-2143.

[7] H. Figge, T. Grote, N. Froehleke, J. Boecker and P. Ide, "Paralleling of LLC resonant converters using frequency controlled current balancing," in *Proc. Power Electron. Specialists Conf. (PESC)*, Island of Rhodes, Greece, 2008, pp. 1080-1085.

[8] B.-C. Kim, K.-B. Park, C.-E. Kim, G.-W. Moon, "Load sharing characteristic of two-phase interleaved LLC resonant converter with parallel and series input structure," in *Proc. Energy Conversion Congr. and Expo. (ECCE)*, San Jose, CA, 2009, pp. 750-753.

[9] W.-J. Gu and K. Harada, "A new method to regulate resonant converters," *IEEE Trans. Power Electron.*, vol. 3, no. 4 pp. 430-439, Oct. 1988.

[10] "L6599 High-voltage resonant controller," STMicroelectronics, Datasheet, Feb. 2009.