Predictable Auxiliary Switching Strategy to Improve Unloading Transient Response Performance for DC–DC Buck Converter

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***Abstract*—In this paper, a novel control strategy is presented, which is capable of controlling a 12-V–1.5-V main buck converter and an auxiliary circuit to achieve significantly improved unloading response performance. While the charge balance controller minimizes the settling time of the main buck converter, the auxiliary circuit is controlled in boundary conduction mode (BCM) for a predictable pattern of auxiliary switching to reduce the output overshoot. Therefore, the reliability and dynamic performance of the entire system is significantly enhanced. Compared with existing technologies, the proposed BCM auxiliary switching strategy achieves improved output voltage overshoot and reduced auxiliary power losses at the same time. Furthermore, numerical analysis of the improved output voltage overshoot and reduced auxiliary power losses has been conducted for a design guideline. Finally, simulation and experimental results are provided to verify the proposed scheme on a 12-V–1.5-V 10-A buck converter prototype.**

***Index Terms*—Boundary conduction mode (BCM), buck converter, capacitor charge balance controller (CBC), controlled auxiliary current (CAC), fast transient response, predictable auxiliary switching.**

I. Introduction

As THE computing capabilities of high-performance digital devices continue to expand, the demand on the power supplies for powering such devices becomes increasingly stringent. Thus, extensive research has been conducted, developing advanced controllers which improve the transient performance of buck converters to their physical limits. In [1]–[14], controllers have been presented, which apply second-order sliding surfaces, precalculated switching time intervals, or capacitor charge balance methodologies to reduce the voltage deviation and settling time of a buck converter, undergoing a load transient, to its virtually optimal level. However, in [1] and [6], it is demonstrated that, for a commonly used 12-V–1.5-V buck converter even under optimal control, the undesired large output voltage overshoot still dominates the output capacitance requirement, because of the much worse and marginally improved unloading response performance. To address the asymmetrical response, a two-stage power conversion scheme is presented in [12], which creates a 5-V intermediate dc bus voltage to balance the stage conversion ratio close to 50% but adds more power loss, cost, and board space to the entire system.

Many auxiliary circuitries are reviewed in [14] to reduce the output voltage overshoot, and the one shown in Fig. 1, coupled with its control law, has the following advantages: 1) predictable behavior, allowing for a simplified design; 2) inherent overcurrent protection; and 3) low peak-current-to-average-current ratio, allowing for the use of smaller components. However, the auxiliary converter operates for very high switching frequency (more than megahertz) during the activation period under a relatively complex average current mode control law, which downgrades the enhancement if applied to a multiphase buck converter. In [15], another overshoot reduction solution using the aforementioned auxiliary circuit with an external energy storage capacitor and synchronous rectifier (SR) implementation is provided; however, the practicality is limited due to the additional linear compensator, the subsequent high-frequency switching of the auxiliary converter and the unimproved settling time. In [18], a similar paralleled SR buck converter is used to achieve fast response of the main converter. Output voltage is monitored to activate and deactivate the auxiliary circuit. The single pulse auxiliary current behavior is not fully predictable: 1) No inherent overcurrent protection is available to avoid auxiliary inductance saturation, and 2) auxiliary switching frequency is not under control or switching frequencies may become excessive when the output voltage (or derivative of the output voltage) begins to oscillate around the threshold points [14].

In this paper, a practical auxiliary current control strategy is presented to improve unloading transient performance, which has the following unique advantages: 1) predictable auxiliary switching pattern based on the main–auxiliary inductance ratio; 2) the auxiliary circuit operating at relatively low frequency to reduce the switching loss; 3) further voltage overshoot reduction; and 4) minimizing the settling time of unloading response based on charge balance principles.

This paper is organized as follows. In Section II, the operating principles of the proposed scheme are presented. The

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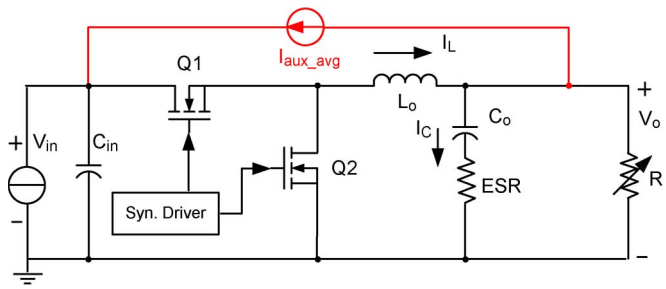

Fig. 1. Simplified model of the proposed CAC.

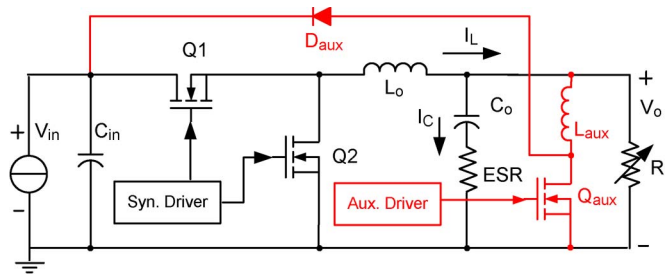

Fig. 2. MOSFET–diode implementation of the CAC.

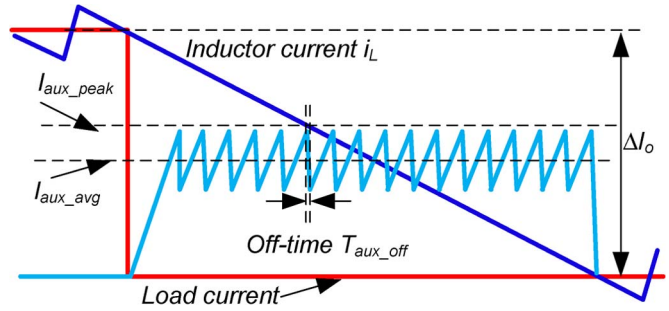

Fig. 3. PCM constant off-time operation of the proposed controller in [14].

analysis of voltage overshoot and power loss is made in Section III, followed by hardware implementation in Section IV. The simulation and experimental results are shown in Section V. The conclusions are drawn in Section VI.

II. Operating Principles of the Proposed Control Scheme

Because of the asymmetrical response in a low-duty-cycle dc–dc conversion application (e.g., 12-V–1.5-V buck converter), to adhere to voltage specifications, capacitor selection must be based on the larger voltage overshoot condition [14]. By using charge balance controller (CBC) or other fast response controllers, undershoot is much lower than overshoot and easier to meet the derivation specifications. So, the proposed scheme will focus on addressing the much higher overshoot. When a buck converter undergoes an unloading transient, it is important to reduce the current going through the output capacitor in order to reduce the output voltage overshoot. As stated in [5], the load current falls at a much higher slew rate than the inductor current; the capacitor must absorb charge (and thus, output voltage increases). The voltage overshoot may be reduced by modifying the output filter parameters, i.e., by decreasing the size of the output inductor (resulting in decreased efficiency due to larger peak and, thus, rms MOSFET current levels and/or increased switching frequency) or by increasing the size of the output capacitor (resulting in a significantly higher cost of the buck converter).

Alternatively, the amount of charge absorbed by the capacitor can be reduced by diverting excess current from the output inductor of the buck converter to the converter's input through operation of the proposed controlled auxiliary circuit. As will be shown, a large reduction in the output voltage overshoot can be realized by the addition of a small inductor, MOSFET, and diode. The auxiliary circuit can be modeled as a controlled current source, drawing current from the output capacitor of the buck converter and transferring it to the input of the buck converter. Fig. 1 shows the model of such method when used with a synchronous buck converter. The controlled auxiliary current (CAC) is only active during step-down load current transients (i.e., before and after an unloading transient, the circuit operates as a conventional buck or synchronous buck converter).

Fig. 2 shows the implementation of the auxiliary circuit used in this paper. An alternate implementation would involve using a second MOSFET (instead of $D_{\rm aux}$) for synchronous rectification. As is shown, the auxiliary circuit resembles a small boost converter connected in antiparallel with the buck converter.

In [14], a CAC is presented to improve the transient response of a buck converter, as shown in Fig. 3. The activation duration (when the auxiliary current is operating) is regulated based on charge balance control principle. That method has the following advantages: 1) predictable behavior, allowing for a simplified design; 2) inherent overcurrent protection; and 3) low peak-current-to-average-current ratio, allowing for the use of smaller components.

This method also estimates the magnitude of the unloading transient and sets the auxiliary current proportional to the transient magnitude. This allows for greater design flexibility and increases the auxiliary circuit efficiency for unloading transients of lower magnitude. The auxiliary is controlled by constant off-time peak current control scheme shown in Fig. 3.

However, this controller requires the high switching frequency of the auxiliary circuit. For example, in order to maintain the average value of the auxiliary current for a two-phase voltage regulator (VR) with 360 nH per phase output inductance, the switching frequency of the auxiliary switch will be above 5 MHz, resulting in highly increased switching losses, gate drive losses, and auxiliary MOSFET driver cost. Also, the controller design is relatively complex with constant $T_{\rm aux\_off}$ delay time injection, load current estimation, and filtered current sensing.

In this paper, a new auxiliary switching pattern is presented based on charge balance control to resolve the aforementioned issues. In order to achieve charge balance, the proposed pattern includes precisely CAC wave shape and predictable activation time. The current shape of the auxiliary circuit is controlled by peak current mode (PCM) but in boundary conduction mode (BCM), and the peak current level is set to be equal to the current step value ΔI_o. So, the triangular auxiliary current will be switched between zero and ΔI_o (shown in Figs. 7 and 11). On the other hand, the activation time of the auxiliary current can be simply and reliably controlled by counting the

predictable number of auxiliary switching based on the design parameter. In this way, the auxiliary switching frequency and power losses can be significantly reduced.

III. Voltage Overshoot Estimation and Design Guidelines

In this section, the numerical analysis of the voltage overshoot improvement is presented. More detailed derivations of the equations in this section will be provided in the Appendix.

A. Voltage Overshoot Estimation Using the Proposed CAC

Without loss of generality, it is assumed that the auxiliary circuit is switched for n times under BCM PCM control, where integer n is the number of auxiliary switching cycles. Upon that, the instantaneous output voltage variation can be expressed as (1), shown at the bottom of the page, for two intervals depending on the ON/OFF state of the auxiliary circuit and the Nth time of switching, where $T_{\rm aux}$ is the switching period of the auxiliary current and $d_{\rm aux}$ is the duty cycle of the auxiliary converter.

The output overshoot/maximum voltage will occur at the time $t_{\rm ost}$ in (2), when the derivative of (1) is zero during the $(N'+1)$th switching, where N' is calculated in (3) depending on the parity of n

$$t_{\rm ost} = \frac{D_{\rm aux}+N'}{D_{\rm aux}+n}\cdot nT_{\rm aux} \tag{2}$$

$$N' = \begin{cases} \frac{n-1}{2}, & (\text{when } n \text{ is odd}) \\ \frac{n}{2}-1, & (\text{when } n \text{ is even}). \end{cases} \tag{3}$$

Based on the average auxiliary current $L_{\rm aux\_avg}$ without considering the auxiliary inductor current ripple under the BCM PCM control, a simplified equation is provided as a practical method to calculate the overshoot in (4). The symbols L_o, C_o, ESR, ΔI_o, V_o, and $L_{\rm aux}$ represent the output inductance, output capacitance, equivalent series resistance, load step value, output voltage, and auxiliary inductance, respectively,

$$\Delta V_o \approx \frac{\left(\frac{\Delta I_o}{2}\right)^2\cdot L_o^2+\text{ESR}^2\cdot C_o^2\cdot V_o^2}{2V_o\cdot L_o\cdot C_o}+\frac{\left(\frac{\Delta I_o}{2}\right)^2\cdot L_{\rm aux}}{2V_o\cdot C_o}. \tag{4}$$

Another advantage of the proposed scheme is that, under a certain value of step-down load transient, the number n of auxiliary switching can be predicted using the input and output voltage information as well as the inductance ratio of L_o and $L_{\rm aux}$. The number of switching n can be estimated using (5), where

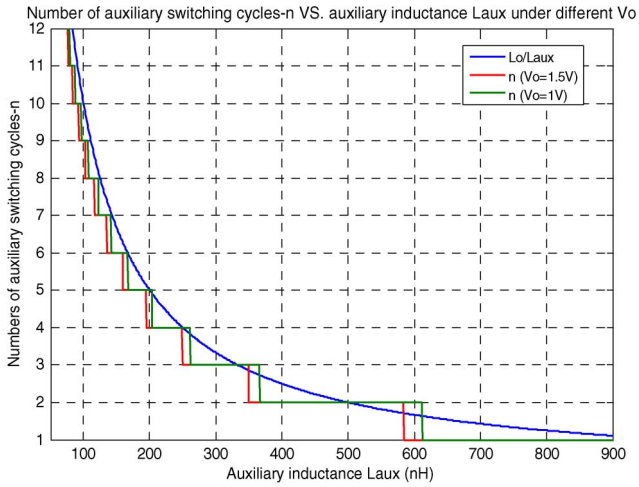

Fig. 4. Number of auxiliary switching cycles n (as well as the ratio of $L_o/L_{\rm aux}$) and the auxiliary inductance value under different output voltages V_o.

$[]_{\rm int}$ indicates the rounding down operation. It is noted that n is independent of the load transient step value ΔI_o. Another remarkable advantage of this proposed scheme is the insensitivity of the ESR in the output capacitor. According to the charge balance concept which remains valid regardless of ESR, once the CAC switches following the proposed pattern for n times, the excess charge in the output capacitor will be removed. As a result, the output voltage will recover to the reference value

$$n = \left[\frac{(V_{\rm in}-V_o)L_o}{L_{\rm aux}\cdot V_{\rm in}}+0.5\right]_{\rm int}. \tag{5}$$

Fig. 4 shows the relationship between the number of auxiliary switching cycles n (as well as the ratio of $L_o/L_{\rm aux}$) and the auxiliary inductance value under different output voltages V_o. So, based on the power circuit design parameters ($V_{\rm in}$, V_o, L_o, and $L_{\rm aux}$), the necessary cycles of auxiliary switching for fast recovering the overshoot can be counted by a counter for n. By this means, it becomes very straightforward but reliable for the CBC controller to deactivate the CAC (as soon as the count reaches n).

Fig. 5 illustrates the impact of rounding down operation of n on the settling time. In Fig. 5(a) ($[[(V_{\rm in}-V_o)/V_{\rm in}*L_o/L_{\rm aux}]-n<0.5$), the CAC will be deactivated before the inductor current reaches the new load level I_{o2}. A second overshoot occurs, and the settling time is longer than the ideal case shown in Fig. 5. On the contrary, if ($[[(V_{\rm in}-V_o)/V_{\rm in}*L_o/L_{\rm aux}]-$

$$\Delta v_o(t)=\begin{cases} \frac{1}{C_o}\left[\Delta I_o\cdot t-\frac{V_o}{2L_o}t^2-\frac{N\cdot\Delta I_o\cdot T_{\rm aux}}{2}-\int\limits_0^{(t-N\cdot T_{\rm aux})}\frac{V_o}{L_{\rm aux}}t\cdot dt\right] & (NT_{\rm aux}\le t<NT_{\rm aux}+d_{\rm aux}T_{\rm aux}) \\ \qquad (N=0,1,2\ldots,n) \\ \frac{1}{C_o}\left[\Delta I_o\cdot t-\frac{V_o}{2L_o}t^2-\frac{N\cdot\Delta I_o\cdot T_{\rm aux}}{2}-\frac{V_{\rm in}-V_o}{2V_{\rm in}}T_{\rm aux}\Delta I_o\right. & \\ \quad \left.-\int\limits_{(t-N\cdot T_{\rm aux}-d_{\rm aux}T_{\rm aux})}^{T_{\rm aux}}\frac{(V_{\rm in}-V_o)(T_{\rm aux}-t)}{L_{\rm aux}}dt\right] & (NT_{\rm aux}+d_{\rm aux}T_{\rm aux}\le t<(N+1)T_{\rm aux}) \\ \qquad (N=0,1,2\ldots,n) \end{cases} \tag{1}$$

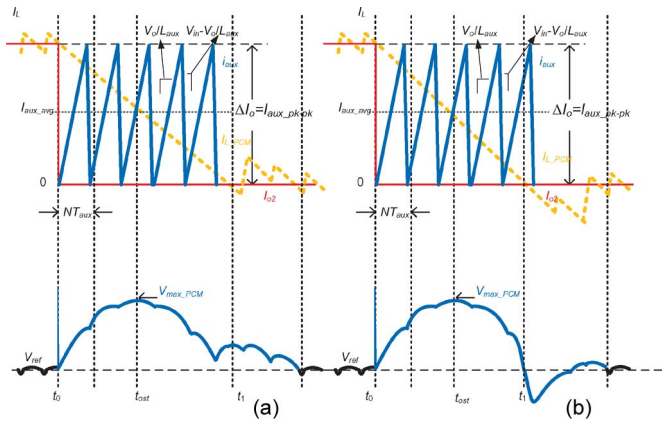

Fig. 5. Effect of rounding down operation of n on the settling time. (a) $[(V_{\rm in}-V_o)/V_{\rm in} * L_o/L_{\rm aux}]-n<0.5$. (b) $[(V_{\rm in}-V_o)/V_{\rm in} * L_o/L_{\rm aux}]-n\geq 0.5$.

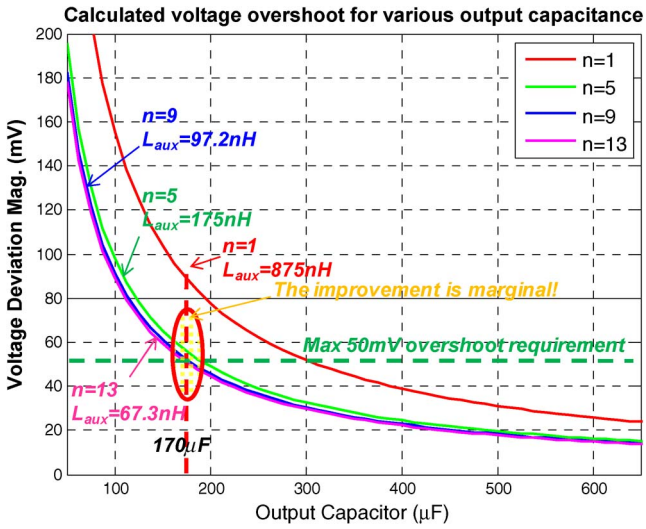

Fig. 6. Estimated voltage overshoot for various times of CAC switching and different output capacitances for an unloading transient of 10 A ($V_{\rm in}=12$ V, $V_o=1.5$ V, and $L_o=1$ μH).

$n\geq 0.5$), as shown in Fig. 5(b), the CAC activates longer than required, so that a voltage undershoot appears and increases the settling time, too. However, it is noted that the output overshoot equations in (1) are still valid because they are actually not dependent on the number of n. Moreover, the time instant $t_{\rm ost}$ can be expressed more generally in

$$t_{\rm ost}=\frac{\Delta I_o+\frac{V_o}{L_{\rm aux}}NT_{\rm aux}}{\frac{V_o}{L_o}+\frac{V_o}{L_{\rm aux}}}=\frac{\Delta I_o\cdot L_{\rm aux}L_o+V_o\cdot NT_{\rm aux}\cdot L_o}{V_o(L_{\rm aux}+L_o)}. \tag{6}$$

Fig. 6 gives the overshoot voltage for various numbers of auxiliary switching cycles using the proposed BCM PCM CAC. By choosing proper auxiliary inductance $L_{\rm aux}$, the number of auxiliary switching n can be controlled according to (5).

For example, as shown in Fig. 7, $n=1$ means that, in order to meet the overshoot requirement, the auxiliary circuit will be activated for one switching cycle during the unloading transient, which can be achieved by selecting $L_{\rm aux}=875$ nH and output capacitance $C_o=300$ μF, as shown in Fig. 7(a). Moreover, for $n=5$, the auxiliary circuit will be activated

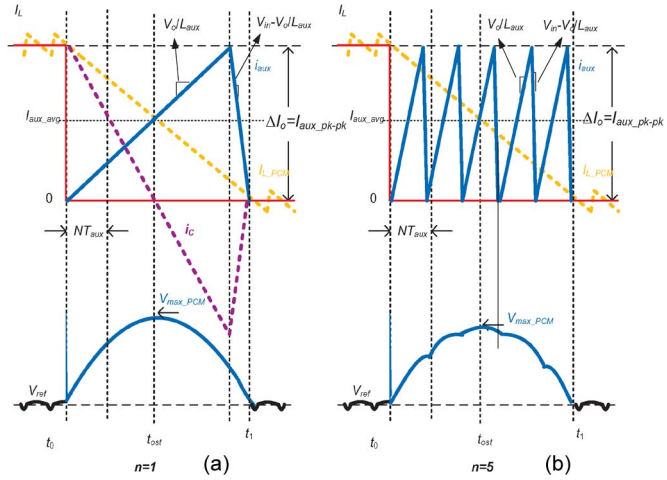

Fig. 7. CAC switching for n cycles by selecting different $L_{\rm aux}$ values. (a) $n=1$; $L_{\rm aux}=875$ nH. (b) $n=5$; $L_{\rm aux}=175$ nH ($V_{\rm in}=12$ V, $V_o=1.5$ V, and $L_o=1$ μH).

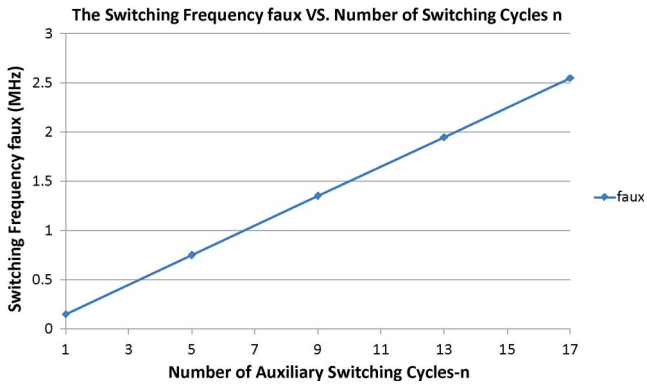

Fig. 8. Plot of switching frequency $f_{\rm aux}$ versus the number n of switching cycles under 10-A unloading transient.

for five switching cycles with selecting $L_{\rm aux}=175$ nH and $C_o=185$ μF, as shown in Fig. 7(b).

It is also noted from Figs. 4 and 6 that, the lower the auxiliary inductance $L_{\rm aux}$ is, the more the number n of auxiliary switching cycles and the better the unloading transient performance will be. However, from the simulation result shown in Fig. 6, the improvement is marginal when the auxiliary inductance $L_{\rm aux}$ becomes too small (i.e., $L_{\rm aux}<100$ nH and $n>9$), but on the contrary, low $L_{\rm aux}$ will increase the auxiliary switching frequency $f_{\rm aux}$ and harm the overall efficiency due to the more cycles of auxiliary switching.

The switching frequency of the auxiliary circuit is only determined by the ratio of inductances and the load step value but not the main converter switching frequency. For example, in the prototype under 10-A unloading transients, the main converter switching frequency is 450 kHz, the auxiliary switching frequency will be about 1.3 MHz by choosing $n=9$, and the auxiliary switching can be controlled down to 750 kHz if $n=5$ is chosen. In Fig. 8, it shows that the switching frequency of the auxiliary FET $f_{\rm aux}$ increases linearly with the number of switching n. When the switching frequency $f_{\rm aux}$ is much higher than 1 MHz, the cost of the auxiliary MOSFET driver will increase dramatically, resulting in extra/high cost of the CAC implementation. Therefore, design compromise

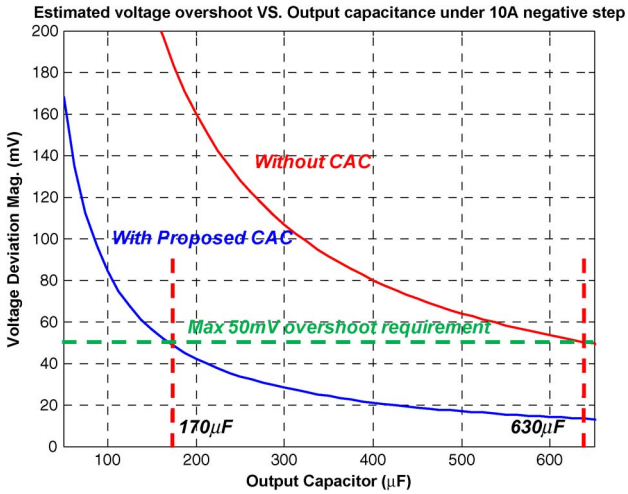

Fig. 9. Estimated voltage overshoot for various output capacitances with and without BCM PCM CAC for an unloading transient of 10 A ($V_{\rm in} = 12$ V, $V_o = 1.5$ V, and $L_o = 1$ μH, $L_{\rm aux} = 100$ nH).

should be made for output voltage overshoot and switching frequency/switching loss the auxiliary circuit. So, finally, $n = 9$ is chosen to achieve a performance balance between output voltage overshoot improvement and auxiliary power loss.

Furthermore, in Fig. 9, it reveals that, in order to meet the overshoot requirement at 50 mV under 10-A step-down load transient, 630-μF output capacitance is required for CBC-controlled buck converter without CAC, while, by using the proposed BCM-PCM-controlled CAC, the required output capacitance can be reduced by 73.0% to 170 μF. As a result, the output capacitance can be implemented with ceramic capacitors, resulting in reduced motherboard area and improved output voltage ripple.

B. Auxiliary Circuit Power Loss Analysis

There are three main sources of conduction loss pertaining to the proposed circuit [14]: the auxiliary inductor $L_{\rm aux}$, the auxiliary FET $Q_{\rm aux}$, and the auxiliary diode $D_{\rm aux}$.

By calculating the rms auxiliary current in (7), the inductor conduction loss can be calculated. But in the loss analysis due to the very low dc resistance and sensing resistance $R_{\rm Laux}$ of the auxiliary inductor $L_{\rm aux}$, the auxiliary inductor conduction loss is in 10-mW order and ignored

$$I_{\rm aux(rms)} = I_{\rm aux\_avg}\sqrt{1+\frac{1}{3}\left(\frac{I_{\rm aux\_pk-pk}}{2I_{\rm aux\_avg}}\right)^2}. \quad (7)$$

The rms current of the auxiliary FET and the average current of the auxiliary diode can be calculated using

$$I_{\rm Qaux(rms)} = I_{\rm aux\_avg} \cdot \sqrt{\frac{V_{\rm in}-V_o}{V_{\rm in}}}\sqrt{1+\frac{1}{3}\left(\frac{I_{\rm aux\_pk-pk}}{2I_{\rm aux\_avg}}\right)^2} \quad (8)$$

$$I_{\rm Daux(avg)} = I_{\rm aux\_avg}\left(1-\frac{V_{\rm in}-V_o}{V_{\rm in}}\right). \quad (9)$$

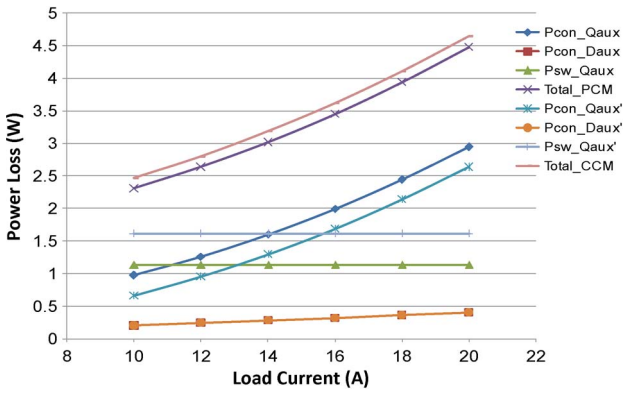

Fig. 10. Comparison results of loss breakdown based on different control schemes (the power circuit design parameters: $V_o = 1.5$ V, $f_s = 450$ kHz, $L_o = 1$ μH, $R_L = 1$ mΩ, $L_{\rm aux} = 100$ nH, $RL_{\rm aux} = 0.2$ mΩ, $RQ_{\rm aux} = 30$ mΩ, $V_{\rm diode} = 0.32$ V, and $T_{\rm fall} = 2$ ns).

The conduction loss for the auxiliary FET and auxiliary diode can be calculated using

$$P_{\rm con\_Qaux} = I^2_{\rm Qaux(rms)} \cdot R_{\rm Qaux} \quad (10)$$

$$P_{\rm con\_Daux} = I_{\rm Daux(rms)} \cdot V_{\rm diode}. \quad (11)$$

Since a Schottky diode is utilized, it is assumed that the switching loss of the diode is negligibly small compared to the FET switching loss and the total conduction loss. Generally, the switching loss for the auxiliary FET can be calculated using (12), where $T_{\rm rise}$ is the rise time of the auxiliary FET and $I_{\rm on}$ is the instantaneous auxiliary current when $Q_{\rm aux}$ is turned on, respectively. $T_{\rm fall}$ equals the typical fall time of the auxiliary FET. $I_{\rm off}$ equals the instantaneous auxiliary current when $Q_{\rm aux}$ is turned off, which is equal to the peak auxiliary current

$$P_{\rm sw\_Qaux} = \frac{1}{2} f_{\rm aux} \cdot V_{\rm in} \cdot (T_{\rm rise} \cdot I_{\rm on} + T_{\rm fall} \cdot I_{\rm off}). \quad (12)$$

Because of the zero turn-on current under BCM operation of the CAC, the switching loss of the auxiliary FET can be simplified in

$$P_{\rm sw\_Qaux} = \frac{1}{2} f_{\rm aux} \cdot V_{\rm in} \cdot T_{\rm fall} \cdot I_{\rm off}. \quad (13)$$

In Fig. 10, according to the previous equations, the power loss analysis is shown for comparison between the proposed control strategy (BCM) and the existing control scheme (CCM) with the same CAC power components. The conduction losses of auxiliary MOSFET and the Schottky diode, MOSFET switching loss, and total losses are represented as $P_{\rm con\_Qaux}$, $P_{\rm con\_Daux}$, $P_{\rm sw\_Qsw}$, and Total_PCM for the proposed control strategy, while $P_{\rm con\_Qaux}{}'$, $P_{\rm con\_Daux}{}'$, $P_{\rm con\_Qsw}{}'$, and Total_CCM are for the existing control scheme, respectively [14]. It is noted that the conduction loss of the auxiliary diode is unchanged using the proposed scheme because of the same average current. The conduction loss of the auxiliary MOSFET using the proposed BCM PCM controller is higher than that of the auxiliary MOSFET controlled by the existing scheme [14] due to the larger inductor current ripple and, thus, the rms current value. However, compared to the existing scheme, the switching loss of the auxiliary MOSFET and the total losses are

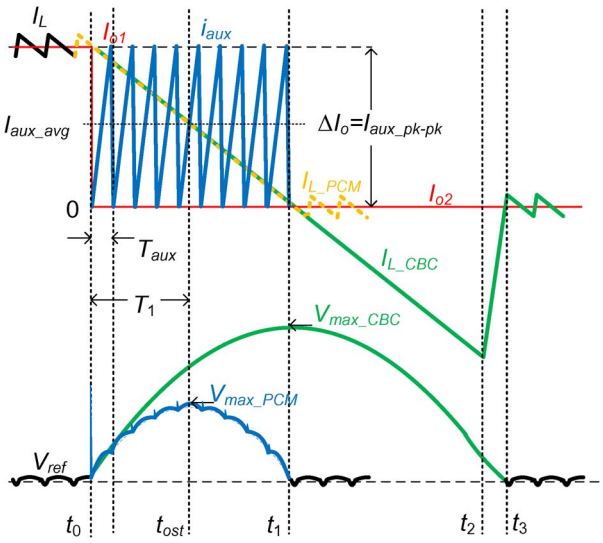

Fig. 11. BCM PCM CAC and normal CBC operation waveforms.

reduced using the BCM-PCM-controlled CAC. It is also worth noting that the auxiliary FET switching loss is independent of the load current level.

In a 15-W (1.5-V/10-A) buck converter with CAC, under 10-A unloading transient, a low-profile SOT-23 Fairchild FDN359BN [19] can be used as the auxiliary MOSFET $Q_{\rm aux}$. It should be noted that a higher rating or paralleled MOSFETs can be utilized for better efficiency and higher load step value. For example, under 10-kHz frequent load transient, CAC is activated 6.6% of the time and consumes about 150 mW (1% of the full power). On the other hand, about $21 * 22$-μF output capacitance can be reduced. If 0805 ceramic capacitors are used, the board area is about 300 mm^2 (5 mm $*$ 60 mm). The prototype CAC is fitted in 195 mm^2 (13 mm $*$ 15 mm). So, net PCB space saving is available by using the proposed scheme.

Several unique advantages of the proposed control strategy are discussed in this section. First, the auxiliary current (CAC) will be operated in BCM at reduced switching frequency (the CAC falls to zero at the end of each switching cycle), such that the switching power loss can be decreased and a commonly used pulsewidth-modulation (PWM) driver can be used to drive the auxiliary switch $Q1$. Furthermore, according to the design ratio between the main output inductance (L_o) and the auxiliary inductance $(L_{\rm aux})$, the number of auxiliary switching cycles is predictable, which significantly enhances the reliability of the proposed control scheme. For example, if the output inductance $L_o = 1$ μH and the auxiliary induction $L_{\rm aux} \approx 100$ nH, the number of auxiliary switching cycles will be $n = 9$. Moreover, the proposed scheme can be simply scaled and extended to multiphase VR with much lower equivalent output inductance; on the contrary, for this application, previous schemes may badly suffer from the impossibly high-frequency switching or low auxiliary inductance for maintaining the CAC level [14], [15].

IV. Implementation of the Proposed Strategy CAC

The proposed BCM PCM CAC is shown in Fig. 11. During steady-state operation or step-up loading transient, the CAC is deactivated, and the main buck converter is regulated by an analog CBC (discussed in [17], but other CBC controllers/schemes are also applicable) [16]. When the unloading transient happens, the CAC will be operated for rapidly removing the extra capacitor charge energy back to the input source through the Schottky diode $D_{\rm aux}$. The operations of the CAC and the proposed control strategy are described as follows (see Fig. 11).

1) It is assumed that the unloading transient happens at t_0, triggering the proposed control scheme to minimize the output voltage overshoot.
2) The main switch $Q1$ will immediately turn off to reduce the additional capacitor charge at t_0, while the S/H circuit sets the peak current reference value $I_{\rm aux\_pk-pk}$ by holding the output of the capacitor current sensing circuit (see Fig. 12).
3) The auxiliary circuit will be controlled using peak current (at $I_{\rm aux\_pk-pk}$) mode method in BCM (see Fig. 11), which can be approximately modeled as a current source connected between output capacitor and input voltage source to minimize the output voltage overshoot (see Fig. 1).
4) After predictable n (to be calculated later in this paper) cycles of auxiliary switching, the output voltage will recover to the reference voltage $V_{\rm ref}$ at t_1, and the normal CBC controller will take over the regulation such that the settling time can be optimized.

From the settling time point of view, when we set the BCM peak current at $I_{\rm aux\_pk-pk}$, equivalently, the average auxiliary current $I_{\rm aux\_avg}$ will be half of the transient load current step value ΔI_o, i.e., $I_{\rm aux\_avg} = 1/2\ \Delta I_o$. Compared with a normal CBC controller in [1], [5], and [17] (see Fig. 11), during unloading transient, the auxiliary current can rapidly balance the capacitor charge at t_1. On the contrary, without the help of CAC, the output capacitor will be charged by the current of $(I_L - I_{o2})$ until t_1. Therefore, the CBC controller requires the negative portion of inductor current to discharge the capacitor. As soon as the capacitor charge is balanced, the output voltage will recover to $V_{\rm ref}$ at t_3 for normal CBC controller [5], [17]. In conclusion, the CAC coupled with CBC controller can significantly reduce the settling time.

The diagram of the proposed BCM PCM strategy to control the CAC is shown in Fig. 12. To set the peak current level of the auxiliary current, the load step value is required to be sensed/calculated. The capacitor current during load transient is an alternative representation of the load step ΔI_o. So, the capacitor current can be rebuilt by active filtering the output voltage [considering ESR in (14)] with an extra pole provided by C_f to attenuate the switching noise

$$C_{1C} \cdot R_{1C} = \left(\frac{C_o}{k}\right) \cdot (\text{ESR} \cdot k) = C_o \cdot \text{ESR}. \qquad (14)$$

The output of the capacitor current sensor $i_{\rm Csen}$, in relation to the actual capacitor current i_C, is equated in

$$i_{\rm Csen} = \frac{R_{2C}}{k} i_C. \qquad (15)$$

So, when the unloading transient is detected by the circuit shown in Fig. 13, the $TransDetect$ signal is pulled low to hold

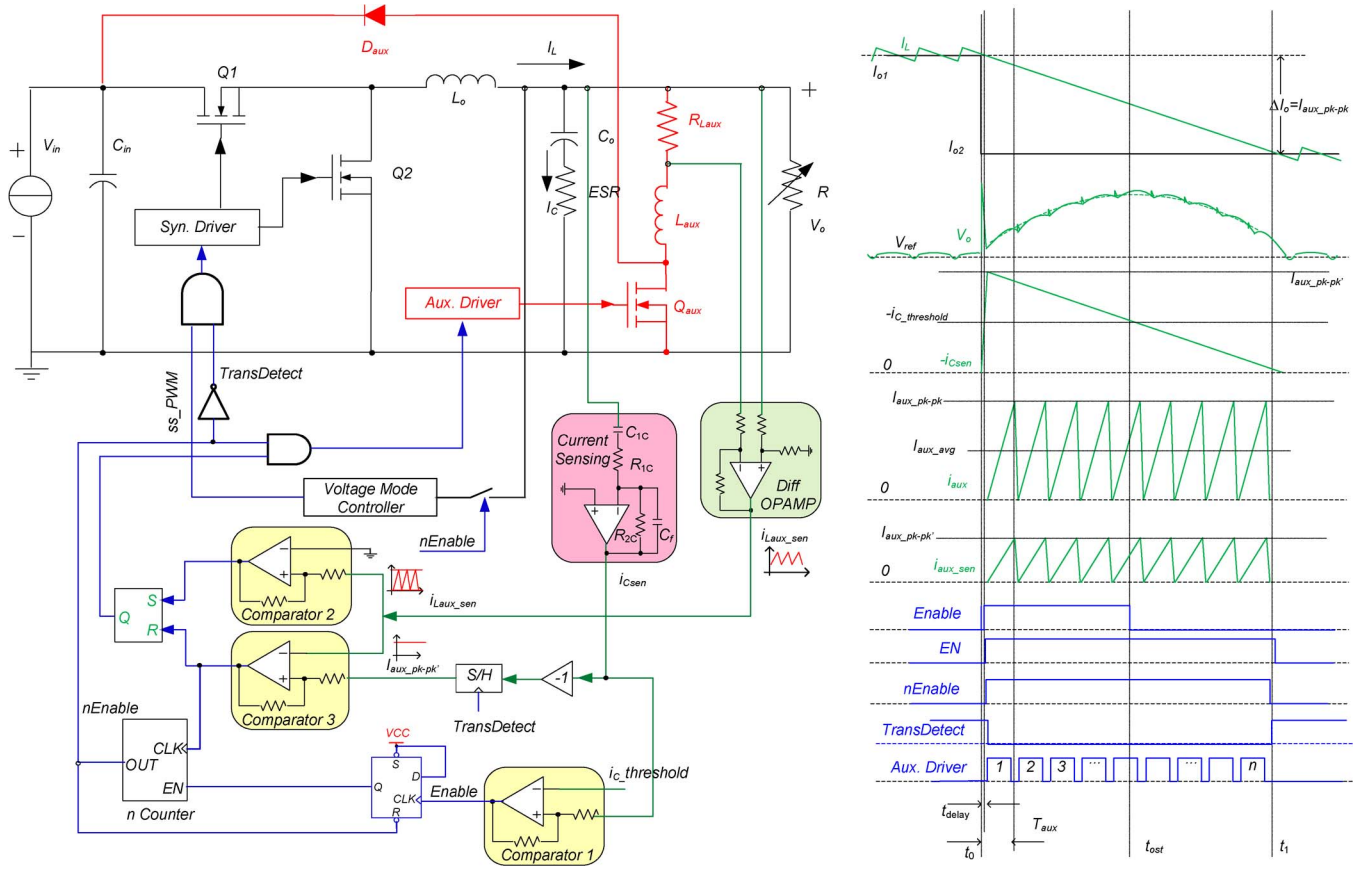

Fig. 12. Hardware implementation of the proposed BCM PCM CAC and key waveforms.

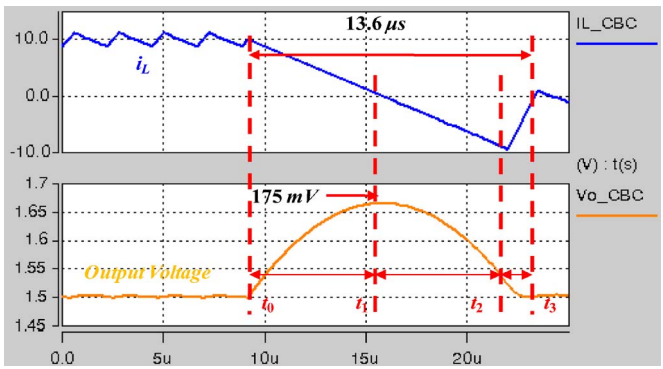

Fig. 13. Simulation results of CBC controller under 10-A–> 0-A unloading transient without CAC for a single-phase buck converter.

the capacitor current sensing signal using S/H, until the count of $nCounter$ reaches n.

When the capacitor current sensing signal i_{Csen} exceeds the threshold level $i_{\mathrm{c\_threshold}}$, the $Enable$ signal will be activated to enable the $nCounter$. A time delay will be introduced, caused by the limited bandwidth of capacitor current sensor and the comparison with threshold. In the implementation, the time interval between t_0 and the activation of CAC is defined as t_{delay}, which is about 80 ns in the prototype. The extra overshoot introduced by this time delay can be estimated using (16). In the prototype, the $\Delta V_{\mathrm{delay}}$ is about 4.5 mV

$$\Delta V_{\mathrm{delay}} = \frac{\Delta I_o \cdot t_{\mathrm{delay}}}{C_o}. \tag{16}$$

A D flip-flop is used to hold the first rising edge of $Enable$ and avoid comparison noise. $nCounter$ is used for counting the precalculated number n of auxiliary switching in (5). When the $nCounter$ reaches n (i.e., the desired number of auxiliary switching cycles), the $nEnable(OUT)$ signal of $nCounter$ will perform the following: 1) deactivate the auxiliary current; 2) reset the EN signal; and 3) generate the CBC PWM signal for the buck converter. The inverted signal of $nEnable$ is called $TransDetect$, which is generated to accomplish the following: 1) hold the $I_{\mathrm{aux\_pk-pk}}$ value for peak current control level and 2) turn off the main switch $Q1$ to achieve CBC and reduce the output voltage overshoot. A differential OPAMP amplifies the voltage across the current sensing resistor R_{Laux} to equalize the auxiliary current i_{aux}, which is compared with $I_{\mathrm{aux\_pk-pk}}$ and GND. Moreover, an SR flip-flop is used to create the PWM signal to the auxiliary driver for switching Q_{aux} and implement the BCM operation shown in Fig. 12. Moreover, when i_{aux} reaches the $I_{\mathrm{aux\_pk-pk}}$, the Comparator 3 outputs a pulse signal to the $nCounter$ for counting the number of auxiliary switching.

V. Simulation and Experimental Verification

A. Simulation Verifications

In order to verify the functionalities of the proposed control strategy, a buck converter with/without CAC undergoing unloading transient condition is simulated. Moreover, the simulation results are shown in Figs. 13 and 14 for comparison

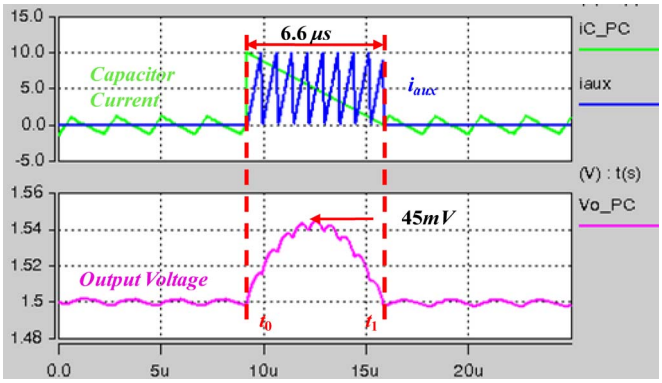

Fig. 14. Simulation results of CBC controller under 10-A–> 0-A unloading transient with proposed CAC for a single-phase buck converter.

between the normal CBC controller in [17] and the proposed control scheme with BCM PCM CAC during 10-A unloading transient. The design parameters are listed as follows: $V_{\rm in} = 12$ V, $V_o = V_{\rm ref} = 1.5$ V, $f_s = 450$ kHz, $L_o = 1$ μH, $R_L = 1$ mΩ, $C_o = 200$ μF, ESR $= 0.1$ mΩ, ESL $= 100$ pH, $L_{\rm aux} = 100$ nH, $R_{\rm Laux} = 0.2$ mΩ, $R_{\rm Qaux} = 30$ mΩ, $V_{\rm diode} = 0.32$ V, $T_{\rm fall} = 2$ ns, and $n = 9$ (using (5), $V_{\rm in} - V_o/V_{\rm in} * L_o/L_{\rm aux} = 8.75$). In addition, the Type III compensator in the CBC controller is well designed with 75-kHz bandwidth and 60° phase margin in [17].

In Fig. 13, the CBC control technology without CAC is employed for optimal response of the single-phase buck converter. The overshoot is 175 mV with 13.6-μs settling time under a 10-A step-down load transient case.

Applying the proposed BCM-PCM-controlled CAC, the output voltage overshoot is reduced to 45 mV, and the settling time is reduced to 6.6 μs, compared to the CBC controlled buck converter without CAC. In other words, the overshoot and the settling time are improved by 74.2% and 51.5%, separately.

B. Experimental Verifications

A single-phase 12-V–1.5-V prototype is built with CAC using the same parameters in the simulation. Experimental results are shown in Figs. 15 and 16 under the unloading transient between full load (10 A) and no load.

In Fig. 15, an analog CBC controller is used to achieve optimal response for buck converter under load transients. However, the overshoot is not improved significantly, as previously discussed. The sensed inductor current is also shown to demonstrate the principle, and a negative portion of current is required from t_1 to t_3 to balance the capacitor charge. Therefore, the overshoot is 180 mV, and the total settling time is 13.6 μs. Moreover, the difference between experimental result in Fig. 15 and simulation in Fig. 13 is mainly caused by different load transient timing.

Using the proposed BCM PCM CAC, the overshoot is decreased by 75.0%, and the settling time is shortened by 53.6%, compared with the optimal response provided by an analog CBC controller without CAC (discussed in [14]). Based on the previous discussion shown in Fig. 6, the number of switching is predictable using (5), and in the experiment, the rounded-off number n is nine.

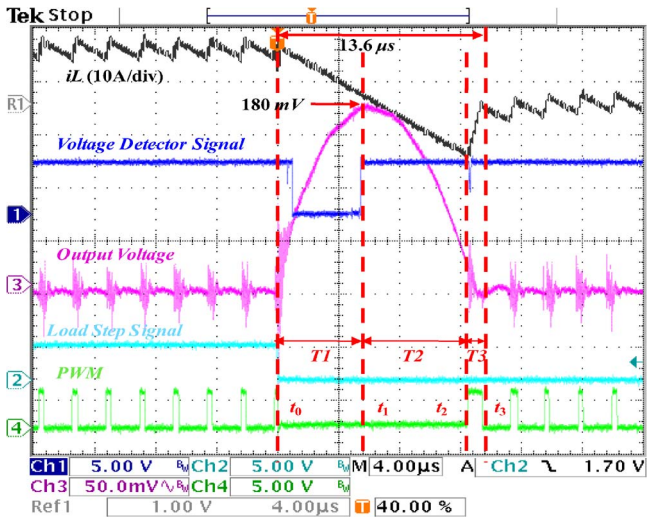

Fig. 15. Experimental results of analog CBC controller under 10-A–> 0-A unloading transient without CAC.

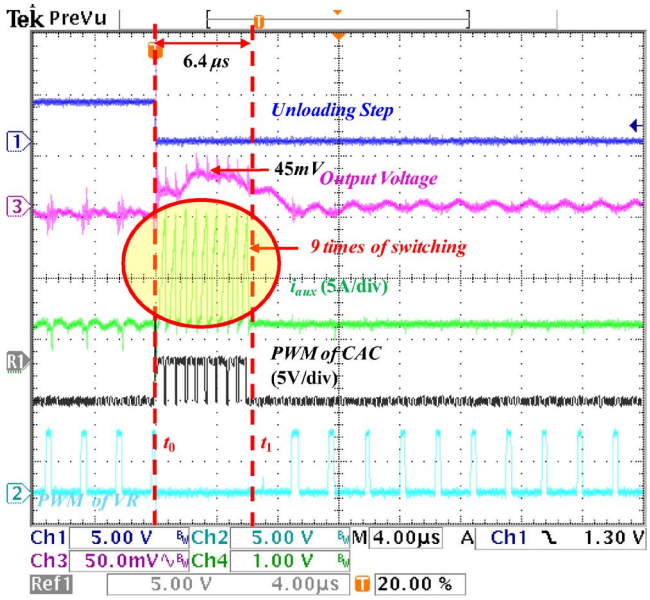

Fig. 16. Experimental results of the proposed BCM PCM controller under 10-A–> 0-A unloading transient with CAC.

VI. Conclusion

In this paper, a practical auxiliary circuit control strategy has been presented to improve unloading transient performance, which has the following unique advantages: 1) predictable auxiliary switching pattern based on the main–auxiliary inductance ratio; 2) the auxiliary circuit operating at relatively low frequency to reduce the switching loss; 3) voltage overshoot reduction; and 4) minimizing the settling time of unloading response based on charge balance principles. The power loss analysis and output voltage overshoot estimation are made in this paper as design guidelines. To meet the maximum overshoot requirement, the output capacitance can be decreased from 630 to 170 μF. Through simulation and experimental results, under 10-A unloading transient, it demonstrates that the proposed control strategy reduces the overshoot by 75% and shortens the settling time by 53.6%.

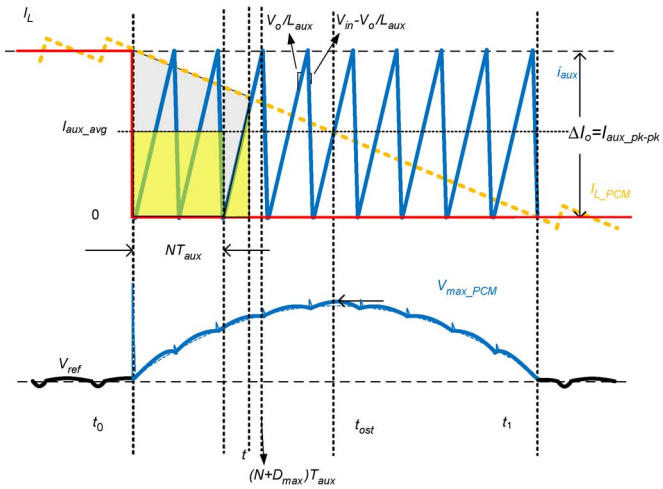

Fig. 17. Overshoot derivation with CAC during ON interval.

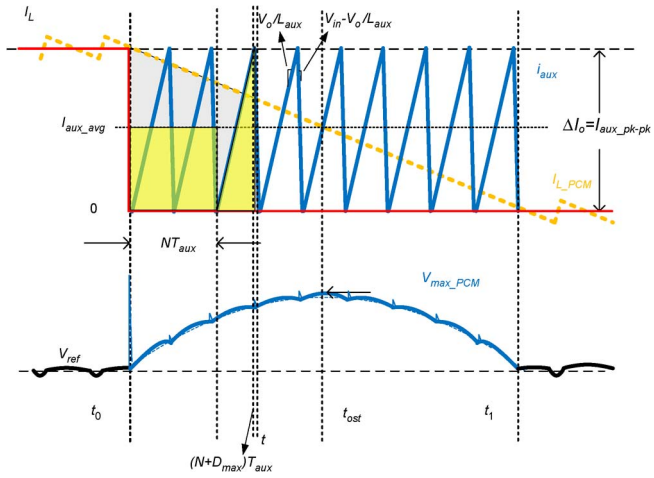

Fig. 18. Overshoot derivation with CAC during OFF interval.

APPENDIX

In this Appendix, derivations of output voltage overshoot calculation with the proposed scheme in Section III are discussed through details. Without loss of generality, it is assumed that the auxiliary circuit is switched for n times under BCM PCM control, where integer n is the number of auxiliary switching cycles. Upon that, the instantaneous output voltage variation $\Delta v_o(t)$ can be expressed for two intervals depending on the ON/OFF state of the auxiliary circuit and the Nth time of switching, where $T_{\rm aux}$ is the switching period of the auxiliary current and $d_{\rm aux}$ is the duty cycle of the auxiliary circuit. ESR is ignored in this derivation.

As shown in Fig. 17, during ON state of the auxiliary circuit, the output voltage overshoot can be calculated in (A1). The capacitor current is equal to the difference between the inductor current I_L and the auxiliary current $I_{\rm Laux}$. The overshoot is calculated by integrating the capacitor current over time. Alternatively, we can simply calculate the area difference between the trapezoidal area (with stripe) and the shaded area (in yellow). The yellow shaded area can be also considered as the combination of a square [the third term on the right-hand side of (A2)] and a triangle [the fourth term on the right-hand side of (A2)]. Finally, the equation can be simplified in (A2)

$$\begin{aligned}\Delta v_o(t) &= \frac{1}{C_o}\int_0^t (I_L - I_{\rm Laux})\,dt \\ &= \frac{1}{C_o}\int_0^t \left(\Delta I_o - \frac{V_o}{L_o}t\right)dt - \frac{\Delta I_o N T_{\rm aux}}{2C_o} \\ &\quad - \frac{1}{C_o}\int_0^{t-NT_{\rm aux}} \frac{V_o}{L_{\rm aux}}t\cdot dt \end{aligned} \tag{A1}$$

$$\begin{aligned}\Delta v_o(t) &= \frac{1}{C_o}\left[\Delta I_o\cdot t - \frac{V_o}{2L_o}t^2 - \frac{N\cdot\Delta I_o\cdot T_{\rm aux}}{2}\right. \\ &\quad \left. - \int_0^{(t-N\cdot T_{\rm aux})} \frac{V_o}{L_{\rm aux}}t\cdot dt\right] \\ &\quad (NT_{\rm aux} \le t < NT_{\rm aux} + d_{\rm aux}T_{\rm aux}) \\ &\quad (N = 0,1,2\ldots,n). \end{aligned} \tag{A2}$$

Similarly, as shown in Fig. 18, during OFF state of the auxiliary circuit, the output voltage overshoot can be calculated in the following equation based on the geometric areas in yellow and stripe:

$$\begin{aligned}&\Delta v_o(t) \\ &= \frac{1}{C_o}\int_0^t (I_L - I_{\rm Laux})dt = \frac{1}{C_o}\int_0^t \left(\Delta I_o - \frac{V_o}{L_o}t\right)dt \\ &\quad - \frac{\Delta I_o(N + D_{\rm max})T_{\rm aux}}{2C_o} \\ &\quad - \frac{1}{C_o}\int_0^{t-NT_{\rm aux}} \left(\Delta I_o - \frac{V_{\rm in} - V_o}{L_{\rm aux}}t\right)\cdot dt \\ &= \frac{1}{C_o}\left[\begin{array}{l}\Delta I_o\cdot t - \frac{V_o}{2L_o}t^2 - \frac{N\cdot\Delta I_o\cdot T_{\rm aux}}{2} - \frac{V_{\rm in}-V_o}{2V_{\rm in}}T_{\rm aux}\Delta I_o \\ - \int_{(t-N\cdot T_{\rm aux}-d_{\rm aux}T_{\rm aux})}^{T_{\rm aux}} \frac{(V_{\rm in}-V_o)(T_{\rm aux}-t)}{L_{\rm aux}}dt\end{array}\right] \\ &\quad (NT_{\rm aux} + d_{\rm aux}T_{\rm aux} \le t < (N+1)T_{\rm aux}) \\ &\quad (N = 0,1,2\ldots,n). \end{aligned} \tag{A3}$$

The local output maximum voltage will occur during ON state of the auxiliary circuit. The global output overshoot/maximum voltage occurs, when the derivative of (A2) is zero during the $(N'+1)$th switching, expressed in

$$\Delta I_o - \frac{V_o}{L_o}t - \frac{V_o}{L_{\rm aux}}(t - NT_{\rm aux}) = 0. \tag{A4}$$

So, the $t_{\rm ost}$ instant when the peak voltage happens can be solved in

$$t = t_{\rm ost} = \frac{\Delta I_o + \frac{V_o}{L_{\rm aux}} N T_{\rm aux}}{\frac{V_o}{L_o} + \frac{V_o}{L_{\rm aux}}} = \frac{\frac{V_o}{L_o} n T_{\rm aux} + \frac{V_o}{L_{\rm aux}} N T_{\rm aux}}{\frac{V_o}{L_o} + \frac{V_o}{L_{\rm aux}}} = \frac{L_{\rm aux} n T_{\rm aux} + L_o N T_{\rm aux}}{L_{\rm aux} + L_o}. \quad \text{(A5)}$$

As it is assumed, n is an integer. The auxiliary switching cycle $T_{\rm aux}$ can be expressed as in

$$T_{\rm aux} = \frac{\Delta I_o L_o}{n V_o} = \frac{\Delta I_o L_{\rm aux}}{D_{\rm aux} V_o}. \quad \text{(A6)}$$

Therefore, the integer n can be calculated based on

$$n = \frac{D_{\rm aux} L_o}{L_{\rm aux}}. \quad \text{(A7)}$$

Moreover, generally, n can be calculated by rounding down (A7), which is shown in (5). By substituting (A7) into (A5), the following equation can be derived:

$$t_{\rm ost} = \frac{D_{\rm aux} + N'}{D_{\rm aux} + n} \cdot n T_{\rm aux}. \quad \text{(A8)}$$

Although previous (A2) and (A3) give us very accurate result of overshoot voltage, for practical design guideline, under unloading step transient with the CAC, the output voltage can be estimated as (A9) using the parabolic curve analysis in [17], [20], and [14, eq. (9)]. Based on the average auxiliary current $L_{\rm aux\_avg}$ without considering the auxiliary inductor current ripple under the BCM PCM control, a simplified equation is provided as a simplified method to calculate the overshoot in (A9). The symbols L_o, C_o, T_1, ESR, ΔI_o, V_o, and $L_{\rm aux}$ represent the output inductance, output capacitance, time interval between t_0 and $t_{\rm ost}$, equivalent series resistance, load step value, output voltage, and auxiliary inductance, respectively,

$$\Delta v_o(t) = \frac{V_o}{2 L_o C_o}(2 T_1 t - t^2) - \frac{V_o}{L_o}(t - T_1) \cdot \text{ESR} + A_{\rm Iaux}. \quad \text{(A9)}$$

$A_{\rm Iaux}$ equals the extra charge being delivered to the output capacitor while the auxiliary current is ramping to $I_{\rm aux\_avg}$ following t_0. $A_{\rm Iaux}$ is expressed in

$$A_{\rm Iaux} = \frac{\left(\frac{\Delta I_o}{2}\right)^2 L_{\rm aux}}{2 V_o C_o}. \quad \text{(A10)}$$

Based on (A9), the maximum output voltage occurs when the derivative of $\Delta v_o(t)$ equals zero in the following equation [20]:

$$\frac{d \Delta v_o(t)}{dt} = \frac{V_o}{L_o C_o}(T_1 - t - \text{ESR} \cdot C_o) = 0. \quad \text{(A11)}$$

Therefore, the overshoot can be calculated as (A12) by substituting $t = (T_1 - \text{ESR} * C_o)$, where T_1 can be expressed as (A13) [20]

$$\Delta V_o \approx \frac{\left(\frac{\Delta I_o}{2}\right)^2 \cdot L_o^2 + \text{ESR}^2 \cdot C_o^2 \cdot V_o^2}{2 V_o \cdot L_o \cdot C_o} + A_{\rm Iaux} \quad \text{(A12)}$$

$$T_1 = \frac{(\Delta I_o / 2) \cdot L_o}{V_o}. \quad \text{(A13)}$$

By substituting (A10) into (A12), the final equation is shown in (4).

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