Improving the Light Load Efficiency and THD of PFC Converters using a Line Cycle Skipping Method

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***Abstract*— Light load efficiency and total harmonic distortion (THD) of AC-DC converters is of increasing importance when considering the increase in non-linear electronic loads on the modern grid. Efficiency and THD standards are becoming stricter in their requirements to account for this increase in non-linear loads. To address the increasing requirements for higher efficiency and lower THD without increasing the cost or complexity of the design, a Line Cycle Skipping (LCS) method is proposed and its digital control implementation presented. A 100W universal line input voltage PFC boost converter prototype is built to demonstrate the effectiveness of the proposed control method.**

I. INTRODUCTION

With tremendous growth in non-linear electronic loads such as computer electronics and energy efficient lighting, there has been a lot of focus on the design of power factor correction (PFC) in AC-DC converters for such applications. Products that wish to qualify for the Energy Star program must meet or exceed certain efficiency requirements [1, 2]. Also, the total harmonic distortion (THD) of PFC converters must meet the IEC EN 61000-3-2 standard which sets harmonic current limits (for equipment drawing ≤ 16 A per phase) [3]. These standards and regulations are increasingly strict about light load conditions because more devices tend to stay in light load for longer periods of time (e.g. computers, display monitors, etc.); and the poor performance in the light load condition counts for a significant percentage of the total power loss and increase in the overall harmonics injected into the grid [4].

Yet improving the light load and THD performance of PFC converters is challenging due to the following reasons: (a) the switching loss, driving loss and reverse recovery loss of semiconductor components become dominant losses at light load, which is difficult to reduce; (b) due to the difficulties in detecting low-amplitude signals, and the change from CCM to DCM mode, current distortion is much more severe at light load; (c) for boundary conduction mode (BCM), the switching frequency is higher at light load, adding even more losses. Due to these considerations, there have been many methods introduced to improve the light load efficiency and reduce the THD [5-17]. Some research has only addressed the efficiency at the no-load or stand-by condition for PFC converters, and does not address the entire light load range [19-20]. For interleaved PFC topologies, light load efficiency improvements are specific to the topology itself, using phase shedding as the primary means of efficiency improvement [8-10, 14, 17]. One research paper devises a method to improve the light load efficiency for all PFC converters, but at the cost of increasing the THD not unlike phase angle control [18].

Cost is a very important consideration when adopting a method to improve the efficiency and reduce the THD. While adaptive control methods are attractive because of their ability to change control strategies based on the operating conditions, most of these methods require high a cost DSP or FPGA in order to implement the sophisticated techniques [5-8, 12, 16]. A simpler and lower-cost control method would be more attractive and more practical.

In this paper, a Line Cycle Skipping (LCS) control method is proposed to increase the light load efficiency and reduce the THD at light load by skipping one or more entire line cycles with different patterns. Its advantages include: (a) it is very simple and can be implemented using a low cost microcontroller unit (MCU); (b) it can apply to all PFC topologies; (c) the light load efficiency and THD can be maintained at the peak level as if in medium-heavy load condition, shown in Fig. 1 and Fig. 2 respectively.

The following sections are organized as follows: Section II provides the description, analyses, design considerations of the proposed Line Cycle Skipping control method; Section III discuses the digital implementation of the open and closed-loop control scheme for LCS. Section IV presents

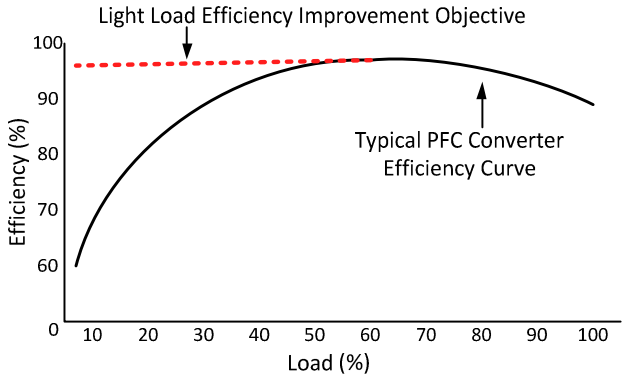

Figure 1. Light load efficiency improvement objective

experimental results; and Section V concludes the paper.

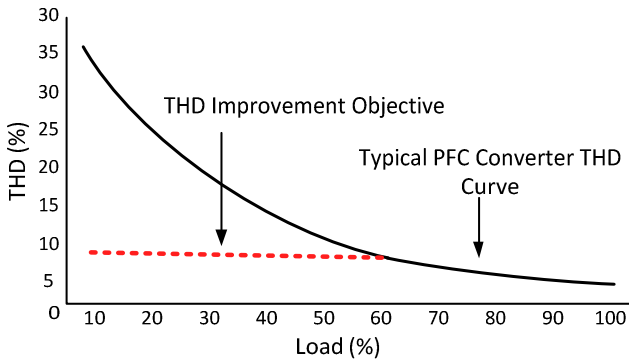

Figure 2. THD improvement objective

II. Proposed Line Cycle Skipping Method

A. Operating Principle

The operating principle of the Line Cycle Skipping (LCS) control method is described as follows: at light load, the controller will turn the PFC off for one or more line cycles depending on the load, and then turns the PFC on for one or for a one-half line cycle and draws an amount of current that corresponds to the peak efficiency power level or the power level of the designer's choice. This way, the PFC is either operating at peak efficiency or completely shut down; thus even if the average output power is low, the efficiency and THD are the same as at the peak efficiency condition. By skipping increasing amounts of line cycles, LCS is able to maintain peak efficiency and low THD throughout the entire light load range.

An example case is given in Fig. 3 to explain the two modes of the proposed LCS method. Fig. 3. describes method 1, known as full line cycle conduction (FLCC), where line current is conducted for one complete line cycle at a power level of 30W and skipped for 2 line cycles with a power draw of 0W. The average power over the entire LCS period is 10W. Fig. 4 describes method 2, known as half line cycle conduction (HLCC), where line current is conducted for one positive half line cycle with a power draw of 30W and skipped for two half line cycles drawing no power. The average output power is 10W, and the next LCS period will draw from the negative half line cycle with the same power draw sequence

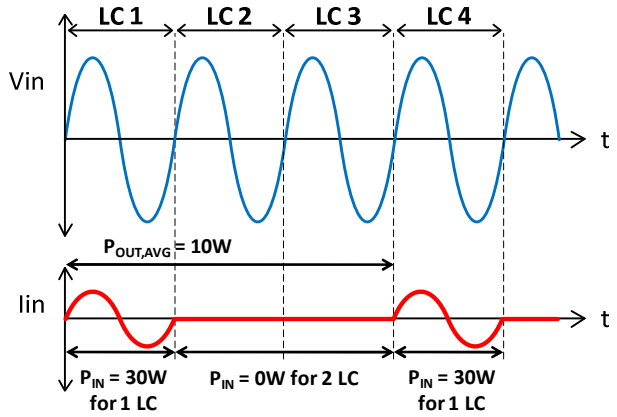

Figure 3. Method 1: full line cycle conduction (FLCC)

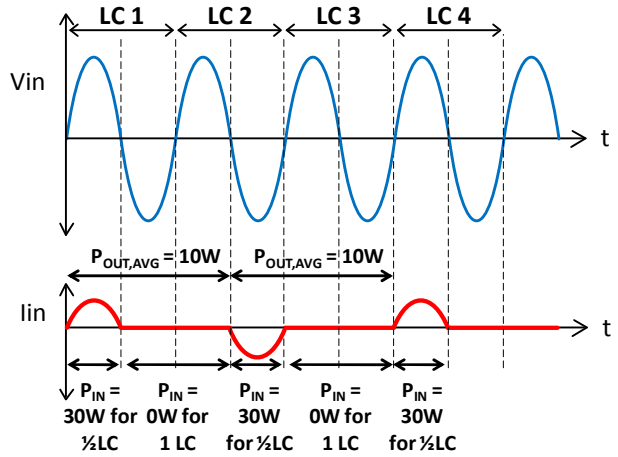

Figure 4. Method 2: half line cycle conduction (HLCC)

as before. In HLCC, line current must be conducted for an equal amount of positive and negative cycles to avoid introducing a DC bias.

B. Analyses of Light Load Efficiency and THD Improvement

Equation (1) is a general equation for the efficiency of a power converter, where the efficiency of a power converter can be determined by the output power divided by the sum of the output power and the power loss of the converter. The losses in (1) can be expanded in (2) and the output power can be determined by the input power over the conduction period when the PFC is on. As seen in (2), the driver loss and converter loss occurs only during the conduction period. The MCU loss occurs throughout the conduction and skipping period in order for the controller to remain active.

$$Eff = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (1)$$

$$Eff = \frac{P_{IN,COND}/(N+1)}{\frac{P_{IN,COND}}{N+1} + P_{DRIVER} * 1 + P_{CVTR@P_{IN}} * 1 + P_{MCU} * (N+1)} \quad (2)$$

The significance of (1) and (2) are highlighted by Figs. 3 and 4 because the operating efficiency is now equal to the average input power during the conduction period. For example, if peak efficiency is to be maintained for load levels below the power level at the peak efficiency, then that power level is used during the conduction period so that the average output power maintains peak efficiency during the entire load range. Based on this, the light load efficiency of the converter will be significantly increased and closely resemble the achievement objective shown in Fig. 1.

The LCS control method can also greatly reduce the THD of a PFC converter. Equation (3) is the equation for THD for line current conducted by a PFC converter, where I_1, I_3, I_5, I_7, I_9, … are the current amplitudes at their respective harmonics.

$$I_{THD} = \frac{\sqrt{I_3{}^2 + I_5{}^2 + I_7{}^2 + I_9{}^2 \ldots}}{I_1} \quad (3)$$

To reduce the THD of a PFC converter, the odd harmonics of the line frequency must be reduced. Ideally, a PFC converter acts like an emulated resistor to change the behavior of the non-linear load into a linear one. Therefore, the power transferred to the load will contain no harmonics. In practice,

however, harmonics are generated over that line cycle and are calculated together as the THD. When the PFC converter is turned off, no higher order harmonics of the fundamental are generated because no current is drawn from the source.

The contribution of harmonics to (4) only occurs during the period in which the PFC converter is turned on. These harmonics are generated during the conduction period, shown in Figs. 3 and 4 where the conduction period for Method 1 conducts 30W for 1 line cycle and Method 2 conducts 30W for one half line cycle. No contribution of harmonics to (4) is generated during the skipping period in either method. The harmonic contribution to (4) for either method would be generated as if the converter was operating at 30W continuously, which has a lower THD compared to operating at 10W. Therefore, the THD at the average output power observed, 10W for methods 1 and 2 respectively, is the same value of THD at 30W.

C. Analysis of output voltage ripple

The output voltage ripple increases when using LCS as compared with conventional operation, where the voltage ripple equation is shown in (3). When using LCS the output

$$\Delta V_o = \frac{P_o}{2\pi f_s V_o C_{OUT}} \quad (3)$$

voltage ripple can be approximated by equation (4), where n is the amount of line cycles skipped. If there is a requirement to fix the output voltage ripple to a certain level then (5) is used to determine what output power levels are possible for every value of n.

$$\Delta V_o = \frac{nP_o}{V_o f_s C_{OUT}} \quad (4)$$

$$P_o < \frac{\Delta V_o V_o f_s C_{OUT}}{n} \quad (5)$$

D. Design Considerations

To implement the LCS control mode, a controller only needs to detect a new half line cycle and be able to conduct sinusoidal line current for the conduction period, as well as not conduct line current for the skipping period. Since the LCS control method is based on the output voltage feedback loop, the proposed method is compatible with all PFC converters that can:

- Detect the zero crossing of the input line voltage
- Detect the output power either directly or indirectly

1) Detecting the zero crossing of the input line voltage

The zero crossing of the line input voltage must be detected in order to determine when a new half line cycle has begun. This sensing can be done after the bridge rectifier or by sensing the input line voltage directly, as shown in [20]. This detection must be done even when the PFC is turned off in order to determine how many line cycles have been skipped and when the exact moment the PFC should be turned back on. This is illustrated in Fig. 4, where the conduction period is 1 line cycle and the skipping period is 2 line cycles.

2) Detecting the output power directly or indirectly

The output power must be detected directly or indirectly in order for the LCS control method to determine the number of cycles to conduct and the number of cycles to skip. An indirect method to detect the output power is to determine the duty cycle in fixed frequency control methods (such as average current mode control), or to determine the on-time of the switch, Ton, in variable frequency control methods (such as BCM control), as it relates to input or output current. A calculation can then be done to determine the approximate output power.

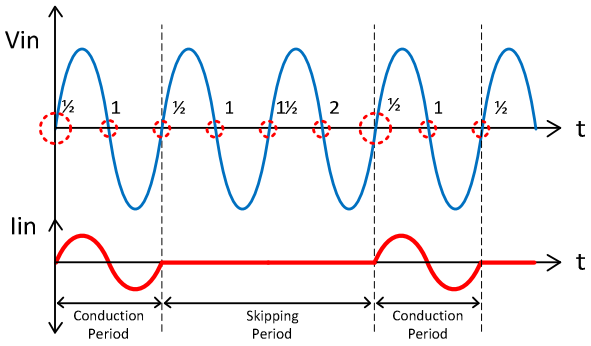

Figure 4. Zero crossing detection and cycle counting of input line voltage for determining conduction period and skipping period

To directly determine the output power, one must sense the average output current or input current as it relates to the output current and output voltage, and then calculate the output power based on these two values. The advantage of the indirect method over the direct method of determining the output power is that no additional components are needed, thereby lowering the cost.

III. Digital Implementation of Open and Closed-Loop Control of LCS

A. Digital Implementation

To implement the LCS control method digitally, the zero crossing of the line input voltage can be easily sensed using an analog to digital converter (ADC) on a MCU. Determining this zero crossing will depend on whether the line voltage is sensed directly or after the bridge rectifier. Using an additional ADC channel, the output voltage must be sensed. This sensing is usually done anyways for output voltage regulation, so the sampled voltage data can be used for both purposes.

The last piece of information needed to implement the LCS control method is the current information. As stated previously, this can be done indirectly, which is preferable because it requires less components than directly sensing, and is insensitive to noise that would otherwise be generated from measuring it directly. The duty cycle or on-time signal sent to the switch(es) will generally correlate with the input and output current information. Using this information, an internal calculation or LUT can be used at the end of each line cycle to determine the average input or output power, so that peak efficiency can be maintained throughout the entire light load range. Fig. 5 shows the digital control implementation for any PFC converter using a bridge rectifier.

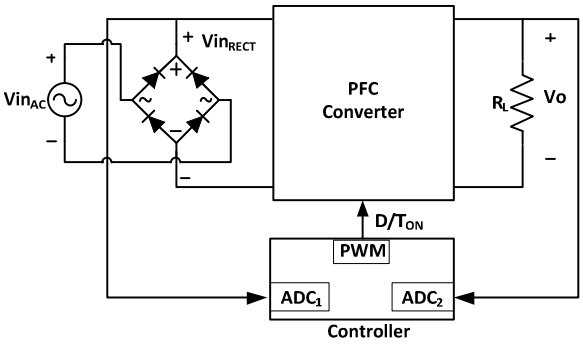

Figure 5. Digital control implementation for PFC converters

B. *Open and Closed-loop control of LCS*

A ST7FLIT19B which is an 8-bit, 8MHz MCU is used to implement the LCS for both open and closed-loop operation [22]. The system block diagram of a CRM boost converter using LCS control is shown in Fig. 6. The CRM voltage loop is unchanged from the conventional control scheme for regulating the output voltage. Input voltage is sensed and the line voltage and frequency is determined, as well as detecting new half line cycles. Open-loop control results are achieved by setting the skipping period at the fixed input voltage and load.

In order to achieve closed-loop control for LCS, look-up tables (LUTs) are utilized in order to relate on-time with output power. Once the PID outputs a new on-time, the output power is determined from a LUT. This is fed into the LCS algorithm where the skipping period is set if the output power enters the light load region and the PFC is automatically enabled and disabled by the algorithm to implement the LCS scheme.

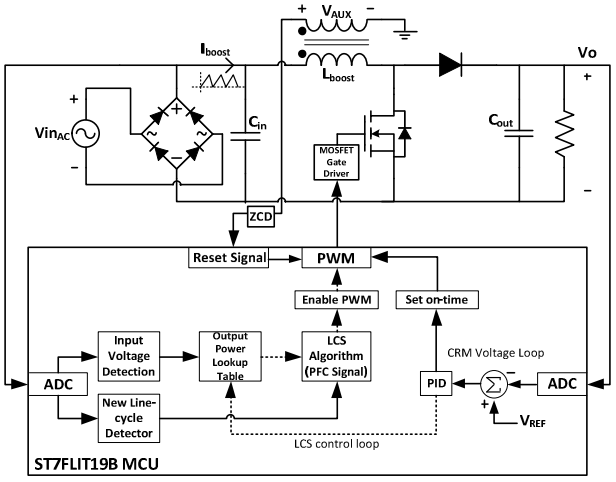

Figure 6. System block diagram for a CRM boost converter using LCS control

IV. Experimental Results

A 100W universal line input voltage PFC boost converter prototype was built and implemented with a ST7FLIT19B MCU to implement the LCS control method in order to improve the light load efficiency and reduce the THD. Fig. 7 is a photo of the experimental prototype from the schematic in Fig. 6. A ST7FLIT19B low cost 8-bit MCU is used for the digital implementation, based off a previous design for a digital ballast [23]. A constant on-time PWM is used to achieve BCM without a current reference calculation. This allows for a low cost MCU to be used in this control method, thereby lowering the total cost of the system.

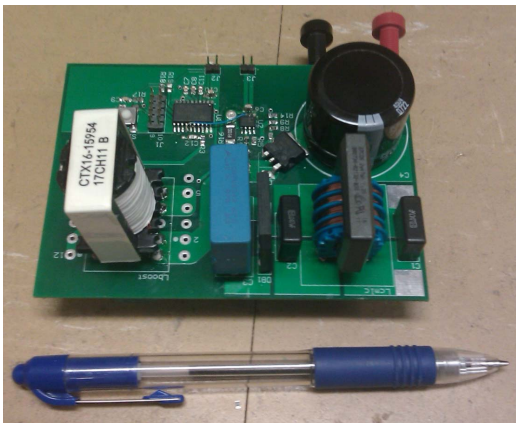

Figure 7. Experimental prototype

Table 1 describes the specifications, components and the values of the components used for the boost converter prototype. Fig. 8 shows the input line voltage and the input line current for the prototype at 50W load operating in conventional BCM with constant on-time. Fig. 9 shows the prototype operating with LCS using Method 1 for an average output power of 25W. Sinusoidal line current is conducted for 1 line cycle at a power level of 50W. The total average power is 25W. Fig. 10 shows input voltage and current waveforms using Method 2 for 10W.

As can be seen in Fig. 11, at 120 V_{RMS} input, the light load efficiency has dramatically increased by using the LCS control method. Efficiency gains as high as 7.2% at 10% load can be observed. Efficiency improvements are significant up to 50% load, when the LCS control method is used. The results for THD with and without LCS are shown in Fig. 12. As can be seen in Fig. 12, the THD is dramatically reduced by up to 15.3% at 10% load. Improvements in THD can also be seen when the LCS control method is used up to 50% load.

Table 1. Prototype specifications

Minimum Switching Frequency	22 kHz
Input Line Voltages, Vin_{AC}	120, 220 V_{RMS}
Output Voltage, *Vo*	400 Vdc
Output Power	100 W
Boost Inductor, L_{boost}	1 mH
Boost Inductor Aux. Winding	1:12 Turns
Input Filter Capacitor, *Cin*	0.47 uF ± 20%
Output Boost Capacitor, *Cout*	120 uF ± 20%
Boost MOSFET	STD10NM60N (600V, 8.0A)
Boost Diode	S8KC-13 (800V, 8.0A)
Diode Bridge Rectifier	GBU6J-BP (600V, 6A)
MCU	ST7FLIT19B, 8MHz
Low Side MOSFET Driver	MCP1407-E

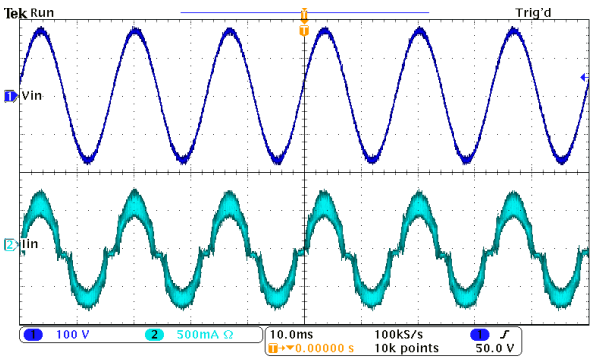

Figure 8. Input voltage and current waveforms at Pin = Po = 50W without LCS

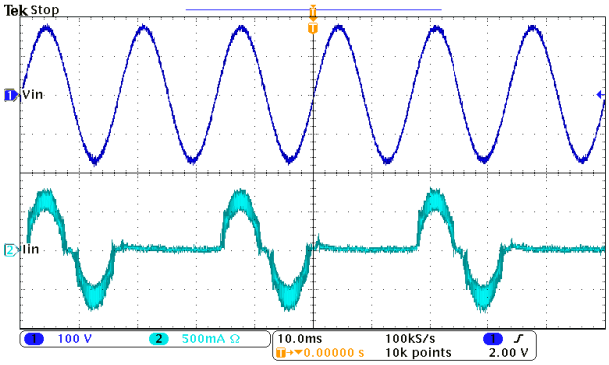

Figure 9. Input voltage and current waveforms at P_{IN} = 50W over the conduction period, $P_{OUT,AVG}$ = 25W for Method 1; 1 LC on, 1 LC off

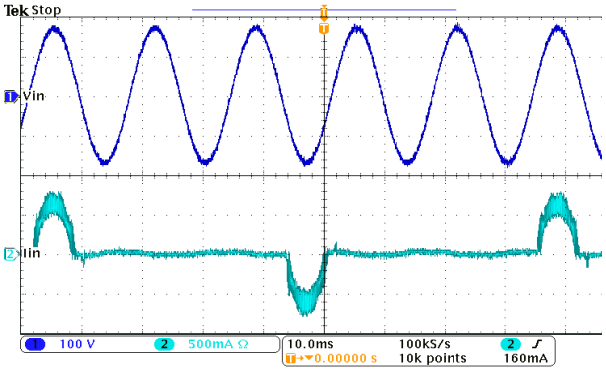

Figure 10. Input voltage and current waveforms at P_{IN} = 50W over the conduction period, $P_{OUT,AVG}$ = 10W for Method 2; 1/2 LC on, 2 LC off

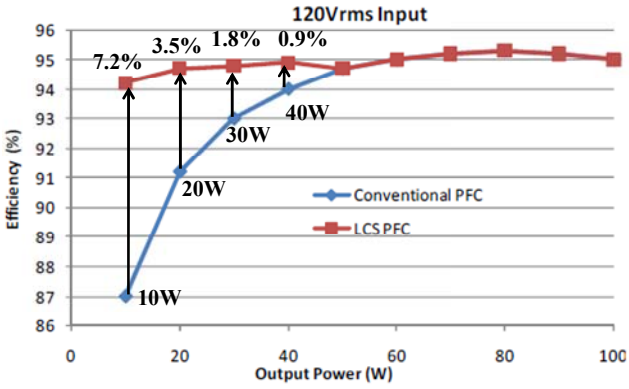

Figure 11. Efficiency results with and without LCS at 120 V_{RMS}

In addition to testing the converter at 120 V_{RMS}, the prototype was also tested at 220 V_{RMS}. As can be seen in Fig. 13, the light load efficiency has also dramatically increased by using the LCS control method at 220 V_{RMS}. Efficiency gains as high as 8.3% at 10% load can be observed. Efficiency improvements are also significant up to 50% load when the LCS control method is used. The results of THD with and without LCS are shown in Fig. 14. As can be seen in Fig. 14, the THD has again dramatically reduced. A reduction of up to 15.3% at 10% load can be observed. Improvements, again, in THD can also be seen when the LCS control method is used up to 50% load.

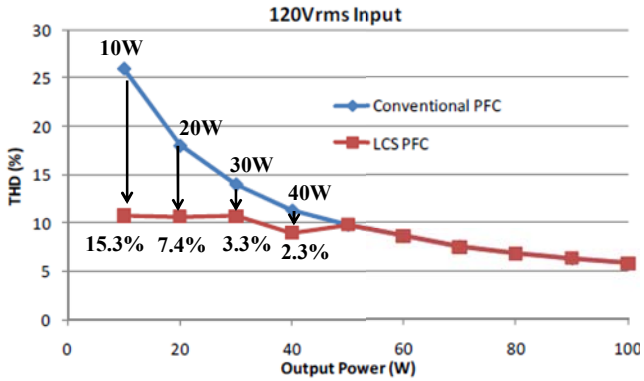

Figure 12. THD results with and without LCS at 120 V_{RMS}

Finally, additional testing at very light load was conducted and includes the controller loss, which has a more pronounced effect at very light load conditions. The conduction period power level was fixed to 30W. The power loss due to the MCU is approximately constant during the conduction period and the skipping period. This value is 47.7mW. The driver loss, however, decreases with the amount of line cycles skipped. This is due to the fact that the driver is idle during the skipping period. If the driver were to run continuously, as is usually the case in the conventional control method, the power consumption for all load levels would be approximately 51.8mW. Using LCS, results were obtained for 1W, 2W and 5W operating at 120 V_{RMS} input, shown in Table 2. The measured waveforms at 1W output are shown in Figs. 15 and 16. Graphs of the efficiency and THD results are shown in Figs. 17 and 18 respectively. As can be seen by Table 2 and Figs. 17 and 18, the MCU loss becomes more of a dominating factor in total loss as cycles skipped increases.

V. Conclusion

In this paper, a Line Cycle Skipping method is proposed to increase the light load efficiency and reduce the THD of a universal line input voltage PFC converter. It dramatically improves the light load efficiency by 7.2% and 8.6% at 10% load for 120 V_{RMS} and 220 V_{RMS} respectively. A reduction of THD by 15.3% and 17.3% at 10% load for 120 V_{RMS} and 220 V_{RMS} respectively, can also be observed using the LCS control method. Even at very light load, the LCS method maintains a high efficiency of 87.3% even at 1W operation, while also reducing the MOSFET driver power loss without additional circuitry.

The LCS control method can be applied to any PFC

Table 2. Very light load efficiency results at 120Vrms

Output Power	Line cycles skipped	Converter Loss	MCU Loss	Driver Loss	Efficiency	THD
1 W	29	72.4 mW	47.7 mW	1.8 mW	87.3%	13.4%
2 W	14	150 mW	47.7 mW	3.5 mW	90.2%	13.6%
5 W	5	420 mW	47.7 mW	8.7 mW	91.6%	13.4%

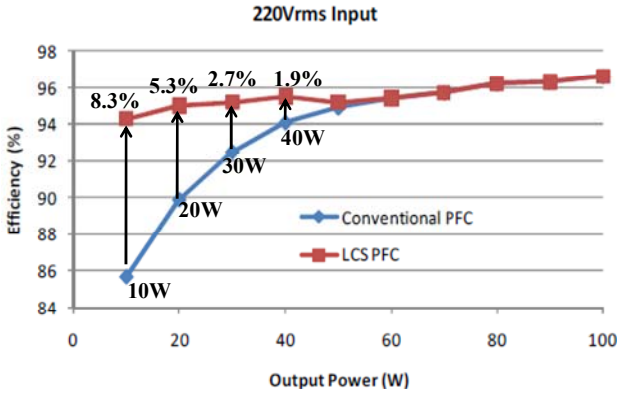

Figure 13. Efficiency results with and without LCS at 220 V_{RMS}

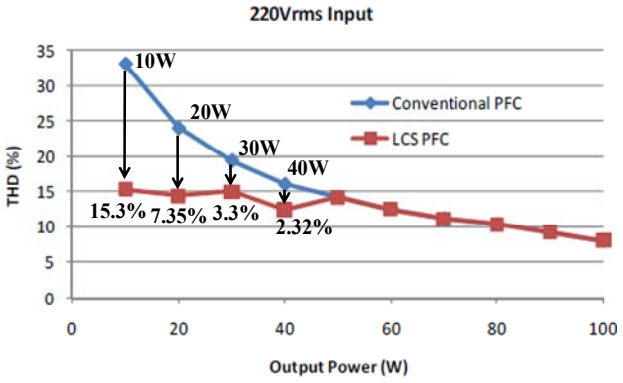

Figure 14. THD results with and without LCS at 220 V_{RMS}

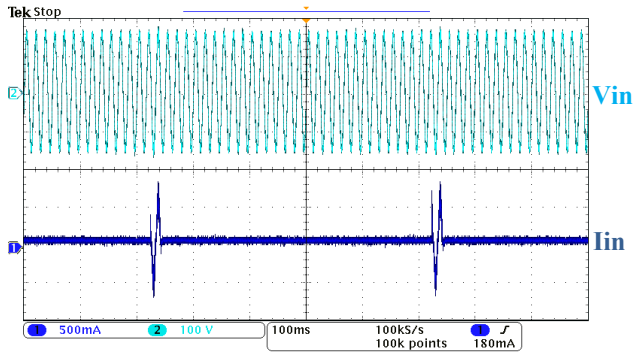

Figure 15. Input voltage and current waveforms at P_{IN} = 30W over the conduction period, $P_{OUT,AVG}$ = 1W for Method 2; 1 LC on, 29 LCs off

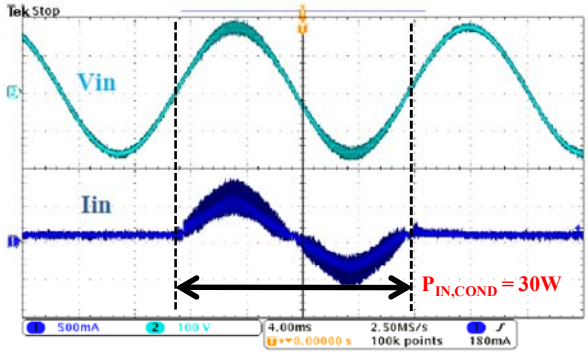

Figure 16. Expanded waveform of Fig. 14, showing conduction period

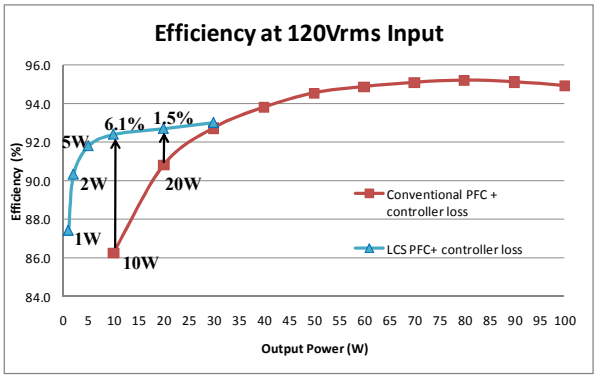

Figure 17. LCS results with fixed conduction at 30 W using 120Vrms input for efficiency

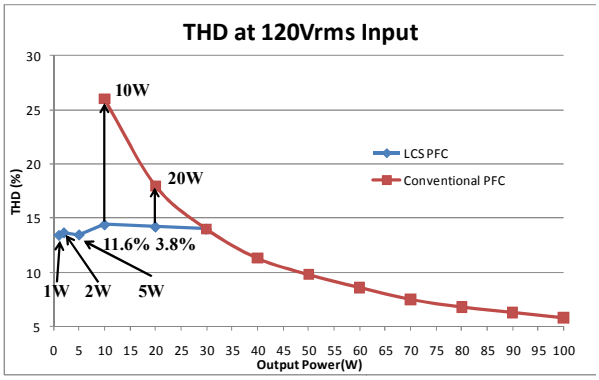

Figure 18. LCS results with fixed conduction at 30 W using 120Vrms input for THD

converter that senses the input line voltage and output power either directly or indirectly, where the latter can be achieved without adding cost or complexity. Due to the simplicity of the LCS method, a low cost MCU is used for the implementation of the control method while achieving the objective light load efficiency results and THD.

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