Digital Implementation of Load Sharing Method for Interleaved LLC Converters

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***Abstract*— LLC converter has been found advantageous in isolated DC-DC applications due to its high efficiency and low cost. However in high-power high-current applications, the high component stress and high conduction loss limit the maximum power capacity and reduce the efficiency. Interleaving technique can be employed to solve this problem, but the component tolerances of the resonant tanks will cause severe load sharing problem. This paper describes digital implementations of switch-controlled capacitor (SCC) modulated multiphase LLC converters (SCC-LLC) to achieve load sharing. A 600W two-phase interleaved SCC-LLC prototype is built to demonstrate the feasibility and advantages.**

I. INTRODUCTION

LLC resonant topology [1-4] has been widely adopted in flat-panel TVs, laptop adapters, computers, and has demonstrated its high efficiency and low cost advantages. It is also under investigation for electric vehicle charger [5], LED lighting [6], and renewable energy [7] applications. However, when the current level increases (e.g. high-performance computer may require 12V, more than 200A output), the LLC topology has the following limitations:

(a) The secondary-side conduction loss is high, which decrease the heavy-load efficiency;

(b) The output current ripple is high, which requires large output capacitance;

(c) The primary-side component stress is high, which limits the maximum power capacity;

(d) The circulation current is high, which decrease the light-load efficiency.

Above problems can be solved by using interleaving technique as has been in VRM applications for CPU. With interleaving, the high conduction loss can be reduced by splitting current into multiple phases; the high current ripple can be cancelled by interleaved phases; the power capacity can be expanded without increasing component stress; and the light-load efficiency can be improved by phase shedding.

However, interleaving requires all the LLC phases operating at the same switching frequency; but at the same switching frequency, the output current of the interleaved LLC phases will be different due to component tolerances of the resonant tanks. [8] gives an example that with commonly seen capacitor and inductor tolerances, one phase may reach peak output current while another phase may not have output current at all. As a result, the highly efficient LLC topology has not been used in high-current applications with the interleaving technique in practise.

Previously proposed load sharing methods for interleaved LLC converters [9-11] all have limitations. The authors of this paper proposed switch-controlled capacitor (SCC) modulated LLC converter (SCC-LLC) in [12] and [8] to solve the load sharing problem. The main idea is to modulate the resonant capacitance in order to compensate the component tolerances, so that load sharing can be achieved when all phases are operating at the same switching frequency. The advantage compared to previous methods is the flexibility to interleave any number of LLC stages and implement phase shedding. This paper discusses the considerations in digital control of the proposed methods in [12] and [8]. Section II describes operation principle of SCC-LLC; Section III describes SCC control mechanism and circuitry; Section IV discusses the digital control loop design; and Section V shows the experimental results from 600W prototypes of both operation schemes.

II. OPERATION PRINCIPLE

The output voltage gain of LLC converter is modulated by the ratio of switching frequency and resonant frequency. Therefore when interleaved, switching frequency cannot be used to independently modulate each LLC power stages, resonant frequency can be used instead, and load sharing can be achieved. The resonant frequency modulation can be achieved by modulating resonant capacitance using switch-controlled capacitor (SCC).

The concept of SCC was introduced in [13], which consists of a capacitor in parallel with switches. By shunting the capacitor in and out the resonant tank, the equivalent

resonant capacitance can be modulated. The proposed topology (SCC-LLC) is shown in Fig. 1. The equivalent resonant capacitance, C_r, is modulated by the SCC.

Depending on the number of switches, there are full-wave and half-wave SCCs. An improved driving scheme is proposed to prevent the MOSFET body diodes from carrying current. They are illustrated in Fig. 2 and Fig. 3.

Fig. 2 shows the structure and waveforms of a full-wave SCC. The operation is described as follows: When a resonant current, I_{AB}, is applied to the SCC, the current zero-crossing points are at angle $0, \pi, 2\pi$ …etc by definition. For a positive half-cycle where the current flows from A to B, the gating signal of S_1 is synchronized at $2n\pi$ ($n \in N$). S_1 is on initially and the current I_{AB} bypasses C_a. S_1 is then turned off at angle $2n\pi+\alpha$, where $\pi/2<\alpha<\pi$. The current flows from A to B via C_a and charges C_a as a result. At the angle $(2n+1)\ \pi$, the resonant current reverses the direction, and begins to discharge C_a. After C_a is fully discharged, and the negative current is about to flow from B to A via S_1's body diode, S_1 is turned on again to prevent the body diode from carrying current. Then S_1 remains on through the next sync point $(2n+2)\ \pi$. After which it keeps on for α angle, and is turned off at angle $(2n+2)\ \pi + \alpha$. S_2 controls the negative half-cycle and has the same procedure, except the sync point is at $(2n+1)\ \pi$. The control parameter is the angle α defined from the sync point to the turn-off point. The interval from the turn-on point to the sync point is synchronous rectification and does not have effect on the capacitance modulation. The equivalent capacitance of the full-wave SCC, C_{SC_FW}, can be modulated by the angle α. The equation is given in (1) [13].

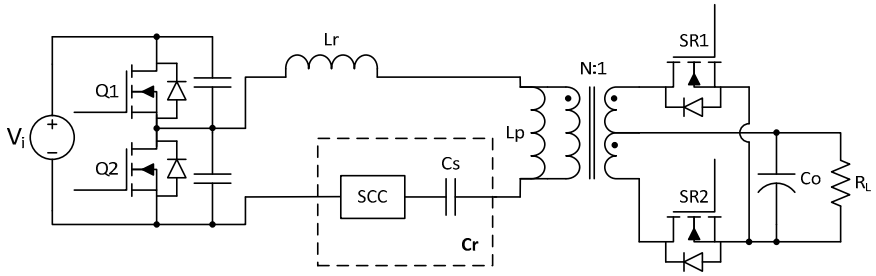

Fig. 1 Topology of the proposed SCC-LLC.

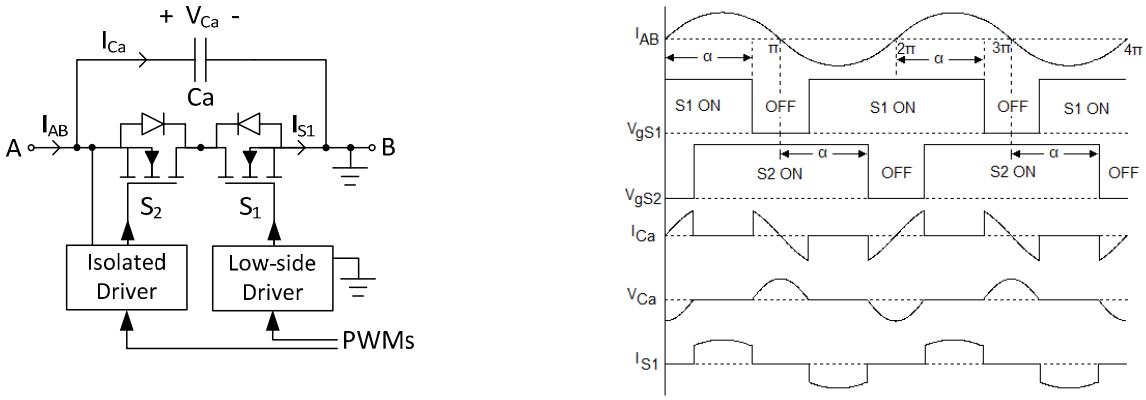

Fig. 2 Structure and waveforms of full-wave SCC.

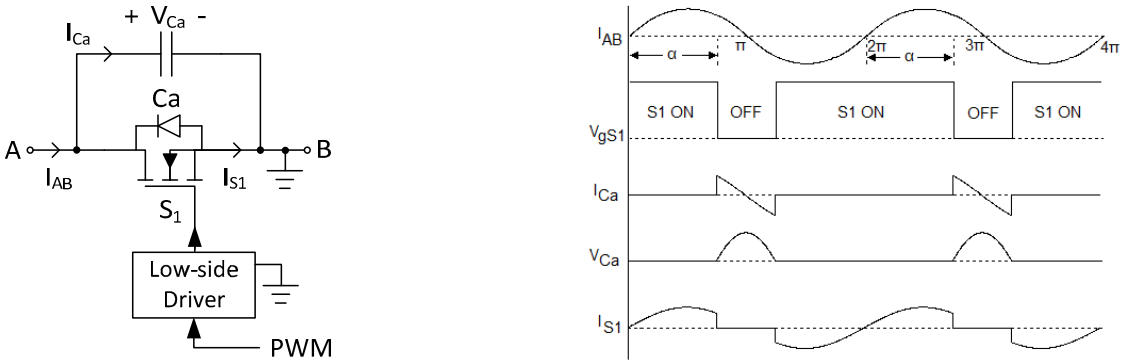

Fig. 3 Structure and waveforms of half-wave SCC.

$$C_{SC\_FW} = \frac{C_a}{2-(2\alpha-\sin 2\alpha)/\pi} \quad (1)$$

Fig. 3 shows the structure and waveforms of a half-wave SCC. The control scheme is similar to that of the full-wave SCC, except the modulation is only in one direction. The control angle range is $0<\alpha<\pi$. The equivalent capacitance of the half-wave SCC, C_{SC_HW}, is given in [14], and is rewritten in (2).

$$C_{SC\_HW} = \frac{2C_a}{2-(2\alpha-\sin 2\alpha)/\pi} \quad (2)$$

The full-wave SCC has symmetrical waveforms, which are desirable in LLC converters. The full-wave SCC is capable of regulating the LLC converter output from light load to full load at a constant switching frequency. The half-wave SCC has asymmetrical waveforms, thus it is only suitable when the resonant capacitance variation range is relatively small, and in which case the asymmetrical effect is negligible. As a result there are two control schemes for SCC-LLC: (a) constant switching frequency with full-wave SCC; (b) variable switching frequency with half-wave SCC. In (a) the full-wave SCC is responsible for both output voltage regulation and load sharing. In (b) the output voltage is regulated by switching frequency, and the half-wave SCC is only responsible for load sharing. Because load sharing only requires a small resonant capacitance variation, the asymmetrical effect of the half-wave SCC is negligible. Implementations of both schemes are discussed in the following sections.

III. Gating Logic of Switch-Controlled Capacitor

As illustrated in Fig. 2 and Fig. 3, the SCC's turn-off point is α angle past the resonant current zero-crossing points, therefore the PWM that controls SCC must be resettable by an external current sensing signal. This function is available in most digital power controllers. An example is the External PWM Reset (XPRES) function available in Microchip Inc.'s dsPIC33F DSC family, which allows an external logic signal to reset the DPWM.

The DPWM that controls the angle α must be synchronized (turn-on) at the current zero-crossing point. However, in order to prevent the SCC MOSFET's body diode from carrying current, it should be turned on as soon as the C_a voltage is discharged to zero. Therefore, a comparator is used to detect the voltage zero-crossing and trigger the SCC turn-on point.

However, because of the propagation delay of the control circuit, it is impossible to turn on the SCC MOSFET when C_a voltage is exactly zero. Therefore a small amount of energy remains in C_a after the SCC MOSFET is turned on. Since the SCC MOSFET short-circuits C_a and forms a closed current path, the remaining energy in C_a will resonate with the trace inductance, causing voltage zero-detection comparator to bounce. This mechanism is illustrated in Fig. 4.

In order to turn on SCC MOSFETs at the first fall-edge of the voltage zero-detection comparator (active-low) and ignore the subsequent bouncing, a SCC gating logic circuit is proposed in Fig. 5. Half-wave SCC is taken as an example. A full-wave SCC needs two sets of such circuit because it has

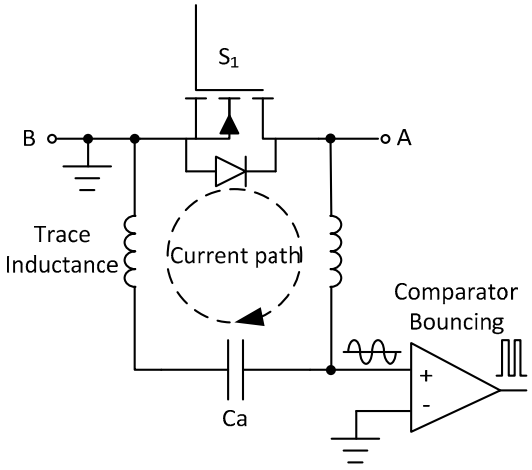

Fig. 4. Mechanism of zero-detection comparator bouncing

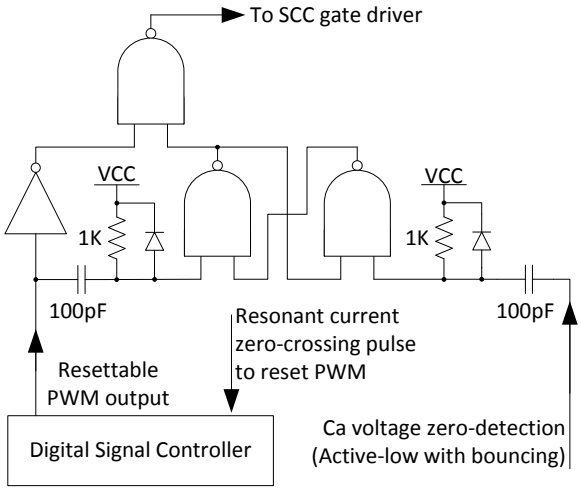

Fig. 5. SCC gating logic circuit.

two switches. The explanation of the SCC gating logic circuit is as follows.

Once the PWM output from DSC goes LOW, it passes through a NOT gate and sets the left input pin of the top NAND gate to HIGH. Meanwhile, it generates a negative pulse to SET the NAND SR latch on the right. Therefore, both input pins of the top NAND gate are HIGH, thus it outputs LOW to turn off the SCC MOSFET. Then the C_a voltage will be first charged and then discharged by the resonant current. When the C_a voltage is positive, the voltage zero-detection comparator will output HIGH, but it does not affect the output state of the SR latch. Once the C_a voltage is returned to zero, the zero-detection comparator will change state to LOW, which generates a negative pulse to RESET the SR latch. Since the right input pin of the top NAND gate is set to LOW by the SR latch, the top NAND gate outputs HIGH to turn on the SCC MOSFET. The SR latch then ignores all the subsequent bouncing from the voltage zero-detection comparator. Sometime later, the PWM is reset by the current zero-crossing signal and changes state from LOW to HIGH. This change passes through the NOT gate and sets the left input pin of the top NAND gate to LOW. Thus both

inputs of the top NAND gate are LOW and the output remains HIGH. This state will continue until the next time the PWM goes LOW. A switching cycle is completed. The negative pulses mentioned above are generated using discrete capacitor, resistor, and diode. It can be also replaced by other fall-edge detection circuits.

IV. Digital Control Loops Implementation

A Microchip DSC dsPIC33FJ32GS606 is used to implement the digital controller. A linear opto-coupler is used to transmit output voltage signal to the primary side. The control loops include a fast voltage loop and a slow load sharing loop. The hardware and firmware implementations for constant switching frequency SCC-LLC is shown in Fig. 6. The explanation is as follows.

The output voltage signal is sampled by an ADC, and then subtracted from a reference voltage value to create an error value. The error value is processed by a voltage-loop control law and becomes a base duty cycle for both SCC PWMs. Two other ADCs are used to sample the peak resonant capacitor voltage of each phase which reflects the output current level. The peak voltage sensing circuitry is adopted from [15]. The error between the two peak voltage values is processed by a load-sharing control law and becomes adjustment values of the base duty cycle. The adjusted duty cycle values are then used to control the SCC PWMs. Each SCC PWM is synchronized with the zero-crossing points of the primary-side current of the corresponding phase. The zero-crossing detection is implemented using a current transformer and a comparator. The synchronization is implemented using the DSC's External PWM Reset (XPRES) function, which allows a logic signal from the current zero-crossing detection circuit to reset the digital PWM.

The hardware and firmware implementations for variable switching frequency SCC-LLC is shown in Fig. 7. The explanation is as follows.

The output voltage signal is sampled by an ADC, and then subtracted from a reference voltage value to create an error value. The error value is processed by a voltage-loop control law and becomes the switching period for both half-bridges and SCC PWMs. The phase shift between the two half-bridges is adjusted according to the switching period. Two other ADCs are used to sample the resonant capacitor voltage, which reflects the output current level. The load sensing method is adopted from [16]. The load current error between the two phases is processed by a load-sharing control law and becomes duty cycles of the SCC PWMs. Each SCC PWM is synchronized with the zero-crossing points of the primary-side current of the corresponding phase. The zero-crossing detection is implemented using a current transformer and a comparator. The synchronization is implemented using the DSC's XPRES function. If one phase is intentionally designed to have a higher gain than the other phase, the higher-gain phase becomes a Master phase and does not need SCC modulation. Only the lower-gain phase uses SCC to match the output current to the Master phase.

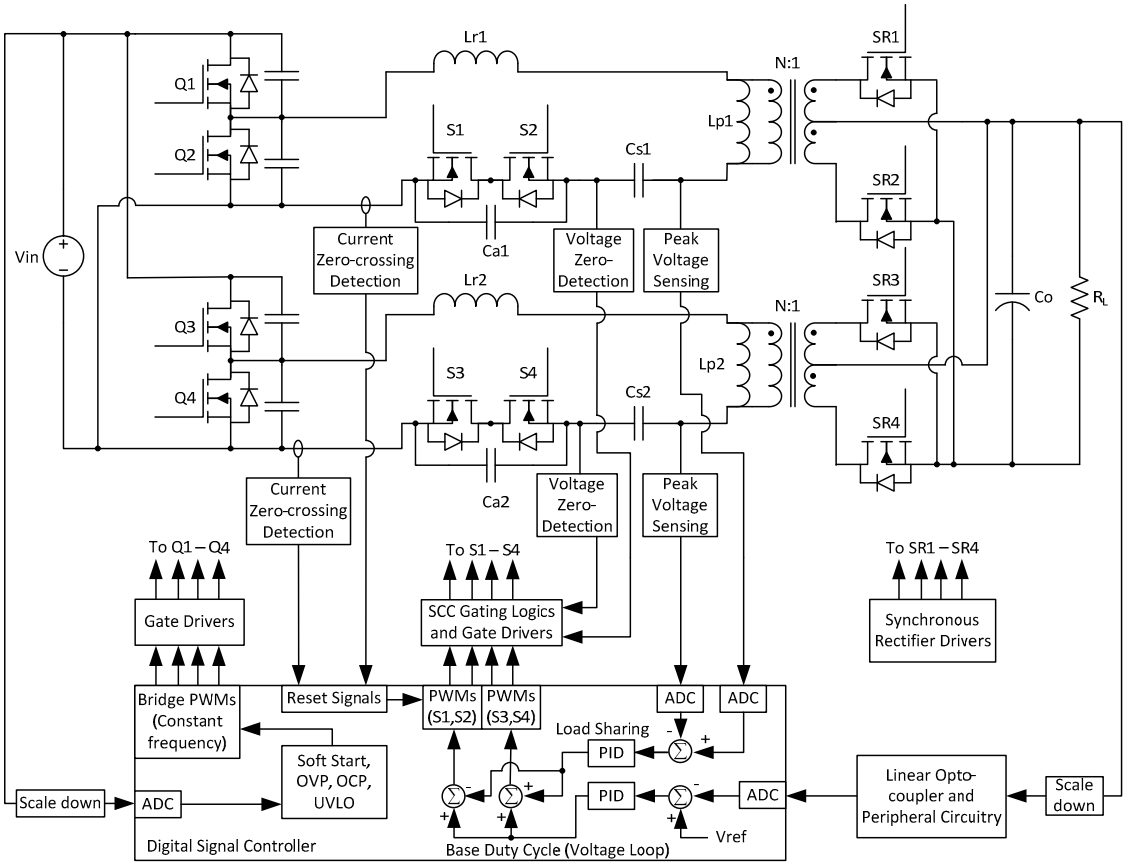

Fig. 6. System block diagram of interleaved constant switching frequency SCC-LLC with full-wave SCC.

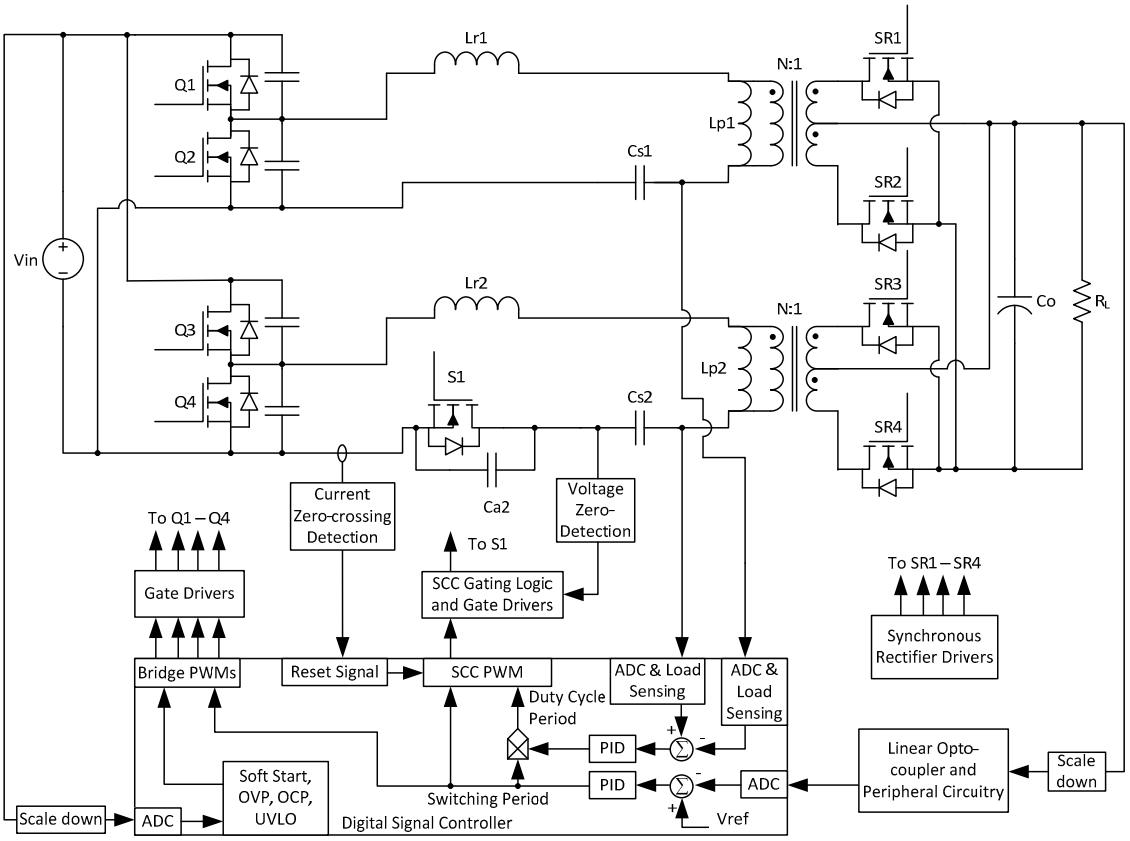

Fig. 7. System block diagram of interleaved variable switching frequency SCC-LLC with half-wave SCC.

V. Experimental Results

A 12V output, 600W two-phase interleaved SCC-LLC is implemented with both full-wave and half-wave SCCs. The design parameters are in Table 1.

Table 1 Prototype parameters

Switching frequency	Constant or variable around 200kHz
Input Voltage	400V nominal/300V minimum
Output Voltage	12V
Output Power	600W (300W × 2)
Transformer Turns Ratio	20:1, Center tapped
Magnetizing Inductance	87μH(Phase1) 85μH(Phase2)
Resonant Inductance	12μH(Phase1) 14μH(Phase2)
Series Capacitance	36nF±5% (12nF× 3, Film)
SCC Capacitance	30nF±3% (10nF× 3, Film)
Output Capacitance	1790μF (100μF× 8 + 330μF× 3)
Half-bridge MOSFET	Infineon IPB60R190C6
SCC MOSFET	Infineon BSC060N10NS3 G
SR MOSFET	Infineon BSC011N03LS

The resonant inductors of the two phases are utilizing the transformers' leakage and are intentionally made non-identical in order to test the proposed load sharing method. The resonant capacitors are also subject to tolerances.

Fig. 8 shows resonant current and C_a voltage waveforms of constant frequency full-wave SCC-LLC converter.

Fig. 9 shows resonant current and C_a voltage waveforms of variable frequency half-wave SCC-LLC converter along with SCC gating signal. Instead of turn-on at the sync points, the SCC MOSFET is turned on as soon as the C_a voltage is discharged to zero, preventing the body diode from carrying current. Small ringing on the C_a voltage after the turn-on point is visible, but it does not affect the SCC operation.

For the purpose of comparison, waveforms of a comparable 12V/600W single-phase LLC converter at 50A load, with identical output capacitance that is used in the prototype SCC-LLC are shown in Fig. 10. The output voltage ripple is 500mV.

Fig. 11 shows waveforms of the full-wave SCC-LLC with constant switching frequency at 50A load. The output voltage ripple is reduced to 180mV.

Fig. 12 shows waveforms of the half-wave SCC-LLC with variable switching frequency at 50A load. The output voltage ripple is 130mV.

Fig. 13 shows the efficiency improvement using the phase-shedding technique in the proposed SCC-LLC. The light-load efficiency at 5A (10%) load is improved from 81% to 90%.

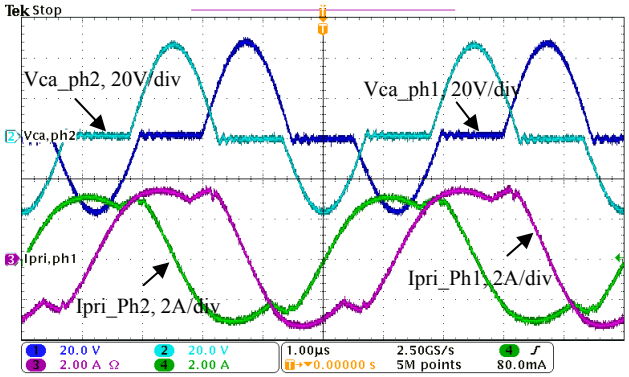

Fig. 8. Operation of full-wave SCC-LLC.

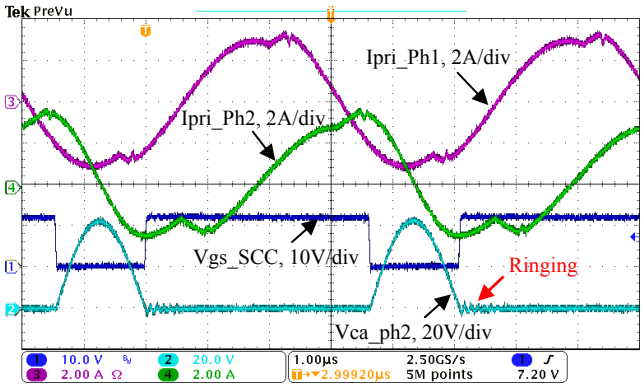

Fig. 9. Operation of half-wave SCC-LLC with SCC gating signal.

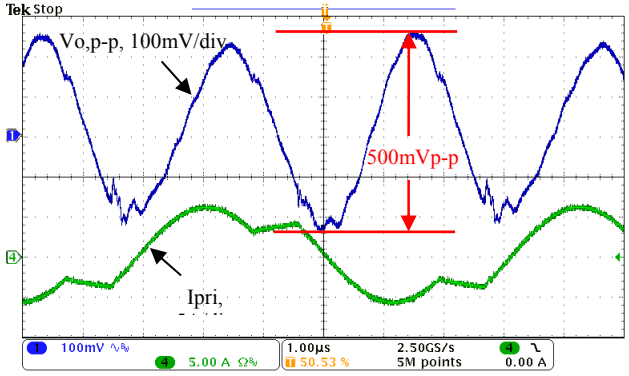

Fig. 10 Output voltage ripple, Io=50A, single phase LLC.

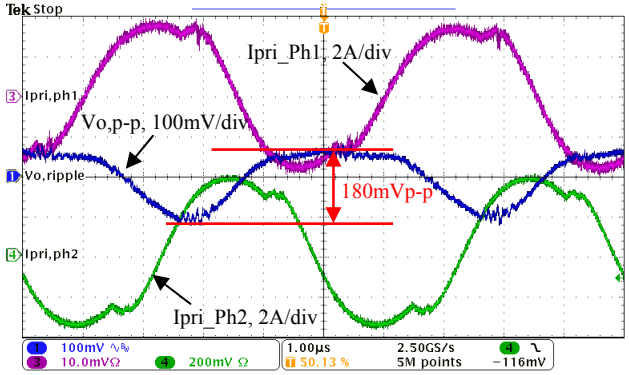

Fig. 11. Output voltage ripple, Io=50A, two-phase interleaved full-wave SCC-LLC with constant switching frequency.

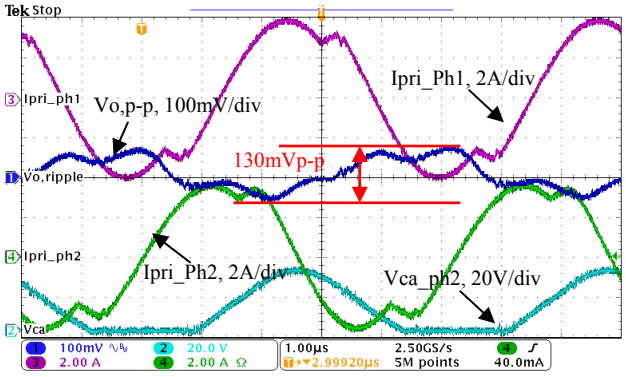

Fig. 12. Output voltage ripple, Io=50A, two-phase interleaved half-wave SCC-LLC with variable switching frequency.

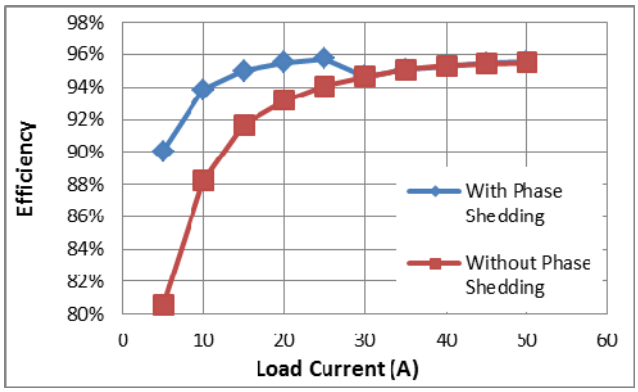

Fig. 13. Efficiency comparison, with and without phase shedding.

VI. Conclusions

In order to improve efficiency in high-current applications, interleaving and phase shedding techniques must be applied to LLC converters. The proposed SCC-LLC converters possess such capabilities and solve the load sharing problem. A significant advantage of the proposed method is the flexibility of interleaving and phase shedding on any number of LLC power stages. The digital implementations of both constant-frequency and variable-frequency control schemes are discussed in this paper in detail. Prototypes of both control schemes show good performances on load sharing, current ripple cancellation and light-load efficiency.

References

[1] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '02)*, 2002, pp. 1108-1112 vol.2.

[2] Y. Zhang, D. Xu, M. Chen, Y. Han, and Z. Du, "LLC resonant converter for 48 V to 0.9 V VRM," in *Proc. Power Electron. Specialists Conf. (PESC '04)*, 2004, pp. 1848-1854 Vol.3.

[3] S. De Simone, C. Adragna, C. Spini, and G. Gattavari, "Design-oriented steady-state analysis of LLC resonant converters based on FHA," in *Int. Symp. Power Electron., Elect. Drives, Autom., Motion (SPEEDAM '06)*, 2006, pp. 200-207.

[4] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. van Wyk, "Optimal design methodology for LLC resonant converter," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '06)*, 2006, p. 6 pp.

[5] F. Musavi, M. Craciun, D. Gautam, M. Edington, W. Eberle, and W. G. Dunford, "Control strategies for a LLC multi-resonant DC-DC converter in battery charging applications," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '13)*, 2013, pp. 1804-1811.

[6] S. Zhao, J. Xu, and O. Trescases, "A dimmable LED driver for visible light communication (VLC) based on LLC resonant DC-DC converter operating in burst mode," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '13)*, 2013, pp. 2144-2150.

[7] J.-H. Jung, H.-S. Kim, J.-H. Kim, M.-H. Ryu, and J.-W. Baek, "High efficiency bidirectional LLC resonant converter for 380V DC power distribution system using digital control scheme," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '12)*, 2012, pp. 532-538.

[8] Z. Hu, Y. Qiu, Y.-F. Liu, and P. C. Sen, "An interleaving and load sharing method for multiphase LLC converters," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '13)*, 2013, pp. 1421-1428.

[9] H. Figge, T. Grote, N. Froehleke, J. Boecker, and P. Ide, "Paralleling of LLC resonant converters using frequency controlled current balancing," in *Proc. Power Electron. Specialists Conf. (PESC '08)*, 2008, pp. 1080-1085.

[10] B.-C. Kim, K.-B. Park, C.-E. Kim, and G.-W. Moon, "Load sharing characteristic of two-phase interleaved LLC resonant converter with parallel and series input structure," in *Proc. Energy Convers. Congr. and Expo. (ECCE'09)*, 2009, pp. 750-753.

[11] E. Orietti, P. Mattavelli, G. Spiazzi, C. Adragna, and G. Gattavari, "Current sharing in three-phase LLC interleaved resonant converter," in *Proc. Energy Convers. Congr. and Expo. (ECCE'09)*, 2009, pp. 1145-1152.

[12] Z. Hu, Y. Qiu, and Y.-F. Liu, "An interleaved LLC resonant converter operating at constant switching frequency," in *Proc. Energy Convers. Congr. and Expo. (ECCE'12)*, Raleigh, NC, 2012, pp. 3541-3548.

[13] W.-J. Gu and K. Harada, "A new method to regulate resonant converters," *IEEE Trans. Power Electron.,* vol. 3, pp. 430-439, 1988.

[14] Y.-T. Chen, W.-M. Lin, and Y.-H. Liu, "Analysis and design of a dimmable electronic ballast controlled by a switch-controlled capacitor," *IEEE Trans. Ind. Electron.,* vol. 52, pp. 1564-1572, 2005.

[15] "L6599 high-voltage resonant controller," STMicroelectronics Datasheet2006.

[16] Z. Hu, Y.-F. Liu, and P. C. Sen, "Cycle-by-Cycle Average Input Current Sensing Method for LLC Resonant Topologies," in *Proc. Energy Convers. Congr. and Expo. (ECCE'13)*, 2013.