A Innovative Current Sensor-less Continuous Conduction Mode PFC Control

Peng Fang, Yan-Fei Liu
Department of Electrical and Computer Engineering
Queen's University
Kingston, ON, Canada
p.fang@queensu.ca, yanfei.liu@queensu.ca

Abstract— **For PFC working under discontinues conduction or critical conduction modes, input current sensing is not required when constant on time control is applied. However, this approach cannot be extended to PFC working under continues conduction mode. In this paper, a innovative input current sensor-less control scheme has been proposed for PFC working under continuous conduction mode. Its value in digitally controlled PFC is great since high resolution and high bandwidth current sampling A/D can be eliminated. The non-ideal effects in input current sensor-less control have also been analyzed in this paper. The proposed PFC control has been verified by our experimental prototype.**

I. INTRODUCTION

For PFC working under continues conduction mode, sensing input current is required in conventional control scheme. Input current is forced to follow current reference so that current shaping is achieved. As discussed in [2-4], obtaining real time input current information is much more difficult than obtaining real time input voltage information in digitally controlled switching mode power supply. High bandwidth and high resolution A/D conversion is required to sense input current in digitally controlled PFC, which increases technical challenge and implementation cost. In order to eliminate high cost A/D converter in digitally controlled PFC, [2-10] have proposed current rebuilding/estimation technologies without sensing input current. The input current rebuilding technology proposed in [4] is by utilizing a virtual current sensor resistor to emulate input current sensing and force virtually sensed input current to follow current reference. The input current rebuilding technology proposed in [7-9] is by using pre-programmed current value in a look-up table to calculated the required duty cycle for every switching period.

Any non-ideal effects from power circuit or control circuit will have consequences on input current shaping. Since the input current is sensed in conventional PFC control and is forced to follow current reference, these non-ideal effects can be automatically compensated. For the current sensor-less PFC control, the non-ideal effects is very critical to the shape of input current. References [3-4] have discussed the non-ideal sources from circuit which degrading the input current shaping performance in current sensor-less solutions.

Input current shaping method in most of the existing PFC control literatures is built upon the concept of forcing input current follow reference current. The computational requirement for this way of current shaping is relatively high in digital control. The duty cycle in every switching cycle is automatically achieved by feedback control. Reference [10] proposed the input current shaping method from the perspective of controlling duty cycle in every switching cycle, however, the control is greatly depended on the circuit parameter and is only suitable for certain application.

In this paper, a simple, innovative continues conduction mode PFC control is proposed. The input current shaping is achieved by directly controlling duty cycle instead of following any reference. No input current sensing is needed in our proposed technology. Non-ideal effects from circuit have been analyzed in detail and compensation method has been introduced to cancel non-ideal effects. An experimental prototype has been built and had demonstrate the effectiveness of the proposed control scheme.

This paper is arranged in the following order. Section II reviews the basic idea of the proposed current shaping scheme; Section III identifies the non-ideal effects from PCB layout and components. A compensation method which is for offsetting non-ideal effects will be introduced in section IV. The control theory and control diagram is described in section V. The experimental results are presented in section VI. Section VII is the conclusion.

II. PROPOSED CURRENT SHAPING SCHEME

For a steady state operated converter, voltage-seconds balance across the inductor is achieved between turn on and turn off. For a steady state operated converter in continuous conduction mode, its duty cycle is solely determined by the input and output voltage if parasitic components have been neglected. We have Eq. (1) to describe the duty cycle of a steady state operated boost converter working under CCM:

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$$D_F = \frac{V_{out} - V_{in}}{V_{out}} \quad (1)$$

In Eq. (1), the duty cycle is notated D_F, which means fundamental duty cycle. This fundamental duty cycle is one of the key concepts to help formulate our proposed PFC control. When a boost converter work as PFC, voltage-seconds balance across the input inductor doesn't exist within one switch cycle. The duty cycle of the boost PFC is at the vicinity of D_F. A boost PFC actually works at the quasi-steady state condition. The duty cycle expression for a boost PFC working under CCM can be described by Eq. (2):

$$D_{PFC} = D_F + D_{crt} \quad (2)$$

D_{PFC} is the duty cycle of a boost PFC. The difference between D_{PFC} and D_F is notated D_{crt} , which means a correction duty cycle. It adapt a steady state operated boost converter to a boost PFC. Since the input and output voltage can be sensed in real time, the fundamental duty cycle, D_F, can be calculated in every switching period. In order to produce a proper value of D_{PFC} for every switching period, we need to discover the value of D_{crt}.

In the following part of equations deriving, we assume that the switching frequency is much higher than the AC line frequency so that the input and output voltage can be considered as constants during one switching period. All non-ideal effects from circuit have been neglected for the time being. For the boost topology, the average voltage across the input inductor can be described by Eqs. (3), (4) and (5)

- On time

$$\langle V_{on\_L} \rangle = V_{in} \times D_{PFC} \quad (3)$$

- Off-time

$$\langle V_{off\_L} \rangle = -(V_{out} - V_{in}) \times (1 - D_{PFC}) \quad (4)$$

- One switch cycle

$$\langle V_L \rangle = \langle V_{on\_L} \rangle + \langle V_{off\_L} \rangle \quad (5)$$

$\langle V_{on\_L} \rangle$, $\langle V_{off\_L} \rangle$ and $\langle V_L \rangle$ represent the averaged voltage across the input inductor during the switch on time, the switch off time and the whole switch period respectively. Substituting equations (1), (2), (3), (4) into (5), the averaged voltage across the input inductor for the entire switch period becomes:

$$\langle V_L \rangle = V_{out} \times D_{crt} \quad (6)$$

An non-zero voltage, $\langle V_L \rangle$, across the input inductor will lead to the change of inductor's averaged current. The averaged current change, $\Delta\langle I_L \rangle$, after a switching period becomes:

$$\Delta\langle I_L \rangle = \frac{\langle V_L \rangle \times T}{L} = \frac{V_{out} \times D_{crt}}{L} \times T \quad (7)$$

Then the slope of the averaged input current can be described by equation (8):

$$\frac{d\langle I_L \rangle}{dt} = \frac{V_{out} \times D_{crt}}{L} \quad (8)$$

From Eq. (8), we can see that the input inductor current changes is dictated by D_{crt} since V_{out} and L are constant. In order to shape the averaged input inductor current to follow the input voltage, Eq. (9) need to be satisfied:

$$\langle I_L \rangle = K_1 \times V_{in} \quad (9)$$

Which then yields:

$$\frac{d\langle I_L \rangle}{dt} = K_1 \times \frac{dV_{in}}{dt} \quad (10)$$

Coefficient K_1 is a constant during a half-line cycle. Comparing Eqs. (9) and (10) yields:

$$D_{crt} = \frac{K_1 \times L}{V_{out}} \times \frac{dV_{in}}{dt} \quad (11)$$

Since K_1, L and V_{out} are all constants, equation (11) can be rewritten:

$$D_{crt} = K_2 \times \frac{dV_{in}}{dt} \quad (12)$$

Equation (12) reveals that in order to shape the input current to be a replica of input voltage, D_{crt} should be proportional to the derivative of input voltage.

Figure 1 plots D_{PFC} , D_P and D_{crt} along the change of input voltage angle for a boost PFC in a half-line cycle. For every switching period, D_{crt} is added to D_F to form the duty cycle D_{PFC} for a boost PFC.

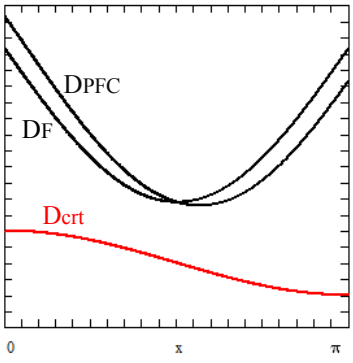

Fig. 1 PFC duty cycle plot V.S input voltage angle

Figure 2 visually explains why and how to adapt fundamental duty cycle, D_F, to D_{PFC} for a PFC application. Input current shaping is achieved by modulating the on time of every switch period. The saw-tooth signal is compared with the modulation signal. The crossover of the modulation signal and the saw-tooth signal terminates the on time pulse. V_F, V_{crt} and V_{PFC} is the modulation signal corresponding to

the generation of the duty cycle D_F, D_{crt} and D_{PFC} respectively.

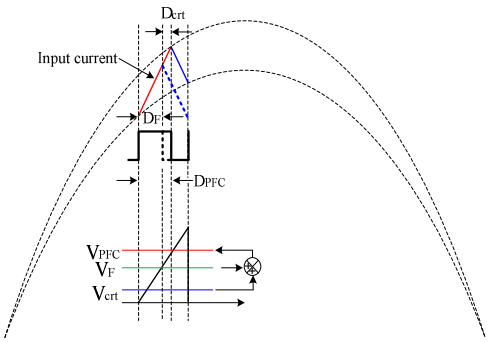

Fig. 2 PFC input current shaping by modulating duty cycle

Besides shaping input current to follow input voltage, the amplitude of the input current need also be controlled. Equation (13) describes the instantaneous value of averaged the input current:

$$\langle I_L(t)\rangle = \langle I_L(t_0)\rangle + \int_{t_0}^{T} \frac{V_{out} \times D_{crt}(t)}{L} dt \qquad (13)$$

For PFC application, the input current start from zero at the beginning of a half-line cycle, so $\langle I_L(t_0)\rangle$ is zero in Eq. (13). By reviewing Eq. (13), we know that the instantaneous averaged input current is proportional to the integration of D_{crt}. Figure 3 shows controlling input current amplitude by linearly scaling D_{crt} .

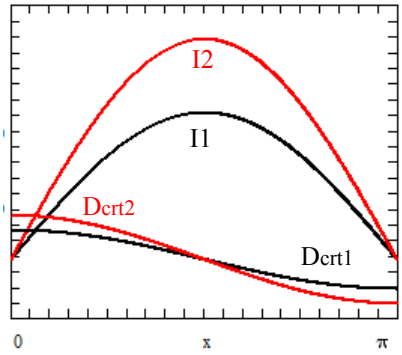

Fig. 3 Input current amplitude control

D_{crt1} corresponds to the generation of input current curve I_1 and D_{crt2} corresponds to the generation of input current curve I_2.

III. NON-IDEAL EFFECTS

In the above discussion, we neglected the non-ideal effects from circuit. For input current sensor-less PFC control, these non-ideal effects have critical impact on the final shape of input current. In this section, we will discussed the non-ideal effects in detail.

Non-ideal effects from circuit can greatly degrade the current shaping performance of input current sensor-less schemes in general . In our previous discussion, all equations derived is based on an ideal case. However, the non-ideal device characteristics we neglected will have a profound effect on how better we can shape input current. These non-ideal device characteristics include comparator input offset and its output delay, MOSFET and diode voltage drop, inductor internal resistance, gate driver circuit delay, etc. Figure 4 illustrate the power circuit of a boost converter containing parasitic components.

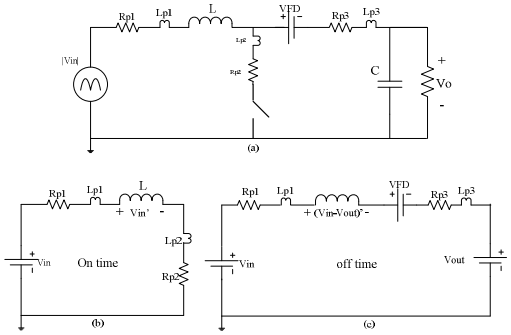

Fig. 4 (a) A boost converter model with parasitic components; (b) Equivalent circuit during on time; (c) Equivalent circuit during switching off time.

When the parasitic components participate in the operation of circuit, the equation set we derived in the previous section is not accurate anymore. During on time, the voltage across inductor is V_{in}' instead of V_{in}, and the voltage across inductor during turn off become $(V_{in} - V_{out})'$ instead of $(V_{in} - V_{out})$. The input current shaped by our proposed scheme will deviate from our expected result.

Besides the non-ideal elements from power circuit, control circuit will also contribute non-ideal elements. Such as the offset voltage and output delay from comparator, MOSEFT gate driver delay, etc. The real duty cycle presenting will deviate from the theoretical value. Figure 5 illustrates the different between the effective duty cycle and the calculated value introduced by comparator offset voltage.

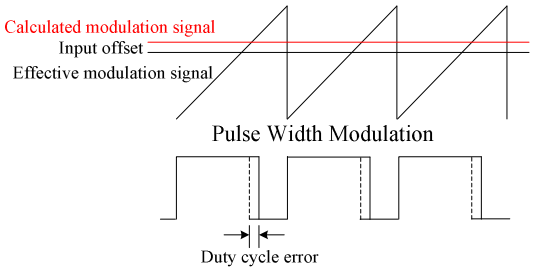

Fig. 5 Duty cycle error from comparator offset voltage

IV. DUTY CYCLE COMPENSATION FOR NON-IDEAL EFFECTS

When the circuit is ideal, the input current can be shaped to be a replica of input voltage. The input current starts from zero at the beginning of a half-line cycle and return to zero

again at the end of that half-line cycle. Figure 6 shows how input current is shaped along the change of D_{crt}. The instantaneous averaged input current, $\langle I_L(t)$, is actually proportional to the integration of D_{crt} as described by Eq.(13). The input current reaches the peak value the moment curve D_{crt} intersecting x-axis. Area A, which is the integration of D_{crt} above x-axis, can represent how much growth of the input current during the rising section. Area B, which is the integration of D_{crt} below x-axis, can represent how much receding of input current during the falling section.

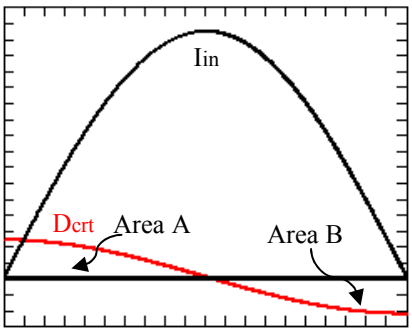

Fig. 6 Input current V.S correction duty cycle $\boldsymbol{D_{crt}}$

For the case with the perfect sinusoidal input voltage, it seems very obvious that area A equals to area B due to the symmetric operation between the current rising and falling sections. The input current change after one half-line cycle operation is zero. This conclusion can be extended to the case when input voltage is an arbitrary AC waveform. By revisiting equation (12) & (13), we can describe the current change after a half-line cycle by equation (14):

$$\begin{aligned}\langle I_L(T)\rangle - \langle I_L(0)\rangle &= \int_0^T \frac{V_{out}\times D_{crt}(t)}{L}dt \\ &= K_1 \times \int_0^T \left(\frac{dV_{in}(t)}{dt}\right)dt\end{aligned} \quad (14)$$

The term $\int_0^T \left(\frac{dV_{in}(t)}{dt}\right)dt$ in equation (14) means the input voltage change after a half-line cycle, which is always zero by definition. So the input current starts from zero will go back to zero again after a half-line cycle operation, which is irrelevant to the shape of input voltage.

When the non-ideal effects participate in the operation of circuit, situation will be very much different. The averaged voltage across input inductor during switch on time and off time can be rewritten :

- On-time

$$\begin{aligned}\langle V_{on\_L}\rangle &= V_{in}' \times D_{PFC}' = (V_{in} + \Delta v_{in})\times D_{PFC}' \\ &= V_{in}\times(D_{PFC}' + D_{err1})\end{aligned} \quad (15)$$

- Off-time

$$\begin{aligned}\langle V_{off\_L}\rangle &= -(V_{out} - V_{in})' \times (1 - D_{PFC}') \\ &= -[(V_{out} - V_{in}) + \Delta(v_{out} - v_{in})]\times(1 - D_{PFC}') \\ &= -(V_{out} - V_{in})\times(1 - D_{PFC}' - D_{err2})\end{aligned} \quad (16)$$

In the equation (15) & (16), V_{in}' and $-(V_{out} - V_{in})'$ represent the actual voltage across inductor due to non-ideal effects from power circuit. D_{PFC}' represents the actually duty cycle generated by control circuit when non-ideal effects have came into play. The error voltage, Δv_{in} and $\Delta(v_{out} - v_{in})$, have been equivalently represented as duty cycle error D_{err1} and D_{err2}. For duty cycle error introduced by the control circuit, duty cycle D_F ,D_{crt} D_{PFC} and can be rewritten as:

$$D_F' = D_F + D_{err3} \quad (17)$$

$$D_{crt}' = D_{crt} + D_{err4} \quad (18)$$

$$D_{PFC}' = D_F + D_{crt} + D_{err3} + D_{err4} \quad (19)$$

Substituting equation (6), (15), (16), (17) , (18) and (19) into Eq. (5), yields:

$$\begin{aligned}\langle V_L\rangle &= V_{out}\times(D_{crt} + D_{err1} + D_{err2} + D_{err3} + D_{err4}) \\ &= V_{out}\times(D_{crt} + D_{err\_equ})\end{aligned} \quad (20)$$

$$D_{err\_equ} = D_{err1} + D_{err2} + D_{err3} + D_{err4} \quad (21)$$

In Eq. (21), all duty cycle errors from power circuit and control circuit have been expressed equivalently by D_{err_equ}. This equivalent duty cycle error occurring in every switching period will accumulate and lead to the happening of two scenarios shown in Fig. 7:

Case A: Area A is smaller than Area B in Fig. 6, input current hit zero early than input voltage.

Case B: Area A is larger than Area B in Fig. 6, input current is still above zero when input voltage hit zero.

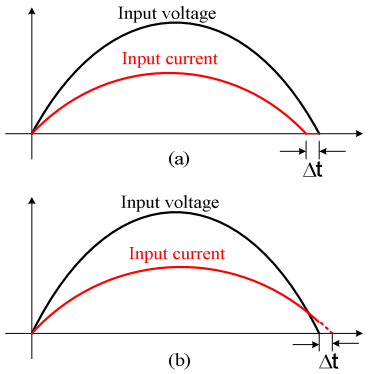

Fig. 7 (a) Input current hit zero early than input voltage; (b) Input current hit zero later than input voltage.

Reference [3] had discussed the scenario of case A and compensation method has been proposed. We generalize the consequence of non-ideal effects in this paper by including case B in our discuss. A compensation duty cycle notated D_{comp} is introduced in our proposed scheme to cancel D_{err_equ} . D_{comp} is a constant value which equals to the averaged duty cycle error in a half-line cycle and described by Eq. (21):

$$D_{comp} = \frac{\sum_{k=1}^{N} D_{err\_equ(k)}}{N} \quad (22)$$

$D_{err\_equ(k)}$ represents the equivalent duty cycle error in the k_{th} switching period while there are N times switching period exists in a half-line cycle. The value of D_{comp} is difficult to be estimated by circuit parameter. A circuit for automatically producing D_{comp} can be designed. Figure 8 shows the principle of the circuit.

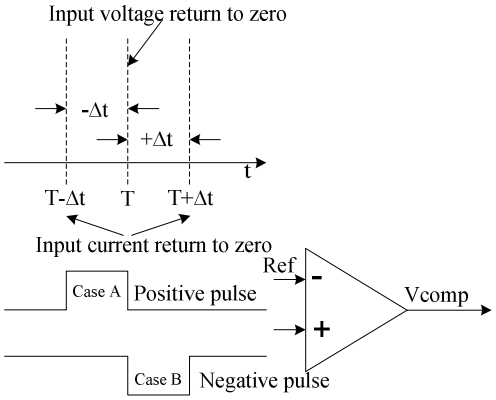

Figure 8 Duty cycle compensation circuit

In case A, the input current hit zero at time $\mathbf{T-\Delta t}$ while input voltage is still above zero. During the time slot $[\mathbf{T-\Delta t, T}]$, the input current enter into discontinues conduction mode. A positive voltage pulse with length of $\mathbf{\Delta t}$ will be generated. This positive pulse will be averaged and be compared to the reference voltage. In our design, the reference voltage is zero, which set the objective of minimize mismatch time $\boldsymbol{\Delta t}$ to zero. The averaged positive pulse is fed into the non-inverting input of amplifier, which will increase the output voltage $\boldsymbol{V_{comp}}$.

In case B, a negative pulse will be generated. A special treatment must be made when case 2 happened. By looking at Fig. 7(b), we know that the input current is still above zero when input voltage hits zero. If we continue the switching operation, the input current will start to increase instead of going down. When case B happens, the converter will be fully turned off until input current drop to zero.

V_{comp} responds for the generation of D_{comp}. A higher value V_{comp} generates a higher D_{comp} and vise verse. V_{comp} will finally settle down at the value keep Δt close to zero. The function of voltage V_{comp} will be further described in the control diagram.

The criteria of zero crossing of input current has been omitted in our above discussion. Since our proposed technology is for PFC working under CCM, a close approximation of input current reach zero is when input current enter into DCM operation. Reference [3] had discussed the detailed circuit implementation base on this criteria.

V. CONTROL THEORY

Figure 9 shows the control diagram of the proposed current shaping scheme. By detecting the zero crossing of input voltage and input current, the duty cycle compensation block generate V_{comp}. V_{comp} responds for the producing of D_{comp} , which is used to cancel duty cycle error introduced by non-ideal effects from circuit. When case B described in section IV happens, gate driver will be disabled. The converter will be in fully off mode until input current drop to zero.

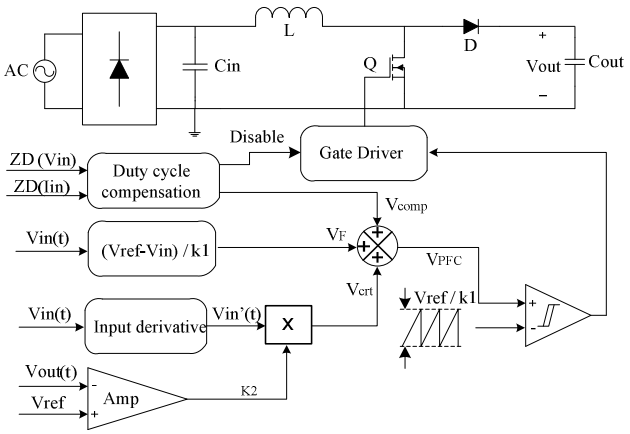

Fig. 9 Block diagram of proposed control scheme

V_{crt} is the production of input voltage derivative and constant K_2. The output voltage feedback loop control the value of K_2 so that scale V_{cort} up and down and further the amplitude of input current as discussed in section II. V_{crt} responds for the producing of duty cycle D_{crt}.

The voltage V_F is generated by calculation. It defines the fundamental duty cycle for boost converter. The sum of V_{cort}, V_F and V_{comp} is the final modulation signal, V_{PFC}, for PFC control. V_{PFC} is compared with fixed frequency saw-tooth signal with peak to peak amplitude $\frac{V_{out}}{K1}$, which outputs pulse with duty cycle D_{PFC} to perform power factor correction.

VI. EXPERIMENTAL RESULT

Table 1 shows the key circuit parameters of our experimental prototype.

Table 1 CIRCUIT PARAMETERS

AC line voltage	110V
AC line Frequency	60Hz
Output inductor	1mH
Switching frequency	40kHz
Output capacitor	470uF
Output voltage	200V
Output resistor	600Ω

Figure 10 shows the critical control signal waveform. The final pulse width modulation signal V_{PFC} is compared with the saw-tooth waveform to generate duty cycle for every switch period.

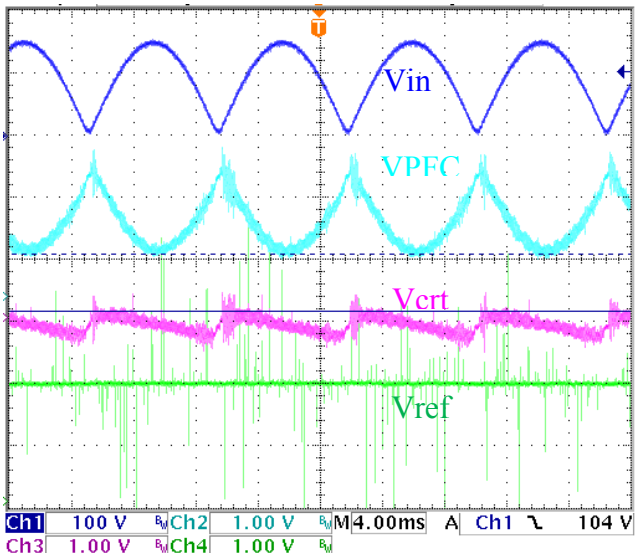

Fig. 10 Critical control signals in proposed scheme

As we can see from Fig. 10 that there are noticeable high frequency ripple and noise superimposing on the theoretical waveform of V_{PFC}. This may degrade the performance of our circuit to some extent. This situation can be improved with better PCB layout and better designed high frequency filter.

Figure 11 shows the input current shaping result. A in phase input current has been produced with our proposed current shaping method. A better current waveform should be able to achieve if the high frequency noise can be removed from control signal. A 0.98 PF has been obtained from our experimental prototype under the above shown circuit parameters.

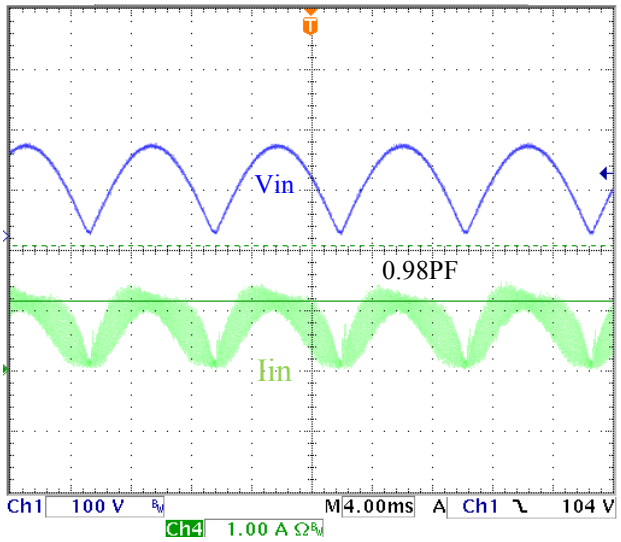

Fig. 11 Input current shaping waveform

VII. CONCLUSION

In this paper, a innovative input current sensor-less control scheme for PFC working under continues conduction mode has been proposed. The detailed current shaping method has been analyzed and non-ideal effects from circuit, which degrading the current sensor-less PFC control in general, has also been discussed in this paper. Duty cycle compensation to cancel the duty cycle error from non-ideal effects has been included in this paper. A boost PFC experimental prototype has been built with analog control circuit. An in phase input current shaping result has achieved in our experimental prototype without input current sensing. The proposed control scheme can be further implemented in digitally controlled version to justify its value of eliminating high bandwidth. high resolution A/D converter.

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