Voltage-Based Charge Balance Controller Suitable for Both Digital and Analog Implementations

Liang Jia, *Member, IEEE*, and Yan-Fei Liu, *Senior Member, IEEE*

***Abstract*—In this paper, a novel voltage-based charge balance control algorithm is presented, which is suitable for both digital and analog implementations for buck converter to achieve near-optimal dynamic performance. First, this paper presents a new derivation of practical charge balance equations based on simplified differential equations. This deviation is applicable to both fast input voltage and load step transients. The final algorithm does not require complex calculations and accurate knowledge of the output filter *LC* parameter. Second, the proposed voltage-based charge balance controller does not require accurate current sensor or fast analog-to-digital converter. Instead, to detect the critical time instant when the inductor current equals the new load current, a practical extreme voltage detector is introduced to capture the output voltage peak/valley information. Third, this algorithm is simple to be implemented by either low-cost digital signal processing devices (such as microcontroller unit) or analog circuits. Both digital and analog experimental prototypes are built to verify the feasibility and advantages of the new method.**

***Index Terms*—Adaptive voltage positioning (AVP), capacitor charge balance controller, dc–dc buck converters, digital control, extreme voltage detector, fast transient performance, optimal control.**

I. Introduction

With the revolution of integration technology, it is possible to fabricate powerful microprocessors with more and more transistors on chip, resulting in higher load demand. On the other hand, to maintain/reduce the overall power consumption, the output voltage level of the microprocessor keeps dropping. As a result, the requirements of voltage regulator (VR) for powering next-generation microprocessor are more and more stringent, that is, low-output overshoot/undershoot and short settling time (under increasingly large load transients). So it becomes much more difficult to meet the certain requirements using conventional linear-mode controllers, such as voltage- and current-mode controllers, of which the design is normally made with the help of small-signal model analysis. Due to the undesired response performance, a large volume of output capacitance is always used which occupies a big board area with linear-mode controllers. To break the bandwidth barrier for faster transient response, couples of analog controllers and digital control algorithms have been introduced to achieve this objective [1]–[24].

As one of the practical optimal control candidates, the capacitor charge balance concept was first introduced and implemented digitally in [5] for achieving minimum voltage variations and settling time. An analog implementation is presented in [19] to reduce the reaction time and improve the performance. Using field-programmable gate array (FPGA), extensive work has been conducted in designing digital charge balance control (CBC) controllers that further improves robustness [6], [8]–[12], [18], practical performance [6], [11], [12], and simplicity of the control system [6], [22]. However, all the previous schemes are not able to address at least one of the following limitations, resulting in high cost, power consumption, and long development time for controlled products:

1) Complex real-time calculation is embedded in the algorithm, like division and square root [5], [7], which requires high-speed digital control devices for working out operations in a limited time interval. And it results in high implementation cost and controller power consumption.
2) Algorithm requires the knowledge of parameters of output filter (output capacitance C_o and/or inductance L_o) in the buck converter to perform the charge balance concept, limiting the practicality/robustness of the previous schemes [5]–[7], [13], [14], [21].
3) A fast or asynchronous analog-to-digital converter (ADC) [6]–[11] is required to detect the instant when the inductor current equals the new load current, resulting in higher ADC power loss and cost.
4) Certain type of current sensor is needed to implement the proposed scheme for estimation and time detection, resulting in more cost and/or poor accuracy [5], [13], [18] and bad reliability (capacitor current sensor introduces high *dv*/*dt* noise) of the overall system [6], [18].
5) It is difficult to apply adaptive voltage positioning (AVP) or load-line regulation using proposed schemes for powering modern processors such as Intel modules [5]–[7], [14], [15].
6) Due to the complexity of the proposed algorithm and implementation limitation, it is only suitable for either digital or analog implementation.

This paper presents a novel voltage-based algorithm for CBC controller to resolve the aforementioned issues, which can be implemented by either a low-cost microcontroller unit (MCU)

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or analog devices. In order to reduce computation load/the complexity of the algorithm, this paper uses a novel and practical way to derive the charge balance equations. Unlike the previous research work that has always selected the capacitor charge and discharge integrals associated with the inductor and load current as the starting point (including [6]–[11]), in this paper, a set of simplified differential equations are used to achieve a new output voltage curve analysis-based derivation. The proposed algorithm can be extended for AVP applications with simple modifications. In addition, in order to reduce the ADC cost and power consumption, an analog extreme voltage detector is proposed to capture the output voltage peak/valley and design guideline is provided. The new method can be implemented by either a low-cost MCU or analog devices [operational amplifier (OPAMP), comparator, and sample/hold (S/H)]. In this way, no special IC is needed and customers can implement the proposed control algorithm immediately. In addition, output voltage information is a must for linear voltage-based controller. Therefore, output voltage-based charge balance concept will be a simple, practical, and cost-effective implementation.

The original idea of this paper is first presented in [4], and it mainly discusses the feasibility of the algorithm (for both load and input voltage step transient), practical extreme voltage detector for t_1, delay/ESR related accuracy estimation. And based on the same detector, a fully analog implementation is reported in [19] to present an analog integrated circuit solution for CBC.

Different from the previous publications [4], [19], this paper presents the original idea from a bigger picture and covers the full derivations and benefits of the algorithm for the purpose of applied implementations. It focuses on 1) more detailed algorithm derivations by using output voltage curve analysis instead of geometrical charge/discharge calculation for both non-AVP and AVP applications; 2) more detailed design and implementation for both digital and analog domains including signal conditioning circuit design, t_0, t_1, t_2, and t_3 detectors; and 3) advantages of two implementations are compared for different applications.

This paper is organized as follows. In Section II, the basic idea of charge balance concept will be reviewed. In Section III, mathematical formulas of the proposed algorithm based on simplified differential equations are derived. In Section IV, the extension of the proposed scheme for AVP is presented. In Section V, the digital implementation and design guidelines are provided for the proposed V-CBC algorithm and extreme voltage detector. In Section VI, a fully analog implementation is presented using OPAMPs, comparators, and S/Hs. Finally, the simulations and experimental results are demonstrated in Section VII to validate the proposed control algorithm. The conclusion is drawn in Section VIII.

II. Basis of the CBC Concept

The principle of capacitor charge balance has been used extensively for the purpose of steady-state modeling and analysis of dc–dc converters. For reference, Fig. 1 shows a synchronous buck converter, which is a general topology for VR application.

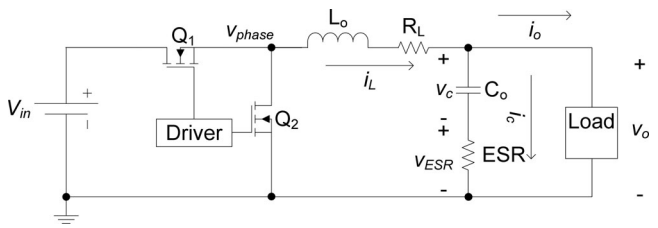

Fig. 1. Synchronous buck converter.

As the principle of capacitor charge balance presents, in steady state, the average value of the capacitor current over one switching period must be equal to zero. This condition must be satisfied in order for the output voltage to be identical at the beginning and at the end of a switching cycle. The following equation represents the principle of capacitor charge balance for a buck converter under steady state:

$$\frac{v_c[(N+1)T_{\rm sw}]-v_c(NT_{\rm sw})}{T_{\rm sw}} = \frac{1}{C_o}i_{c\_{\rm avg\_sw}}=0 \rightarrow \frac{1}{T_{\rm sw}}\int_{NT_{\rm sw}}^{(N+1)T_{\rm sw}} i_c(t)dt=0. \quad (1)$$

In (1), v_c represents the capacitor voltage (neglecting ESR and ESL), $i_{c\_{\rm avg\_sw}}$ is the capacitor current over the steady-state switching period, C_o represents the output capacitor value, and $T_{\rm sw}$ is the switching period of the converter. By recognizing that the integral period of (1) may be extended over the total transient time of a dc–dc converter, following equation is developed:

$$v_c(t_b)-v_c(t_a)=\frac{1}{C_o}i_{c\_{\rm avg\_trans}} = 0 \rightarrow \frac{1}{t_b-t_a}\int_{t_a}^{t_b} i_c(t)dt=0. \quad (2)$$

In (2), time instant t_a represents the beginning of the transient period and time instant t_b represents the end of the transient interval. $i_{c\_{\rm avg\_trans}}$ equals the average capacitor current over the transient period. Equation (2) indicates that as long as the integral of the capacitor current equals zero over the duration of the transient interval (i.e., the charge removed from the capacitor equals the charge delivered to the capacitor), the output voltage at the end of the transient will equal the voltage at the beginning of the transient. Thus, if at t_b, the inductor current i_L equals the load current and (2) has been satisfied, the output voltage will have returned to its reference voltage, and therefore, the converter has recovered from the transient event. The objective of the controller is to drive the buck converter such that the inductor current and the output voltage return to their respective steady-state values simultaneously at t_b. Therefore, the charge balance principle is a practical solution for achieving minimal settling time [5], [18] following transients.

During the steady state, linear voltage-mode controller is used extensively as a part of the charge balance controller to achieve tight output voltage regulation. Following rapid transients, for all the CBC-based controllers [5]–[16], the time instants t_1 (inductor current reaches new load current level) and t_2 (pulsewidth

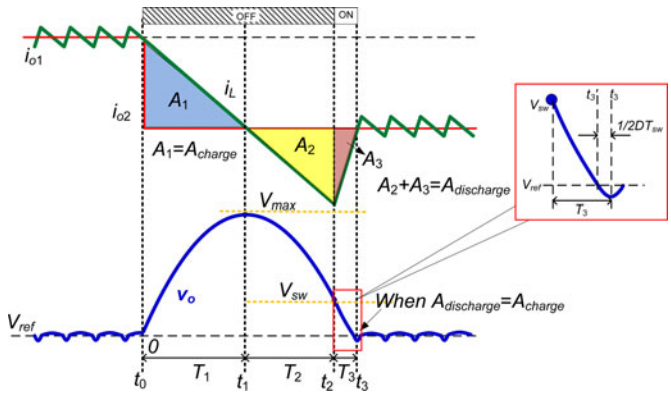

Fig. 2. Capacitor charge integral areas during an unloading step transient.

modulation (PWM) changing ON/OFF state) are very important to arrange the desired ON/OFF control actions, accordingly.

The CBC controller proposed and implemented using FPGA in [5] is based on time detection of t_0–t_3 (see Fig. 2) but requires inductor current sensing and real-time complex calculations to implement CBC. The algorithm is parameter dependent on output inductance and capacitance. The time-based method proposed in [6] uses a digital double integrator to detect the time instants t_1 and t_2, but a capacitor current estimation is required and implemented using high-speed FPGA. Another CBC controller is proposed and implemented using FPGA in [7], taking advantage of continuous time concept; however, the robustness of algorithm is limited and complex calculation is needed in real time to decide the $t_{\rm on}$ and $t_{\rm off}$ time for optimal control. The optimal control algorithm proposed in [6]–[12] is implemented also using FPGA and it applies similar geometric equation as [5] to derive the algorithm, but the time instants are determined by output voltage information instead of time intervals. However, a high-speed ADC or an asynchronous ADC is required to detect the voltage peak/valley, resulting in high cost of the implementation. A digital current-mode CBC controller is presented in [13], but because of the real-time complex calculation, a fast digital processing device is required. Also in order to set the current limit level, high-speed ADC and digital-to-analog converter (DAC) are necessary, resulting in high implementation cost and power loss.

An analog implementation of CBC controller is presented in [18] based on an analog double integrator, but the capacitor current sensor introduces high *dv*/*dt* noise, limited robustness, and ESR mismatching issues. Also, it is difficult to apply the AVP technique in this implementation. A mixed signal implementation is discussed in [15] and the time detection is based on output capacitor-ESR matching circuit, so the robustness is still limited.

The algorithm discussed in [3] focuses on solving very significant ESR impact and improving accuracy of previous methods, in which ESR is negligible in the applications such as in [4], [8]–[11], and [19]. So in order to detect t_1 when the inductor current equals load current, a curve-fitting method is utilized to build an ideal capacitor voltage curve using three output voltage samples. And for t_2 detection, time control is preferred for design simplicity. Moreover, the proposed method in [3] is more suitable for digital implementation.

In this paper, a practical extreme voltage detector is presented to find t_1 and the output voltage peak/valley is sampled. And in place of calculating interval T_2 [5], [7], [18], the time information t_2 is mapped to the switching point voltage (SPV) $V_{\rm sw}$ in the output voltage waveform. In other words, t_2 is determined by sensing the time instant when the output voltage equals $V_{\rm sw}$. The algorithm is derived based on output voltage curve analysis instead of balancing the geometric area of capacitor charge. Also an extension can be made for AVP application and input voltage step transient based on this SPV information [3].

III. Basic Idea of Voltage-Sensing-Based Charge Balance Control (V-CBC)

The CBC controller is usually designed for applications in which the load current slew rate is significantly larger than the inductor current slew rate. Therefore, in this analysis, it is assumed that the load current steps instantaneously from I_{o1} to I_{o2} and that the controller is able to react to the step with negligible delay. In the case when the load current slew rate is comparable to the inductor current, conventional voltage-mode controller will be capable of maintaining acceptable output regulation. It is also assumed that the load current remains constant for the duration of the transient period. For VR applications, sufficiently large output capacitance is required to suppress the output voltage deviation. And also for the low-voltage rating, often, the paralleled ceramic output capacitors could provide very low ESR ($<$1 mΩ). So in the following discussion, an ideal dc–dc buck converter model is examined. And the starting time t_0 is set to be 0 in the analysis for simplification in Fig. 2.

A. V-CBC Principles for a Buck Converter Undergoing an Unloading Transient

In this section, the new derivation method of CBC equations is discussed. Based on simplified solution of differential equations, the output voltage can be expressed as a piecewise parabolic function.

Step 1: Time Interval T_1 ($t_0 \le t < t_1$) for an Unloading Step Transient

In this interval, the top MOSFET Q1 of buck converter (see Fig. 1) is turned OFF. The inductor current decreases linearly, so during the time period t_0–t_1 capacitor current i_c can be approximated as a linear function in the following equation, where m_2 is the falling slew rate of the inductor current $m_2 = V_o/L_o$, V_o is the output voltage, and L_o is the output inductance

$$i_c(t)|_{t_0-t_1} = i_L - i_{o2} = -m_2(t-t_1) = -\frac{V_o}{L_o}(t-t_1). \quad (3)$$

Based on the relationship of capacitor current and voltage in (4), the capacitor voltage can be expressed, where $V_c(t_0)$ is the initial capacitor voltage. With negligible ESR, as an alternative approach for solving differential equations, the capacitor/output voltage v_o can be approximated with a parabola in (5) based on

its current i_c in the (3)

$$i_c(t) = C_o \frac{dv_c}{dt} \leftrightarrow v_c(t) = V_c(t_0) + \frac{1}{C_o}\int_{t_0}^{t} i_c \cdot dt \tag{4}$$

$$v_o(t) = v_c(t) = V_{\rm ref} + \frac{1}{C_o}\int_{t_0}^{t} i_c dt = V_{\rm ref} + \frac{m_2}{2C_o}T_1^2 - \frac{m_2}{2C_o}(t-t_1)^2. \tag{5}$$

Step 2: Time Interval T_2 ($t_1 \le t < t_2$) for an Unloading Step Transient

During this interval, the top MOSFET Q1 is still OFF. So the capacitor current follows the same slew rate as Step 1. When the inductor current i_L reaches the new steady-state load current I_{o2} at t_1, the output voltage v_o reaches its peak value, $V_{\max}$. Similarly, the capacitor current i_c can be expressed in (6), and the instantaneous output voltage v_o will be able to be computed in (7) based on the voltage $V_{\max}$ at t_1 as initial value of this period

$$i_c(t)|_{t_1-t_2} = -m_2(t-t_1) = -\frac{V_o}{L_o}(t-t_1) \tag{6}$$

$$v_o(t) = V_{\max} + \frac{1}{C_o}\int_{t_1}^{t} i_c dt = V_{\max} - \frac{m_2}{2C_o}(t-t_1)^2. \tag{7}$$

According to (7), the output voltage at t_2, called SPV, $V_{\rm sw}$, in this paper, is expressed as

$$V_{\rm sw} = v_o(t_2) = V_{\max} - \frac{m_2}{2C_o}(t_2-t_1)^2 = V_{\max} - \frac{m_2}{2C_o}T_2^2. \tag{8}$$

Step 3: Time Interval T_3 ($t_2 \le t \le t_3$) for an Unloading Step Transient

The top MOSFET Q1 of the buck converter is turned ON at t_2. The capacitor current increases linearly. Referring to the rising slope of the inductor current [$m_1 = (V_{\rm in} - V_o)/L_o$] in this interval, the capacitor current can be written as (9) and the time intervals T_2 and T_3 will follow the relationship expressed in (10):

$$i_c(t)|_{t_2-t_3} = m_1(t-t_3) = \frac{V_{\rm in}-V_o}{L_o}(t-t_3) \tag{9}$$

$$\frac{T_2}{T_3} = \frac{m_1}{m_2} = \frac{V_{\rm in}-V_o}{V_o}. \tag{10}$$

The instantaneous output voltage v_o can be calculated in (11) based on the capacitor current i_c information in (9), where $V_{\rm sw}$ is the initial value at t_2 in this interval

$$v_o(t) = V_{\rm sw} + \frac{1}{C_o}\int_{t_2}^{t} i_c(t)|_{t_2-t_3} \cdot dt = V_{\rm sw} + \frac{m_1}{2C_o}\left(t^2 + 2t_2t_3 - t_2^2 - t_3t\right). \tag{11}$$

According to (11) and the zoomed figure in Fig. 2, the output voltage at t_3 can be calculated in (12) and the inductor current is reaching the new load current level at the same time

$$v_o(t_3) = V_{\rm sw} + \frac{m_1}{2C_o}\left(-t_3^2 + 2t_2t_3 - t_2^2\right) = V_{\rm sw} - \frac{m_1}{2C_o}T_3^2. \tag{12}$$

In the zoomed figure, at t_3', the output voltage reaches the reference voltage $V_{\rm ref}$ and can be calculated in (13) based on (11)

$$v_o(t_3') = V_{\rm ref} = V_{\rm sw} - \frac{1}{2C_o}m_1\left[T_3^2 - \left(\frac{1}{2}DT_{\rm sw}\right)^2\right]. \tag{13}$$

So the SPV voltage $V_{\rm sw}$ can be calculated using (14), where the symbol $T_{\rm sw}$ represents the switching period and the $V_{\rm ref}$ is for the output voltage reference

$$V_{\rm sw} = \frac{1}{2C_o}m_1\left[T_3^2 - \left(\frac{1}{2}DT_{\rm sw}\right)^2\right] + V_{\rm ref}. \tag{14}$$

Without sacrificing the accuracy of the algorithm a lot, especially when the switched-mode power supply operates at a high frequency (>100 kHz) and narrow duty ratio (12–1.5 V), the item $(1/2DT_{\rm sw})^2$ can be neglected in (14). For example, in the experiment, T_3^2 is about 40 times larger than $(1/2DT_{\rm sw})^2$. And we obtain

$$V_{\rm sw} = \frac{1}{2C_o}m_1T_3^2 + V_{\rm ref}. \tag{15}$$

Therefore, by substituting (8) into (15), the voltage $V_{\rm sw}$ can be expressed as

$$V_{\rm sw} = \frac{m_2}{m_1}\cdot\frac{m_2}{2C_o}T_2^2 + V_{\rm ref} = \frac{m_2}{m_1}(V_{\max} - V_{\rm sw}) + V_{\rm ref}. \tag{16}$$

After that, the $V_{\rm sw}$ can be solved by moving $V_{\rm sw}$ terms on both sides of (16) to one side. The intermediate result is shown as follows:

$$V_{\rm sw} = \frac{\frac{m_2}{m_1}V_{\max} + V_{\rm ref}}{1 + \frac{m_2}{m_1}}. \tag{17}$$

After substituting (10) into (17) and simplifying, the final equation for calculating $V_{\rm sw}$ is expressed as

$$V_{\rm sw} = DV_{\max} + (1-D)V_{\rm ref}. \tag{18}$$

In (18), only coefficient multiplications and additions are required based on the steady-state duty cycle D and voltage information $V_{\max}$ and $V_{\rm ref}$. Therefore, SPV can be simply calculated by low-cost MCU in about ten system clock cycles. Or an OPAMP circuitry can be used to generate the analog signal of $V_{\rm sw}$ based on $V_{\max}$, $V_{\rm ref}$, and gains of D and $(1-D)$.

However, to implement (18), the peak voltage information $V_{\max}$ is required. Therefore, an analog extreme voltage detector is employed in this paper to locate the voltage peak at time instant t_1, which is discussed in detail in Section V-A.

B. V-CBC Equation for a Buck Converter Undergoing a Loading Step Transient

Similar to the previous section, this section derives the equation of SPV $V_{\rm sw}$ for loading step transient based on the waveforms shown in Fig. 3.

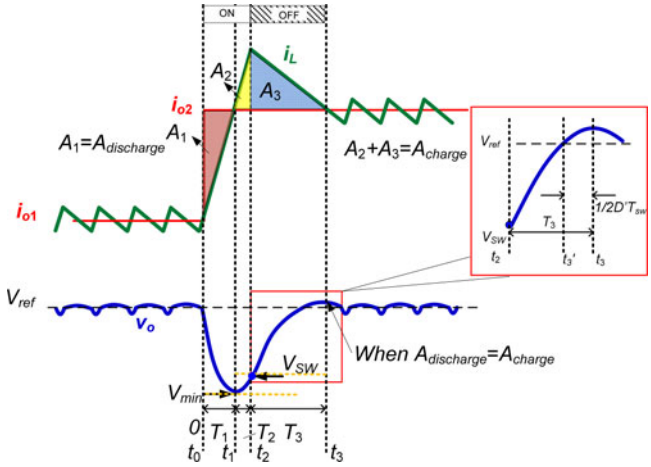

Fig. 3. Capacitor charge integral areas during a loading step transient.

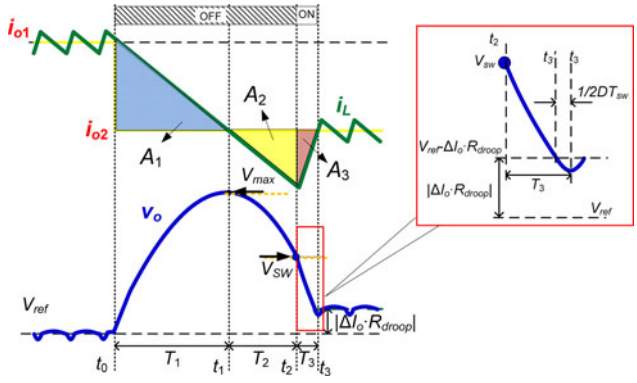

Fig. 4. Inductor current and capacitor voltage waveforms for AVP applications under unloading step transient case (R_{droop}: droop resistance).

During the time intervals t_0–t_2 and t_2–t_3, the capacitor current can be expressed as a linear function in (19) and (20), respectively

$$i_c(t)|_{t_0-t_2} = m_1(t - t_1) \tag{19}$$

$$i_c(t)|_{t_2-t_3} = -m_2(t - t_3). \tag{20}$$

Based on the simplified differential equations, the voltage V_{sw} can be calculated using (21), where the symbol T_{sw} is the switching period and V_{ref} is the output voltage reference, while (22) provides the formula for voltage V_{min}

$$V_{\mathrm{sw}} = V_{\mathrm{ref}} - \frac{1}{2C_o} m_2 \left[T_3^2 - \left(\frac{1}{2} D' T_{\mathrm{sw}} \right)^2 \right] \tag{21}$$

$$V_{\mathrm{min}} = V_{\mathrm{sw}} - \frac{1}{2C_o} m_1 T_2^2 \tag{22}$$

Similarly, the item $(1/2D'T_{\mathrm{sw}})^2$ can be ignored in (21), where $D' = 1 - D$. For example, in the experiment, T_3^2 is about ten times larger than $(1/2D'T_{\mathrm{sw}})^2$. Therefore, the voltage V_{sw} can be derived as (23), where $m_1/m_2 = (V_{\mathrm{in}} - V_o)/V_o = T_3/T_2$. By combining (21) and (22), the SPV can be expressed as follows:

$$V_{\mathrm{sw}} = V_{\mathrm{ref}} + \frac{m_2(V_{\mathrm{max}} - V_{\mathrm{sw}})}{m_1} = DV_{\mathrm{ref}} + (1 - D)V_{\mathrm{min}}. \tag{23}$$

According to the voltage V_{sw}, we can change the main switch state from on-state to off-state at t_2. Using the derived (18) and (23), only coefficient multiplications and additions are required in the calculation, so the first drawback discussed in Section I can be solved. Since (18) and (23) are independent of neither inductance nor capacitance, the second prementioned drawback in Section I is also solved.

This derivation provides a unique feature for optimizing both load and input voltage transients [3]. To optimize the input voltage transient, the two-switching-cycle compensation algorithm proposed in [17] has several limitations, such as, losing its applicability for the ultrafast/large input voltage change scenarios ($\geq$2.5 V) and requiring accurate output filter component value (L_o and C_o) and current sensing information to calculate the formulas and control the converter. Although the input voltage transient slew rate is often limited by the input filter which in fact weakens the practicability and advantage of the CBC controller for improving input voltage transient cases, it is definitely the unique feature for the proposed algorithm to solve both of the transient cases from input and output sides without adding algorithm complexity. But, because of the limited space, this paper only focuses on fast load transient cases.

Although in the deviation, the ESR is ignored for simplification, previous research has been conducted to verify that the main effect of ESR will be estimation error of V_{sw} ($<$5%) and slightly longer recovery time [3]. Therefore, even with significant ESR, the proposed V-CBC algorithm still maintains very good accuracy [3].

IV. Application Extensions of the Proposed V-CBC Algorithm

The proposed V-CBC algorithm can be extended for AVP technique with small modifications. In this case, inductor current sensing is required for load-line regulation. AVP (also known as load-line regulation) has increasingly become a requirement in many buck converter applications, for example, Intel's CPU VRs. Load-line regulation essentially involves outputting lower voltages during higher load current conditions. This assists in improving the overall transient performance of the converter and decreasing power consumption of the load device.

A. V-CBC Principles for a Buck Converter Undergoing an Unloading Transient With AVP

In unloading transient cases, V_{max} value will be usually larger than the voltage positioning window $|\Delta I_o \cdot R_{\mathrm{droop}}|$ shown in Fig. 4. At time instant t_3, instead of recovering the output voltage to V_{ref}, the AVP technique maintains the new steady-state output voltage depending on the load line at $V_{\mathrm{ref}} - \Delta I_o \cdot R_{\mathrm{droop}}$.

Similarly, the SPV V_{sw} can be calculated by referring to the analysis of parabolic curve during t_1–t_2 in (7). Considering the new AVP level, the SPV V_{sw} can also be expressed during t_2–t_3. In the zoomed figure, at t_3', the output voltage reaches the reference voltage V_{ref} and can be calculated in the following

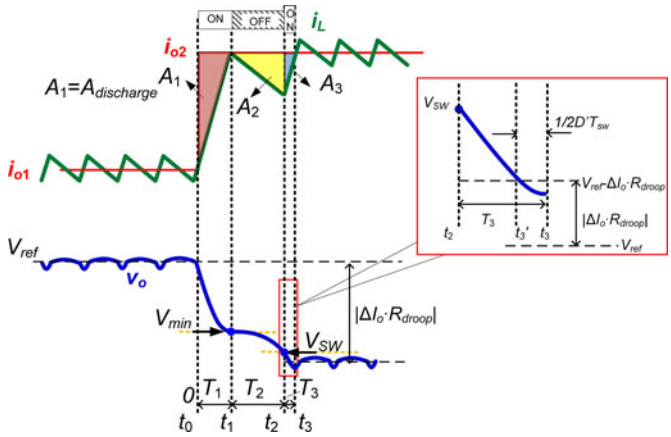

Fig. 5. Inductor current and capacitor voltage waveforms for AVP applications under loading step transient case.

equation based on (11):

$$v_o(t_3') = V_{\text{ref}} - \Delta I_o \cdot R_{\text{droop}} = V_{\text{sw}} - \frac{1}{2C_o} m_1 \left[T_3^2 - \left(\frac{1}{2} D T_{\text{sw}} \right)^2 \right]. \quad (24)$$

And, as previously discussed, the term $(1/2DT_{\text{sw}})^2$ can be ignored in (24) when the buck converter is operated at high switching frequency and narrow output duty ratio

$$V_{\text{sw}} = \frac{1}{2C_o} m_1 T_3^2 + (V_{\text{ref}} - R_{\text{droop}} \cdot \Delta I_o). \quad (25)$$

Therefore, by substituting the (7) into (25), the voltage V_{sw} can be expressed as

$$V_{\text{SW}} = \frac{m_2}{m_1} \cdot \frac{m_2}{2C_o} T_2^2 + (V_{\text{ref}} - R_{\text{droop}} \cdot \Delta I_o) = \frac{m_2}{m_1} (V_{\max} - V_{\text{sw}}) + (V_{\text{ref}} - R_{\text{droop}} \cdot \Delta I_o). \quad (26)$$

After that, the V_{sw} can be solved by moving V_{sw} terms on both sides of the (26) to one side. The simplified equation of the SPV V_{sw} is

$$V_{\text{sw}} = DV_{\max} + (1 - D)(V_{\text{ref}} - R_{\text{droop}} \cdot \Delta I_o). \quad (27)$$

It is noted from the (27) and (18), we can simply replace the voltage V_{ref} with the new load-line voltage at $V_{\text{ref}} - \Delta I_o \cdot R_{\text{droop}}$.

B. V-CBC Equation for a Buck Converter Undergoing a Loading Step Transient

For loading transient, the undershoot $V_{\min}$ is usually smaller than the voltage positioning window $|\Delta I_o \cdot R_{\text{droop}}|$ shown in Fig. 5. The switching sequences are slightly different from the previous non-AVP cases and unloading AVP case. Instead of keeping turning ON the top MOSFET Q1, during t_1 and t_2, the top MOSFET will be turned OFF. But the same SPV V_{sw} concept applies and when output voltage lower than V_{sw}, the top MOSFET will be switched on again. Similarly, at t_3, when the output voltage reaches the voltage positioning level $|\Delta I_o \cdot R_{\text{droop}}|$, the linear voltage-mode controller will take over the regulation.

Based on the similar parabolic functions in Section III-B, the output voltage v_o can be considered as three pieces of parabolas, which are the intervals of t_0–t_1, t_1–t_2, and t_2–t_3, respectively.

During t_1 and t_2, the capacitor current can be expressed in (28) and the parabolic output voltage waveform can be calculated in (29)

$$i_c(t)|_{t_1-t_2} = -m_2(t - t_1) = -\frac{V_o}{L_o}(t - t_1) \quad (28)$$

$$v_o(t) = V_{\min} + \frac{1}{C_o} \int_{t_1}^{t} i_c dt = V_{\min} - \frac{m_2}{2C_o} (t - t_1)^2. \quad (29)$$

At t_2, the SPV can be calculated as

$$v_o(t_2) = V_{\text{sw}} = V_{\min} - \frac{1}{2C_o} m_2 T_2^2. \quad (30)$$

The capacitor current and output voltage during t_2 and t_3 can be expressed by

$$i_c(t)|_{t_2-t_3} = m_1(t - t_3) = \frac{V_{\text{in}} - V_o}{L_o}(t - t_3) \quad (31)$$

$$v_o(t) = V_{\text{sw}} + \frac{1}{C_o} \int_{t_2}^{t} i_c(t)|_{t_2-t_3} \cdot dt = V_{\text{sw}} + \frac{m_1}{2C_o} \left(t^2 + 2t_2 t_3 - t_2^2 - t_3 t \right). \quad (32)$$

Using the parabolic equation in (32), the output voltage at t_3' during loading transient with AVP can be calculated using (33), where the symbol T_{sw} is the switching period and the V_{ref} is the output voltage reference

$$v_o(t_3') = V_{\text{ref}} - R_{\text{droop}} \cdot \Delta I_o = V_{\text{sw}} - \frac{1}{2C_o} m_1 \left[T_3^2 - \left(\frac{1}{2} D' T_{\text{sw}} \right)^2 \right]. \quad (33)$$

Similarly, the item $(1/2D'T_{\text{sw}})^2$ can be ignored in (33) to obtain the SPV V_{sw} in the following equation, where $D' = 1 - D$:

$$V_{\text{sw}} = (V_{\text{ref}} - R_{\text{droop}} \cdot \Delta I_o) - \frac{1}{2C_o} m_1 T_3^2. \quad (34)$$

Therefore, combining (30) and (34), the simplified V_{sw} can be expressed as

$$V_{\text{sw}} = D(V_{\text{ref}} - R_{\text{droop}} \cdot \Delta I_o) + (1 - D) V_{\min}. \quad (35)$$

The proposed V-CBC can be applied to AVP operation with two minor implementation modifications: 1) adding inductor current sensing and 2) one more ADC channel to the MCU or one more analog input signal to OPAMP. In this section, the analysis is conducted and the implementation modification will be discussed in the Sections V and VI.

V. Digital Implementation of the Proposed V-CBC Algorithm

The high-level system diagram of the digital implementation of the proposed V-CBC algorithm for a synchronous buck converter for both non-AVP and AVP applications is illustrated in

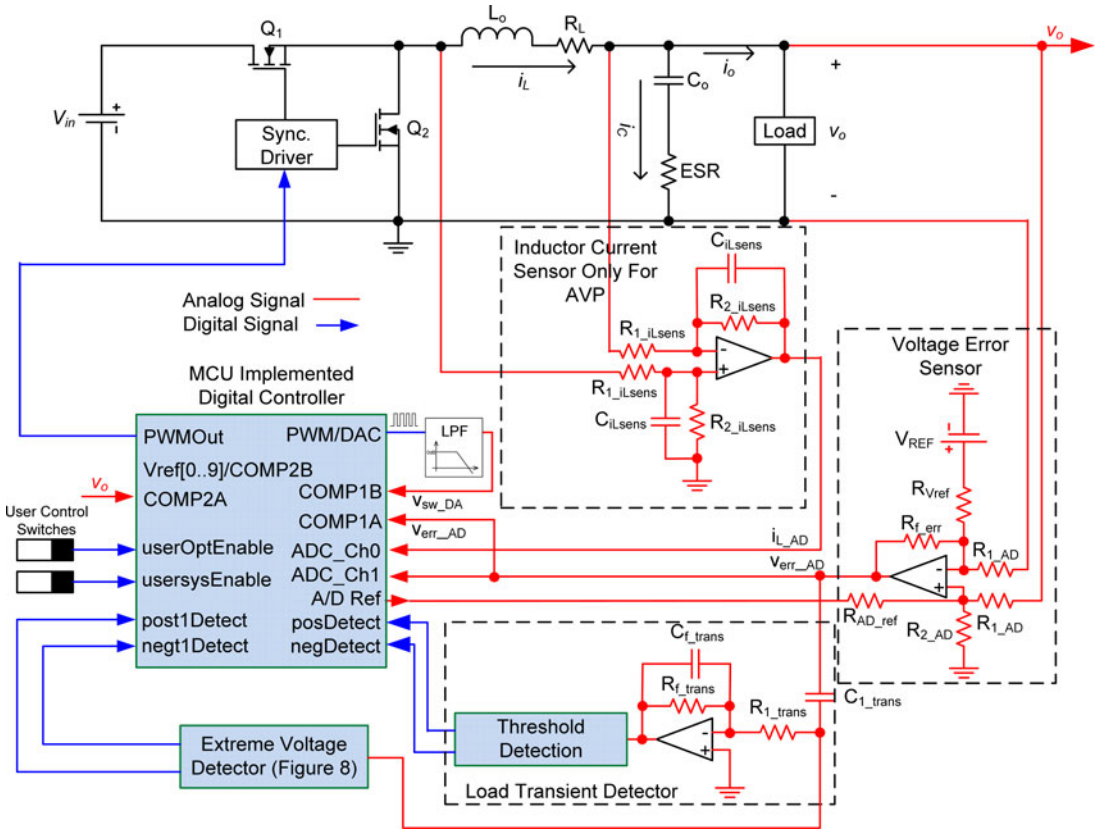

Fig. 6. Hardware implementation diagram of the digital control system.

Fig. 6. The main function blocks are extreme voltage detector, load transient detector, voltage error sensor, and the MCU controller. Although analog circuit is utilized in this implementation to improve the digital controller's major drawback of discrete sampling, the proposed controller is classified as digital controller because 1) the algorithm for $V_{\rm sw}$ in (18), (23), (27), and (35), and PID controller are calculated using the MCU and 2) the controller offers digital flexibility such as dynamic voltage identificator (VID) and on-the-fly AVP.

A. *Extreme Voltage Detector Design (For t_1 Detection)*

Because of the current sensor mismatching [13], [18], noise, ADC cost, and accuracy issue [6], [7], [9]–[12] as mentioned previously, a practical extreme voltage detector is used in this paper to detect t_1 and above all, to sample the peak/valley voltage $V_{\rm max}$/$V_{\rm min}$. In Fig. 7, for example, during an unloading step transient, the output voltage overshoot is delayed with a period of time $t_{\rm delay}$, and represented as $v_{o\_{\rm delay}}$. This delay can be equalized with first-order OPAMP circuit based on *Padè* Approximation [27] in (36). Then, both v_o and $v_{o\_{\rm delay}}$ will be fed to a comparator. The delay time $t_{\rm delay}$ and the error voltage $v_{\rm err}$ is related to each other. Based on a selected $t_{\rm delay}$, the $v_{\rm err}$ can be estimated, and thus, the comparator hysteresis can be set. In this way, as soon as the absolute value of voltage difference between the original voltage v_o and the delayed voltage $v_{o\_{\rm delay}}$ is less than $v_{\rm err}$ (set by the hysteresis of the comparator), the comparator output will change from low to high and t_1 is detected. The rising edge is used to trigger the ADC to sample the output voltage, and therefore, $V_{\rm max}$ can be obtained.

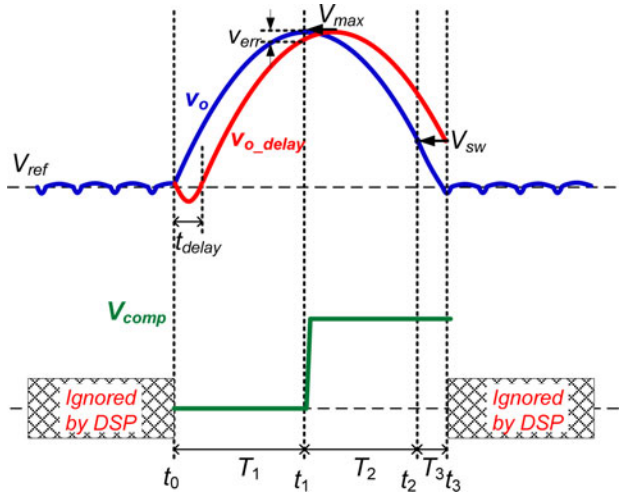

Fig. 7. Illustration of the proposed analog extreme voltage detector under unloading step transient case for t_1 detection and $V_{\rm max}$ sensing.

In Fig. 8, an adjustable delay circuit is synthesized based on the *Padè* approximation

$$\frac{v_{o\_{\rm delay}}}{v_o} = e^{-\tau s} \approx \frac{1-\tau s/2}{1+\tau s/2} = \frac{1-R_T C_T s}{1+R_T C_T s}. \tag{36}$$

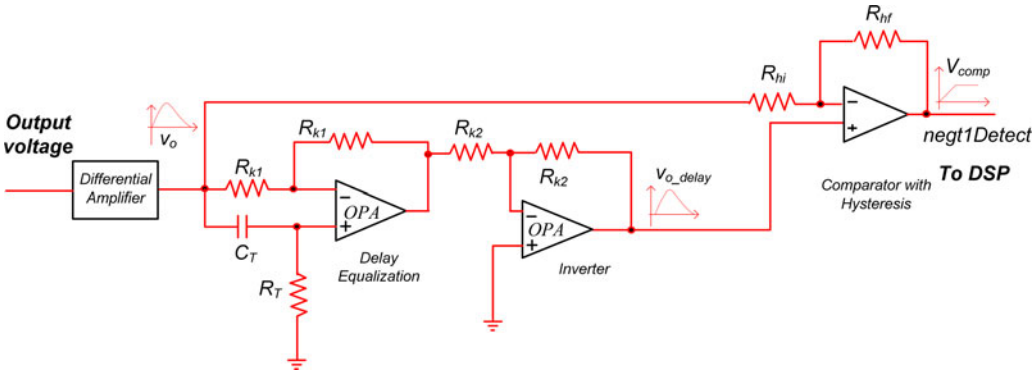

Fig. 8. Hardware implementation of the detector based on the adjustable delay circuit.

In this circuit, the delay time constant τ can be adjusted by the product of R_T and C_T (i.e., $\tau = 2R_T \cdot C_T$). And the inserted delay time $t_{\rm delay}$ can be compensated to a certain acceptable degree, with the help of the lead time (provided by ESR and equals ESR$*C_o$ [4]) and comparator hysteresis configuration (which can adjust the $v_{\rm err}$ band in Fig. 7).Therefore, the output comparator is connected with a hysteresis configuration and the one with latched output function is more preferred for blanking steady-state comparison "noise," such as TL3016 (TI Company) [25]. For example, for unloading transient case shown in Fig. 7, R_T and C_T can be chosen to be 500 Ω and 330 pF, so that a delay time $\tau = 330$ ns can be implemented. According to the parabolic function derived in (7), the voltage difference $V_{\rm err}$ in Fig. 7 can be estimated in this design, which is about 2 mV. Once the power stage and $t_{\rm delay}$ are decided, this voltage difference $V_{\rm err}$ will become a constant, which is independent on the load step value ΔI_o. The hysteresis can be adjusted to the same voltage as $V_{\rm err}$ by choosing for example $R_{hf} = 500$ kΩ and $R_{hi} = 1$ kΩ, so that the inserted delay time τ can be compensated. On the contrary, if ADC is used to implement the same functionality, a 10-bit asynchronous ADC with 2-mV resolution or a high-speed 3.3-MHz synchronous ADC is required, resulting in higher cost and power consumption.

B. Load Transient t_0 Detector, t_2 Detector, and t_3 Detector

As illustrated in Fig. 6, the output of the voltage error sensor is also fed into a transimpedance amplifier configuration. The transimpedance amplifier is used to asynchronously detect load transients. The transimpedance amplifier and threshold levels can be designed similar to [18]; however, since the output is not used to determine the capacitor zero crossover point t_1, it is not necessary to precisely match the C_o and ESR time constant of the output capacitor. In addition, a capacitor $C_{f\_\rm trans}$ can be added in parallel with the feedback resistor to attenuate high-frequency noise.

Based on the low-cost MCU TMS320F28027 [26], the calculated digital value $V_{\rm sw}$ in (18) and (23) is converted to analog signal by using a high-resolution PWM (HRPWM) [29] port as a DAC [28]. The HRPWM frequency is set to be 7.5 MHz and the equivalent PWM resolution is 9 bit [26]. A second-order low-pass filter with crossover frequency at around 750 kHz is used to smooth the HRPWM signal. The integrated comparator COMP1 will compare $V_{\rm sw\_DA}$ (COMP1B) with the amplified output voltage $V_{\rm err\_AD}$ (COMP1A) to determine time instant t_2 and the buck converter switches will change the ON/OFF state.

The time instant t_3 when the output voltage recovers to $V_{\rm ref}$ will be detected by using another integrated comparator COMP2 in the MCU. The voltage reference $V_{\rm ref}$ [0.9] from an internal 10-bit DAC [30] is fed to COMP2B. The output voltage (COMP2A) compares with the 10-bit DAC reference (COMP2B). When COMP2 outputs falling edge, CBC is achieved at t_3 and the PID controller will take over the output voltage regulation.

Another available method used extensively in previous work such as [5] and [10] to detect t_2 and t_3 is sampling the output voltage continuously at high frequency. The sampled voltage will be compared with $V_{\rm sw}$ and $V_{\rm ref}$ digitally. However, a significant advantage of applying analog comparison in this paper is to avoid the requirement of fast ADC sampling.

C. Signal Conditioning Circuitry Design Guidelines

A dual-channel ADC in MCU is employed to sample output voltage error $v_{\rm err\_AD}$ and the inductor current $i_{L\_\rm AD}$. The inductor current measurement information is only used to implement the extension for AVP technique [4].

The output voltage error $v_{\rm err\_AD}$ is calculated in the analog domain through use of the OPAMP configuration illustrated in Fig. 6. As will be discussed, the output of the voltage error sensor is used for steady-state operation and transient detection during a load transient. The output of the voltage error sensor is calculated as follows:

$$v_{\rm err_{AD}} = R_{f\_\rm err} \cdot \left(\frac{v_o}{R_{1\_\rm AD}} + \frac{V_{\rm AD\_ref}}{R_{\rm AD\_ref}} - \frac{V_{\rm ref}}{R_{V_{\rm ref}}} \right). \quad (37)$$

$V_{\rm AD\_ref}$ represents the upper bound of the ADC conversion range. $R_{f\_\rm err}/R_{1\_\rm AD}$ and $R_{f\_\rm err}/R_{V\_\rm ref}$ should be equal and selected based on the desired gain of $v_{\rm err\_AD}$. To level-shift the error voltage to the centre of the ADC conversion range, $R_{f\_\rm err}/R_{AD\_\rm ref} = 1/2$. $R_{2\_\rm AD}$ should be selected based on the following equation:

$$R_{2\_\rm AD} = \frac{R_{f\_\rm err}}{1 + \frac{R_{f\_\rm err}}{R_{V\_\rm ref}} - \frac{R_{f\_\rm err}}{R_{\rm AD\_ref}}}. \quad (38)$$

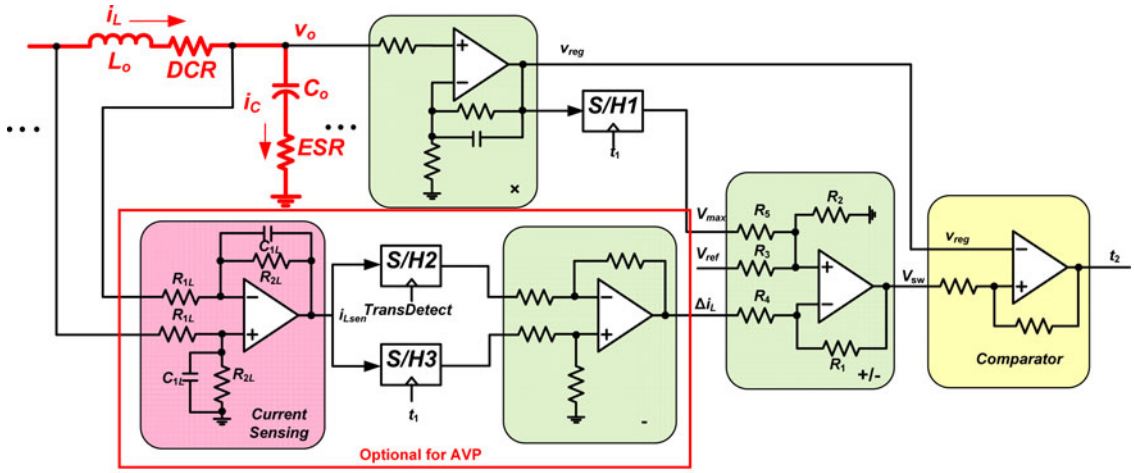

Fig. 9. Simplified schematic of the proposed analog CBC controller implementation for computing $V_{\rm sw}$ and detecting t_2 for unloading transient.

D. AVP Implementation

As shown in Fig. 6, the inductor current is reconstructed by matching the corner frequency of the low-pass filter with that of the inductor based on the following equation to filter the voltage across the output inductor:

$$R_{2_{iL\,\rm sens}} \cdot C_{iL\rm sens} = \frac{L_o}{R_L}. \tag{39}$$

The output of the inductor current sensor $i_{L\_\rm AD}$, in relation to the inductor current i_L, is given as

$$i_{L_{\rm AD}} = R_L \cdot \frac{R_{2\_iL\rm sens}}{R_{1\_iL\rm sens}} \cdot i_L. \tag{40}$$

Therefore, the selection of $R_{2\_iL\rm sens}/R_{1\_iL\rm sens}$ should be based on the maximum expected inductor current and the conversion range of the ADC. In order to achieve AVP, Δi_L information is required. So the inductor current i_L is sampled at t_0 and t_1, respectively, and the difference Δi_L is calculated as $i_L(t_1) - i_L(t_0)$ using MCU.

So by using the digital implementation with the extreme voltage detector, the third drawback in Section I is solved without relying on fast ADC sampling. No accurate current sensing is needed in the non-AVP application and this implementation also shows a simple extension to AVP application. Therefore, the fourth and fifth drawbacks are overcome.

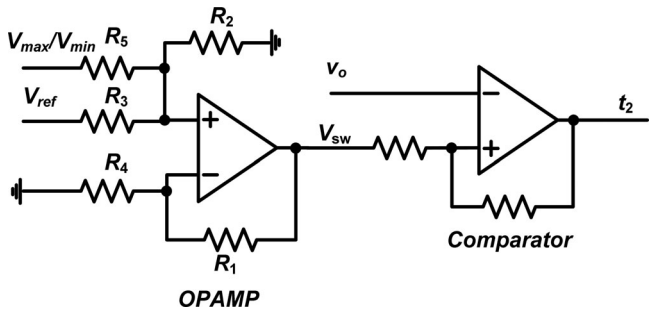

Fig. 10. Analog implementation for calculating $V_{\rm sw}$ and t_2 determination.

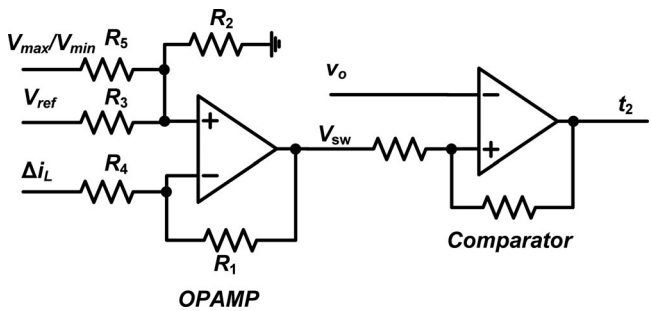

Fig. 11. Analog implementation modification for calculating $V_{\rm sw}$ and t_2 determination in AVP applications.

VI. Analog Implementation of the Proposed V-CBC Algorithm

The implementation and design of the proposed analog charge balance controller will be discussed in this section. The three main components of the proposed analog charge balance controller are: 1) an extreme voltage detector to determine t_1 (when the inductor current reaches the new load current level); 2) an analog circuitry consisting of OPAMP and comparator to determine the switching instant t_2; and 3) associated logic to control the components 1 and 2 and the converter's PWM signal. Fig. 9 shows the block diagram of the CBC method.

The detection of t_1 is very similar to digital implementation, except that the output signal of the extreme voltage detector (shown in Fig. 8) will be used to sample/hold the $V_{\rm max}/V_{\rm min}$ by using S/H1(shown in Fig. 9). In this analog implementation, the critical time point t_2 can be determined by comparing instant output voltage v_o with SPV $V_{\rm sw}$.

To implement AVP, the inductor current sensor is required and the load step value Δi_L can be generated by using two S/Hs (S/H2 and S/H3). The S/H timing is controlled by the controller logic according to t_0 (from transient detector) and t_1 (from extreme voltage detector output) in Fig. 9. Then, Δi_L is obtained by subtracting $i_L(t_0)$ from $i_L(t_1)$ using OPAMP-based circuitry. More detailed design information will be provided in this section.

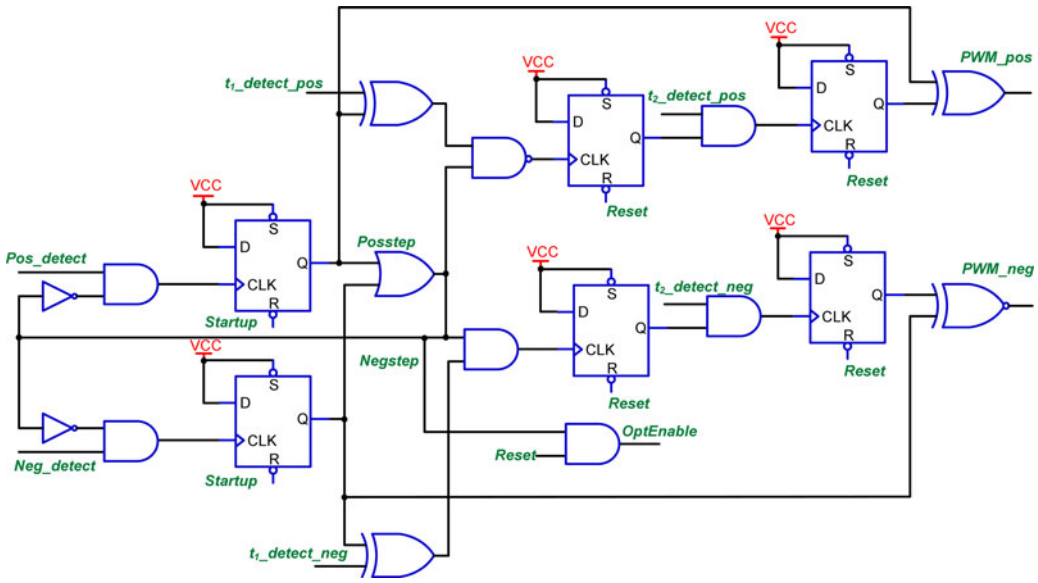

Fig. 12. Simplified schematic of the proposed AV-CBC controller logic circuit.

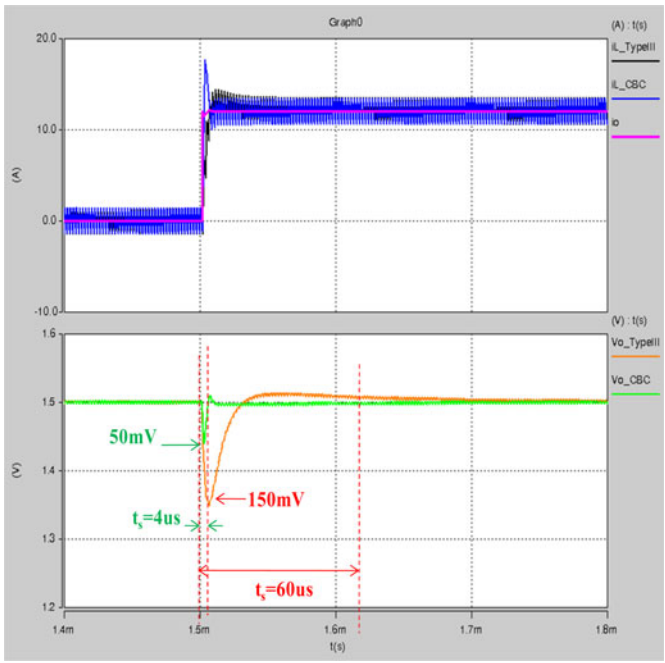

Fig. 13. Simulation results under 0 A → 12 A positive load transient.

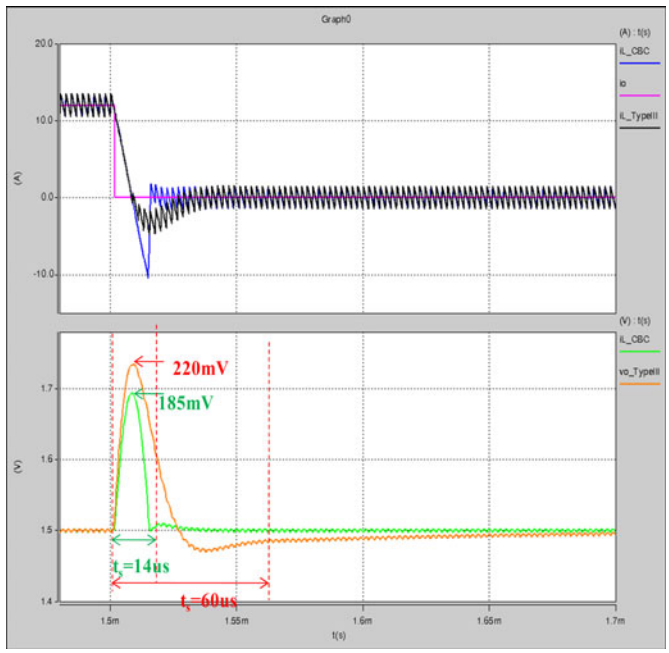

Fig. 14. Simulation results under 12 A → 0 A negative load transient.

A. Analog Circuitry Design for t_2 Detection

The design of the analog circuitry for t_2 detection in unloading transient is presented as an example in this section and the hardware schematic is shown in Fig. 10, for non-AVP application. And for AVP operation, the inverting port of the OPAMP will be tied to Δi_L in Fig. 11.

It is noted that OPAMP and comparator circuit can be used to implement (18) and determine t_2. The OPAMP serves as an amplifier with constant gain for $V_{\max}$ and V_{ref} and an adder to sum up the information at the noninverting port.

And the hardware modification for AVP operation is also minor, shown in Fig. 11, the inductor current sensor is required to feed the load-line information to the inverting port of the OPAMP to implement (27) and (35).

To implement (27) and (35), an analog OPAMP adder/subtractor is employed following the formula in (41). And the design parameters can be selected using (42)–(44), referring

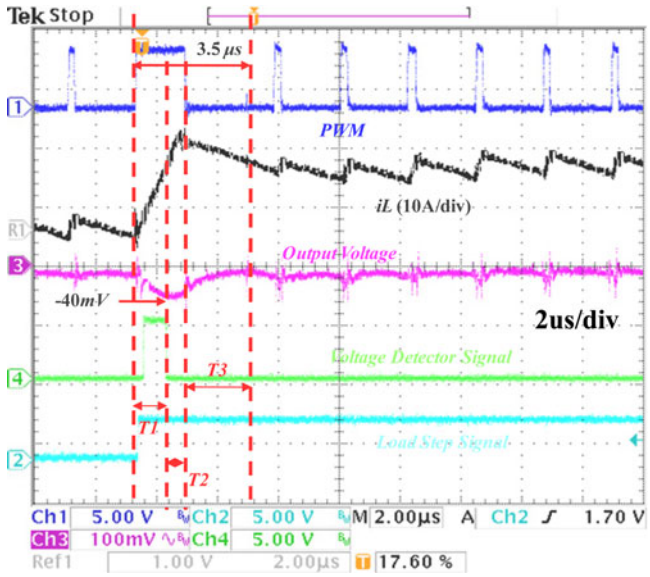

Fig. 15. Experimental results (0 → 12 A positive load transients) using proposed AV-CBC controller (2 μs/div).

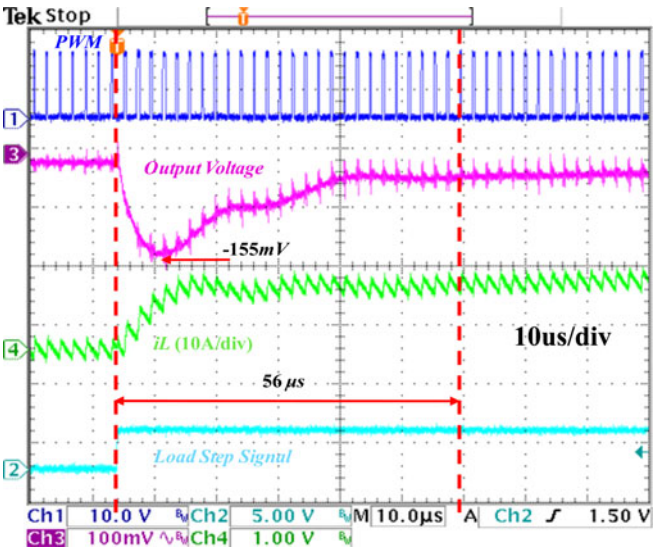

Fig. 16. Experimental results (0 → 12 A positive load transients) using Type III compensator (10 μs/div).

to (27) and (41):

$$V_{\rm SW} = \left(1+\frac{R_1}{R_4}\right)\left(\frac{R_2}{R_5+R_2}V_{\max} + \frac{R_2}{R_3+R_2}V_{\rm ref}\right) - \frac{R_1}{R_4}\cdot\Delta i_L \tag{41}$$

$$D = \left(1+\frac{R_1}{R_4}\right)\frac{R_2}{R_5+R_2} \tag{42}$$

$$1-D = \left(1+\frac{R_1}{R_4}\right)\frac{R_2}{R_3+R_2} \tag{43}$$

$$(1-D)\cdot R_{\rm droop} = \frac{R_1}{R_4}. \tag{44}$$

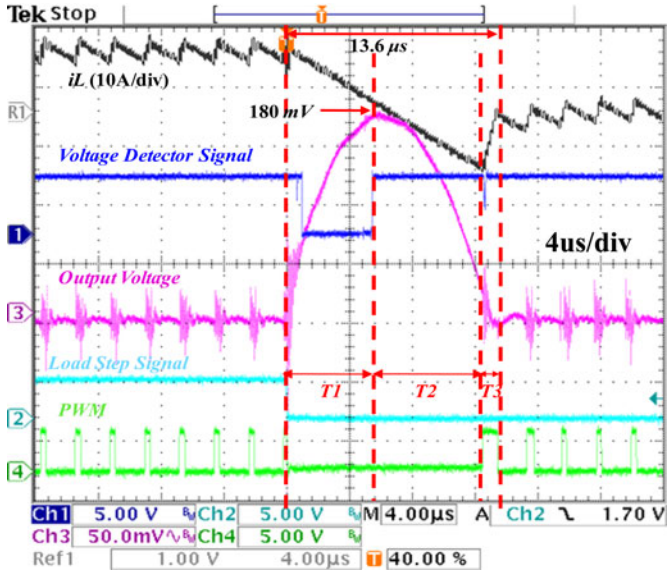

Fig. 17. Experimental results (12 → 0 A negative load transients) using proposed AV-CBC controller (4 μs/div).

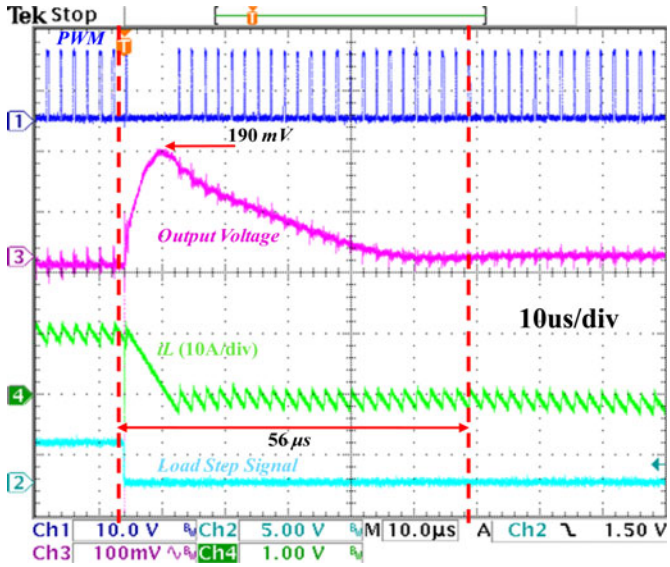

Fig. 18. Experimental results (12 → 0 A negative load transients) using Type III compensator (10 μs/div).

B. Logic Circuit for Balance Controller

The controller logic block is responsible for: 1) registering a load current transient, 2) switching control from the linear controller to the charge balance controller during the transient interval and providing PWM control signals, 3) providing control signals to the extreme voltage detector, linear-mode controller, and S/Hs during the transient interval, 4) registering time instants (at t_1 and t_2), and 5) reactivating the linear controller at the end of the transient interval (at t_3). The controller logic is shown in Fig. 12, and it can be easily integrated into an analog IC.

TABLE I
VOLTAGE VARIATION AND SETTLING TIME IN THE SIMULATION AND EXPERIMENT UNDER DIFFERENT CASES

Controller \ Case	0 A → 12 A (Simulation)	0 A → 12 A (Experiment)	12 A → 0 A (Simulation)	12 A → 0 A (Experiment)
AV-CBC	50mV/4us	40mV/3.5us	185mV/14us	180mV/13.6us
Type III	150mV/60us	155mV/56us	220mV/60us	190mV/56us

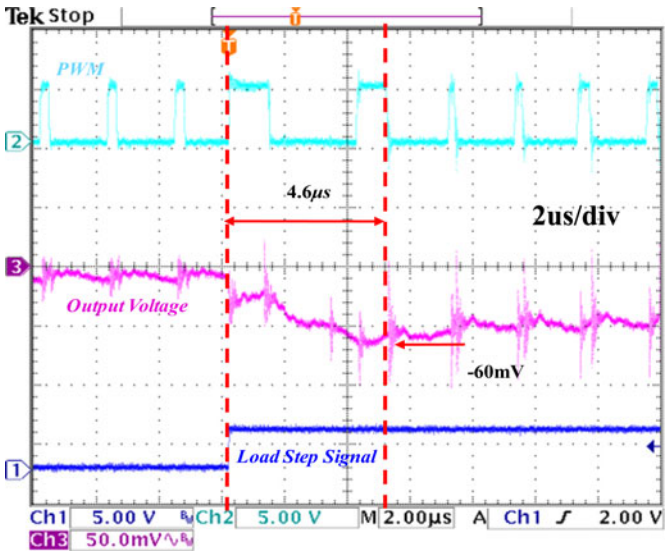

Fig. 19. Experimental result of positive 12-A load transients under AVP operation using proposed AV-CBC controller (2 μs/div).

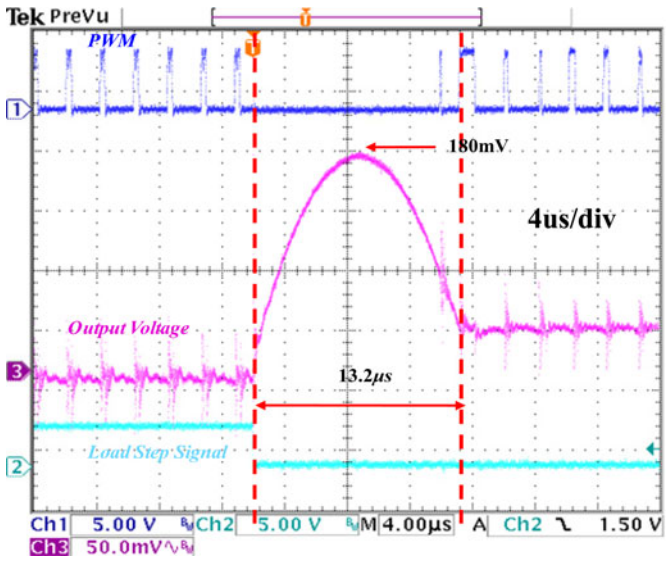

Fig. 20. Experimental result of negative 12-A load transients under AVP operation using proposed AV-CBC controller (4 μs/div).

The analog implementation overcomes the fourth and fifth drawbacks in Section I as the digital implementation and also demonstrates a good solution for the last drawback.

VII. SIMULATION AND EXPERIMENTAL VERIFICATIONS

Because of the very similar performance of the digital and analog implementations [3], [19] and limited space of this paper, only analog implementation verifications are provided through details.

A. Simulation Results

In order to verify the functionality of the proposed analog implementation of V-CBC (AV-CBC), a buck converter undergoing different transient conditions is simulated. And the simulation results are shown in Figs. 13 and 14 for comparison between the proposed AV-CBC controller and the conventional voltage-mode controller. The nominal design parameters are listed as follows: $V_{\rm in} = 12$ V, $V_o = V_{\rm ref} = 1.5$ V, $f_s = 450$ kHz, $L = 1$ μH, $R_L = 1$ mΩ, $C = 200$ μF, ESR $= 0.1$ mΩ, and ESL $=$ 100 pH. The Type III compensator is well designed with 75-kHz bandwidth and 60° phase margin in the following simulations. The simulator used in this section is Saber [31].

Under 12-A positive load step transient, compared to linear voltage-mode controller, the voltage overshoot is reduced by 66.7% and the settling time is shortened by 93.3%. Although, under the negative 12-A step load transients, the voltage undershoot is only reduced by 19.0% due to the narrow operating duty ratio and the settling time is still significantly reduced by about 76.7%.

B. Design Prototype and Experimental Results

A 12 V–1.5 V prototype is designed using the following parameters: $V_{\rm in} = 12$ V, $V_o = V_{\rm ref} = 1.5$ V, $f_s = 450$ kHz, $L = 1$ μH, $R_L = 1$ mΩ, $C = 200$ μF, ESR $= 0.1$ mΩ, and ESL $=$ 100 pH. An FPGA (EP2C70F896C6, Cyclone II, Altera) is employed to implement the proposed AV-CBC controller logic (in Fig. 12). The analog linear-mode controller is implemented by using ISL6559 controller (Intersil Co.) [32]. The extreme voltage detector delay is set to be 100 ns for loading transient and 330 ns for unloading transient. Accordingly, the voltage $V_{\rm err}$ is about 2 mV in both the cases. Experimental results are shown in Figs. 15–18, under the load current step changes between no load (0 A) and full load (12 A).

Figs. 15 and 16 show comparative results for a buck converter undergoing a 0 A → 12 A positive load step transient using proposed AV-CBC controller and using conventional voltage-mode controller. The voltage detector signal is shown for time detection of t_1. In order to illustrate the operation of the AV-CBC controller, the CBC intervals have been shown in the figures.

It is demonstrated that under a positive 12-A load current step transient, the settling time is reduced from 56 μs (using

TABLE II
ESTIMATED STEADY-STATE RIPPLE (PEAK TO PEAK) CONTENT/PERCENTAGE WITH DIFFERENT CONTROLLERS

Controller \ Case	0 A (Simulation)	0 A (Experiment)	12 A (Simulation)	12 A (Experiment)
AV-CBC	4mV/0.27%	~5mV/0.33%	4mV/0.27%	~7mV/0.47%
Type III	4mV/0.27%	~5mV/0.33%	4mV/0.27%	~7mV/0.47%

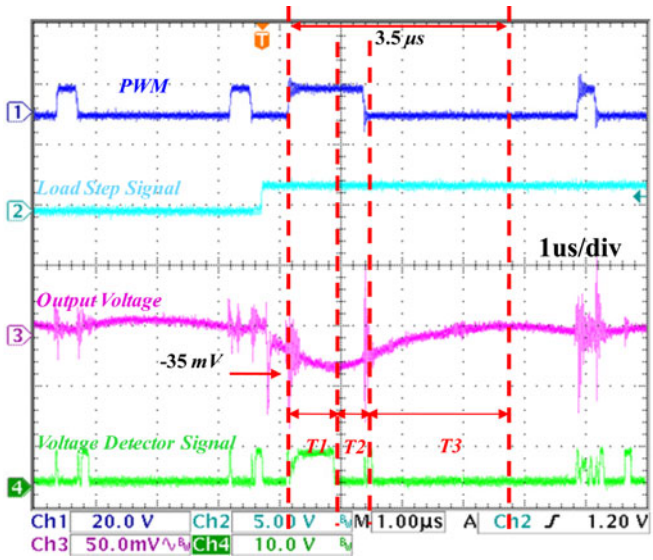

Fig. 21. Experimental results of the buck converter under loading step transient case 0–10 A using digital V-CBC controller (1 μs/div).

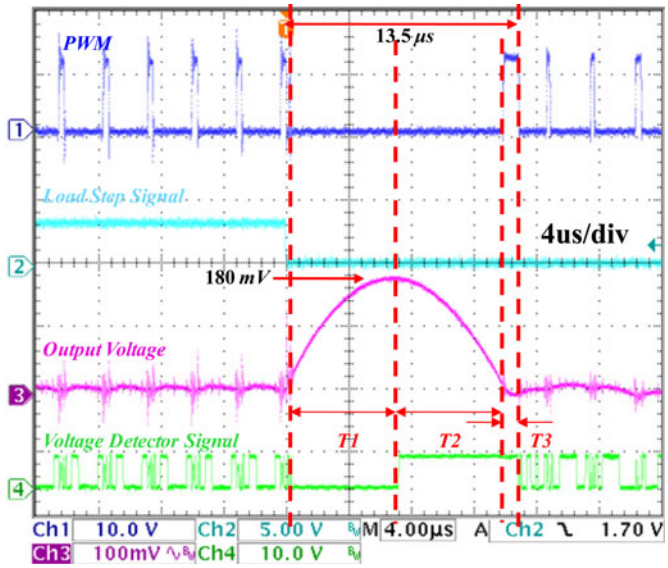

Fig. 22. Experimental results of the buck converter under unloading step transient case 10–0 A using digital V-CBC controller (4 μs/div).

linear voltage-mode controller) to 3.5 μs (using AV-CBC). In other words, the settling time of the buck converter with AV-CBC is shorten by 93%, compared to that of the voltage-mode-controlled buck converter. And the experimental result is in close correspondence of the simulation result (4 μs).

Also, it is shown that voltage undershoot is reduced from 155 mV (using the linear controller) to 40 mV (using AV-CBC). The undershoot of the buck converter with AV-CBC controller is reduced by 74% compared to that of the voltage-mode controller buck converter. And the 40-mV undershoot is closed to the simulated result (50 mV) and the difference is caused by the different loading step instants.

Figs. 17 and 18 show a voltage-mode-controlled buck converter and the AV-CBC controlled buck converter undergoing a 12 A $\rightarrow$ 0 A load step change, separately.

It is demonstrated, under a 12-A load negative current step transient, the settling time is reduced from 56 μs (using linear voltage-mode controller) to 13.6 μs (using AV-CBC). In other words, the settling time of the buck converter with AV-CBC is shorten by 75%, compared to that of the voltage-mode-controlled buck converter. And the experimental result is in close correspondence of the simulation result (14 μs).

Also, it is shown that voltage overshoot is only reduced from 190 mV (using the linear controller) to 180 mV (using AV-CBC) based of the narrow operating output ratio at 12–1.5 V. But the 180-mV overshoot is closed to the simulated result (185 mV). The voltage variation and settling time in simulation and experiment are summarized in Table I.

The AVP technique is applied to the AV-CBC controller with simple modification on top of the non-AVP AV-CBC scheme. And in the experimental results shown in Figs. 19 and 20, the droop resistance is selected to be 5 mΩ.

It is demonstrated that, for a 12-A positive load step transient, the undershoot is 0 mV at –60-mV AVP regulation in Fig. 19. And the settling time is 4.6 μs. The experimental result in Fig. 20 demonstrates that the overshoot is 120 mV above the AVP regulation level of 60 mV (180 mV in total) with 13.2-μs settling time under a 12-A negative step load transient.

In Table II, steady-state ripple content is compared between the proposed AV-CBC and Type III compensator. Under steady state, the same linear Type III controller is applied to AV-CBC. Based on the same power stage design parameters (output inductance and capacitance), the output voltage ripple will be equal in both of the cases in steady state.

Digital implementation results of proposed algorithm shown in Figs. 21 and 22 are also provided to demonstrate similar results to the AV-CBC [4]. Under 10-A loading transient, the voltage undershoot is about 35 mV and settling time is about 3.5 μs. While, under 10-A unloading transient, the voltage overshoot is about 180 mV and settling time is about 13.5 μs.

VIII. Conclusion

In this paper, a voltage-based CBC algorithm based on simplified differential equations is proposed to optimize the response of buck converters. A new derivation method of practical CBC algorithm is presented for both the input and load transients. An extreme voltage detector (based on delay equalization) is employed to detect the critical time instant t_1, when output voltage peak/valley appears. SPV concept is applied to determine the time instant to switch over the ON/OFF state of the MOSFET in the buck converter. Simulation model and hardware prototype of a synchronous 12–1.5 V buck converter have been made. It is demonstrated through simulations and experimental results that the proposed V-CBC algorithm can be implemented using both low-cost MCU and analog devices to optimize the transient response performance. Through the comparison experiments of AV-CBC, under the load transient cases, for loading step, the voltage undershoot is suppressed by 74% and settling time is improved by 93%, while, for unloading step, the converter overshoot is reduced by 5% and settling time is shortened by 75%. Also, the AVP extension of the proposed algorithm is demonstrated.

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