A New Digital Control Algorithm for Dual-Transistor Forward Converter

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***Abstract*—In this paper, a new digital control algorithm is presented to improve the dynamic performance of the dual-transistor forward converter (DTFC) during a transient event. The algorithm uses a linear control scheme under the stable-state condition and the charge balance control scheme under the transient condition. Based on the principle of capacitor charge balance, the proposed algorithm predicts the switch over time to achieve optimal transient response for a DTFC, thus the minimal voltage derivation and recovery time are achieved when the load current has a step change. Compared with a conventional voltage mode controller, the proposed algorithm provides a much better dynamic performance. Furthermore, simulation and experiment results demonstrate the effectiveness of the algorithm.**

***Index Terms*—Dc-dc power conversion, digital control, predictive control, transient response.**

I. Introduction

THE forward converter technology has been widely used for low-voltage and high-current applications with a power level up to 250 W [1]–[4]. Considerable research has been proposed to enhance efficiency of the forward converter at high switching frequencies. However, the forward converter suffers from high voltage stress, which limits its use in conventional application. Half-bridge or full-bridge dc-dc converters are introduced to solve the problem [5]–[8], but these topologies have a well known risk of direct break-through failures, as the devices are directly connected across the power source. Dual-transistor forward converter (DTFC) is more reliable, and thus attracts a lot of research attention [9]–[11]. In [10], a zero-voltage transition (ZVT) technique has been presented for DTFC. In [11], The Input-series and output-parallel (ISOP) connected DTFC for high voltage input and high current output applications is investigated.

While many papers have been reported on the soft-switching techniques of the DTFC, few works has been done on the dynamic performance improvement of the forward converter. In fact, there is an increasing requirement for better dynamic performance of the DTFC, such as small output voltage overshoot and the recovery time, etc. Some work has been done to improve transient response of other topologies. In [12], the theory of fuzzy logic control and state observer is applied to the current feedback control of a boost converter. In [13], Proportional-integral (PI) and sliding mode controls are combined to regulate a fourth-order Cuk converter under large signal variations. In [14], a sliding mode input-output linearization controller is presented to improve the transient response and disturbance rejection of the zero-voltage switching (ZVS) CLL-T resonant converter. In [15], the window transient enhancement (WTE) and overshoot suppression (OSS) technique are presented for a current mode boost converter. However, these methods cannot provide the minimum voltage overshoot/undershoot and recovery time. In [16], by using the principle of capacitor charge balance control (CBC) during a transient event, a digital controller predicts the optimal recovery time for a buck converter. But it requires a sampling delay and a complex mathematical computation. In [17] a novel analog CBC controller is proposed with a low-cost control scheme. Compared to the digital control scheme in [16], the sampling delay is removed. Based on the principle of CBC, Couples of analog controllers and digital control algorithms have been reported to improve the dynamic response of other power converters (such as the Boost converter, the Buck-Boost converter) [18]–[20]. In [21]–[24], other digital optimal schemes are discussed for dc-dc converters, however, these controllers suffer at least one of the following draw backs: 1) complex mathematical functions; 2) slow reaction to load change, moreover, these controllers are unsuitable for DTFC because that the maximum duty cycle in DTFC is limited by 50%.

In this paper, a new digital control algorithm is discussed for DTFC to enhance the dynamic performance during a transient condition. The optimal switching time is predicted by using the principle of the CBC. Considering the maximum duty cycle is limited, an approximate calculation is introduced in the proposed algorithm, which can be extended to other isolation converters.

The paper is organized as follows. In Section II, the outline of the algorithm operation is presented in order to analyze the dynamic response of DTFC. In Section III, the mathematical analysis is investigated, which is expressed by a simple approximation calculation and some key equations. The implementation of the proposed digital controller is explained in Section IV. Simulation and experimental results are presented in Section V. Section VI is the conclusion.

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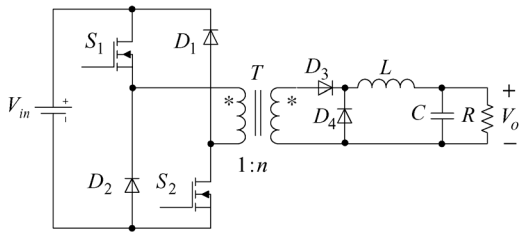


Fig. 1. Dual transistor forward converter (DTFC).

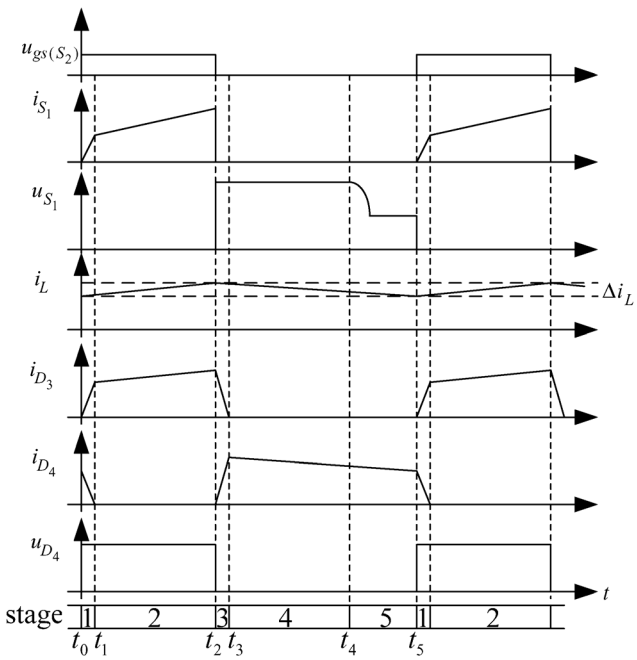


Fig. 2. Main waveforms of dual-transistor forward converter.

II. Outline of the Algorithm Operation

A. The Operation of the DTFC

The Dual-transistor forward converter (DTFC), as shown in Fig. 1, consists of switches S_1, S_2, diodes D_1, D_2, the transformer T, the rectifier diode D_3, the free wheeling diode D_4 and the output filter circuit.

There are 5 operation stages for the DTFC, and the main theoretical waveforms are illustrated in Fig. 2.

Stage 1 $(t_0 \sim t_1)$*:* Before time t_0, the transformer T has been reset, while the free wheeling diode D_4 conducts the load current. At time t_0, switches S_1 and S_2 turn on simultaneously, the load current is commutated from the free wheeling diode D_4 to the rectifier diode D_3.

Stage 2 $(t_1 \sim t_2)$*:* At time t_1, the commutation between D_3 and D_4 is completed. During this stage, the current in S_1 and S_2 increases linearly, the power is transferred from the input source to the load.

Stage 3 $(t_2 \sim t_3)$*:* At time t_2, switches S_1 and S_2 turn off simultaneously, while the clamp diode D_3 and D_4 turn on. As a result, the transformer T is being reset, the voltage on switches S_1 and S_2 are equal to $V_{\rm in}$. The diode D_3 is inverse biased and the load current is commutated from D_3 to D_4 before time t_3.

Stage 4 $(t_3 \sim t_4)$*:* In this stage, the transformer T is still being reset, the load current flows through the free wheeling diode D_4.

Stage 5 $(t_4 \sim t_5)$*:* During this stage, the transformer T is completely reset and diodes D_1 and D_2 stop conducting. The voltage on switches S_1 and S_2 decrease to $V_{\rm in}/2$.

The operation of the next cycle is identical with the five stages operation described above.

During the transformer reset operation over $(1 - {\rm D})T_{\rm s}$, the voltage applied to the primary-side of the transformer is $-V_{\rm in}$. This fact imposes the restriction, where the maximum duty ratio of the DTFC is limited to 50%, to avoid the saturation of the magnetic core in the transformer.

B. The Principle of the Charge Balance Control

Before the introduction of the principle of the CBC, some assumptions should be considered:

1) the ESR and ESL can be neglected;
2) the value of the inductor and capacitor keeps constant;
3) the input voltage keeps unchanged during the transient;

The principle of capacitor charge balance, which is widely used in steady-state modeling and analysis of dc-dc converters, means the average value of the capacitor current over one duty cycle must be equal to zero.

$$v_c(t_{k+1}) - v_c(t_k) = \frac{i_{c\_avg}}{C} = 0 \rightarrow \frac{\int_{t_k}^{t_{k+1}} i_c(t)dt}{t_{k+1} - t_k} = \frac{\int_{t_k}^{t_{k+1}} i_c(t)dt}{T_s} = 0 \tag{1}$$

In (1), v_c represents the voltage of the output capacitor, t_k and t_{k+1} respent the beginning of the switching cycle kT_s and $(k+1)T_s$, i_{c_avg} is the output capacitor current over one switching period during the steady-state. C is the value of the output capacitor and T_s is the switching period of the DTFC.

It should be noted that the (1) can be extended over the transient time of the DTFC by the following equation:

$$v_c(t_b) - v_c(t_a) = \frac{i_{cavg}}{C} = 0 \rightarrow \frac{\int_{t_a}^{t_b} i_c(t)dt}{t_b - t_a} = 0 \tag{2}$$

Where t_a represents the beginning time of the transient period, and t_b represents the end time of the transient period. If (2) is satisfied, that means the output voltage returns to the reference voltage after a transient period, furthermore, if the inductor current i_L equals to the new load current at time t_b, the DTFC has recovered from a transient event. Thus this concept can be used to minimize the voltage deviation and predict the optimal recovery time.

C. The Key Steps of the Proposed Algorithm

The optimal curves of the inductor current and output voltage under a positive load current change are depicted in Fig. 3. In the beginning of the transient, the capacitor has to discharge because the inductor current cannot change instantaneously. A portion of the load current is supplied by the capacitor, which causes the output voltage to decrease from the reference voltage.

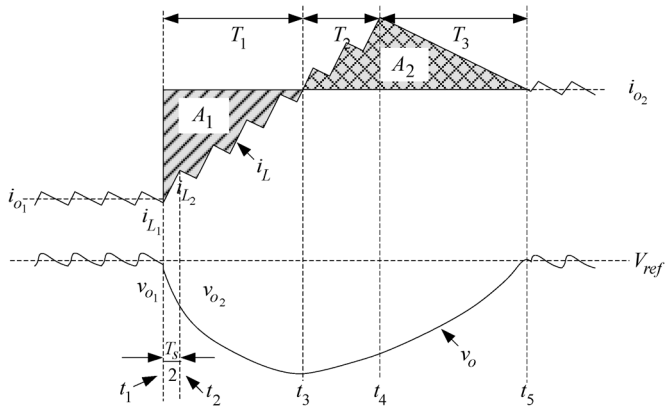


Fig. 3. Optimal dynamic response of a DTFC under a load current positive step.

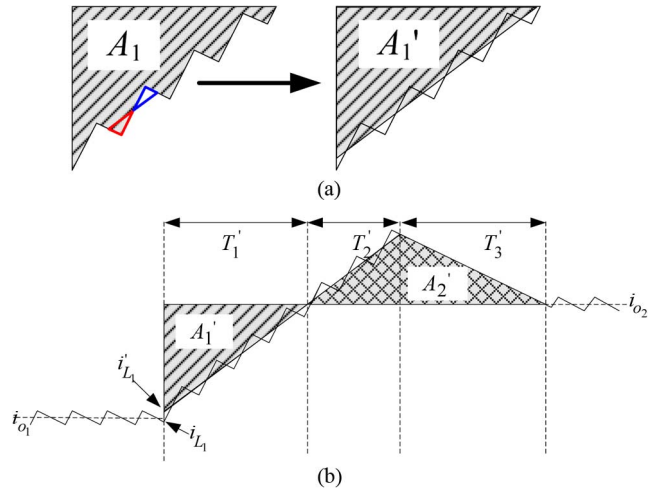


Fig. 4. Approximate calculation of A1, A2 for a positive load step. (a) Example of approximate calculation. (b) Modified portion of discharge/recharge.

As the duty cycle is set to maximum value (50%), the inductor current rises quickly. Once i_L exceeds the new load current (at t_3), the capacitor starts to recharge and the output voltage increases. The duty cycle keeps 50% until the inductor current reaches the peak value (at t_4). During T_3, the duty cycle will be set to 0% which drives i_L to drop with its maximum slew rate. The DTFC will recover from a positive load step fully (at t_5) when both of i_L and v_o reach their new steady-state value. After t_5, linear control loop takes over.

Thus, the key steps of the proposed algorithm can be listed as following:

1) detect a load current change(positive/negative step change) immediately;
2) change to the optimal control scheme and set the duty cycle to maximum value 50% (a positive step change) or minimum value 0% (a negative step change), which drives i_L rise/fall at its maximum slew rate;
3) after i_L reach its peak point t_4 (calculated by principle of capacitor charge balance), set the duty cycle to 0% (a positive step change) or 50% (a negative step change);
4) return to the linear control scheme when the transient ends at t_5;

From the Fig. 3, it is clearly that the whole transient period can be divided into two parts: the duty cycle keeps maximum (50%) before t_4 and the duty cycle varies to 0% until t_5. In other words, the two parts determine the discharge portion (A_1) and the recharge portion (A_2). Thus, the key point of the proposed algorithm is to calculate T_2 (determined by t_4) and T_3 (determined by t_5) accurately such that the charge of the capacitor keeps balance at the end of a transient period.

III. Mathematical Analysis of the Proposed Algorithm

A. The Method of the Approximate Calculation

Based on the analysis presented in Section II, the discharge portion (A_1) and the recharge portion (A_2) should be obtained firstly, however, as shown in Fig. 3, A_1 and A_2 are irregular graphics which are difficult to calculate. A simple and effective method (shown in Fig. 4) is introduced to solve this problem:

Using the principle that the area of a triangle (marked with red line in Fig. 4(a) is equal to that of its vertical angle triangle (marked with blue line in Fig. 4(a)), the irregular portions can be rearranged into triangles (Fig. 4(b)), which are very easy to calculate.

B. The Equation for the DTFC Undergoing a Positive Load Step Change

The mathematical analysis for the DTFC undergoing a positive load step change can be described briefly as:

1) detect the load change and estimate the new load current
Once the output voltage exceeds a predefined threshold, the optimal control scheme is activated. By sensing the inductor current i_{L_1}, i_{L_2} and output voltage v_{o_1}, v_{o_2} at t_1 and t_2 (Fig. 3), the new load current i_{o_2} can be estimated as:

$$i_{o_2} = \frac{1}{2}\left(i_{L_1} + i_{L_2}\right) - 2\frac{C}{T_s}\left(v_{o_2} - v_{o_1}\right) \tag{3}$$

2) calculate the capacitor discharge portion A_1'
As shown in the Fig. 4(b), the rising and falling slew rate of the inductor current should be modified as:

$$\left.\frac{di_L}{dt}\right|_{\text{rising}} = \frac{nv_{in} - 2v_o}{2L} = m_1 \quad \left.\frac{di_L}{dt}\right|_{\text{falling}} = -\frac{v_o}{L} = -m_2 \tag{4}$$

Where v_{in}, v_o are the input and output voltage, n represents the turns ratio of the transform.
Based on the new load current i_{o_2} and the m_1 in (4), T_1' and A_1' are obtained in (5):

$$T_1' = \frac{i_{o_2} - i_{L_1}'}{m_1}, \qquad A_1' = \frac{1}{2}T_1'\left(i_{o_2} - i_{L_1}'\right) \tag{5}$$

In (5), i_{L_1}' is the modified inductor current in Fig. 4(b), which is calculated as:

$$i_{L_1}' = i_{L_1} + \frac{nv_{in}}{L}\frac{T_s}{8} \tag{6}$$

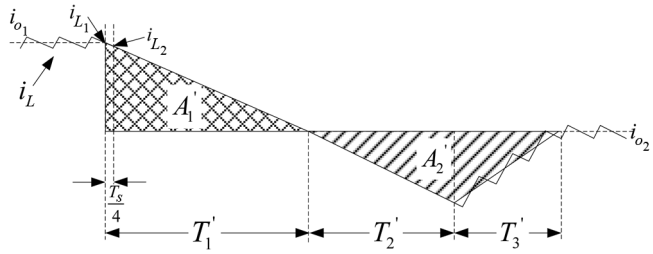


Fig. 5. Approximate calculation of A1, A2 for a negative load step.

3) calculate the capacitor charge portion A_2'
In order to keep the charge balance of the capacitor at the end of a transient event, $A_1' = A_2'$ must be satisfied, where the capacitor charge portion A_2' can be rewritten as:

$$A_2' = \frac{1}{2}(T_2' + T_3')(i_{L_3} - i_{o_2}), \quad i_{L_3} = i_{o_2} + m_2 T_3' = i_{o_2} + m_1 T_2' \tag{7}$$

The ratio of the T_2'/T_3' can be derive from (7):

$$\frac{T_2'}{T_3'} = \frac{m_2}{m_1} \tag{8}$$

Thus, by using (5), (7), (8), the optimal transient time T_2', T_3' can be given by (9):

$$T_2' = \sqrt{\frac{A_1'}{K}}, \quad K = \frac{m_1(m_2 + m_1)}{2m_2}, \quad T_3' = \frac{m_1}{m_2} T_2' \tag{9}$$

4) calculate T_2 and T_3
Compared the Fig. 3 with the Fig. 4(b), it is observed that T_2 and T_3 can be derived in (10):

$$T_2 = T_2' - T_s/4, \quad T_3 = T_3' + T_s/4 \tag{10}$$

C. The Equation for the DTFC Undergoing a Negative Load Step Change

A similar analysis can be carried for a negative load step change based on Fig. 5.

Firstly, the new load current is estimated as:

$$i_{o2} = \frac{1}{2}(i_{L_1} + i_{L_2}) - C(v_{o_2} - v_{o1})\frac{4}{T_S} \tag{11}$$

Secondly, the charge portion A_1' can be calculated:

$$T_1' = \frac{i_{L_1} - i_{o_2}}{m_2}, \qquad A_1' = \frac{1}{2} T_1' (i_{L_1} - i_{o_2}) \tag{12}$$

the discharge portion A_2' is:

$$A_2' = \frac{1}{2}(T_2' + T_3')(i_{o_2} - i_{L_3}), \quad i_{L_3} = i_{o_2} - m_2 T_3' = i_{o_2} - m_1 T_2' \tag{13}$$

Similarly, by using (8), (12), (13), and considering the condition $A_1' = A_2'$, the optimal transient time T_2', T_3' can be given by:

$$T_2' = \sqrt{\frac{A_1'}{K}}, \quad K = \frac{m_2(m_1 + m_2)}{2m_1}, \quad T_3' = \frac{m_2}{m_1} T_2' \tag{14}$$

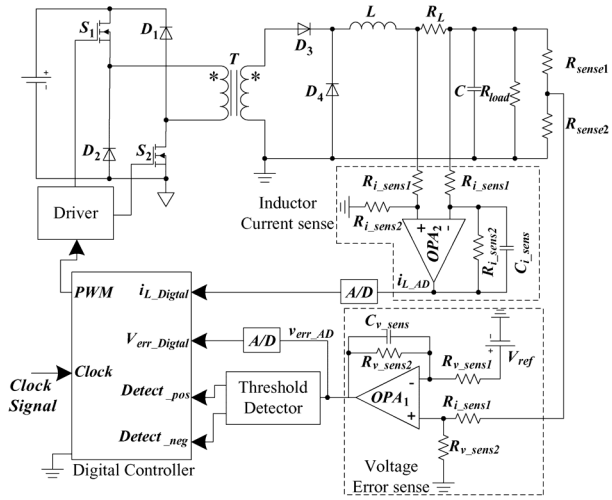


Fig. 6. Experimental block diagram of a DTFC with the proposed algorithm.

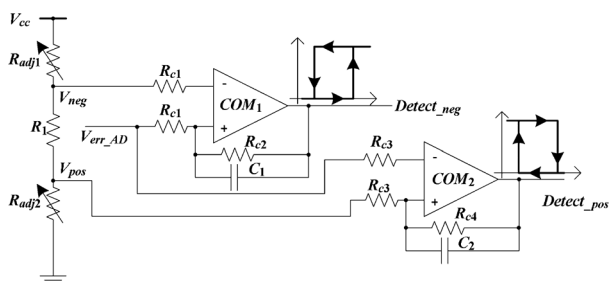


Fig. 7. Implementation of the load change detector.

Thus, the transient time can be obtained:

$$T_2 = T_2' + T_s/4, \quad T_3 = T_3' - T_s/4 \tag{15}$$

The main differences between positive and negative steps when applying the proposed scheme, is the change of the duty cycle during the transient period. If there is a positive step change, the duty cycle operated with the maximum value 50% (during time period $T_1 + T_2$) and the minimum value 0% (during time period T_3), while under an negative step change, the duty cycle is set as the minimum value 0% (during time period $T_1 + T_2$) and the maximum value 50% (during time period T_3).

IV. The Implementation of the Proposed Digital Control System

The hardware implementation diagram of the proposed charge balance control algorithms is shown in Fig. 6.

A. The Threshold Detector Design

Because it is critical for the load estimation in the proposed algorithm, a practical threshold detector is used in this paper to detect the load current change.

In Fig. 7, two ultrafast comparator (TL 3016) are constructed, the amplified voltage V_{err_AD}, which is derived from the voltage error sense Block, and the threshold voltage V_{neg} and V_{pos} will be fed to the comparators. In this way, as soon as the error voltage reached the threshold voltage (set by the hysteresis of the comparator), the comparator will be trigged,

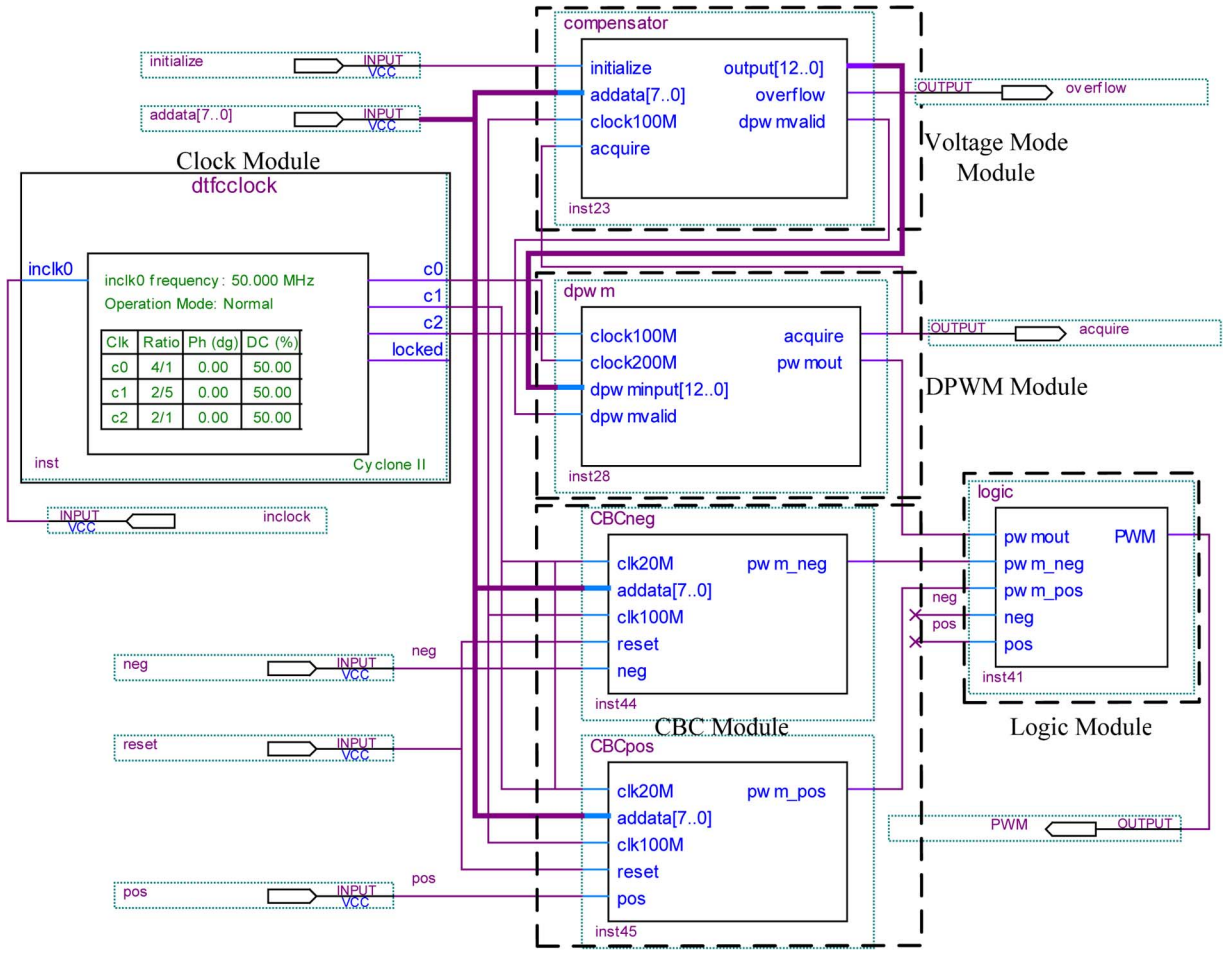


Fig. 8. Block diagram implementation of the proposed algorithms in FPGA.

the output will jump from low to high. Thus, the rising edges can be used to activate the optimal control scheme.

B. The Digital Controller Based on FPGA

As shown in Fig. 8, the proposed algorithm is programmed by Block diagram method in FPGA [25], [26], with the logic elements (543), registers (310) and memory bits (118,856).

In Fig. 8, the Clock Module products the clock signals, which is used in other Modules and A/D sample. The Voltage Mode Module provides a digital PID controller, with the following equation:

$$d(k) = d(k-1) + Ae(k) + Be(k-1) + Ce(k-2) \quad (16)$$

Where the coefficients are given as:

$$A = K_p + \frac{T}{\tau_i} + \frac{\tau_d}{T}, \quad B = -K_p - \frac{2\tau_d}{T}, \quad C = \frac{\tau_d}{T} \quad (17)$$

In (17), K_p, τ_i, τ_d are the parameters of the PID controller, T is the sample period.

As soon as the digital duty cycle (12 bits) is obtained, by using the mixed method of the counter (8 bits) and delay line (4 bits) [27], [28], the DPWM Module converter the digital control signal to the required PWM signal.

In order to facilitate the calculation of the proposed algorithm, the LPM_ROM Block is used in the CBC Module to provide a control data table, which is calculated off-line. In this way, the digital controller response to the load transient very quickly by look-up table method.

V. Simulations and Experimental Results

In order to verify the performance of the proposed method, A DTFC, undergoing a load current change, was designed. The parameters of the DTFC were provided as follows: $V_{\rm in} = 48\,{\rm V}$, $V_{\rm o} = 12\,{\rm V}$, $f_{\rm s} = 250\,{\rm kHz}$, $L = 15\,\mu{\rm H}$, $C = 100\,\mu{\rm F}$, ${\rm n} = 5:6$.

A. Simulation Results

Simulation is performed by Matlab/Simulink to verify the effectiveness of the proposed control algorithm. As comparison, a well-designed digital PID controller (Bandwidth ≈ 50 kHz, Phase margin $\approx 55°$) is also simulated.

$$d(k) = d(k-1) + 35.083e(k) - 66.33e(k-1) + 31.35e(k-2) \quad (18)$$

Fig. 9(a) illustrates the different dynamic performance of a voltage-mode controlled DTFC converter and a CBC controlled DTFC converter, while a positive load step change (from 3 A to 6 A). It is observed that, by using the conventional voltage mode controller, the undershoot of the output voltage is 1.7 V, and the recovery time is 180 μs. While using the proposed CBC algorithm,

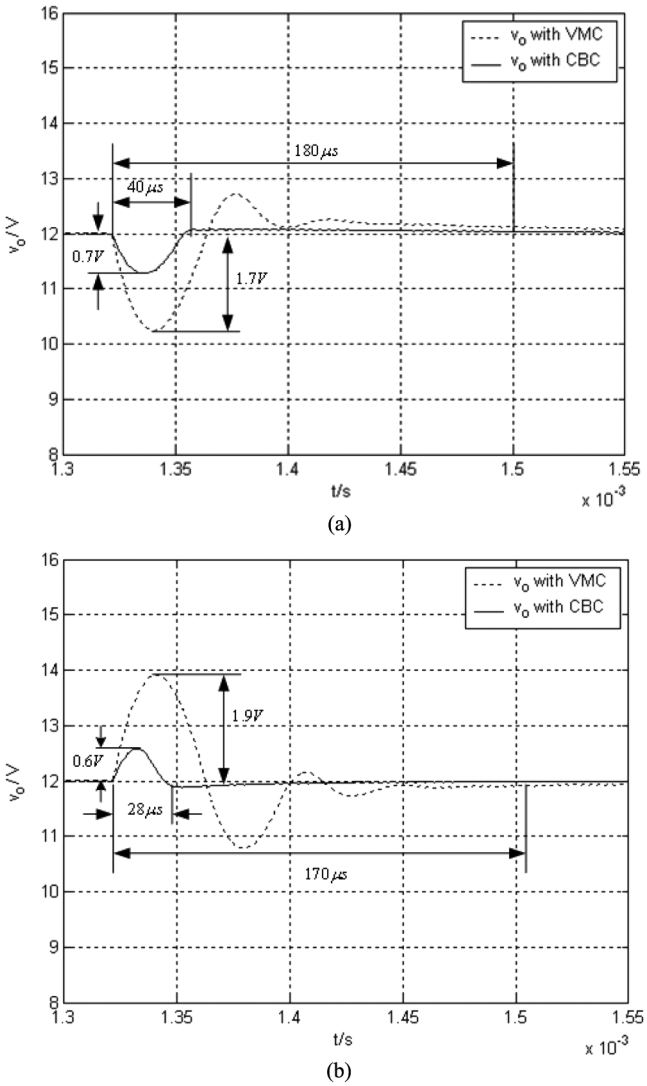


Fig. 9. Simulation results of output voltage response to a load current change. (a) Positive load step change 3 A → 6 A. (b) Negative load step change 6 A → 3 A.

the overshoot is reduced to 0.7 V, which is improved by 54%, and the settling time is reduced to 40 μs, which is improved by 77% compared to that of the voltage-mode controlled converter.

For a negative load step change (from 6 A to 3 A), Fig. 9(b) shows the output voltage response of a voltage-mode controlled DTFC converter and a CBC controlled DTFC converter. With the proposed controller, the overshoot is reduced to 0.6 V, which is improved by 68%, and the settling time is reduced to 28 μs, which is improved by 83% compared to that of the voltage-mode controlled converter.

It is demonstrated through the simulation that the settling time of the converter with proposed algorithm is improved significantly compared to that of the voltage-mode controlled converter.

B. Experimental Results

An experimental prototype of a DTFC was designed and implemented with FPGA by using the aforementioned algorithm, which is shown in Fig. 10.

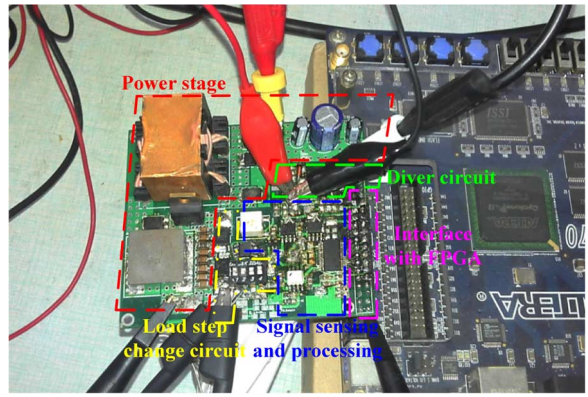


Fig. 10. Photograph of a 100 W prototype.

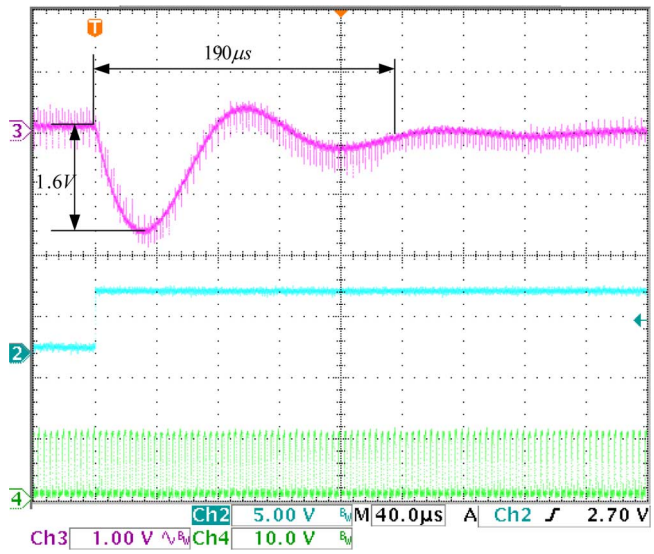


Fig. 11. Experimental results of positive load transient case 3 A → 6 A using linear mode controller.

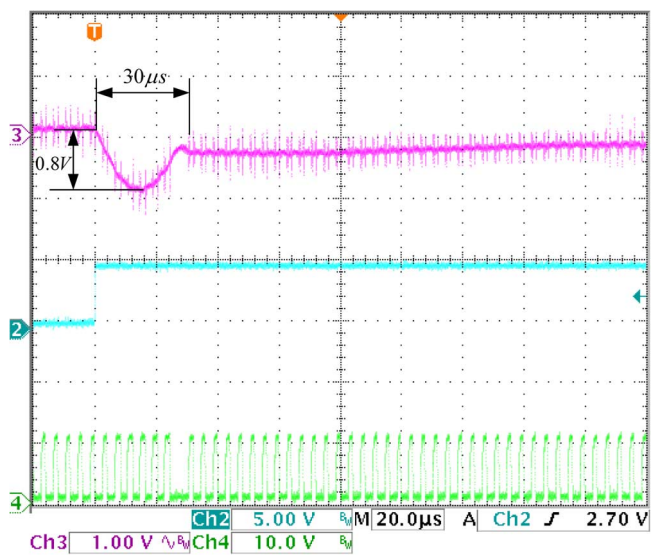


Fig. 12. Experimental results of positive load transient case 3 A → 6 A using CBC controller.

With the same parameters of the DTFC in the simulation, the maximum of the duty cycle is limited as 48% to avoid the magnetic field saturation of the transformer's core.

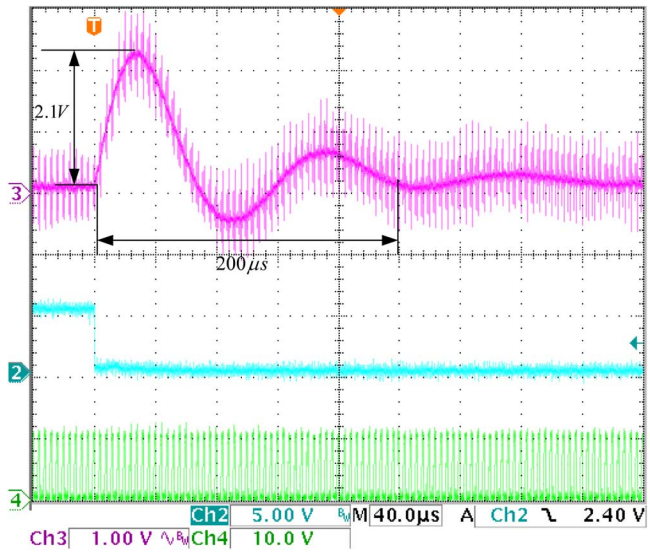


Fig. 13. Experimental results of negative load transient case 6 A → 3 A using linear mode controller.

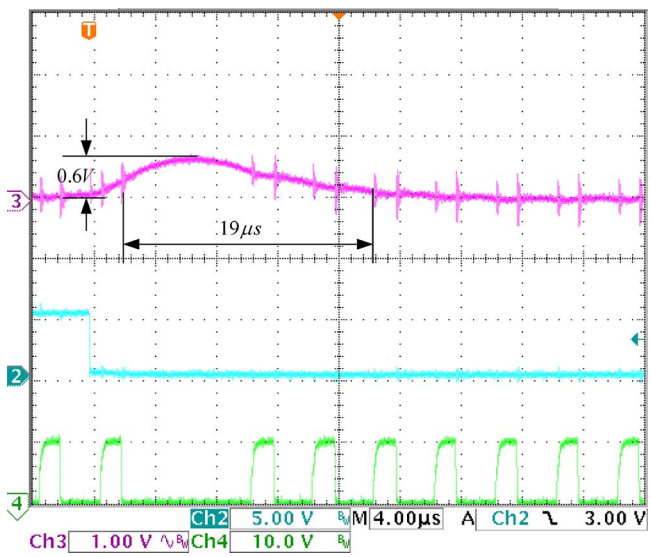


Fig. 14. Experimental results of negative load transient case 6 A → 3 A using CBC controller.

As shown in Fig. 11 and Fig. 12, the experimental results demonstrate the transient performance of conventional voltage mode controller under the load step change from 3 A to 6 A.

Limited by the bandwidth, the voltage mode controller has a large voltage variations and a long recovery time. For a positive load transient, the undershoot voltage is about 1.6 V with 190 μs settling time. While, the overshoot voltage is 2.1 V with 200 μs settling time during a negative load transient.

Experimental results of proposed CBC controller under the load step change from 6 A to 3 A are shown in Fig. 13 and Fig. 14. Compare to the voltage mode controller, the undershoot voltage is reduced by 50% with the recovery time is shortened by 80% for a positive load step change, while the overshoot voltage is reduced by 71% with the recovery time is shortened by 90% for an negative load step change.

VI. Conclusion

A new digital control algorithm has been presented for improving the dynamic performance of a DTFC. Using the principle of capacitor charge balance, the minimal voltage deviation and recovery time are derived by calculating the optimal switch over time. Due to the limitation of the maximum duty cycle of the DTFC, an approximation calculation is presented to simplify the design. Both the simulation results and experimental results demonstrated that the proposed controller had a superior performance when compared to the conventional controller.

It should be noted that the proposed algorithm can also be applied to other isolation converters, such as half-bridge, full-bridge, active clamped forward converters.

References

[1] K. Park, G. Moon, and M. Youn, "Series-input series-rectifier interleaved forward converter with a common transformer reset circuit for high-input-voltage applications," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3242–3253, Nov. 2011.

[2] A. Abramovitz, T. Cheng, and K. Smedley, "Analysis and design of forward converter with energy regenerative snubber," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 667–676, Mar. 2010.

[3] K. B. Park, C. E. Kim, and G. W. Moon, "Three-switch active-clamp forward converter with low switch voltage stress and wide ZVS range for high-input-voltage applications," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 889–898, Apr. 2010.

[4] D. Wang, X. N. He, and J. J. Shi, "Design and analysis of an interleaved flyback-forward boost converter with the current autobalance characteristic," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 489–498, Feb. 2010.

[5] A. Jangwanitlert and J. Songboonkaew, "An asymmetrical half-bridge forward converter with current doubler," in *Proc. 2010 Int. Conf. Electr. Eng./Electronics Computer Telecommunications Inf. Technol.*, Chiang Mai, Thailland, May 2010, pp. 507–511.

[6] C. H. Chien, Y. H. Wang, and B. R. Lin, "Zero-voltage switching DC/DC converter with two half-bridge legs and series-parallel transformers," *IET Power Electron.*, vol. 5, no. 4, pp. 419–427, 2012.

[7] V. Vaisanen, T. Riipinen, and P. Silventoinen, "Effects of switching asymmetry on an isolated full-bridge boost converter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2033–2044, Aug. 2010.

[8] E. H. Kim and B. H. Kwon, "Zero-voltage- and zero-current-switching full-bridge converter with secondary resonance," *IEEE Trans. Ind. Electron.*, vol. 25, no. 8, pp. 1017–1025, 2010.

[9] Q. H. Chang, W. Jian, and H. R. Zhang, "An improved two-transistor forward converter with integrated magnetics," in *Proc. ICEMS*, Tokyo, Japan, Feb 2009, pp. 1952–1957.

[10] Y. T. Yue and L. Yan, "A novel high power factor soft-switching communication power supply," in *Proc. 6th IEEE ICIEA*, Jun. 2011, pp. 341–344.

[11] K. Li and D. S. Sha, "Stability mechanism analysis of input-series and output-parallel connected DC-DC converters," in *Proc. ICIST*, Mar. 2012, pp. 109–111.

[12] G. Feng, W. F. Zhang, and Y. F. Liu, "A new current feedback fuzzy logic controller with extended state observer for DC-to-DC converters," in *Proc. 19th Annual IEEE Applied Power Electronics Con. APEC*, 2004, vol. 3, pp. 1771–1777.

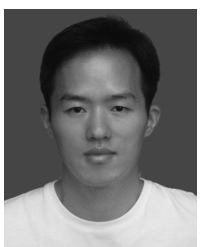
[13] C. Zengshi, "PI and sliding mode control of a cuk converter," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3695–3703, Aug. 2012.

[14] J. L. Sosa, M. Castilla, J. Miret, and L. S. Moreno, "Sliding-mode input-output linearization controller for the DC/DC ZVS CLL-T resonant converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1554–1564, Mar. 2012.

[15] Y. K. Luo, C. C. Chiou, C. H. Wu, K. H. Chen, and W. C. Hsu, "Transient improvement by window transient enhancement and overshoot suppression techniques in current mode boost converter," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2753–2761, Oct. 2011.

[16] G. Feng, E. Meyer, and Y. F. Liu, "A new digital control algorithm to achieve optimal dynamic response performance in DC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1489–1498, Jul. 2007.

[17] E. Meyer and Y. F. Liu, "A quick capacitor charge balance control method to achieve optimal dynamic response for buck converters," in *Proc. 2007 IEEE Power Electronics Specialists Conf. PESC*, Jun. 2007, pp. 1549–1555.
[18] X. D. Liu, L. Ge, W. Fang, and Y. F. Liu, "An algorithm for Buck-Boost converter based on the principle of capacitor charge balance," in *Proc. 2011 6th IEEE ICIEA*, Jun. 2011, pp. 1365–1369.
[19] W. Fang, Y. J. Qiu, X. D. Liu, and Y. F. Liu, "A new digital capacitor charge balance control algorithm for boost DC/DC converter," in *Proc. 2010 IEEE ECCE*, Sept 2010, pp. 2035–2040.
[20] L. Jia and Y. F. Liu, "A simplified charge balance control for better unloading response," in *Proc. 2012 IEEE ISIE*, May 2012, pp. 111–116.
[21] Y. Wen and O. Trescases, "DC-DC converter with digital adaptive slope control in auxiliary phase for optimal transient response and improved efficiency," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3396–3409, Jul. 2012.
[22] P. Cortes, F. Quiroz, and J. Rodriguez, "Predictive control of a grid-connected cascaded H-bridge multilevel converter," in *Proc. EPE*, Sep 2011, pp. 1–7.
[23] L. Corradini, A. Costabeber, P. Mattavelli, and S. Saggini, "Parameter-independent time-optimal digital control for point-of-load converters," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2235–2248, Oct. 2009.
[24] A. Costabeber, L. Corradini, P. Mattavelli, and S. Saggini, "Time optimal, parameters-insensitive digital controller for DC-DC buck converters," in *IEEE Power Electronics Specialists Conf.*, 2008, pp. 1243–1249.
[25] E. W. Zurita-Bustamante, J. Linares-Flores, E. Guzman-Ramirez, and H. Sira-Ramirez, "A comparison between the GPI and PID controllers for the stabilization of a DC-DC "buck" converter: A field programmable gate array implementation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 489–498, Nov. 2011.
[26] B. Alecsa, M. N. Cirstea, and A. Onea, "Simulink modeling and design of an efficient hardware-constrained FPGA-based PMSM speed controller," *IEEE Trans. Ind. Informat.*, vol. 8, no. 3, pp. 554–562, 2012.
[27] V. Yousefzadeh, T. Takayama, and D. Maksimovi, "Hybrid DPWM with digital delay-locked loop," in *Proc. IEEE Workshops COMPEL*, Jul. 2006, pp. 142–148.
[28] G. L. Sheng, Z. X. Chen, Z. J. Chen, and Y. F. Liu, "Design and implementation of a high resolution DPWM based on a low-cost FPGA," in *Proc. 2010 IEEE E ECCE*, Sep. 2010, pp. 2306–2311.



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