A Dual-Channel Isolated Resonant Gate Driver for Low Gate Drive Loss in ZVS Full-Bridge Converters*

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***Abstract*— As the switching frequency increases, to reduce the gate drive loss combined with the Zero-Voltage-Switching (ZVS) technique is meaningful for the widely used Full-Bridge (FB) converters. A dual-channel isolated Resonant Gate Driver (RGD) is proposed in this paper. The proposed RGD is able to provide two isolated complementary drive signals for two power MOSFETs in one bridge leg. Furthermore, the proposed RGD reduces about 79% gate drive loss compared to the conventional Voltage Source Driver (VSD). In addition, the negative gate drive voltage provided by the proposed RGD prevents the false trigger problem. The optimum design of the proposed RGD is given in detail. A 200-VDC input, 48-V/ 20-A output and 500-kHz phase-shift ZVS FB converter with the proposed RGD was built to verify the advantage and efficiency improvement.**

Index Terms: Resonant Gate Driver (RGD), power MOSFET, Zero-Voltage Switching (ZVS), Full-Bridge (FB)

I. INTRODUCTION

In recent years there has been a trend to increase the switching frequency to reduce the size and volume of the passive components, such as inductors, transformers, and capacitors [1]. The objectives of this trend are to increase the power density. Normally, as the switching frequency increases, the switching loss and gate drive loss increase if the conventional voltage drivers are used [2]-[3]. In the past two decades, a lot of work has been done on reducing, or eliminating the switching loss. Soft switching technique is one of the effective solutions to reduce the switching loss in high-frequency operations. With Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS), the Full-Bridge (FB) converters exhibit lower switching loss and are widely used in many applications [4]-[5]. However, there was little work related to reducing gate drive loss until recently the switching frequency starts to be above 1 MHz in low voltage and high current applications such as Voltage Regulators (VRs) [6]-[9]. Therefore, the target to minimize the gate drive loss at high frequency becomes an interesting topic combined with the ZVS technique in the FB converters.

Recently, many Resonant Gate Drivers (RGDs) have been proposed with the objective of recovering the gate energy lost in a conventional gate driver [10]-[13]. The RGD in [11] is designed for two ground-sharing power MOSFETs. Basically, this RGD is only able to drive two power MOSFETs sharing the same ground and not applicable to the power MOSFETs in one bridge leg. So the RGD is not suitable for the FB converter with two bridge legs. The RGD in [12] is designed for two power MOSFETs in one bridge leg. The resonant inductor of the RGD suffers the input voltage. When the input voltage becomes high, the resonant inductance should have to increase significantly, which is not suitable for the FB converters. Furthermore, this RGD can not provide the negative gate drive voltage to prevent the false trigger in the FB converters. The RGD in [13] can overcome the disadvantages of the dual channel RGD in [12], but this RGD has its own limitation when applied to the FB converters. It needs four drive switches and a resonant inductor for single power MOSFET. This increases the complexity and cost significantly when it is applied to a FB converter with four power MOSFETs.

The objective of the paper is to propose a dual-channel isolated RGD solution suitable for the FB converters. The proposed RGD is able to drive two MOSFETs in one bridge-leg with the controlled dead time, which leads to the simplicity and low cost. The negative gate drive voltage ensures high reliability of the turn-off status to avoid fast *dv/dt* problem over the previously proposed RGDs. These benefits make the proposed one suitable for the FB converters.

II. Proposed Resonant Gate Driver

A. Analysis of the Conventional Voltage Source Driver and the Proposed RGD in [13]

Fig. 1 shows the conventional Voltage Source Driver (VSD) in the FB configuration for a single power MOSFET. In this circuit, S_1-S_4 are drive switches, R_{ext} is the external

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resistance, R_g is the gate resistance, C_{g_Q} represents the input capacitance of the power MOSFET Q, i_g is the gate current, and v_{gs} is the gate-to-source voltage. When S_1 and S_4 are on, v_{gs} is equal to V_c and the power MOSFET Q is on. When S_2 and S_3 are on, v_{gs} is equal to $-V_c$ and Q is off. However, during the turn-off transition, the electric charge $2C_{g\_Q}V_c^2$ provided by the dc power supply is dissipated in the resistors R_{ext} and R_g entirely. Furthermore, as the switching frequency increases, the drive power consumption increases proportionally.

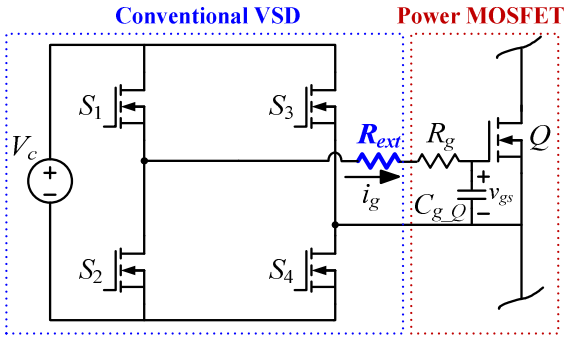


Fig. 1 Conventional gate drive circuit

In the FB converters, the conventional transformer coupled VSD shown in Fig. 2 is widely used. S_1-S_4 are the drive switches, D_1-D_4 are the freewheel diodes, R_{ext1} and R_{ext2} are the external resistors, R_{g1} and R_{g2} are the gate mesh resistance. This VSD has the ability to drive two power MOSFETs in one bridge leg with isolation, leading to the low complexity and high reliability. Unfortunately, in this VSD, the energy provided to drive the power MOSFETs still dissipates totally in the resistors R_{g1}, R_{ext1}, R_{g2}, and R_{ext2}.

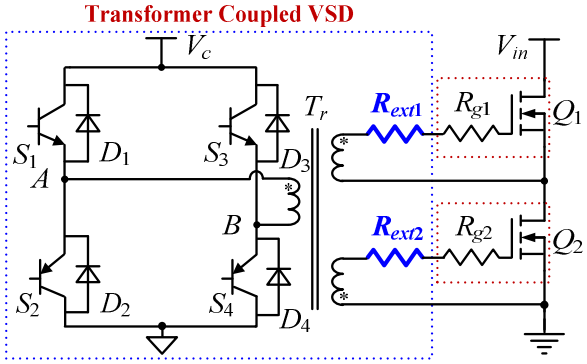


Fig. 2 The conventional transformer coupled VSD

Fig. 3 (a) shows the proposed RGD in [13]. S_1-S_4 are drive switches, L_r is the resonant inductor. Fig. 3 (b) shows the equivalent circuit of the RGD in [13]. C_{g_Q} represents the input capacitance of the power MOSFET Q. v_g is the controllable voltage source decided by the drive switches S_1-S_4. This RGD utilizes the series L-C resonance to recycle the electric charge stored in C_{g_Q}. However, it is designed for one single MOSFET. Each gate-driving circuit requires four drive switches (S_1-S_4) and an independent dc power supply (i.e. V_c). It should be noted that in one bridge leg, two MOSFETs do not share the same ground and therefore, two independent dc power supplies are required if this RGD is used. As a result, in a FB converter, two bridge legs require sixteen drive switches and four independent dc power supplies with some auxiliary components. This increases the complexity and the cost significantly and also results in the low reliability.

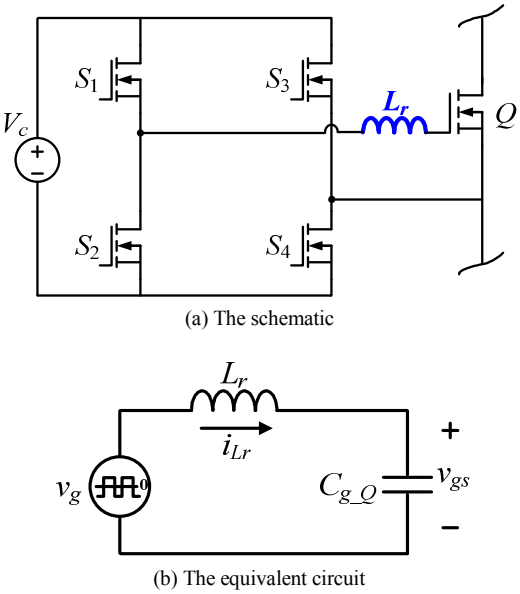


Fig. 3 The RGD proposed in [13]

B. The Proposed Isolated RGD

To overcome the drawbacks of the above circuits, the proposed isolated RGD is shown in Fig. 4. The circuit consists of four drive switches S_1-S_4, the drive transformer T_r (turn radio 1:1:1), two resonant inductors L_{r1} and L_{r2}. L_{r1} and L_{r2} can be the leakage inductance of the transformer. Q_1 is the high side switch and Q_2 is the low side switch in one bridge leg.

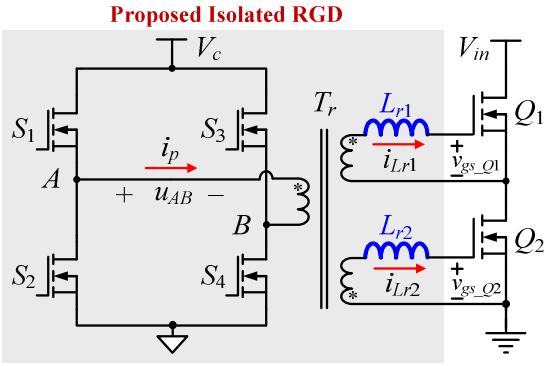


Fig. 4 The proposed isolated RGD

The gate waveforms of four drive switches, S_1-S_4, the voltage between A and B, u_{AB}, the primary side current, i_p, along with the resonant inductor current, the gate-to-source voltage v_{gs_Q1}, v_{gs_Q2} are illustrated in Fig. 5. S_1 and S_2, S_3 and S_4 are switched out of phase with the complementary control respectively. It is observed that the pulse width of u_{AB} is controlled by the switching status of the four drive switches S_1-S_4. i_{L1} and i_{L2} are the resonant current through L_{r1} and L_{r2}, respectively. The value of i_p is the sum of the absolute value of i_{L1} and i_{L2}. The inductor current i_{L1}, i_{L2}, i.e., the gate current of power MOSFET is sinusoidal and discontinuous, which reduces the additional conduction loss. The proposed RGD turns the MOSFETs on and off by using the resonant current

injected into the input capacitance as shaded during [t_1, t_2] and [t_3, t_4], respectively. Moreover, the gate-to-source voltage v_{gs_Q1} and v_{gs_Q2} are complementary and sinusoidal during the switching transition.

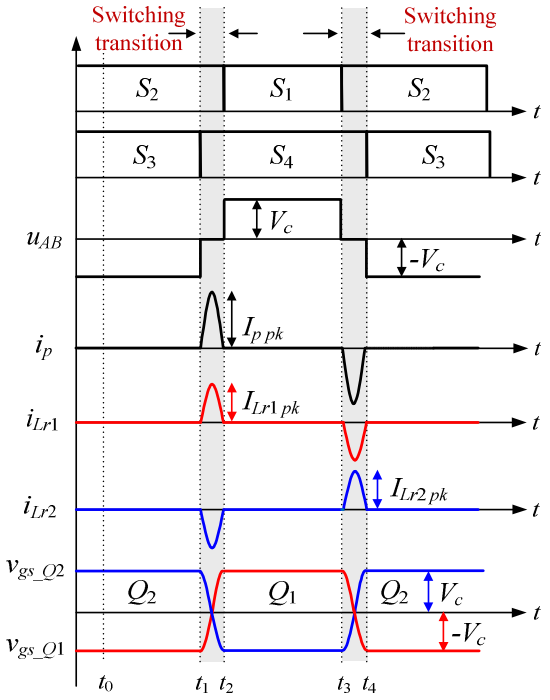


Fig. 5 The key waveforms of the proposed RGD

The proposed RGD is controlled in the complementary mode and provides two drive signals with duty cycle D and 1-D respectively. It is observed that no current flows through the dc power supply V_c. Therefore, the power supply provides no electric power to the gate drive circuit theoretically during the switching transition, which indicates that the gate drive loss is reduced significantly by the proposed RGD. Furthermore, the RGD is able to provide a negative gate voltage to the MOSFET and prevent the false trigger due to the fast *dv/dt* problem in the FB converter.

The number of drive switches and independent dc power supplies required to drive a FB converter are compared between the proposed isolated RGD and the RGD in [13], which is shown in Table I. Essentially, the RGD in [13] needs sixteen drive switches and four independent dc power supplies for a FB converter. The proposed isolated RGD needs eight drive switches and one independent dc power supply. It is observed that the proposed isolated RGD needs much less drive switches and power supplies, which can minimize the cost and increase the reliability.

Table I THE NUMBER OF DRIVE SWITCHES AND INDEPENDENT DC POWER SUPPLIES

	Number of Drive Switches	Number of Independent DC Power Supplies
RGD in [13]	16	4
Proposed RGD	8	1
Reduction	**50 %**	**75 %**

III. Loss Comparison and Benefits

A. Loss Comparison between the Proposed RGD and the Conventional VSD

This section analyzes the loss of the proposed RGD and makes a comparison between the conventional VSD. To demonstrate the gate drive loss saving with the proposed RGD, the design parameters are given in Table II. The design parameters provided in this part agree with the experimental parameters.

Table II DESIGN PARAMETERS OF THE PROPOSED RGD

Switching Frequency, f_{sw}	500 kHz
Gate Drive Voltage, V_c	15 V
Resonant Inductor, L_{r1},L_{r2}	246 nH
Power MOSFET, Q_1,Q_2	IPP50R199CP
Total Gate Charge, Q_g	50 nC
Internal Gate Resistance, R_g	2.2 Ω
Drive MOSFETs, S_1-S_4	FDN335N
Total Gate Charge, Q_{g_s}	3.7 nC
On Resistance, $R_{DS(on)}$	0.07 Ω
Output Capacitance, C_{oss}	80 pF

Although the proposed RGD does not have any power consumption in theory, the resistance in the circuit produces the power consumptions in practical. As the two power MOSFETs are controlled in the complementary mode, one of two gate drive channels is chosen to analyze. R_{sg} is the sum of the winding resistance in resonant inductor and transformer, and the gate-pattern resistance inside the power MOSFET. R is the total resistance existing in the current loop, which is given by R=2$R_{DS(on)}$+R_{sg}. The proposed RGD utilizes the L-C resonance to change the gate-to-source voltage applied to the input capacitance. As the resistance R exists in the resonant circuit, the absolute value of the gate-to-source voltage decreases after each switching transition, which is equal to the voltage drop ΔV. The value of ΔV can be calculated by the simplified R-L-C circuit. Then, the dc power supply provides an amount of electric energy, which is equal to $2C_{iss}V_c\Delta V$ for turn on and turn off process. Therefore, the electric power to compensate for the voltage drop ΔV is

$$P_c = 2f_{sw}C_{iss}V_c\Delta V \quad (1)$$

Although the total gate charge of S_1-S_4 is low, it may still cause some losses at high switching frequency. The switching frequency of these four MOSFETs is the same as the f_{sw} of the power MOSFETs. The total gate drive loss of S_1-S_4 is

$$P_s = 4Q_{g\_s}V_{gs\_s}f_{sw} \quad (2)$$

where Q_{g_s} is the total gate charge of drive MOSFETs, V_{gs_s} is the drive voltage of S_1-S_4.

In addition, the dc power supply should charge the output capacitance C_{oss} in the drive MOSFETs S_1-S_4 in each switching cycle. Thus, the electric power P_r is

$$P_r = 4C_{oss}V_c^2f_{sw} \quad (3)$$

The drive transformer is not ideal actually, so the loss exists. The transformer loss consists of the magnetic hysteresis loss, eddy-current loss and residual loss. The total transformer loss is

$$P_t = \eta f_s^{\alpha} B_m^{\beta} V \quad (4)$$

where η is the loss coefficient, α is the frequency index (>1), β is the magnetic induction index (>1), B_m is the magnetic induction, and V is the volume of the magnetic core.

Therefore, the power consumption P_{d_RGD} for driving two MOSFETs in one bridge leg with the proposed RGD is

$$P_{d\_RGD} = 2P_c + P_s + P_r + P_t \quad (5)$$

For comparison, the conventional transformer coupled VSD in Fig. 2 is analyzed. The gate drive loss for one power MOSFET with the conventional VSD is calculated. Take account of the negative gate voltage, the dc power supply has to provide an electric energy as large as $2C_{iss}V_c^2$ to turn the power MOSFET on and off. This electric energy provided by the dc power supply is consumed in the gate resistor R_g. Therefore, the power loss P_g in the gate resistor is

$$P_g = 4 f_{sw} C_{iss} V_c^2 \quad (6)$$

From (2), (3), (4) and (6), the power consumption for driving two MOSFETs in one bridge leg with the conventional transformer coupled VSD is

$$P_{d\_conv.} = 2P_g + P_s + P_r + P_t \quad (7)$$

Based upon the design parameters and the above equations, the calculated results are provided in the Table III. With the proposed RGD, the gate drive loss of two MOSFETs in one bridge leg is reduced from 3.14 W to 0.66 W (a reduction of 79.0 %). Meanwhile, the drive loss of four power MOSFETs in a FB converters is reduced from 6.28 W to 1.32 W (a reduction of 79.0 %), translating into an efficiency improvement of 0.5 percent in a 1-kW FB converter.

Table III GATE DRIVE LOSS COMPARISON BETWEEN THE PROPOSED RGD AND CONVENTIONAL VSD

	Drive Loss of Two MOSFETs in one Bridge Leg	Drive Loss of Four MOSFETs in a FB Converter
Conventional Driver	3.14 W ($P_{d\_conv.}$)	6.28 W
Proposed RGD	0.66 W (P_{d_RGD})	1.32 W
Loss Reduction (%)	**79.0 %**	

B. Benefits of the Proposed Isolated RGD

With the above comparison, the advantages of the proposed isolated RGD are highlighted as follows:

1) Significant reduction of gate drive loss

Compared to the conventional gate driver, the energy stored in the input capacitance can be recovered in the proposed RGD. The resonance between the resonant inductor and input capacitance makes the energy to return to the input capacitance and reverses the polarity of the input capacitance.

2) High reliability of the turn-off status

The RGD is able to provide a negative gate voltage to the MOSFET and improves the reliability due to fast dv/dt problem in high power and high voltage applications.

3) Capability to provide two isolated complementary drive signals

The proposed RGD has the ability to drive two MOSFETs in a bridge-leg and makes the power segment and control segment to be isolated, which leads to the simplicity and low cost.

IV. Optimal Design of the Proposed RGD

In the proposed isolated RGD, the inductance value of L_{r1} and L_{r2} are usually equal as $L_{r1}= L_{r2}= L_r$. To select the proper resonant inductance L_r, two issues have to be taken into consideration: the driving speed and gate drive loss.

The rising time t_r and falling time t_f of driving a power MOSFET affect the design value of L_r. In the proposed RGD, the characteristic impedance of the resonant inductor L_r and the input capacitance C_{iss} is much larger than the total resistance in the resonant circuit, so the resistance has no effect on the natural resonance between L_r and C_{iss}. As shown in Fig. 6, the gate drive voltage of power MOSFET Q_1 or Q_2 is sinusoidal during the turn on transition from $-V_c$ to V_c. The rising time t_r defined as the interval for V_{gs} to rise from zero to V_c is

$$t_r = \frac{1}{2}\pi\sqrt{L_r C_{iss}} \quad (8)$$

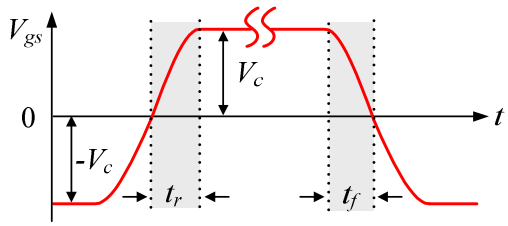


Fig. 6 t_r and t_f in the switching period

Similarly, the falling time t_f defined as the interval for V_{gs} to fall from V_c to zero is

$$t_f = \frac{1}{2}\pi\sqrt{L_r C_{iss}} \quad (9)$$

From (8) and (9), the larger L_r is, the slower the power MOSFET is driven. With ZVS operation of one bridge leg, usually at most 5% of the switching period is allowed. Hence,

$$t_d = t_r + t_f = \pi\sqrt{L_r C_{iss}} \le \frac{5\%}{f_s} \quad (10)$$

where t_d is the total driving time of the power MOSFET. The NMOSFET IPP50R199CP from Infineon is chosen as the power MOSFET, and the total gate charge Q_g=50 nC when V_{gs}=15 V. The relationship between the value of L_r and the driving time t_d is illustrated in Fig. 7. It is observed that with the increasement of the resonant inductor L_r, the driving time t_d increases.

From (10), the maximum value of L_r follows

$$L_r \le \frac{\left(\frac{5\%}{\pi f_s}\right)^2}{C_{iss}} \tag{11}$$

Based upon the given design parameters, the value of L_r is calculated less than 300 nH from (11) as shown in Fig. 7.

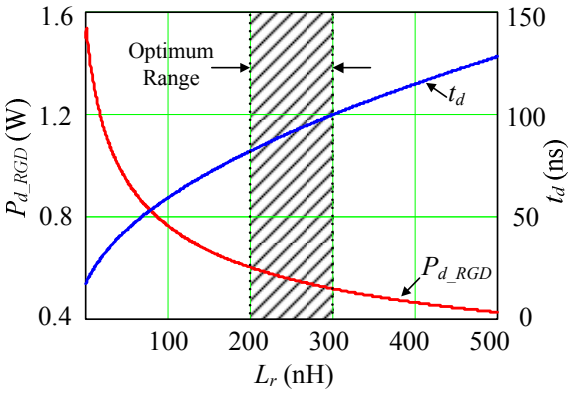


Fig. 7 The optimum range of the value of L_r

On the other hand, a larger L_r is more effective in reducing the gate drive loss. As analysed in section III, from (5), P_{d_RGD} as a function of the resonant inductance L_r is also illustrated in Fig. 7. It is observed that with the increase of the resonant inductance L_r, the gate drive loss P_{d_RGD} is reduced. Furthermore, the rate of change of gate drive loss reduction is slow when the resonant inductance L_r becomes large. The drive loss reduction is expected to be more than 75.0 %. Hence,

$$\frac{P_{d\_conv.} - P_{d\_RGD}}{P_{d\_conv.}} \ge 75\% \tag{12}$$

where $P_{d\_conv.}$ is the gate loss of two power MOSFETs in one bridge leg with the conventional VSD.

From (12), as P_{d_RGD} is a function of L_r, the value of L_r can be solved to be larger than 200 nH as shown in Fig. 7.

As a conclusion, considering the driving speed and the gate drive loss, the value of L_r is 200-300 nH for the optimum design in the proposed RGD with the desired specifications shown in Fig. 7.

V. Experimental Results and Discussion

A 200-VDC input, 48-V/ 20-A output and 500-kHz phase-shift ZVS FB converter with the proposed RGD was built to verify the advantage. The schematic of the FB converter with the proposed RGD is shown in Fig. 8. The components used are as follows: IPP50R199CP is used as the power MOSFET Q_1-Q_4; the Schottky diode DSSK60-02A is used as the rectifier D_{R1} and D_{R2}; the output inductance L_f is 6 uH and the output capacitance C_f is 3000 uF. The FDN335N is used as the drive switch S_1-S_8 and the gate drive voltage V_c=15 V. The leakage inductances of the drive transformer T_{r1} and T_{r2} are 270 nH, which are measured by the HEWLETT PACKARD 4284A precision LCR meter. Because the value of the leakage inductance fits the optimum design range as shown in Fig. 7, they can be used as the resonant inductance L_{r1} and L_{r2} in this case. The photo of the prototype is shown in Fig. 9.

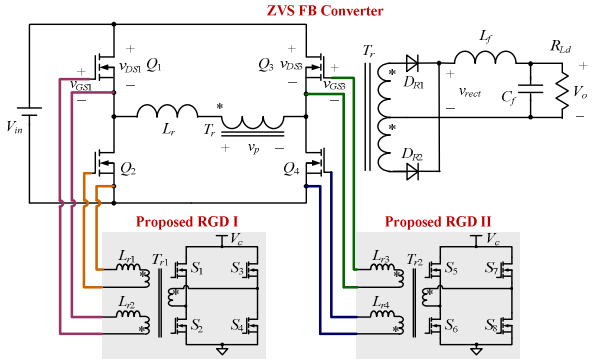


Fig. 8 The schematic of the FB converter with the proposed RGD

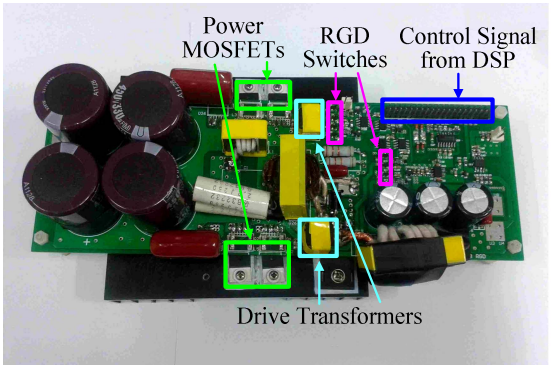


Fig. 9 Photograph of the prototype

Fig. 10 illustrates the voltage of primary-side v_p and the rectifier voltage v_{rect} of the power transformer in the FB converter. It is observed that the primary voltage v_p is a modulated pulse waveform since the phase-shift control is applied to the ZVS FB converter through the proposed RGD. The corresponding waveform of the secondary side v_{rect} is obtained through the full-wave rectifier.

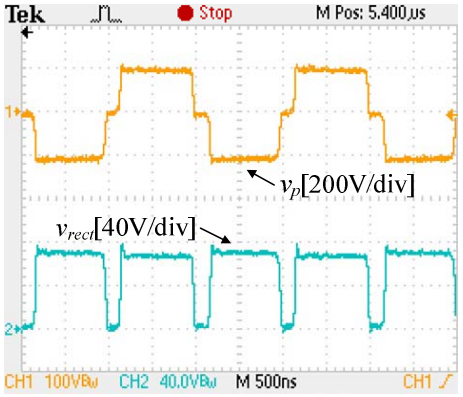
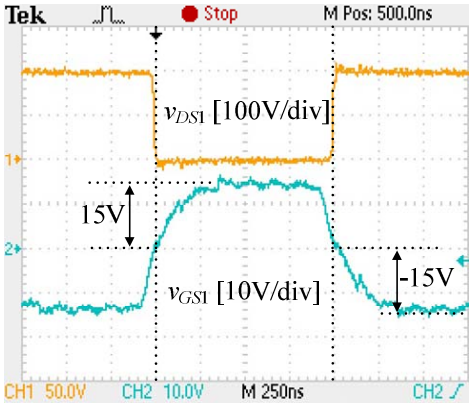


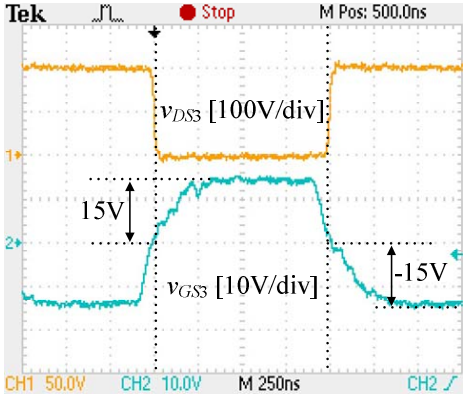
Fig. 10 The waveforms of v_p and v_{rect}

Fig. 11 illustrates the drain-source voltage v_{DS1} and the gate-source voltage v_{GS1} of the power MOSFET Q_1 in the FB converter. Fig. 11 (a) shows that the FB converter realizes ZVS for the leading leg under 1/2 load. As the output capacitance of the main power MOSFET is discharged by the energy of the output inductance, the drain-to-source voltage

v_{DS} reaches zero, and then the gate drive voltage is applied to turn on the MOSFET with ZVS. Similarly, Fig. 11 (b) illustrates v_{DS3} and v_{GS3} of the power MOSFET Q_3 in the FB converter. This waveforms show that the FB converter realizes ZVS for the lagging leg under 2/3 load. The proposed RGD is compatible with ZVS technique for the FB converter, and the switching loss and the gate drive loss can be both reduced.



(a) ZVS for the leading leg in 1/2 load



(b) ZVS for the lagging leg in 2/3 load

Fig. 11 The waveforms of ZVS

Fig. 12 shows the resonant inductor current i_{Lr1} and the gate-to-source voltage v_{gs_Q1}.The waveforms of i_{Lr1} and v_{gs_Q1} are sinusoidal during the switching transition, which indicates the resonance between the resonant inductor and the input capacitance. It is observed that when Q_1 is off, the gate drive voltage v_{gs_Q1} is -15 V, which improves the reliability due to fast *dv/dt* problem in the FB converters.

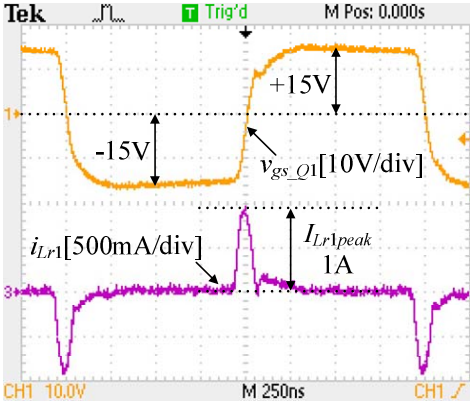


Fig. 12 Gate drive voltage and resonant inductor current

Fig. 13 shows the resonant inductor current i_{Lr1}, i_{Lr2} and the gate drive voltage v_{gs_Q1}, v_{gs_Q2}, which agrees with the theoretic waveforms in Fig. 5. It is observed that the gate drive voltage v_{gs_Q1} and v_{gs_Q2} are complementary, the directions of the resonant inductor current i_{Lr1} and i_{Lr2} are also opposite. This experimental waveform indicates that the proposed RGD has the ability to drive two power MOSFETs in one bridge leg, leading to the low complexity and cost in the FB converters.

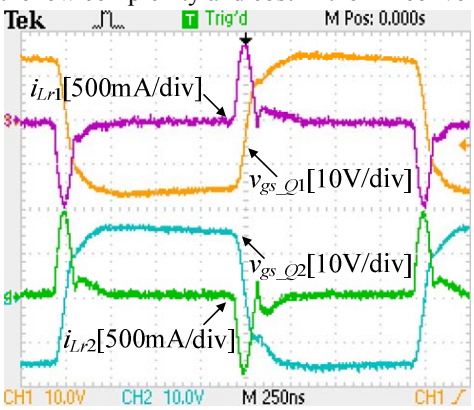


Fig. 13 Two complementary drive voltage and resonant inductor current

Fig. 14 illustrates the relationship between v_{gs_Q1}, i_{Lr1} and the voltage between A and B, v_{AB} during the turn on interval. It is observed that the resonance only happens during the stage of v_{AB}=0. This interval, i.e. v_{AB}=0, is the key difference between the conventional VSDs from the control strategy. During this interval, the proposed RGD utilizes the L-C resonance to recover the gate drive energy stored in the input capacitance of the power MOSFET. Therefore, the gate drive loss can be reduced significantly compared to the conventional VSDs. For the turn off interval, the detailed waveforms are similar to the turn on interval.

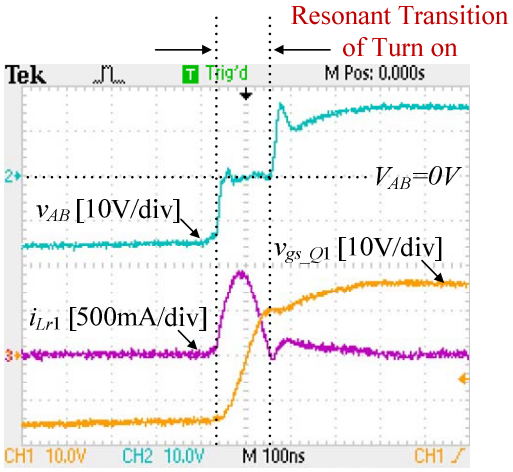


Fig. 14 Resonant switching transition: v_{gs_Q1}, i_{Lr1} and v_{AB}

Fig. 15 shows the waveforms of the gate drive voltage of Q_1 and Q_2. It is observed that the waveforms of gate drive voltage of Q_1 and Q_2 are complementary and there is no voltage overlap between two drive voltage signals. Therefore, the short-through problem can be prevented in the FB converters.

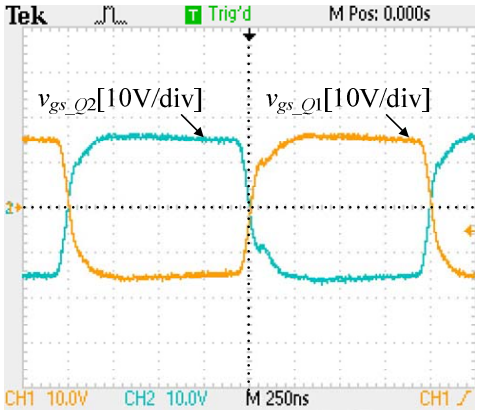


Fig. 15 Gate drive voltage of Q1 and Q2

Fig. 16 shows the measured efficiency comparison between the proposed RGD and the conventional transformer coupled VSD. It is observed that at 4 A, the efficiency is improved from 84.7% to 86.7% (an improvement of 2.0%). At 12A, the efficiency is improved from 91.4% to 92.2% (an improvement of 0.8%). It should be also noted that because of the low gate drive loss, the proposed RGD improves the efficiency effectively in full load range over the conventional transformer coupled VSD.

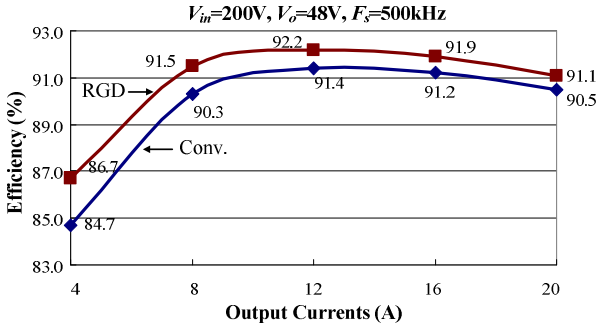


Fig. 16 Efficiency comparison

VI. CONCLUSION

An isolated RGD for two MOSFETs in one bridge-leg is proposed in this paper. The proposed RGD can provide two complementary drive signals to drive two MOSFETs, which can be used to drive the HB leg in FB converters. The proposed RGD consumes no electric power theoretically. Moreover, with the negative drive voltage capability, the proposed RGD ensures high reliability in the FB converters over the previously proposed RGDs. The loss analysis of the proposed isolated RGD and the comparison between the conventional gate driver are provided. The optimal design procedure is presented in detail. A 200-V input, 48-V output and 500-kHz phase-shift ZVS FB converter was built to verify the advantages of the proposed isolated RGD. Compared with the conventional gate driver, the proposed isolated RGD improves the efficiency from 84.7% to 86.7% (an improvement of 2.0%) at 4 A, and at 12 A, from 91.4% to 92.2% (an improvement of 0.8%).

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