Low Cost Microcontroller Based Implementation of Robust Voltage Based Capacitor Charge Balance Control Algorithm

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***Abstract*—In this paper, a low cost microcontroller based control method utilizing the concept of capacitor charge balance is presented to achieve a near-optimal transient response for Buck converters. First, this paper presents a new derivation of practical charge balance equations based on simplified differential equations. The final implementation does not require complex calculations and accurate knowledge of the output filter LC parameter. The hardware implementation only requires the output voltage information so that no extra sensing circuitry is needed compared with voltage mode controller. Also, this algorithm can be simply extended to adaptive voltage positioning (AVP) application. Second, due to the simplicity of this algorithm, a low cost microcontroller unit (MCU) based controller can be implemented to shorten the developing period for users. Thirdly, unlike previous work, the proposed voltage based CBC (V-CBC) controller does not require accurate current sensor or fast analog-to-digital converter (ADC). Instead, to detect the critical time instant when the inductor current equals the new load current, a practical extreme voltage detector is introduced to capture the output voltage peak/valley information. Experimental prototype is built to verify the feasibility and advantage of the new method.**

***Index Terms*—Adaptive voltage positioning (AVP), capacitor charge balance controller, dc-dc Buck converters, digital control, extreme voltage detector, fast transient performance, optimal control.**

I. Introduction

With the revolution of integration technology, it is possible to fabricate powerful microprocessors with more and more transistors on chip, resulting in higher load demand. On the other hand, to maintain/reduce the overall power consumption, the output voltage level of the microprocessor keeps dropping. As a result, the requirements of voltage regulator (VR) for powering next-generation microprocessor are more and more stringent, that is, low output overshoot/undershoot and short settling time (under increasingly large load transients). So it becomes much more difficult to meet the certain requirements using conventional linear mode controllers such as voltage and current mode controllers of which the design is normally made with the help of small signal model analysis. Due to the undesired response performance, a large volume of output capacitance is always used which occupies a big board area with linear mode controllers. To break the bandwidth barrier for faster transient response, couples of analog controllers and digital control algorithms have been introduced in some previous literatures to achieve this objective [1]–[26].

As one of the practical optimal control candidates, the capacitor charge balance concept was first introduced and implemented digitally in [6] for achieving minimum voltage variations and settling time. Furthermore, the CBC (charge balance control) concept can be implemented using digital signal processing devices. Using field-programmable gate array (FPGA), extensive work has been conducted in designing digital CBC controllers that further improves robustness [7], [9]–[13], [19], practical performance [7], [12], [13] and simplicity of the control system [7], [24]. However, all the previous schemes are not able to address at least one of the following limitations, so advanced FPGA and specific IC have been chosen for implementation, resulting in longer development time, higher cost and power consumption for controlled products.

1. Complex real-time calculation is embedded in the algorithm, like division and square root [6], [8] which requires high speed digital control devices for working out operations in a limited time interval. And it results in high implementation cost and controller power consumption.
2. Algorithm requires the knowledge of parameters of output filter (output capacitance C_o and/or inductance L_o) in Buck converter to perform the charge balance concept, limiting the practicality/robustness of the previous schemes [6]–[8], [14], [15], [23].
3. A fast or asynchronous analog to digital converter (ADC) [7]–[12] is required to detect the instant when the inductor current equals the new load current, resulting in higher ADC power loss and cost.
4. Certain type of current sensor is needed to implement the proposed scheme for estimation and time detection, resulting in high cost and/or poor accuracy [6], [14], [19] and bad reliability (capacitor current sensor introduces high dv/dt noise) of the overall system [7], [19], [27].
5. It is difficult to apply adaptive voltage positioning (AVP) or load line regulation using proposed schemes for powering modern processors such as Intel modules [6]–[8], [15], [16].

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Thanks to the development of semiconductor technology, most of the microcontroller units (MCUs) available in the market offer multiple function blocks such as PWM, ADC, and digital communication to the users. The price of the MCU is mainly determined by arithmetic core speed, ADC/DAC maximum sampling rate/resolution, number of I/O ports, etc. This paper presents a novel implementation of CBC controller to resolve the above issues using low cost MCU. First, to reduce computation load/the complexity of the algorithm, this paper proposed a novel and practical way to derive the charge balance equations. The previous research work has always selected the capacitor charge and discharge integrals associated with the inductor and load current as the starting point (including [7]–[12]). However, in this paper, a set of simplified differential equations are used so that a new output voltage curve analysis based derivation is achieved. This analysis provides a **unique** possibility for the proposed voltage based CBC algorithm to optimize all different fast transients including load and input voltage changes [4]. But, because of the limited space, this paper only focuses on step load transient cases though. The proposed algorithm can be extended for AVP applications with simple modifications. Second, to take full advantage of the resource in low cost MCU, such as PWM and integrated comparator, and reduce the ADC cost and power consumption, an analog extreme voltage detector is proposed and design guideline is provided.

This paper is organized as follows. In Section II, the basic idea of charge balance concept will be reviewed. In Section III, mathematical derivations of the proposed algorithm are discussed. In Section IV, the extensions of the proposed scheme for adaptive voltage positioning is presented. In Section V, the implementation and design guidelines are provided for the proposed mixed-signal control system and extreme voltage detector. Finally, the simulations and experimental results are demonstrated in Section VI to validate the proposed control algorithm. The conclusion is drawn in Section VII.

II. Basis of Charge Balance Control Concept

The principle of capacitor charge balance has been used extensively for the purpose of steady-state modeling and analysis of DC-DC converters. As the principle of capacitor charge balance presents, in steady-state, the average value of the capacitor current over one switching period must be equal to zero. This condition must be satisfied in order for the output voltage to be identical at the beginning and at the end of a switching cycle. Equation (1) represents the principle of capacitor charge balance for a Buck converter under steady state

$$\begin{aligned}&\frac{v_c\left[(N+1)\,T_{\rm sw}\right]-v_c\left(NT_{\rm sw}\right)}{T_{\rm sw}}\\&\quad=\frac{1}{C_o}i_{c\_{\rm avg\_sw}}\\&\quad=0\rightarrow\frac{1}{T_{\rm sw}}\int_{NT_{\rm sw}}^{(N+1)T_{\rm sw}}i_c\left(t\right)dt=0.\end{aligned}\tag{1}$$

In (1), v_c represents the capacitor voltage (neglecting ESR and ESL), $i_{\rm c\_avg\_sw}$ is the capacitor current over the steady-state switching period, C_o represents the output capacitor value and $T_{\rm sw}$ is the switching period of the converter. By recognizing that the integral period of (1) may be extended over the total transient time of a DC-DC converter, (2) is developed

$$\begin{aligned}\frac{v_c\left(t_b\right)-v_c\left(t_a\right)}{t_b-t_a}&=\frac{1}{C_o}i_{c\_{\rm avg\_trans}}\\&=0\rightarrow\frac{1}{t_b-t_a}\int_{t_a}^{t_b}i_c\left(t\right)dt=0.\end{aligned}\tag{2}$$

In (2), time instant t_a represents the beginning of the transient period and time instant t_b represents the end of the transient interval. $i_{\rm c\_avg\_trans}$ equals the average capacitor current over the transient period. Equation (2) indicates that as long as the integral of the capacitor current equals zero over the duration of the transient interval (i.e., the charge removed from the capacitor equals the charge delivered to the capacitor), the output voltage at the end of the transient will equal the voltage at the beginning of the transient. Thus, if at t_b, the inductor current i_L equals the load current and (2) has been satisfied, the output voltage will have returned to its reference voltage and, therefore, the converter has recovered from the transient event. The objective of the controller is to drive the Buck converter such that the inductor current and the output voltage return to their respective steady-state values simultaneously at t_b. Therefore, the charge balance principle is a practical solution for achieving minimal settling time [6], [19] following transients.

Typical waveform during an unloading transient is shown in Fig. 1 using CBC or similar types of optimal controllers. The CBC controller proposed and implemented using FPGA in [6] is based on time detection of t_0-t_3, but requires inductor current sensing and real time complex calculations to implement charge balance control. The algorithm is parameter dependent on output inductance and capacitance. The time based method proposed in [7] uses a digital double integrator to detect the time instants t_1 and t_2, but a capacitor current estimation is required and implemented using high speed FPGA. Another CBC controller is proposed and implemented using FPGA in [8], taking advantage of continuous time concept, however, the robustness of algorithm is limited and complex calculation is processed in real time to decide the $t_{\rm on}$ and $t_{\rm off}$ time for optimal control. On the other hand, the optimal control algorithm proposed and implemented also using FPGA in [7]–[13] applies similar geometric equation as [6] to derive the algorithm, but the time instants are determined by output voltage information instead of time intervals. However, a fast ADC or an asynchronous ADC is required to detect the voltage peak/valley, resulting in high cost of the implementation. Also, it is difficult to apply AVP technique in this implementation. A digital current mode CBC controller is presented in [14], but because of the real time complex calculation, a fast digital processing device is required. Also in order to set the current limit level, high speed ADC and DAC are necessary, resulting in high implementation cost and power loss. A mixed signal implementation is discussed in [16] and the time detection is based on output capacitor-*ESR* matching circuit, so the robustness is still limited. A sensorless adaptive voltage positioning scheme is discussed in [20] based on duty cycle compensation algorithm. The controller is designed using linear mode compensation, but the response is not optimal and the algorithm requires complex real time calculation and high

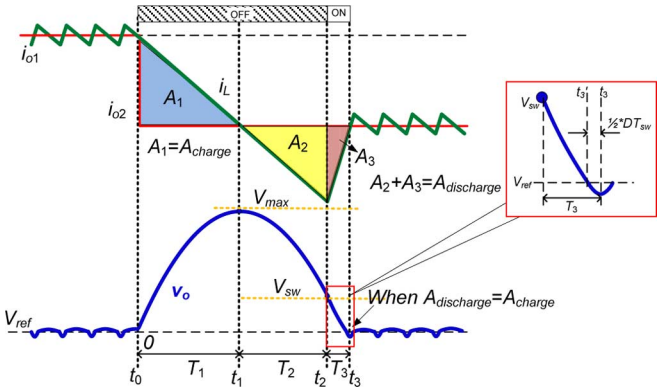

Fig. 1. Capacitor charge integral areas during an unloading step transient.

speed FPGA for implementation. A digital CBC like controller is presented in [21] based on capacitor current sensing and the algorithm is quite similar to the method in [6], [7], [9]–[13] (derived from geometric charge balance). But the implementation requires sensing resistor in series with the output capacitor, resulting in higher power loss, steady-state and transient voltage ripple, which is not preferred for voltage regulator application. Also, the algorithm is parameter dependent and requires high speed digital processing device for computing the real time complex equations in the algorithm.

It is noted that, linear voltage mode controller is used for steady-state operation; while charge balance control is used during transient condition to achieve tight output voltage regulation. As output voltage information is needed for linear voltage mode controller, output voltage sensing based charge balance concept will be a simple, practical and cost effective implementation. Following rapid transients, for all the CBC based controllers [6]–[17], the time instants t_1 (inductor current reaches new load current level) and t_2 (PWM changing ON/OFF state) are very important to arrange the desired ON/OFF control actions, accordingly.

In this paper, a practical extreme voltage detector is present to find t_1 and sample the maximum output voltage peak/valley. And in place of calculating interval T_2 [6], [8], [19], the time information t_2 is mapped to the switching point voltage (SPV) $V_{\rm sw}$, which provides voltage sensing based parameter-independent formula set under transients. The algorithm is derived based on output voltage curve analysis instead of balancing the geometric area of capacitor charge. Also an extension can be made for AVP application and input voltage step transient based on this SPV information [4].

III. Basic Idea of Voltage Sensing Based Charge Balance Control (V-CBC)

A. V-CBC Principles for a Buck Converter Undergoing an Unloading Transient

In this section, the new derivation method of CBC equations is discussed. Based on simplified solution of differential equations, the output voltage can be expressed as a piecewise parabolic function.

The CBC controller is usually designed for applications in which the load current slew rate is significantly larger than the inductor current slew rate. Therefore, in this analysis, it is assumed that the load current steps instantaneously from I_{o1} to I_{o2} and that the controller is able to react to the step with negligible delay. It is also assumed that the load current remains constant for the duration of the transient period. For VRs, sufficiently large output capacitance is required to suppress the output voltage deviation. And also for the low voltage rating, often, the paralleled ceramic output capacitors could provide very low ESR ($< 1\ \mathrm{m\Omega}$). So in the following discussion, an ideal dc-dc Buck converter model is examined. And the starting time t_0 is set to be 0 in the analysis for simplification in Fig. 1. The proposed digital control scheme is only activated during load transients, so it will not affect the steady state power conversion efficiency of the main Dc-Dc converter.

1) Step 1: Time Interval $T_1(t_0 \le t < t_1)$ for an Unloading Step Transient: In this interval, the top MOSFET of Buck converter is turned off. The inductor current decreases linearly, so during the time period $t_0 - t_1$ capacitor current i_c can be approximated as a linear function in (3), where m_2 is the falling slew rate of the inductor current $m_2 = V_o/L_o$, V_o is the output voltage and L_o is the output inductance

$$i_c(t)|_{0-t_1} = -m_2(t-t_1) = -\frac{V_o}{L_o}(t-t_1). \tag{3}$$

Based on the relationship of capacitor current and voltage in (4), the capacitor voltage can be expressed, where $V_c(t_0)$ is the initial capacitor voltage. With negligible ESR, as an alternative approach for solving differential equations, the capacitor/output voltage v_o can be approximated with a parabola in (5) based on its current i_c in the (3), where $V_{\rm ref}$ is for the output voltage reference

$$i_c(t) = C_o\frac{dv_c}{dt} \leftrightarrow v_c(t) = V_c(t_0) + \frac{1}{C_o}\int_{t_0}^{t} i_c \cdot dt \tag{4}$$

$$\begin{aligned} v_o(t) = v_c(t) &= V_{\rm ref} + \frac{1}{C_o}\int_{t_0}^{t} i_c dt \\ &= V_{\rm ref} + \frac{m_2}{2C_o}T_1^2 - \frac{m_2}{2C_o}(t-t_1)^2. \end{aligned} \tag{5}$$

2) Step 2: Time Interval T_2 $(t_1 \le t < t_2)$ for an Unloading Step Transient: During this interval, the top MOSFET is still off. So the capacitor current follows the same slew rate as Step 1. When the inductor current i_L reaches the new steady-state load current I_{o2} at t_1, the output voltage v_o reaches its peak value, $V_{\max}$. Similarly, the capacitor current i_c can be expressed in (6), and the instantaneous output voltage v_o will be able to be computed in (7) based on the voltage $V_{\max}$ at t_1 as initial value of this period

$$i_c(t)|_{t_1-t_2} = -m_2(t-t_1) = -\frac{V_o}{L_o}(t-t_1) \tag{6}$$

$$\begin{aligned} v_o(t) &= V_{\max} + \frac{1}{C_o}\int_{t_1}^{t} i_c dt \\ &= V_{\max} - \frac{m_2}{2C_o}(t-t_1)^2. \end{aligned} \tag{7}$$

According to (7), the output voltage at t_2, called switching point voltage (SPV, $V_{\rm sw}$) in this paper, is expressed in (8)

$$V_{\rm sw} = v_o\left(t_2\right) = V_{\max} - \frac{m_2}{2C_o}\left(t_2 - t_1\right)^2 = V_{\max} - \frac{m_2}{2C_o}T_2^2. \tag{8}$$

3) Step 3: Time Interval T_3 $(t_2 \le t \le t_3)$ for an Unloading Step Transient: The top MOSFET of the Buck converter is turned on at t_2. The capacitor current increases linearly. Referring to the rising slope of the inductor current m_1 [i.e., $m_1 = (V_{in} - V_o)/L_o$] in this interval, the capacitor current can be written as (9) and the time intervals T_2 and T_3 will follow the relationship expressed in (10)

$$i_c\left(t\right)|_{t_2-t_3} = m_1\left(t - t_3\right) = \frac{V_{in} - V_o}{L_o}\left(t - t_3\right) \tag{9}$$

$$\frac{T_2}{T_3} = \frac{m_1}{m_2} = \frac{V_{in} - V_o}{V_o}. \tag{10}$$

The instantaneous output voltage v_o can be calculated in (11) based on the capacitor current i_c information in (9), where $V_{\rm sw}$ is the initial value at t_2 in this interval

$$\begin{aligned} v_o\left(t\right) &= V_{\rm sw} + \frac{1}{C_o}\int_{t_2}^{t} i_c\left(t\right)|_{t_2-t_3}\cdot dt \\ &= V_{\rm sw} + \frac{m_1}{2C_o}\left(t^2 + 2t_2t_3 - t_2^2 - t_3t\right). \end{aligned} \tag{11}$$

According to the (11) and the zoomed figure in Fig. 1, the output voltage at t_3 can be calculated in (12) and the inductor current is reaching the new load current level at the same time

$$v_o\left(t_3\right) = V_{\rm sw} + \frac{m_1}{2C_o}\left(-t_3^2 + 2t_2t_3 - t_2^2\right) = V_{\rm sw} - \frac{m_1}{2C_o}T_3^2. \tag{12}$$

In the zoomed figure, at t_3', the output voltage reaches the reference voltage $V_{\rm ref}$ and can be calculated in (13) based on (11), where D represents the steady-state duty ratio

$$v_o\left(t_3'\right) = V_{\rm ref} = V_{\rm sw} - \frac{1}{2C_o}m_1\left[T_3^2 - \left(\frac{1}{2}DT_{\rm sw}\right)^2\right]. \tag{13}$$

So the SPV voltage $V_{\rm sw}$ can be calculated using (14), where the symbol $T_{\rm sw}$ represents the switching period

$$V_{\rm sw} = \frac{1}{2C_o}m_1\left[T_3^2 - \left(\frac{1}{2}DT_{\rm sw}\right)^2\right] + V_{\rm ref}. \tag{14}$$

Without sacrificing the accuracy of the algorithm a lot, especially when the switched-mode power supply operates at a high frequency ($>$ 100 kHz) and narrow duty ratio (12–1.5 V), the item $(1/2{}^*DT_{\rm sw})^2$ can be neglected in the (14). For example, in the experiment, T_3^2 is about 40 times larger than $(1/2{}^*DT_{\rm sw})^2$. And (15) is obtained

$$V_{\rm sw} = \frac{1}{2C_o}m_1T_3^2 + V_{\rm ref}. \tag{15}$$

Therefore, the voltage $V_{\rm sw}$ can be expressed as (16) by substituting the (10) into (15)

$$V_{\rm sw} = \frac{m_2}{m_1}\cdot\frac{m_2}{2C_o}T_2^2 + V_{\rm ref} = \frac{m_2}{m_1}\left(V_{\max} - V_{\rm sw}\right) + V_{\rm ref}. \tag{16}$$

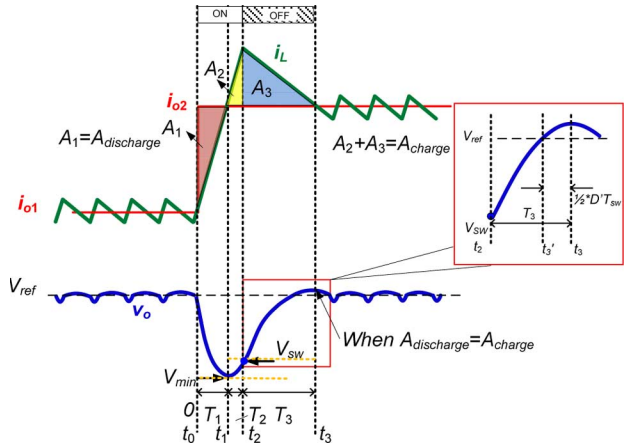

Fig. 2. Capacitor charge integral areas during a loading step transient.

After that, the $V_{\rm sw}$ can be solved by moving $V_{\rm sw}$ terms on both sides of the (16) to one side. The intermediate result is shown in the (17)

$$V_{\rm sw} = \frac{\frac{m_2}{m_1}V_{\max} + V_{\rm ref}}{1 + \frac{m_2}{m_1}}. \tag{17}$$

After substitute (10) into (17) and make a simplification, the final equation for calculating $V_{\rm sw}$ is expressed in (18)

$$V_{\rm sw} = DV_{\max} + \left(1 - D\right)V_{\rm ref}. \tag{18}$$

In (18), only coefficient multiplications and additions are required based on the steady-state duty cycle D and voltage information $V_{\max}$ and $V_{\rm ref}$. Therefore, SPV can be simply calculated by low cost MCU in about 10 system clock cycles. It is also worth noting that since neither inductance nor capacitance occurs in the equation, the robustness of the proposed algorithm is significantly enhanced.

However, to implement (18), the peak voltage information $V_{\max}$ is required. Therefore, an analog extreme voltage detector is employed in this paper to locate the voltage peak at time instant t_1, which is discussed in details in Section V-A.

B. V-CBC Equation for a Buck Converter Undergoing a Loading Step Transient

A similar analysis as was performed in Section III-A can be carried out for a loading step transient based on Fig. 2.

During the time intervals $t_0 - t_2$ and $t_2 - t_3$, the capacitor current can be expressed as a linear function in (19) and (20), respectively

$$i_c\left(t\right)|_{t_0-t_2} = m_1\left(t - t_1\right) \tag{19}$$

$$i_c\left(t\right)|_{t_2-t_3} = -m_2\left(t - t_3\right). \tag{20}$$

Based on the simplified differential equations, the voltage $V_{\rm sw}$ can be calculated using (21), while the (22) provides the formula for voltage $V_{\min}$

$$V_{\rm sw} = V_{\rm ref} - \frac{1}{2C_o}m_2\left[T_3^2 - \left(\frac{1}{2}D'T_{\rm sw}\right)^2\right] \tag{21}$$

$$V_{\min} = V_{\rm sw} - \frac{1}{2C_o} m_1 T_2^2. \quad (22)$$

Similarly, the item $(1/2^*D'T_{\rm sw})^2$ can be ignored in the (21), where $D' = 1 - D$. Therefore, the voltage $V_{\rm sw}$ can be derived as (23), where $m_1/m_2 = (V_{in} - V_o)/V_o = T_3/T_2$. According to the voltage $V_{\rm sw}$, we can change the main switch state from on-state to off-state at t_2. By combining (21) and (22), the SPV can be expressed in (23), in which neither inductor nor capacitor value is required

$$V_{\rm sw} = V_{\rm ref} + \frac{m_2 (V_{\max} - V_{\rm sw})}{m_1} = DV_{\rm ref} + (1-D)V_{\min}. \quad (23)$$

C. Regarding Assumptions Involving m_1 and m_2

It is noted that m_1 and m_2 will not remain constant in actual condition during a load transient due to the varying output voltage. This simplification was made in order to allow for a practical implementation of a charge balance controller. For this reason, it is claimed that the controller can only yield a "near-optimal" transient response. However, the simplification does not degrade the performance significantly due to the following reasons:

i) For a low duty ratio Buck (e.g., 12–1.5 V), the undershoot (due to a loading step) will be much smaller than the overshoot (due to an unloading step transient). Thus, for a properly designed Buck, the output voltage deviation during a load transition would be very small.

ii) For an unloading step transient, the output voltage can vary significantly (typically 10% of the steady-state voltage). However, since the SPV is determined by the D and $(1-D)$ in (18), for example, a single phase 12–1.5 V Buck converter with 1 μH output inductance and 180 μF output capacitance, under 10 A step-down load transient the overshoot will be about 0.2 V, and the exact SPV $V_{\rm sw}$ is 1.528 V considering varying duty cycle, however, using constant duty ratio D, the calculated $V_{\rm sw}$ is 1.525 V, causing a very small error of 3 mV.

D. Regarding Assumptions Involving Ignored ESR in the Output Capacitor

Based on the parabolic curve analysis proposed in [4], the output voltage of a Buck converter can be expressed as a parabola function of time, even when we take the ESR of the output capacitor into account. In Fig. 3, ideal output voltage (solid curve) and nonideal voltage with ESR (dashed curve) are shown. The following conclusions in [4] remain valid: 1) the ideal and nonideal output waveforms are parabolic curves with the same quadratic term coefficient; 2) the ideal waveform and nonideal waveform intersects at $(t_1, V_{\max})$; 3) the leading time t_{ESR}, of nonideal curve caused by ESR, equals the product of ESR and output capacitance C_o (i.e., ESR^*C_o); and 4) the initial value of nonideal output voltage, V_{ESR} equals the product of ESR and the load step ΔI_o (i. e $ESR^*\Delta I_o$). Using (7), the voltage difference/error between ideal curve

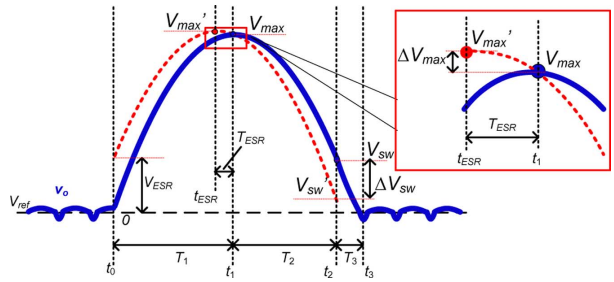

Fig. 3. Impact of output capacitor ESR on the output voltage.

peak voltage $V_{\max}$ and nonideal curve peak voltage $V_{\max}$' can be expressed in (24) for unloading transient cases

$$\Delta V_{\max} = V'_{\max} - V_{\max} = \frac{m_2}{2C_o} (ESR \cdot C_o)^2. \quad (24)$$

Similarly, for loading transient cases, the formula can be found in (25)

$$\Delta V_{\min} = \frac{m_1}{2C_o} (ESR \cdot C_o)^2. \quad (25)$$

Using the same design example in Section V-C and choose $ESR = 0.5$ mΩ. The error $\Delta V_{\max}/\Delta V_{\min}$ in both of the transient cases will be less than 1 mV.

Further applying the curve analysis, the SPV difference/error $\Delta V_{\rm sw}$ between ideal and nonideal curves can be expressed in (26), for unloading transient cases

$$\Delta V_{\rm sw} = V_{\rm sw} - V'_{\rm sw} = \frac{m_2}{2C_o} \left[(T_2 + ESR \cdot C_o)^2 - T_2^2 \right] + \Delta V_{\max}. \quad (26)$$

Similarly, for loading transient cases, the formula can be found in (27)

$$\Delta V_{\rm sw} = \frac{m_1}{2C_o} \left[(T_2 + ESR \cdot C_o)^2 - T_2^2 \right] + \Delta V_{\min}. \quad (27)$$

Using the same design example in Section III-C, the error $\Delta V_{\rm sw}$ will be about 1.3% (2 mV) for 10 A loading case and 3.1% (4.7 mV) for 10 A unloading case. So the proposed algorithm derived in Sections III-A and III-B offers very good accuracy under the ideality assumptions.

IV. Application Extensions of the Proposed MCU Based V-CBC Controller

In addition to the application of optimizing the load step transients discussed in the previous sections, the proposed controller can be extended for adaptive voltage positioning technique with small modifications. In this case, inductor current sensing is required for load line regulation.

Adaptive voltage positioning (also known as Load-line regulation) has increasingly become a requirement in many Buck converter applications, for example, Intel's CPU VRs. Load-line regulation essentially involves outputting lower voltages during higher load current conditions. This assists in improving the overall transient performance of the converter along while decreasing power consumption of the load device.

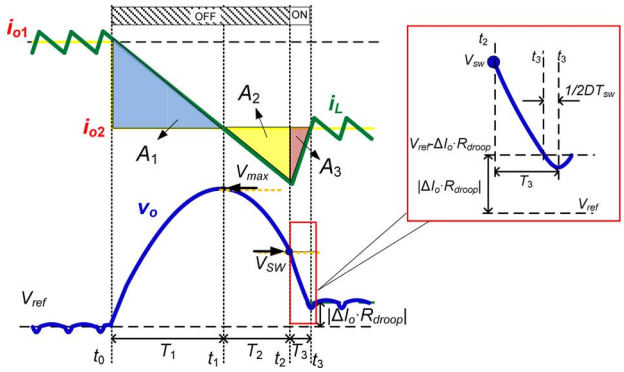

Fig. 4. Inductor current and capacitor voltage waveforms for AVP applications under unloading step transient case (R_{droop}: droop resistance).

The proposed MCU based V-CBC controller can be applied to AVP operation with two minor modifications, (a) adding inductor current sensing and (b) one more ADC channel to the MCU. In this section, the analysis will be conducted and the implementation modification will be discussed in the Section V-B

It is observed in Fig. 4, for AVP application, the difference of operation is in the interval $t_1 - t_3$. At time instant t_3, instead of recovering the output voltage to $V_{\rm ref}$, the AVP controller maintains the new steady-state output voltage depending on the load line at $V_{\rm ref} - \Delta I_o \cdot R_{\rm droop}$.

Similarly, the switching point voltage $V_{\rm sw}$ can be calculated in (28) by referring the parabolic curve during $t_1 - t_2$ in (7)

$$V_{\rm sw} = V_{\rm max} - \frac{m_2}{2C_o} T_2^2. \tag{28}$$

Considering the new adaptive voltage positioning level, the switching point voltage $V_{\rm sw}$ can also be expressed during $t_2 - t_3$. And, as previously discussed, the term $(1/2^* DT_{\rm sw})^2$ can be ignored in (29) when the Buck converter is operated at high switching frequency and narrow output duty ratio

$$V_{\rm sw} = \frac{1}{2C_o} m_1 \left[T_3^2 - \left(\frac{1}{2} DT_{\rm sw} \right)^2 \right] + \left(V_{\rm ref} - R_{\rm droop} \cdot \Delta I_o \right). \tag{29}$$

By substituting (28) into (29), the switching point voltage $V_{\rm sw}$ can be calculated in (30)

$$V_{\rm sw} = DV_{\rm max} + (1 - D) \left(V_{\rm ref} - R_{\rm droop} \cdot \Delta I_o \right). \tag{30}$$

It is noted from the (30) and (18), we can simply replace the voltage $V_{\rm ref}$ with the new load line voltage at $V_{\rm ref} - \Delta I_o \cdot R_{\rm droop}$. In the same way, the switching point voltage under loading step transient is able to be expressed in (31).

$$V_{\rm sw} = D \left(V_{\rm ref} - R_{\rm droop} \cdot \Delta I_o \right) + (1 - D) V_{\rm min}. \tag{31}$$

V. Hardware Implementation Diagram of the Proposed Digital Control System

The high-level system diagram of the digital charge balance controller for a synchronous Buck converter is illustrated in Fig. 5.

A. Extreme Voltage Detector Design (for t_1 Detection)

Because of the current sensor mismatching [14], [19], noise, ADC cost and accuracy issue [7], [8], [10]–[13] as mentioned above, a practical extreme voltage detector is used in this paper to detect t_1 and above all, to sample the peak/valley voltage $V_{\rm max}/V_{\rm min}$. In Fig. 6, for example, during an unloading step transient, the output voltage overshoot is delayed with a period of time $t_{\rm delay}$, and represented as $v_{o\_{\rm delay}}$. This delay can be equalized with first-order OPAMP circuit based on *Padė* Approximation [30] in Fig. 6. Then, both v_o and $v_{o\_{\rm delay}}$ will be fed to a comparator. The delay time, $t_{\rm delay}$ and the error voltage $v_{\rm err}$ is related to each other. Based on a selected $t_{\rm delay}$, the $v_{\rm err}$ can be estimated and thus the comparator hysteresis can be set. In this way, as soon as the voltage difference between the original voltage and the delayed voltage reaches $v_{\rm err}$ (set by the hysteresis of the comparator), the comparator output will change from low to high and t_1 is detected. The rising edge is used to trigger the ADC to sample the output voltage and therefore, $V_{\rm max}$ can be obtained.

In Fig. 7, an adjustable delay circuit is synthesized based on the *Padė* approximation (32)

$$\frac{v_{o\_{\rm delay}}}{v_o} = e^{-\tau s} \approx \frac{1 - \frac{\tau s}{2}}{1 + \frac{\tau s}{2}} = \frac{1 - R_T C_T s}{1 + R_T C_T s}. \tag{32}$$

In this circuit, the delay time constant τ can be adjusted by the product of R_T and C_T (i.e., $\tau = 2R_T \cdot C_T$). And the inserted delay time $t_{\rm delay}$ can be compensated to a certain acceptable degree, with the help of the lead time (provided by ESR and equals $ESR^* C_o$ [5]) and comparator hysteresis configuration (which can adjust the $v_{\rm err}$ band in Fig. 6). Therefore, the output comparator is connected with a hysteresis configuration and the one with latched output function is more preferred for blanking steady-state comparison "noise", such as TL3016 (TI Company) [28]. For example, for unloading transient case shown in Fig. 6, R_T and C_T can be chosen to be 500 Ω and 330 pF, so that a delay time $\tau = 330$ ns can be implemented. According to the parabolic function derived in (7), the voltage difference $v_{\rm err}$ in Fig. 6 can be estimated in this design, which is about 2 mV. The hysteresis can be adjusted to the same voltage as $v_{\rm err}$ by choosing for example $R_{hf} = 500$ kΩ and $R_{hi} = 1$ kΩ, so that the inserted delay time τ can be compensated. On the contrary, if ADC is used to implement the same functionality, a 10 bit asynchronous ADC with 2 mV resolution or a high speed 3.3 MHz synchronous ADC is required, resulting in higher cost and power consumption.

B. Signal Conditioning Circuitry Design Guidelines

A single dual-channel analog-to-digital converter (ADC) is employed to sample output voltage error $v_{\rm err\_AD}$ and the inductor current $i_{\rm L\_AD}$. The inductor current measurement information is only used to implement the extension for AVP technique [5]. As shown in Fig. 5, the inductor current is reconstructed by matching the corner frequency of the low-pass filter with that of the inductor based on (33) to filter the voltage across the output inductor

$$R_{2_{\rm iLsens}} \cdot C_{\rm iLsens} = \frac{L_o}{R_L}. \tag{33}$$

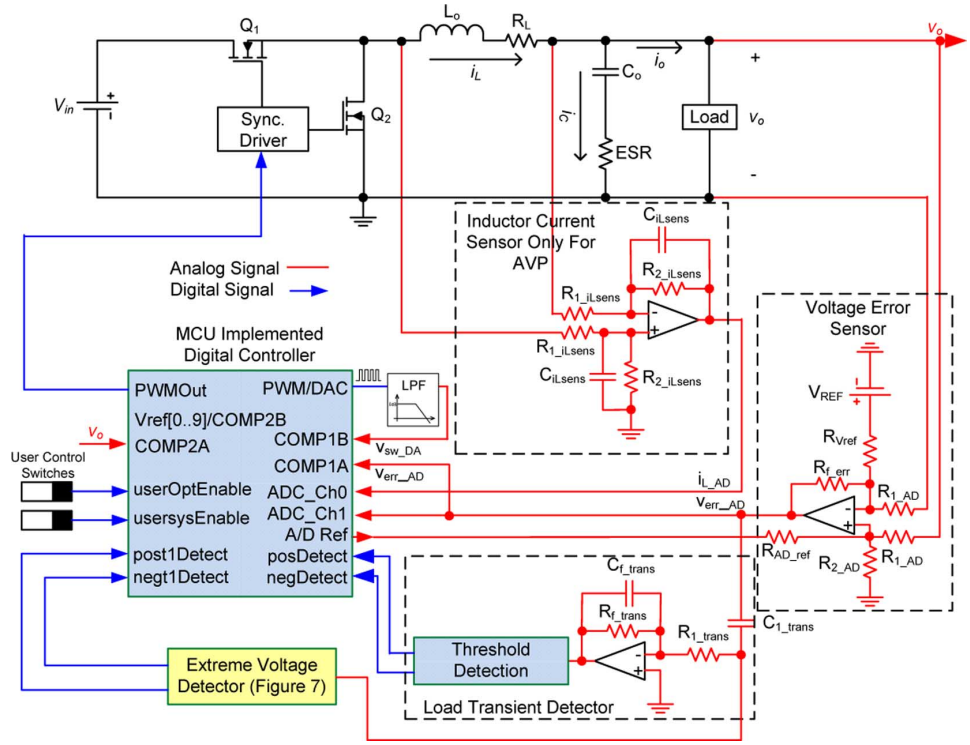

Fig. 5. Hardware implementation diagram of the digital control system.

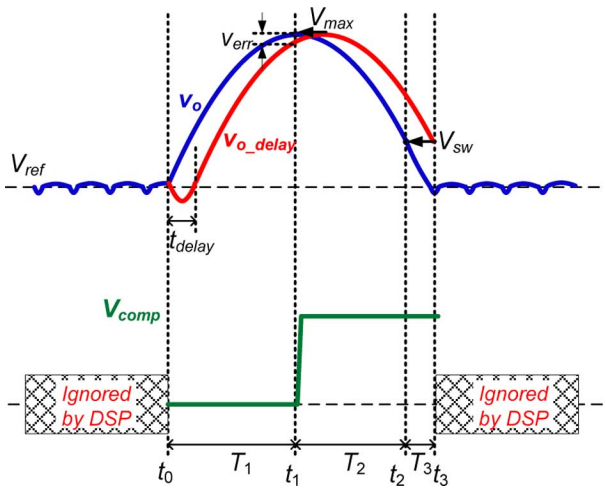

Fig. 6. Illustration of the proposed analog extreme voltage detector under unloading step transient case for t_1 detection and $V_{\max}$ sensing.

The output of the inductor current sensor $i_{\mathrm{L\_AD}}$, in relation to the inductor current i_L is equated in (34)

$$i_{L_{\mathrm{AD}}} = R_L \cdot \frac{R_{2\_\mathrm{iLsens}}}{R_{1\_\mathrm{iLsens}}} \cdot i_L. \tag{34}$$

Therefore, the selection of $R_{2\_\mathrm{iLsens}}/R_{1\_\mathrm{iLsens}}$ should be based on the maximum expected inductor current and the conversion range of the ADC.

The output voltage error $v_{\mathrm{err\_AD}}$ is calculated in the analog domain through use of the OPAMP configuration illustrated in Fig. 5. As will be discussed, the output of the voltage error sensor is used for steady-state operation, and transient detection during a load transient. The output of the voltage error sensor is calculated in (35)

$$v_{\mathrm{err}_{\mathrm{AD}}} = R_{f\_\mathrm{err}} \cdot \left(\frac{v_o}{R_{1\_\mathrm{AD}}} + \frac{V_{\mathrm{AD\_ref}}}{R_{\mathrm{AD\_ref}}} - \frac{V_{\mathrm{ref}}}{R_{\mathrm{Vref}}} \right). \tag{35}$$

V_{AD_ref} represents the upper bound of the ADC conversion range. $R_{f\_\mathrm{err}}/R_{1\_\mathrm{AD}}$ and $R_{f\_\mathrm{err}}/R_{V\_\mathrm{ref}}$ should be equal and selected based on the desired gain of $v_{\mathrm{err\_AD}}$. To level-shift the error voltage to the centre of the ADC conversion range, $R_{f\_\mathrm{err}}/R_{\mathrm{AD\_ref}} = 1/2$. R_{2_AD} should be selected based on (36)

$$R_{2\_\mathrm{AD}} = \frac{R_{f\_\mathrm{err}}}{1 + \frac{R_{f\_\mathrm{err}}}{R_{V\_\mathrm{ref}}} - \frac{R_{f\_\mathrm{err}}}{R_{AD\_\mathrm{Ref}}}}. \tag{36}$$

C. Load Transient (t_0) Detector, t_2 Detector, and t_3 Detector

As illustrated in Fig. 5, the output of the voltage error sensor is also fed into a trans-impedance amplifier configuration. The trans-impedance amplifier is used to asynchronously detect load transients. The trans-impedance amplifier and threshold levels can be designed similar to [19]; however, since the output is not used to determine the capacitor zero cross-over point t_1, it is not necessary to precisely match the C_o and ESR time constant of the output capacitor. In addition, a capacitor C_{f_trans} can be added in parallel with the feedback resistor to attenuate high-frequency noise.

The calculated digital value V_{sw} in (18) and (23) is converted to analog signal by using a high resolution PWM (HRPWM) [32] port as a digital analog converter (DAC) [31]. The HRPWM frequency is set to be 7.5 MHz and the equivalent

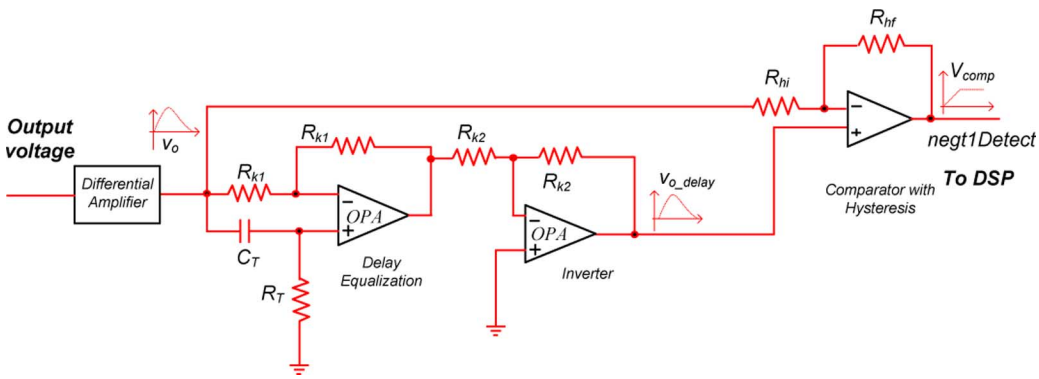

Fig. 7. Hardware implementation of the detector based on the adjustable delay circuit.

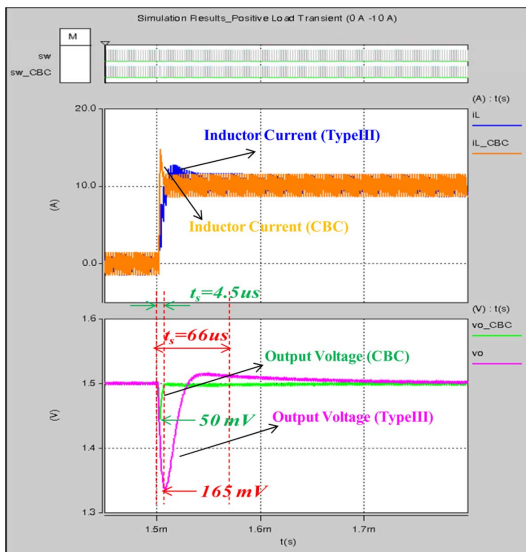

Fig. 8. Simulation results of loading step transient case for comparison between V-CBC and linear mode of controller $(0\ \mathrm{A} \rightarrow 10\ \mathrm{A})$.

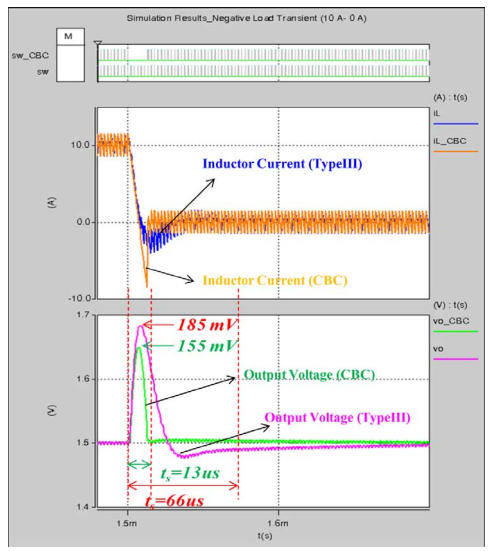

Fig. 9. Simulation results of unloading transient case for comparison between V-CBC and linear mode of controller $(10\ \mathrm{A} \rightarrow 0\ \mathrm{A})$.

PWM resolution is 9 bit [29]. A second order low-pass filter with crossover frequency at around 750 kHz is used to smooth the HRPWM signal. The integrated comparator COMP1 will compare $v_{\mathrm{sw\_DA}}$ (COMP1B) with the amplified output voltage $v_{\mathrm{err\_AD}}$ (COMP1A) to determine time instant t_2 and the Buck converter switch will change the ON/OFF state.

The time instant t_3 when the output voltage recovers to V_{ref} will be detected by using another integrated comparator COMP2 in the MCU. The voltage reference $V_{\mathrm{ref}}[0..9]$ from an internal 10 bit DAC [33] is fed to COMP2B. The output voltage (COMP2A) compares with the 10 bit DAC reference (COMP2B). When COMP2 outputs falling edge, CBC is achieved at t_3 and the PID controller will take over the output voltage regulation.

VI. Simulations and Experimental Verifications

A. Simulation Results

In order to verify the functionalities of the proposed optimal algorithm, a dc-dc Buck converter undergoing load step transient conditions is simulated. The design parameters are listed as follows: input voltage $V_{in} = 12$ V, output voltage $V_o = 1.5$ V, switching frequency $f_s = 350$ kHz, output inductance $L_o = 1\ \mu$H, DCR $R_L = 1\ \mathrm{m}\Omega$, output capacitor $C_o = 180\ \mu$F, $ESR = 0.5\ \mathrm{m}\Omega$, $ESL = 100$ pH.

As comparison, a well-designed digital PID controller (bandwidth: ≈ 40 kHz, Phase margin $\approx 60^\circ$) is also simulated for regulating the dc-dc buck converter shown in Figs. 8 and 9. The PWM signal is shown for the comparison between proposed V-CBC controller (sw_CBC) and linear voltage mode controller (sw) in the top section. The inductor current (i_L) and output voltage waveforms (v_o) are also demonstrated with two types of controllers shown on the bottom sections.

To sum up, under the load transient cases, for loading step, the proposed controller improves the dynamic performance by reducing the undershoot (by 70%) and settling time (by 93%), compared to the conventional voltage mode control. While, under unloading transient, the overshoot is reduced by 16% and settling time is shortened by 80% with the help of the proposed MCU based V-CBC controller.

B. Prototype Design and Experimental Results

A 12 V–1.5 V prototype shown in Fig. 10 is designed using the same parameters in the simulation and a fixed-point 32-bit

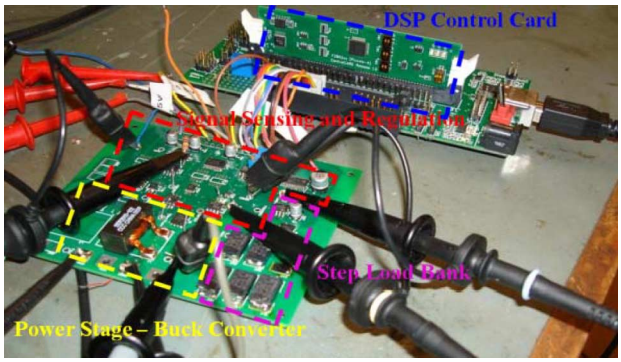

Fig. 10. Experimental prototype of the proposed V-CBC controlled dc-dc Buck converter.

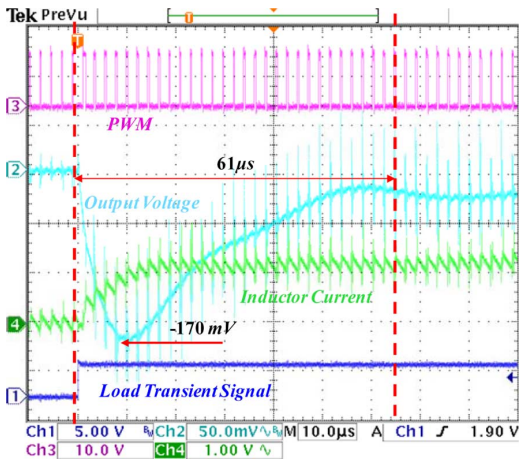

Fig. 11. Experimental results of Buck converter under loading step transient case 0 A- 10 A using linear mode controller.

MCU TMS320F28027 [29] is employed to implement the proposed V-CBC control algorithm. Figs. 11–14, show comparative results for a Buck converter undergoing load step transients using conventional voltage mode controller and proposed MCU based V-CBC controller. The voltage detector signal is shown for time detection of t_1. In order to illustrate the operation of the V-CBC controller, the charge balance control intervals have been shown in the figures.

Experimental results, shown in Figs. 11 and 13, demonstrate the transient performance of conventional linear voltage mode controller (bandwidth: ≈ 40 kHz, Phase margin $\approx 60°$) under the load current step change between no load (0 A) and full load (10 A). Limited by the bandwidth, the linear voltage mode controller will cause larger voltage variations and longer recovery time. For loading step transient, the voltage undershoot is about -170 mV with 61 μs settling time, while, the overshoot is about 185 mV with 56 μs settling time.

It is demonstrated, under a 10 A loading step transient, the settling time is reduced from 61 μs (using voltage mode controller) to 3.5 μs (using CBC). In other words, the settling time of the Buck converter with CBC is shortened by 94.3% compared to that of the voltage mode controlled Buck converter. And the experimental result is in close correspondence of the calculated settling time (4 μs) and the simulation result (3.5 μs). Also, it is shown in that voltage undershoot is reduced from -170 mV

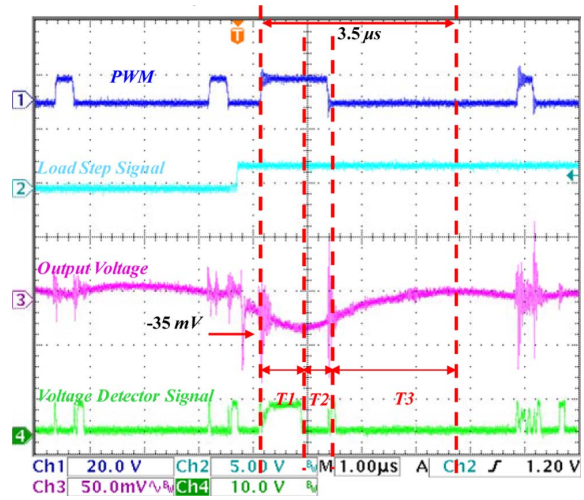

Fig. 12. Experimental results of Buck converter under loading step transient case 0 A- 10 A using V-CBC controller.

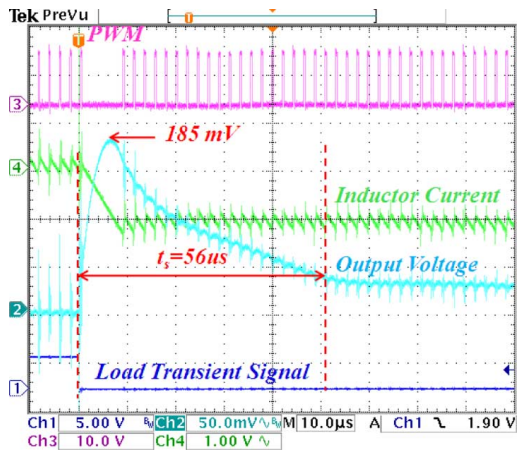

Fig. 13. Experimental results of Buck converter under unloading step transient case 10 A- 0 A using linear mode controller.

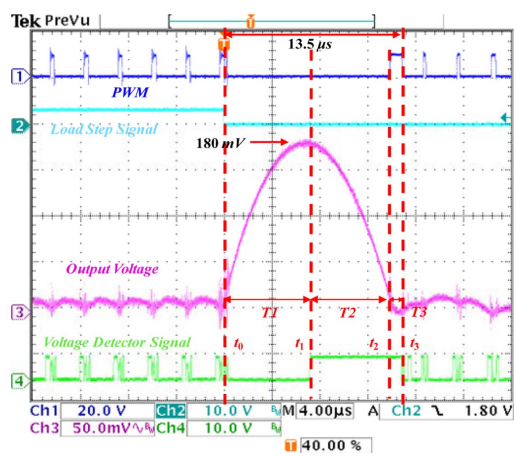

Fig. 14. Experimental results of Buck converter under unloading step transient case 10 A- 0 A using V-CBC controller.

(using the linear controller) to -35 mV (using CBC). The undershoot of the Buck converter with CBC controller is reduced by 79.4% compared to that of the voltage mode controller Buck converter. And the -35 mV undershoot is accordance with the

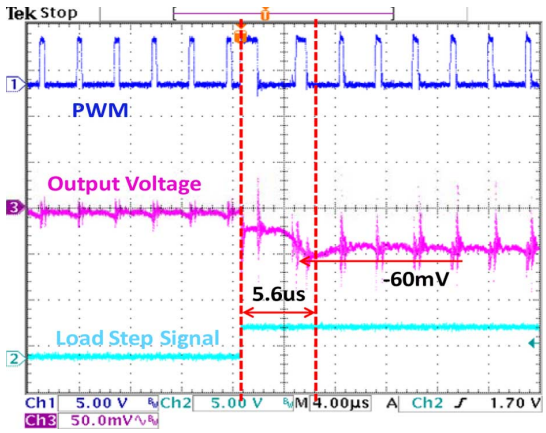

Fig. 15. Experimental result of 10 A loading step transients under AVP operation using proposed V- CBC controller.

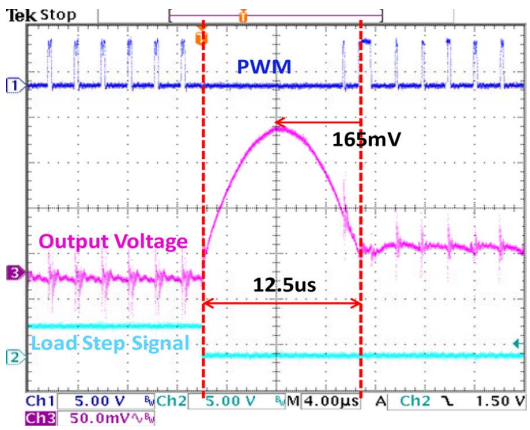

Fig. 16. Experimental result of 10 A unloading step transients under AVP using proposed V- CBC controller.

calculated undershoot $(-25\ \mathrm{mV})$ and the simulated undershoot $(-35\ \mathrm{mV})$.

Figs. 13 and 14 show a voltage mode controlled Buck converter and the CBC controlled Buck converter undergoing a $10\ \mathrm{A} \rightarrow 0\ \mathrm{A}$ load step change, separately.

It is demonstrated, under a 10 A unloading step transient, the settling time is reduced from 56 μs (using voltage mode controller) to 13.5 μs (using CBC). In other words, the settling time of the Buck converter with CBC is shortened by 75%, compared to that of the voltage mode controlled Buck converter. And the experimental result is in close correspondence of the calculated settling time (14 μs) and the simulation result (14.5 μs).Also, it is shown that voltage overshoot is only reduced from 185 mV (using the linear controller) to 180 mV (using CBC) based of the narrow operating output ratio at 12 –1.5 V. But the 180 mV overshoot is accordance with the calculated undershoot (185 mV) and the simulated (185 mV).

Using the same prototype setup, the adaptive voltage positioning technique is applied to the V-CBC controller with simple modification on top of the nonAVP V-CBC scheme. And in the experimental results shown in Figs. 15 and 16, the droop resistance is selected to be $5\ \mathrm{m}\Omega$. It is demonstrated that, for a 10 A loading step transient, the undershoot is $-10\ \mathrm{mV}$ at $-50\ \mathrm{mV}$ AVP regulation. And the settling time is 5.6 μs. The experimental result in Fig. 16 demonstrates that the overshoot is 115 mV above the AVP regulation level of 50 mV (165 mV in total). The settling time using AVP technique is within 25 us [33]. For higher current step for computer CPU voltage regulator, multiphase buck convertor with equivalently lower inductance and higher capacitance will be desired to further reduce the overshoot and settling time.

VII. Conclusions

In this paper, a voltage sensing based charge balance control algorithm is proposed to optimize the response of Buck converters without relying on LC filter parameters. An extreme voltage detector (based on delay equalization) is employed to detect the critical time instant t_1, when output voltage peak/valley appears. Switching point voltage concept is applied to determine the time instant to switch over the ON/OFF state of the MOSFET in the Buck converter. The proposed V-CBC controller algorithm is derived based on output voltage curve analysis. Simulation model and hardware prototype of a synchronous 12 V–1.5 V Buck converter have been made. It is demonstrated through simulations and experimental results, that the proposed MCU based V-CBC controller can be implemented for low-ESR designed Buck converter to optimize the transient response performance. Through the comparison experiments, under the load transient cases, for loading step, the voltage undershoot is suppressed by 79% and settling time is improved by 94%, while, for unloading step, the converter overshoot is reduced by 3% and settling time is shortened by 76%. Also, the robustness enhancement of the proposed algorithm is discussed and demonstrated.

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