# Adaptive Continuous Current Source Drivers for 1-MHz Boost PFC Converters

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***Abstract*—Recently, current source drivers (CSDs) have been proposed to reduce the switching loss and gate drive loss in megahertz (MHz) dc–dc converters, in which the duty cycle normally has a steady-state value. However, different from dc–dc converters, the duty cycle of the power factor correction (PFC) converters is modulated fast and has a wide operation range during a half-line period in ac–dc applications. In this paper, an adaptive full-bridge CSD is proposed for the boost PFC converters. The proposed CSD can build adaptive drive current inherently depending on the drain current of the main power MOSFET. Compared to the CSDs with the constant drive current, the advantage of the adaptive drive current is able to reduce the switching loss further when the MOSFET is with a higher switching current, while minimize the drive circuit loss when the MOSFET is with a lower switching current. Therefore, the adaptive CSD is able to realize better design trade-off between the switching loss and drive circuit loss so that the efficiency can be optimized in a wide operation range. Furthermore, no additional auxiliary circuit and control are needed to realize the adaptive current by the proposed CSD. The experimental results verified the functionality and advantages. For a 1-MHz/300-W boost PFC converter, the proposed CSD improves the efficiency from 89% using a conventional voltage driver to 92.2% (an improvement of 3.2%) with 110 $V_{ac}$ input, 380 V output, and full-load condition.**

***Index Terms*—Boost converter, current source driver (CSD), megahertz (MHz) switching frequency, power MOSFET, power factor correction (PFC).**

## I. Introduction

RESONANT gate drivers (RGDs) are proposed to reduce the gate drive loss of the synch FETs at high frequency (>1 MHz), i.e., $CV^2$ loss associated with the conventional voltage source driver (VSD), in voltage regulators (VRs) applications [1]–[3]. High-efficiency RGDs were proposed for a zero-voltage switching (ZVS) full-bridge (FB) converter and an H-bridge structure based on the GaN devices for a high-power application and the drive loss was reduced by the factor of 10 [4], [5]. Some self-oscillating RGDs (also called soft gating drivers) have been applied to very high frequency (VHF) dc/dc conversions to minimize excessive MOSFET driving loss [6], [7]. Compared to the RGDs, current source drivers (CSDs) can not only recover the excessive gate drive loss, but also reduce the dominant switching losses in hard switching converters. The idea of the CSD circuit is to build a current source (CS) to charge and discharge the power MOSFET gate capacitance so that fast switching speed and reduced switching loss can be achieved. Owing to the CS inductor, the energy stored in the gate capacitance of the MOSFETs can be also recovered, similarly to the RGDs.

Depending on the current types of the CS inductor, the CSD topologies can be categorized as continuous and discontinuous. A low-side and high-side CSD using a coupled inductor was proposed for a synchronous buck VR in [8] and [9]. To eliminate the coupled inductor, a dual-channel CSD with a continuous CS current using a bootstrap technique was proposed in [10] and [11] to achieve the switching loss reduction and gate energy recovery of the synch FETs. Its improved version was presented to optimize the performance of the control FET and synch FET independently in [12]. Similar CSD structure is also applied to the interleaving boost converter for PV applications in [13]. In order to reduce the circulating current and the CS inductance value, the CSDs with the discontinuous current and lower inductance were proposed in [14]–[17]. To overcome the current diversion problem, the blocking diode is introduced to the CSDs and the fast switching capability is further improved in [18] and [19]. However, these CSDs can only provide constant drive current and this may result in lower efficiency when the switching current varies in wide range in PFC applications.

On the other hand, most of present work related to the CSDs is to investigate their applications in dc–dc converters, where the duty cycle normally has a steady-state value. In ac–dc applications, the power factor correction (PFC) technique is widely used. Different from dc–dc converters, the duty cycle of the PFC converters needs to be modulated fast and has a wide operation range. Normally, the switching loss is proportional to the switching current and the drain-to-source voltage. For a boost PFC converter, the input line current follows the input line voltage in the same phase. When the line voltage reaches the peak value of the power MOSFET, the line current also reaches the peak and so does the drain current (i.e., the switching current). This means that the switching loss reaches its maximum value at this moment. The key point here is that the switching current

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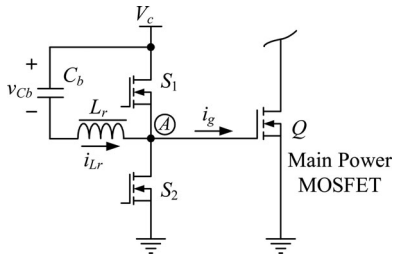


Fig. 1. HB CSD topology.

and thus the switching loss varies widely during a half-line period when the duty cycle modulates to realize unit power factor. Normally, high gate drive current leads to fast switching speed and thus lower switching loss, but results in high drive circuit loss. Therefore, in order to minimize the switching loss and gate drive loss in a wide range, the adaptive drive current is preferred to provide different drive capabilities according to the switching current and the drain voltage. Compared to the adaptive drive current, the gate voltage swing technique of the conventional voltage drivers was proposed to minimize the gate drive loss dynamically depending on load conditions [20].

The objective of this paper is to present a new CSD with the capability to build an adaptive drive current inherently depending on the switching current of the power MOSFET for a boost PFC converter. When the input voltage and current reach the peak value and the switching loss is high, the proposed CSD can provide a stronger drive current to reduce the switching loss further. On the other hand, when the input voltage and current are low, and as a result the switching loss is also low, the proposed CSD provides lower drive current to minimize the drive circuit loss. In this way, the proposed adaptive CSD improves the efficiency in a wide operation range for a boost PFC converter compared to other proposed CSDs previously. Section II presents the proposed CSD and its principle of operation. Section III presents the loss analysis and Section IV provides the procedure of optimal design. Section V contains the experimental results and discussion. Finally, Section VI provides a brief conclusion.

## II. Analysis of CSD Circuits and the Proposed Adaptive CSD for Boost PFC Converters

### A. Analysis of the Half-Bridge CSD

The basic CSD with the continuous inductor current is a half-bridge (HB) structure as shown in Fig. 1 [21]. It consists of two drive MOSFETs $S_1$ and $S_2$. $V_c$ is the drive voltage, $L_r$ is the CS inductor, and $C_b$ is the blocking capacitor. The voltage across the blocking capacitor $C_b$ is $v_{Cb} = (1 - D) \cdot V_c$, which varies with the duty cycle.

In the boost PFC converter, the duty cycle modulates fast with the input line voltage to shape the input current. Fig. 2 shows the simulated waveforms when the HB CSD is applied to a 100-kHz boost PFC converter under CCM. It is observed that the voltage over the blocking capacitor $v_{cb}$ oscillates with the duty cycle during the half-line period. This also leads to the oscillation of the gate drive current $i_{Lr}$ and the unreliable ON and OFF conditions of the power MOSFET. Therefore, the HB CSD circuit could hardly be suitable to the boost PFC converter with fast duty cycle modulation.

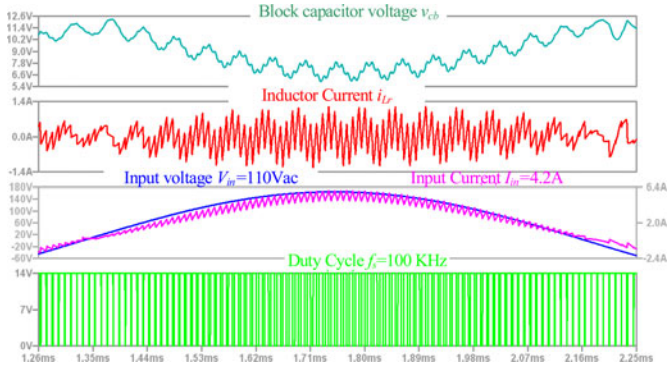


Fig. 2. Simulated waveforms of the boost PFC converter with the HB CSD.

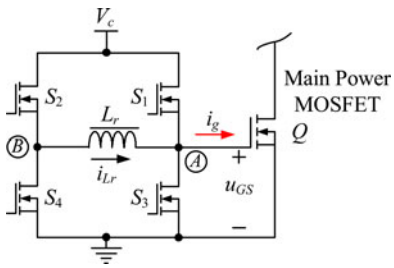


Fig. 3. Proposed CSD Solution for PFC applications.

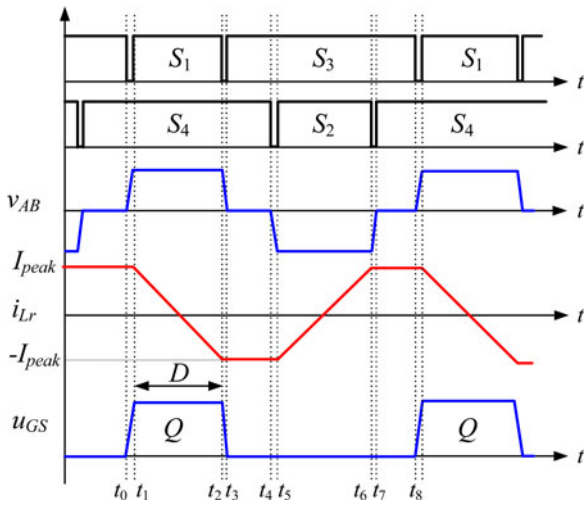


Fig. 4. Key waveforms.

### B. Proposed CSD for a Boost PFC Converter

Fig. 3 shows the proposed CSD circuit for the boost PFC converter. Compared to Fig. 1, $S_2$ and $S_4$ are used to remove the blocking capacitor $C_b$, which forms a FB CSD structure. Since there is no longer any blocking capacitor $C_b$, the proposed CSD can be suitable for the boost PFC converters with the modulated duty cycle. Fig. 4 shows the key waveforms. Fig. 5 shows the single-phase boost PFC stage with the CSD. As seen from Fig. 4,

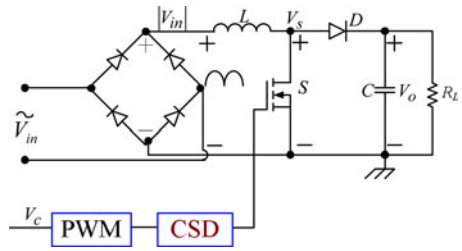


Fig. 5. Proposed CSD solution for the boost PFC converter.

$S_1$ and $S_3$, and $S_2$ and $S_4$ are controlled complementarily with dead time. This is similar to the control of the synchronous buck converters, so the commercial-off-shelf buck drivers can be directly used instead of the discrete components in other CSD circuits [10]–[12]. This much reduces the complexity of the control circuit and level shift circuits.

### C. Principle of Operation

There are eight switching modes in one switching period. The operation of principle is presented as follows. The equivalent circuits of operation are illustrated in Fig. 6. $D_1$–$D_4$ are the body diodes and $C_1$–$C_4$ are the drain-to-source capacitance of $S_1$–$S_4$, respectively. $C_{gs}$ is the gate-to-source capacitor of $Q$.

1) *Mode 1 [$t_0$, $t_1$] [see Fig. 6(a)]*: Prior to $t_0$, $S_3$ is ON and the gate of $Q$ is clamped to ground. At $t_0$, $S_3$ turns OFF and the peak value $I_{\rm peak}$ of the inductor current $i_{Lr}$ charges $C_3$ plus $C_{gs}$ and discharges $C_1$ simultaneously as a CS. Due to $C_1$ and $C_3$, $S_3$ achieves zero-voltage turnoff. The voltage of $C_3$ rises linearly and the voltage of $C_1$ decays linearly.
2) *Mode 2 [$t_1$, $t_2$] [see Fig. 6(b)]*: At $t_1$, the body diode $D_1$ conducts and $S_1$ turns ON with the zero-voltage condition. The gate-to-source voltage of $Q$ is clamped to $V_c$ through $S_1$. During this interval, $i_{Lr}$ decreases and changes its polarity from $I_{\rm peak}$ to -$I_{\rm peak}$.
3) *Mode 3 [$t_2$, $t_3$] [see Fig. 6(c)]*: At $t_2$, $S_1$ turns OFF and the negative peak value -$I_{\rm peak}$ charges $C_1$ and discharges $C_3$ plus $C_{gs}$ simultaneously as a CS. Due to $C_1$ and $C_3$, $S_1$ achieves zero-voltage turnoff. The voltage of $C_1$ rises and the voltage of $C_3$ decreases linearly.
4) *Mode 4 [$t_3$, $t_4$] [see Fig. 6(d)]:* At $t_3$, $D_3$ conducts and $S_3$ turns ON with the zero-voltage condition. The gate-to-source voltage of $Q$ is clamped to ground through $S_3$. The current path during this interval is $S_3$–$L_r$–$S_4$. $i_{Lr}$ circulates through $S_3$ and $S_4$ and remains constant in this interval.
5) *Mode 5 [$t_4$, $t_5$] [see Fig. 6(e)]*: At $t_4$, $S_4$ turns OFF and the negative peak current -$I_{\rm peak}$ charges $C_4$ and discharges $C_2$ simultaneously. Due to $C_2$ and $C_4$, $S_4$ achieves zero-voltage turnoff. The voltage of $C_4$ rises linearly and the voltage of $C_2$ decays linearly.
6) *Mode 6 [$t_5$, $t_6$] [see Fig. 6(f)]*: At $t_5$, $D_2$ conducts and $S_2$ turns ON with the zero-voltage condition. $i_{Lr}$ decreases from -$I_{\rm peak}$ and changes its polarity to $I_{\rm peak}$.
7) *Mode 7 [$t_6$, $t_7$] [see Fig. 6(g)]*: At $t_6$, $S_2$ turns OFF. The peak drive current $I_{\rm peak}$ charges $C_2$ and discharges $C_4$. The voltage of $C_2$ rises linearly and the voltage of $C_4$ decays linearly.
8) *Mode 8 [$t_7$, $t_8$] [see Fig. 6(h)]*: At $t_7$, $D_4$ conducts and $S_4$ turns ON with the zero-voltage condition. The current path during this interval is $S_4$–$L_r$–$S_3$. $i_{Lr}$ circulates through $S_3$ and $S_4$ and remains constant during this interval.

### D. Adaptive Gate Drive Current of the Power MOSFET

As seen from Fig. 4, during $[t_1, t_2]$, the voltage applied to the inductor $v_{AB}$ is the drive voltage $V_c$. According to the inductance volt-second balance law, the relationship between the inductor value $L_r$ and the peak current $I_{\rm peak}$ of the CS inductor is

$$I_{\rm peak} = \frac{V_c \cdot D}{2 \cdot L_r \cdot f_s} \qquad D < 0.5 \tag{1}$$

$$I_{\rm peak} = \frac{V_c \cdot (1-D)}{2 \cdot L_r \cdot f_s} \qquad D > 0.5. \tag{2}$$

For a boost PFC converter with 110 $V_{\rm ac}$ input and 380 V output, the minimum duty cycle is $D_{\min} = 1 - 120 \cdot \sqrt{2}/380 = 0.55$. When $D > 0.5$, the peak value $I_{\rm peak}$ of the inductor current is governed by (2) and is a monotone decreasing function of the duty cycle. Fig. 7 shows the peak current value $I_{\rm peak}$ of the CS inductor as the function of the modulated duty cycle during a half-line period. From Fig. 7, as the input current $i_{\rm ac\_in}$ increases following the input voltage $v_{\rm ac\_in}$, the switching current of the power MOSFET also increase, and the peak value $I_{\rm peak}$ of the CS inductor current also increases accordingly, and this leads to a higher driver current, faster switching speed, and thus lower switching loss. On the other hand, as $i_{\rm ac\_in}$ decreases following $v_{\rm ac\_in}$, the switching current also decreases, which leads to lower circulating loss in the drive circuit. As a conclusion, the peak value $I_{\rm peak}$ of the CS inductor (i.e., drive current for the power MOSFET) is able to behave adaptively according to the MOSFET switching current. This property of inherent adaptive drive current of the proposed CSD will benefit the overall efficiency during a wide operation range, without requiring additional auxiliary circuitry and control.

### E. Application Extension

Moreover, the presented adaptive CSD circuit with one inductor can drive two interleaved boost PFC converters directly as shown in Fig. 8. The advantage is that only single FB CSD is required. It is noted that $Q_1$ and $Q_2$ are turned ON and OFF by the peak current of the CS inductor so that fast switching speed and switching loss reduction can be realized. In addition, $S_1$, $S_3$ and $S_2$, $S_4$ are with complementary control, respectively, and therefore, the commercial buck drivers with two complementary drive signals can be directly used to the CSD circuit. This much reduces the complexity of the CSD circuit implementation with the discrete components. Other benefits of this proposed topology include low current stress of the power MOSFETs, ripple cancellation of input current, and reduced boost inductances.

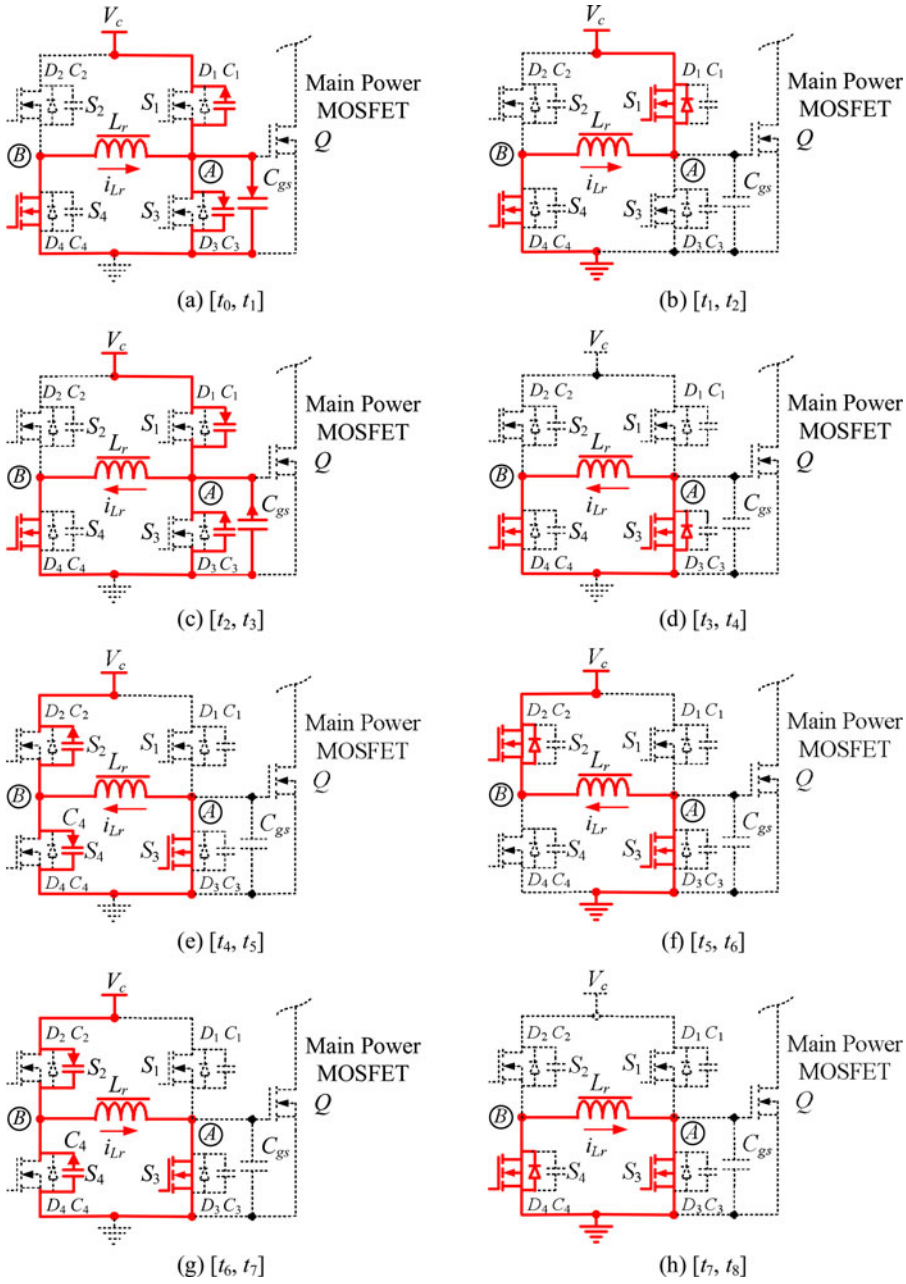


Fig. 6. Equivalent circuits of operation modes: (a) $[t_0, t_1]$, (b) $[t_1, t_2]$, (c) $[t_2, t_3]$, (d) $[t_3, t_4]$, (e) $[t_4, t_5]$, (f) $[t_5, t_6]$, (g) $[t_6, t_7]$, and (h) $[t_7, t_8]$.

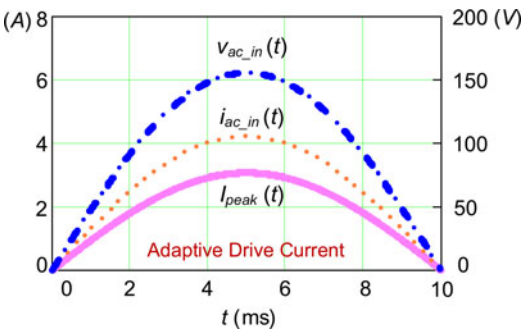


Fig. 7. Adaptive drive current with the input line voltage and input current.

## III. Loss Analysis of the Proposed Adaptive CSD for a Boost PFC Converter

In order to provide the design guideline and optimization, the loss analysis of the proposed adaptive CSD for the boost PFC converter is presented in this section. Basically, the loss of the circuit includes the loss of the PFC power stage and the CSD circuit.

### A. Loss Analysis of a Power Stage

The efficiency of the PFC stage is determined by the losses of the input diode bridge, the boost inductor, the main power MOSFET, and the rectifier diode, and they are analyzed as follows [22], [23]. Because the power MOSFET and boost diode

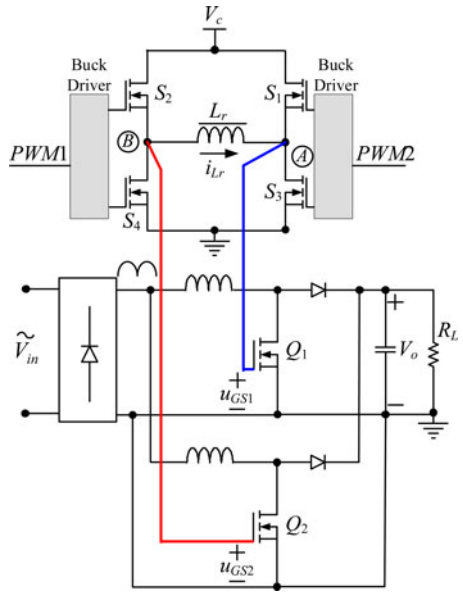


Fig. 8. Interleaving boost PFC converters with the proposed adaptive CSD.

are with a hard switching condition, the switching loss is dominant at high frequency.

*1) Loss of the Power MOSFET:* For a single-phase PFC converter, the current waveform of the main power MOSFET is half sinusoidal. The switching loss $P_{\rm sw}$ and conduction loss $P_{\rm cond}$ are, respectively

$$P_{\rm sw} = \frac{2\int_0^{\frac{T_{\rm line}}{2}} \frac{1}{2} f_s V_o I_{L\_\rm peak} \sin(\omega_L t)(T_r + T_f)\cdot dt}{T_{\rm line}} + \frac{1}{3} V_o^2 (C_{oss} + C_d) f_s \quad (3)$$

$$P_{\rm cond} = \frac{2\int_0^{\frac{T_{\rm line}}{2}} [I_{L\_\rm peak} \sin(\omega_L t)]^2 R_{\rm ds\_on} D(t)\, dt}{T_{\rm line}} \quad (4)$$

where $\omega_L = 2\pi \cdot f_L$, and $T_r$ and $T_f$ are the rising time and the falling time of the MOSFET respectively, $I_{L\_\rm peak}$ is the peak current of the boost inductor, $T_{\rm line}$ is the line period, and $f_s$ is the switching frequency. $C_{oss}$ is the MOSFET output capacitance, and $C_d$ is the diode junction capacitance.

*2) Loss of the Boost Diode:* The power losses $P_{\rm bd}$ of the boost diode including the forward conduction loss and the junction capacitance loss are

$$P_{\rm bd} = \frac{2\int_0^{\frac{T_{\rm line}}{2}} I_{L\_\rm peak} \sin(\omega_L t) V_{f\_\rm bd}[1 - d(t)]\, dt}{T_{\rm line}} + C_{\rm bd} V^2 f_s \quad (5)$$

where $V_{f\_\rm bd}$ is the forward voltage drop of the diode and $C_{\rm bd}$ is the junction capacitance of the diode. In the experimental verification, the switching frequency of the boost PFC converter is 1 MHz. In order to minimize the reverse recovery loss, the SiC rectifier CSD06060 from Cree is used. The SiC rectifier has dramatically reduced the reverse recovery charge, so the rectifier's switching loss is not presented in the analysis. However, it should be noted that the diode loss due to the junction capacitance is about 3 W for the CSD06060 at 380 V with 1 MHz switching frequency.

*3) Conduction Loss of the Rectifier Bridge:* The rectifier bridge consists of four rectifier diodes and the conduction loss of the rectifier bridge is

$$P_{\rm rd} = \frac{4}{T_{\rm line}} \int_0^{\frac{T_{\rm line}}{2}} I_{L\_\rm peak} \sin(\omega_L t) V_{f\_\rm rd}\, dt \quad (6)$$

where $V_{f\_\rm rd}$ is the forward voltage drop of the rectifier diodes and $I_{L\_\rm peak}$ is the peak current of the boost inductor.

Table I provides the calculated loss breakdown comparison of the 110 $V_{\rm ac}$ input, 380 V output, and 300 W boost PFC converter with 100 kHz and 1 MHz, respectively. The 600 V/11 A CoolMOS$^{\rm TM}$ SPA11N60 from Infineon is used for the power MOSFET and SiC CSD06060 from Cree is used for the diode. The benefits of the megahertz (MHz) PFC converters include high power density and fast dynamic performance owing to significant reduction of the passive components and EMI filter size [24]–[26].

From Table I, it is noted that when the switching frequency increases from 100 kHz to 1 MHz, the switching loss becomes the dominant loss and increases as much as 25.2 W. This results in a significant efficiency reduction of 6.9% from 95% to 88.1% as calculated.

### B. Loss Analysis of a CSD

In order to improve the efficiency, the proposed CSD is employed to reduce the switching loss of the converter. The total power losses of the CSD circuit are listed as follows:

1) the CS inductor loss

$$P_{\rm copper} = R_{\rm ac} \cdot I_{L\rm RMS}^2 \quad (7)$$

$$P_{\rm ind} = P_{\rm copper} + P_{\rm core} \quad (8)$$

where $I_{L\rm RMS}$ is the RMS value of the CS inductor current, $R_{\rm ac}$ is the ac resistance of the inductor winding, $P_{\rm copper}$ is the copper loss, and $P_{\rm core}$ is the core loss;

2) the mesh resistance loss of the power MOSFET

$$P_{RG} = 2 \cdot R_G \cdot I_{\rm peak}^2 \cdot t_{\rm sw} \cdot f_s \quad (9)$$

$$t_{\rm sw} = T_{r\rm CSD} + T_{f\rm CSD} \quad (10)$$

where $R_G$ is the internal gate mesh resistance, $t_{\rm sw}$ is the switching time of the power MOSFET, $T_{r\rm CSD}$ and $T_{f\rm CSD}$ are the rising time and the falling time of the power MOSFET, respectively, and $I_{\rm peak}$ is the peak value of the CS inductor current;

3) the total conduction loss of $S_1$–$S_4$

$$P_{\rm cond} = 2 \cdot R_{\rm DS(on)} \cdot I_{\rm peak}^2 \cdot \frac{4D - 1}{3} \quad (11)$$

where $R_{\rm DS(on)}$ is the on-resistor of the four switches;

4) the total gate drive loss of four switches

$$P_{\rm gate} = 4 \cdot Q_{g\_s} \cdot V_{gs\_s} \cdot f_s \quad (12)$$

where $Q_{g\_s}$ is the total gate charge of switch and $V_{gs\_s}$ is the drive voltage of the drive switches.

TABLE I
LOSS DISTRIBUTION COMPARISON WITH 100 KHZ AND 1 MHZ: $V_{in} = 110\ \mathrm{V_{ac}}$, $V_o = 380$ V, AND $P_o = 300$ W

| | Driving Loss | FET Switching Loss | FET Conduction Loss | Rectifier Loss | Bridge Loss | Inductor Loss | Total Loss |
|---|---|---|---|---|---|---|---|
| 100 k | 0.12 W | 2.4 W | 4.4 W | 1.5 W | 4.8 W | 2.1 W | 15.3 W |
| 1 M | 1.2 W | 24 W | 4.4 W | 4.0 W | 4.8 W | 2.1 W | 40.5 W |

From (8), (9), (11), and (12), the total loss $P_{CSD}$ of the CSD is

$$P_{\mathrm{CSD}} = P_{\mathrm{ind}} + P_{RG} + P_{\mathrm{cond}} + P_{\mathrm{gate}}. \tag{13}$$

### C. Example of Loss Comparison

In order to demonstrate the loss reduction with the proposed adaptive CSD, a boost PFC converter with the same specifications and components is presented as an example. For the CSD, the drive voltage $V_c$ is 12 V and the CS inductor is 1 $\mu$H (DS3316P, Coilcraft). It should be pointed that the experimental prototype in Section V is with the same specifications and components.

With $V_{\mathrm{in}} = 110\ \mathrm{V_{ac}}$ and $V_o = 380$ V, the duty cycle of the boost PFC converter is

$$D(t) = 1 - \frac{V_{\mathrm{in}} |\sin \omega_L t|}{V_o}. \tag{14}$$

Substituting (14) into (2), the CS inductor peak current $I_{\mathrm{peak}}$ (i.e., the gate drive current $I_g$) is

$$I_g(t) = I_{\mathrm{peak}}(t) = \frac{V_C [1 - D(t)]}{2 f_s L_r} = \frac{V_C V_{\mathrm{in}} |\sin \omega_L t|}{2 f_s L_r V_o} \tag{15}$$

where $V_c$ is the gate drive voltage.

With the proposed adaptive CSD, the switching loss of the power MOSFET is

$$P_{\mathrm{sw\_CSD}}(t) = \frac{1}{2} f_s V_o I_L(t) [T_{r\mathrm{CSD}}(t) + T_{f\mathrm{CSD}}(t)] \tag{16}$$

$$T_{r\mathrm{CSD}}(t) = \frac{Q_{\mathrm{pl}} - Q_{\mathrm{th}} + Q_{gd}}{I_g(t)} \tag{17}$$

$$T_{f\mathrm{CSD}}(t) = \frac{Q_{\mathrm{pl}} - Q_{\mathrm{th}} + Q_{gd}}{|I_g(t)|} \tag{18}$$

where $Q_{\mathrm{pl}}$ is the MOSFET total gate charge at the beginning of the plateau, $Q_{\mathrm{th}}$ is the total gate charge at the threshold, and $Q_{gd}$ is the gate-to-drain charge. $T_{r\mathrm{CSD}}$ is the switching rising time and $T_{f\mathrm{CSD}}$ is the switching falling time. For the power MOSFET of SPA11N60C3 from Infineon, $Q_{\mathrm{th}} = 3.2$ nC, $Q_{\mathrm{pl}} = 6$ nC, and $Q_{gd} = 22$ nC.

Fig. 9 illustrates the switching transition time comparison between the CSD and conventional VSD. $T_{\mathrm{sw\_CSD}}$ and $T_{\mathrm{sw\_conv}}$ represent the switching transition time with the CSD and the conventional VSD, respectively. During $[t_1, t_2]$, during half-line period, it is noted that $T_{\mathrm{sw\_CSD}}$ is always less than $T_{\mathrm{sw\_conv}}$, and moreover, the reduction of the switching transition time between $T_{\mathrm{sw\_CSD}}$ and $T_{\mathrm{sw\_conv}}$ increases when $I_g$ increases. Based on the adaptive drive current concept described in Section II, as $I_g$ modulates with the input line voltage and current (i.e., the switching current), the switching transition time and the switching loss with the CSD are also reduced adaptively.

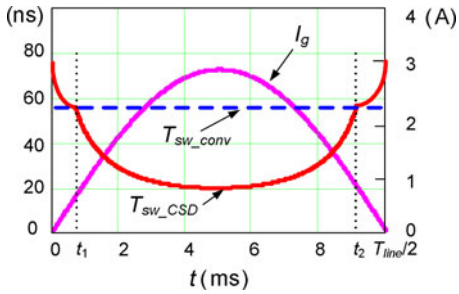


Fig. 9. Switching transient time comparison in half-line period ($V_{in} = 110\ \mathrm{V_{ac}}$, $V_o = 380$ V, $V_c = 12$ V, $P_o = 300$ W, and $L_r = 1$ $\mu$H).

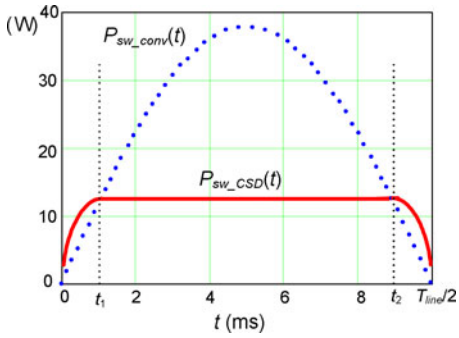


Fig. 10. Calculated switching loss comparison with the CSD and the conventional VSD in half-line period ($V_{\mathrm{in}} = 110\ \mathrm{V_{ac}}$, $V_o = 380$ V, $V_c = 12$ V, $P_o = 300$ W, and $L_r = 1$ $\mu$H).

Another point should be noted that during [0, $t_1$] and $[t_2, T_{\mathrm{line}}/2]$, $T_{\mathrm{sw\_CSD}}$ is higher than $T_{\mathrm{sw\_conv}}$, which means that the switching transition time with the CSD is longer than that with the voltage driver. This is because during these intervals, the gate drive current $I_g$ is not large enough to switch the power MOSFET completely and the CSD behaves as a VSD in part with an effective drive current of about 0.8 A in this case. However, during these intervals, because the switching current is quite low as the input line voltage and current are low, the switching loss is also limited under this hybrid drive condition.

Based on the loss analysis, the calculated switching loss comparison using the Mathcad software is shown in Fig. 10. $P_{\mathrm{sw\_CSD}}$ and $P_{\mathrm{sw\_conv}}$ represent the switching loss with the CSD and the conventional VSD, respectively. Similar to the reduction of the switching transition time as described previously, $P_{\mathrm{sw\_CSD}}$ is always less than $P_{\mathrm{sw\_conv}}$ during $[t_1, t_2]$, and furthermore, the loss reduction becomes larger when $I_g$ modulates with the input line voltage and current. During [0, $t_1$] and $[t_2, T_{\mathrm{line}}/2]$, it should be noted that $P_{\mathrm{sw\_CSD}}$ is slightly higher than $P_{\mathrm{sw\_conv}}$. This is

TABLE II
LOSS BREAKDOWN BETWEEN THE CSD AND THE CONVENTIONAL VSD: $V_{\rm in} = 110\ {\rm V_{ac}}$, $V_o = 380$ V, $V_c = 12$ V, $P_o = 300$ W, $L_r = 1\ \mu$H AND $f_s = 1$ MHZ

| | Driving Loss | FET Switching Loss | FET Conduction Loss | Rectifier Loss | Bridge Loss | Inductor Loss | Total Loss |
|---|---|---|---|---|---|---|---|
| Con. Driver | 1.2 W | 24 W | 4.4 W | 4 W | 4.8 W | 2.1 W | 40.5 W |
| CSD | 2.8 W | 10.5 W | 4.4 W | 4 W | 4.8 W | 2.1 W | 28.6 W |

because the input current and voltage are both quite low during these intervals, and the switching loss occurring then is limited. Overall, the CSD can reduce the switching loss significantly over the conventional VSD.

Table II provides the comparison of the 1 MHz PFC loss distribution. At 110-$V_{\rm ac}$ input, 380-V output voltage, the CSD reduces the total loss of 12 W. This translates into an efficiency improvement of 3.2% (from 89% to 92.2%) at full load.

## IV. OPTIMAL DESIGN OF THE PROPOSED ADAPTIVE CSD FOR A BOOST PFC CONVERTER

In order to optimize the adaptive CSD circuit, the design tradeoff should be made between the switching loss and gate drive circuit loss. The basic idea is to find the optimal solution on the basis of the object function that adds the switching loss and the CSD circuit loss together. The object function should be a U-shape curve as a function of the drive current $I_g$. Once the drive current is decided, the CS inductor value can be obtained from (2). The optimal design method proposed in [27] is for the dc–dc application with the steady-state duty cycle and the constant drive current. However, for the boost PFC converter, the duty cycle modulates during the line period and the drive current is also adjusted to the switching current. Therefore, for the boost PFC converter, the optimal design current uses the maximum CS inductor current $I_{g\max}$ as the design variable.

First, the total switching loss $P_{\rm switchingloss}$ of the power MOSFET during a half-line period as a function of the maximum drive current $I_{g\max}$ is

$$P_{\rm switching\ loss}\left(I_{g\max}\right) = \frac{\int_0^{\frac{T_{\rm line}}{2}} f_s V_o \cdot I_{L\_pk} \sin\left(\omega_L t\right) \cdot \left[T_{r\rm CSD}\left(I_{g\max}\right) + T_{f\rm CSD}\left(I_{g\max}\right)\right] dt}{T_{\rm line}} \tag{19}$$

where $T_{r\rm CSD}$ and $T_{f\rm CSD}$ can be obtained from (19) and (20), respectively.

Second, from (15), the total loss of the CSD as a function of $I_{g\max}$ is

$$P_{\rm CSD}\left(I_{g\max}\right) = P_{\rm ind}\left(I_{g\max}\right) + P_{RG}\left(I_{g\max}\right) + P_{\rm cond}\left(I_{g\max}\right) + P_{\rm gate}. \tag{20}$$

Third, from (19) and (20), in order to find the optimized $I_{g\max}$, the objective function $F(I_{g\max})$ is established adding the switching loss and the CSD loss together as

$$F\left(I_{g\max}\right) = P_{\rm switching\ loss}\left(I_{g\max}\right) + P_{\rm CSD}\left(I_{g\max}\right). \tag{21}$$

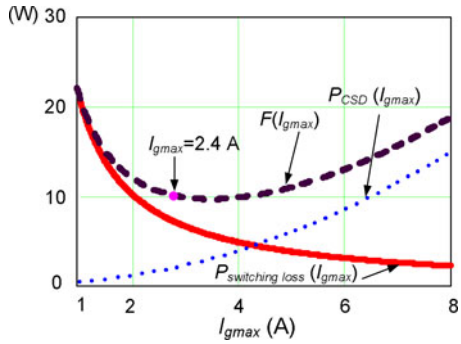


Fig. 11. Objective function $F(I_{g\max})$ as a function of $I_{g\max}$.

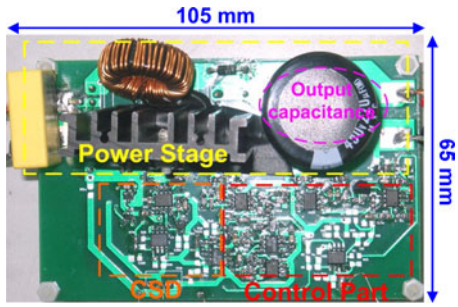


Fig. 12. Photograph of power stage and CSD.

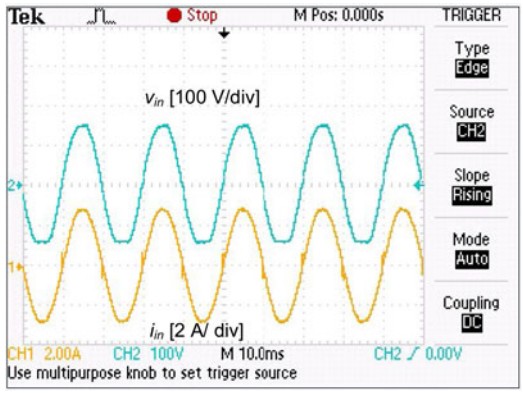


Fig. 13. Input voltage and current of the power stage.

Fig. 11 shows the optimal design curves based on (21). It is noted that the optimal gate drive current is 2.4 A. Based on the selected gate drive current, the calculated CS inductor from (2) is

$$L_r = \frac{V_c V_{\rm inmax}}{2 f_s V_o I_{g\max}} = 1\ \mu{\rm H} \tag{22}$$

where $V_{\rm in} = 110$ V, $f_s = 1$ MHz, $V_o = 380$ V, $P_o = 300$ W, and $I_{g\max} = 2.4$ A. As far as the common source inductance is concerned, the current diversion problem of the CSD results

TABLE III
MEASURED PF VALUES AT DIFFERENT LOADS UNDER 100 $V_{ac}$

| Load Conditions (W) | 25% (75 W) | 50% (150 W) | 75% (225 W) | 100% (300 W) |
|---|---|---|---|---|
| PF | 0.992 | 0.994 | 0.998 | 0.999 |

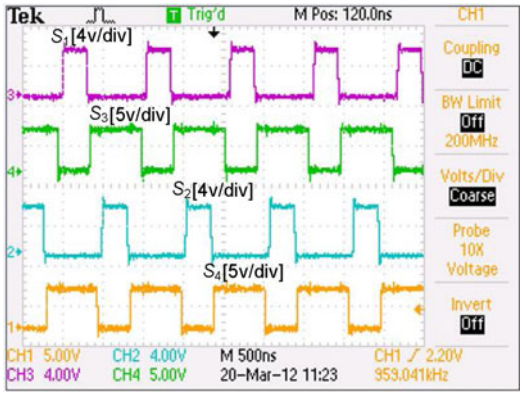


Fig. 14. Drive signals of the CSD switches.

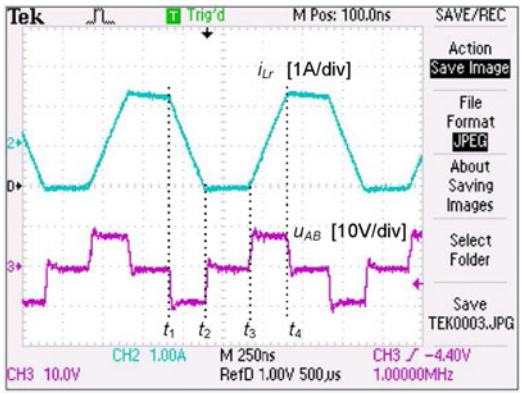


Fig. 15. CS inductor current $i_{Lr}$ and the voltage between $A$ and $B$, $u_{AB}$.

in the reduction of the effective drive current [19]. Therefore, in the experimental prototype, the designed current is chosen as 2 A to optimize the overall efficiency.

## V. EXPERIMENTAL RESULTS AND DISCUSSION

To verify the proposed adaptive CSD, a 110 $V_{ac}$ input, 380 V/300 W output, and 1 MHz CCM boost PFC converter was built. The specifications are as follows: boost inductor $L =$ 100 $\mu$H; output capacitance $C = 220$ $\mu$F; power MOSFET SPA11N60C3, the boost diode CSD06060, the CS inductor $L_r = 1.5$ $\mu$H (DS3316P), and the gate driver voltage $V_c =$ 12 V. Fig. 12 illustrates the photograph of the prototype. Since there is no commercial IC available for MHz PFC applications, the discrete components were used to build the controller, saw tooth generator, and CSD circuit. Two synchronous buck drivers ISL6209 from Intersil are used to drive CSD switches. The discrete multiplies AD633 and comparators are used to implement PFC current loop and generate saw tooth. In order to minimize the negative impact of the parasitics of the discrete components and layout at the switching frequency of 1 MHz, the commercial drive IC LTC4442 from linear technology was chosen as the

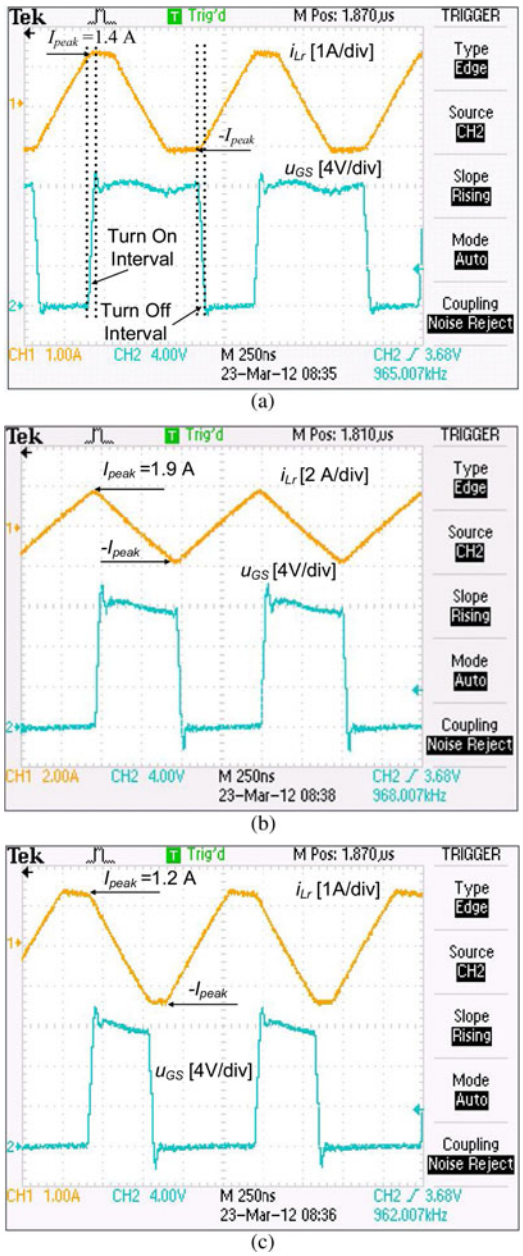


Fig. 16. CS inductor current $i_{Lr}$ and gate drive voltage $u_{gs}$ with different duty cycles: (a) $D > 0.5$, (b) $D = 0.5$, and (c) $D < 0.5$.

conventional voltage driver to the main power MOSFET of the boost converter. This drive IC is a fully integrated conventional voltage driver in SOIC-8 package and is able to provide the peak drive current of around 2 A.

Fig. 13 illustrates the input voltage and current of the power stage. It is observed that the input line current is sinusoidal and is able to follow the input line voltage. The measured PF values are given in Table III according to different loads. The

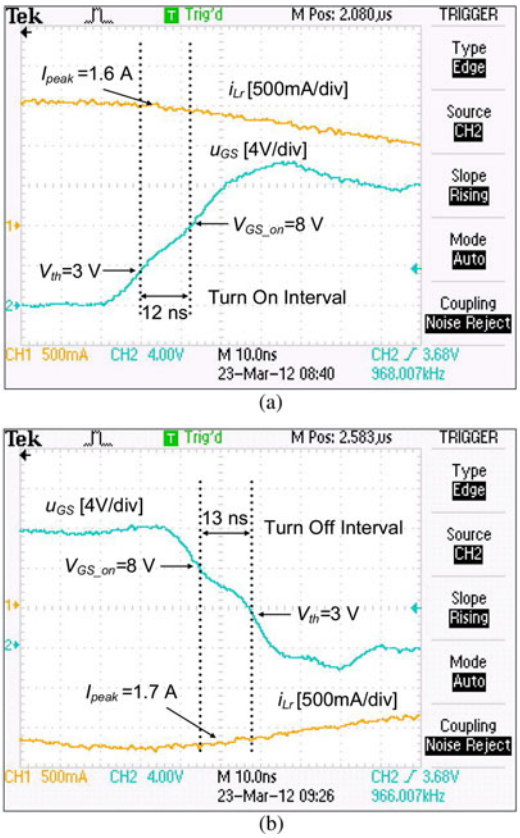


Fig. 17. Turn-on and turn-off intervals: CSD. (a) Turn-on interval. (b) Turn-off interval.

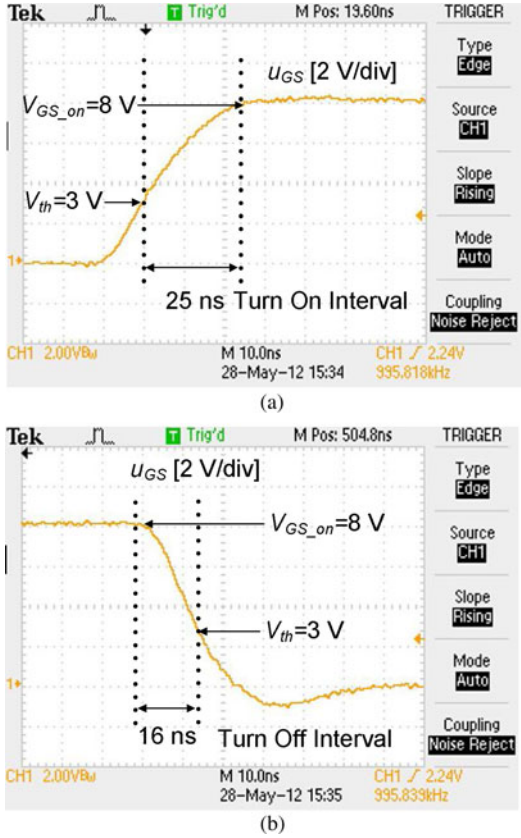


Fig. 18. Turn-on and turn-off intervals: VSD. (a) Turn-on interval. (b) Turn-off interval.

measured PF values are all above 0.99, which are compatible to the industrial standards. The functionality of the power factor correction is realized with the proposed adaptive CSD.

Fig. 14 illustrates the drive signals of $S_1$–$S_4$. They agree with the theoretic waveforms as shown in Fig. 4. Fig. 15 illustrates the CS inductor current $i_{Lr}$, and the voltage between *A* and *B*, $u_{AB}$. During $[t_1,\ t_2]$, the inductor current changes its polarity from the positive peak value to the negative peak value. During $[t_2,\ t_3]$, the CS inductor current is circulating through $S_1$ and $S_2$ and remains constant in this interval. This provides a CS when the power MOSFET is turned OFF. During $[t_3,\ t_4]$, the CS inductor current changes its polarity from the negative peak value to the positive peak value. At $t_4$, the MOSFET can be turned ON with a CS again.

Fig. 16 illustrates the CS inductor current $\mathrm{i}_{Lr}$ and the gate-to-source voltage $\mathrm{u}_{gs}$ with different duty cycles. It is noted that with different duty cycles, the peak current $I_{\mathrm{peak}}$ of the CS inductor also changes adaptively and at the same time, the peak current is used to switch the main power MOSFET to achieve fast switching speed as labeled in *Fig. 16(a)*.

Fig. 17 shows the zoomed CS inductor current $\mathrm{i}_{Lr}$ and the gate drive voltage $\mathrm{u}_{gs}$ during the turn-on and turn-off intervals, respectively. In Fig. 17(a), for the turn-on interval, the peak drive current of the CS inductor is approximately 1.6 A and charges the gate of the power MOSFET from 0 to 12 V. It should be pointed that the turn-on transition starts from the gate voltage arising after the threshold voltage ($V_{\mathrm{th}} = 3$ V for SPA11N60 from Infineon) is reached until the power MOSFET is fully turned ON ($V_{gs\_\mathrm{on}} = 8$ V for SPA11N60 from Infineon). The turn-on transition time is only about 12 ns and this fast switching speed leads to the reduction of the turn on loss. Similarly, for the turn-off interval as shown in Fig. 17(b), the peak drive current of the CS inductor is approximately 1.7 A and the turn-off transition time is only about 13 ns. This also leads to a significant reduction of the turn-off loss.

For comparison, Fig. 18 shows the waveforms of the gate drive voltage during the turn-on and turn-off intervals, respectively. From Fig. 17(a), it is observed that the turn-on transition time of the proposed adaptive CSD is reduced to 12 ns compared to 25 ns of the VSD as seen from Fig. 18(a). Similarly, from Fig. 17(b), the turn-off transition time of the CSD is reduced to 13 ns (a reduction of 23%) compared to 16 ns of the VSD as seen from Fig. 18(b). The reduction of the switching transition time leads to lower switching loss and higher efficiency.

Fig. 19 gives the measured efficiency comparison between the CSD and the conventional VSD with different line voltages under the full-load condition. Due to the fast switching speed and the switching loss reduction of CSD, the efficiency improvement is achieved throughout the whole input line voltage. Particularly, with 110 $\mathrm{V}_{\mathrm{ac}}$ input voltage and 300 W output, an efficiency improvement of 3.2% is achieved, while with 220 $\mathrm{V}_{\mathrm{ac}}$ input voltage, an efficiency improvement of 1.5% is achieved over the conventional VSD. Fig. 20 gives the measured efficiency comparison with different line voltages under the

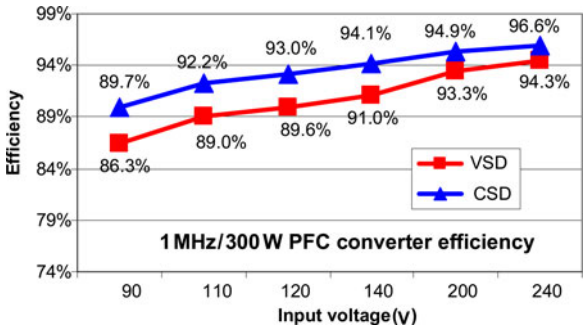


Fig. 19. Efficiency comparison with different line voltages under full load: top: CSD; bottom: conventional VSD.

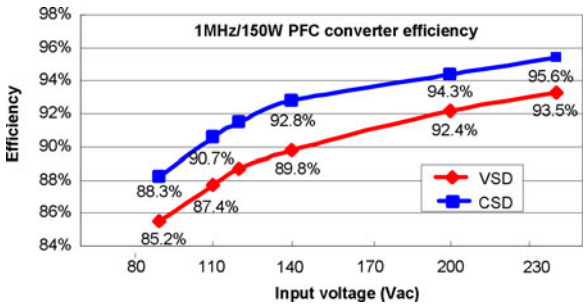


Fig. 20. Efficiency comparison with different line voltages under half load: top: CSD; bottom: conventional VSD.

half-load condition. Similar efficiency improvements are achieved over the VSD due to fast switching speed.

## VI. Conclusion

In this paper, an adaptive FB CSD was proposed for boost PFC converters to achieve fast switching speed and significant switching loss reduction. Compared to other CSDs with the constant drive current, the advantage of the adaptive drive current can achieve further switching loss reduction when the power MOSFET is with a higher switching current while reduce the drive circuit loss when the MOSFET is with a lower switching current. This provides better optimal opportunity with the trade-off between the switching loss reduction and CSD drive circuit loss during a wide operation range. A 300-W/1-MHz boost PFC converter with the universal input line voltage was built to verify the advantages. With 110 $V_{ac}$ input and 380 V/300 W output, the CSD reduces the total loss by 12 W, which translates into an efficiency improvement of 3.2% (from 89.0% to 92.2%). With 220 $V_{ac}$ input and 380 V/300 W output, an efficiency improvement of 1.5% is achieved over the conventional VSD.

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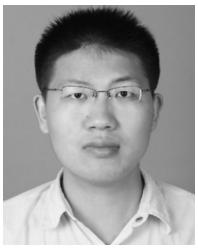

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