Single Stage Primary Side Controlled Offline Flyback LED Driver with Ripple Cancellation

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Abstract— A primary side controlled offline Flyback LED driver is an very attractive LED driver solution due to its low component cost and high efficiency. However, as any other single-stage LED driver, it produce significant low frequency ripple current. In this paper, an innovative primary side controlled Flyback LED driver with low frequency ripple cancellation has been proposed. The low frequency ripple current has been greatly reduced while maintaining multiple primary side controlled LED driver advantages, such as high efficiency, low component cost, and low design complexity. A 35W, 50V-0.7A universal input experimental prototype has been built to verify the proposed technology.

I. INTRODUCTION

Flyback LED driver is an very attractive LED driving solution for low component costs and high efficiency. In order to further reduce component costs and design complexity, primary side current sensing technology with Flyback LED driver has been developed. The secondary side feedback circuit and the opto-coupler can be eliminated with this technology. The detailed operation of a primary side sensed Flyback LED driver has been investigated extensively in [1-10].

As any other conventional single-stage LED drivers, a significant low frequency ripple current will also be produced in a conventional primary side controlled offline Flyback LED driver. The low frequency current ripple presents itself as the low frequency lighting fluctuation - flicker. Two-stage LED driver can achieve very good LED current regulation. However, with resulting high component cost and low efficiency. Various technologies have been proposed in [14-24] in attempts to achieve tight regulated LED current with single stage structure. The technology proposed in [14-17] combines the front PFC stage and the second DC-DC stage. This solution is complicated in design and has a lot limitations. In this solution, power factor correction and DC-DC conversion need to be achieved at the same time with shared power components. The solution proposed in [18-21] uses a bi-directional DC-DC converter to accommodate energy imbalance between AC input side and output side so that a flat LED current can be achieved. However, the

drawback is that over one third of the output power has been converted three times before reaching the output. The overall efficiency is therefore reduced. Besides, the component costs for the bi-directional DC-DC converter is also high. Low frequency ripple cancellation technology based on Flyback LED driver has been proposed in [24]. Tight regulated LED current, high efficiency and satisfactory power factor have all been achieved with only one power stage.

As a further development of the technology proposed in [24], a primary side controlled Flyback LED driver with ripple cancellation has been proposed in this paper. In additional to achieve ripple voltage cancellation, the entire secondary side control circuit and feedback circuit have been relocated to the primary side. The opto-coupler has also been eliminated in the design. A integrated primary side controlled ripple cancellation solution can therefore be created.

This paper is organized as follows. Section II describes the operating principle of the proposed technology. Section III discusses the advantages of the proposed technology. The experimental results of the prototype are presented in section IV and the conclusion is outlined in section V.

II. OPERATING PRINCIPLES

In section II, the operating principle of the proposed technology will be discussed. The power stage structure, realization of primary side voltage sensing, low frequency ripple voltage cancellation, primary side current sensing as well as LED current regulation is included in this section.



Figure 1 High level power stage structure of the proposed technology

A. Power stage structure

Figure 1 demonstrates the high level power structure of the proposed primary side LED driver with low frequency ripple cancellation. The LED voltage, V_{out} , is produced by connecting the Flyback PFC output V_{o1} and the Flyback DC-DC output V_{o3} in series. The Flyback PFC output voltage V_{o1} contains a significant low frequency ripple component. The voltage V_{o1} can be described by (1):

$$V_{o1} = V_{o1 \ dc} + V_{o1 \ rip}(t)$$
(1)

In (1), $V_{ol_{dc}}$ represents the DC component of V_{ol} while $V_{ol_{rip}}(t)$ represents its low frequency ripple component. The Flyback DC-DC output V_{o3} also contains a significant low frequency ripple component and is described by (2):

$$V_{o3} = V_{o3 \ dc} + V_{o3 \ rip}(t) \tag{2}$$

The DC component V_{o3_dc} is needed to maintain V_{o3} above zero. The purpose of connecting voltage V_{o1} and V_{o3} in series is to have their ripple component canceled. As such, their sum, V_{out} , is a DC value and described by (3):

$$V_{out} = V_{o1} + V_{o3}$$

$$= (V_{o1_dc} + V_{o3_dc}) + [V_{o1_rip}(t) + V_{o3_rip}(t)]$$
(3)

As it can be noted from (3), in order to achieve total low frequency ripple cancellation, the following equation must be satisfied:

$$V_{o1 rip}(t) + V_{o3 rip}(t) = 0$$
(4)

Equation (4) implies that $V_{ol_rip}(t)$ and $V_{os_rip}(t)$ are of equal value but with opposite sign. In the proposed technology, $V_{ol_rip}(t)$ is the master signal and $V_{os_rip}(t)$ is its dependent follower.

B. Realization of primary side voltage sensing

In the proposed technology, the entire control and sensing circuit are located at the primary side. As a result, optocoupler and the secondary side compensation circuit can be eliminated in the design. Figure 2 demonstrates the circuit arrangement to achieve this objective.



Figure 2 The proposed primary side controlled LED Driver with ripple cancellation

In order to shape the Flyback DC-DC output V_{o3} , both output voltages V_{o1} and V_{o3} must be sensed. Winding sns_1 from transformer T1 and winding sns_2 from transformer T_2 sense the output voltages V_{o1} and V_{o3} at primary side. The conventional primary side voltage sensing technique can only work for applications where output is a DC value. In the proposed technology, both the Flyback PFC and the Flyback DC-DC outputs contain a significant low frequency ripple voltage. Thus, the conventional primary side sensing technology cannot capture the low frequency ripple voltage, which is the key information to achieve low frequency ripple cancellation.



Figure 3 The principle of primary side voltage sensing illustrated by the Flyback DC-DC converter

An innovative voltage sensing method which accurately captures the low frequency ripple voltage information on primary side has been proposed in this paper. Figure 3 shows the principle of sensing output voltage at the primary side.

The voltage across the secondary winding, V_{sec} , and the voltage across the primary side sensing winding, V_{sns} , of the transformer in the Flyback DCDC have been shown in Figure 3. All parasitic components and diode forward voltage drop have been neglected so that the most important characteristics can be focused.

For Flyback topology based power converter, the voltages across the secondary side winding, V_{sec} , and the voltage across the primary side sensing winding, V_{sns} have a proportional relationship during the switching off period. The voltage relationship is determined by their turns ratio and is described by (5):

$$V_{sns} = \frac{N_{sns2}}{N_{Sec2}} \cdot V_{Sec}$$
(5)

In (5), N_{aux2} and N_{S2} represent the number of turns of the primary side sensing winding and the secondary side winding respectively. As such, the output voltage of the Flyback converter on the secondary side can be sensed on the primary side for every switching cycle. The Flyback PFC output voltage can also be sensed at primary side in the same way. In order to avoid sampling excessive ring voltage occurring right after turn off, a blank time should be applied before sampling the winding voltage at primary side.

C. Realization of ripple voltage cancellation

With both the Flyback PFC output V_{ol} and the Flyback DC-DC output V_{o3} being sensed at primary side, the Flyback DC-DC output voltage V_{o3} can then be shaped at primary side and further voltage ripple cancellation can be achieved. Figure 4 illustrates the realization of ripple voltage cancellation.



Figure 4 Realization of ripple voltage cancellation

 V_{sns1} and V_{sns3} is the sensed results of the Flyback PFC output voltage V_{o1} and the Flyback DC-DC output voltage V_{o3} respectively. In order to add a proper DC level to Flyback DC-DC output V_{o3} , V_{sns1} will be level shifted and become V_{ref} . V_{ref} and V_{sns3} add together and the result signal $V_{control}$ will be fed into the controller of the Flyback DC-DC.

D. Realization of primary side LED current sensing

Primary side current sensing technology has already been analyzed in [1-10]. Figure 5 illustrates the principle of sensing the averaged secondary side current at the primary side.



Figure 5 Primary side LED current sensing principle

The averaged current flow into secondary side in a switching period can be described by (6):

$$I_{\text{sec}_avg} = \frac{n \times I_{pri_pk} \times T_{dis}}{2 \times T_{cvcle}}$$
(6)

In equation (6), n represents the winding's turn ratio between the primary side and the secondary side. I_{pri_pk} is the peak switching current at the primary side, T_{dis} and T_{cyc} represent the secondary side current discharge time and the whole switching period time respectively.

The proposed LED driver solution also implements primary side current sensing technology. In particular, one must ensure that primary side LED current sensing is carried by the Flyback DC-DC instead of the Flyback PFC. The reason why the averaged secondary side current sensing cannot otherwise be carried in Flyback PFC is illustrated in Figure 6.



Figure 6 Current distribution in the transformer of the Flyback PFC

In Figure 6, the aux winding carry significant current during switching off, which will flow into the 12V input side of the Flyback DC-DC. The current sensed at the primary side of the PFC transformer reflects the net sum of the secondary side current and the aux side current, not only the secondary side current. In the Flyback DC-DC transformer, only the secondary side winding carries current during turn off, so the current sensed at its primary side is a true reflection of the secondary side current.

Ε. Realization of LED current regulation



Figure 7 LED current regulation

Figure 7 shows how to achieve LED current regulation. LED current is sensed at primary side. With the peak primary side switching current, I_{pri_pk} , and current discharge time T_{dis} available, the averaged LED current can be calculated. The calculated averaged current I_{avg} is be compared with current reference I_{ref} . The error current I_{err} will then be sent to PFC controller. As such, the output voltage of the Flyback PFC and the LED current can be adjusted automatically.

ADVANTAGE OF THE PROPOSED III. TECHNOLOGY

In order to achieve low ripple current performance as a two-stage LED driver while maintaining both high efficiency and low component costs as a single-stage LED driver. various technologies [14-23] have been proposed. These technologies have certain advantages over conventional one. However, at other hand, they have also encountered new issues. Comparatively, the proposed technology contains collective advantages from both single-stage and two-stage LED drivers while avoids their drawbacks. More importantly, no new issues has arisen. In the following part of this section, the advantages of the proposed technology will be discussed in great detail.

A. High efficiency

As shown in Figure 1, the averaged voltage of V_{al} and V_{a3} are 45V and 5V respectfully, delivering 90% of the output power by the Flyback PFC directly, while 10% of the output power is delivered by the Flyback DC-DC. The power delivered by the Flyback PFC has only been converted once. The input voltage of the Flyback DC-DC is additional output of the Flyback PFC located at primary side, so the power delivered by the Flyback DC-DC has been processed twice. Since the majority of the power delivered to LED Load has only been converted once, the overall efficiency of the proposed technology is very close to that of conventional Flyback LED drivers. The following equation describes the efficiency achievable with the proposed technology.

$$Eff_{pos} = \frac{1}{\frac{0.9}{Eff_{PFC}} + \frac{0.1}{Eff_{PFC} \times Eff_{DCDC}}}$$
(7)

In (7), Eff_{pos} , Eff_{PFC} and Eff_{DCDC} represent the overall efficiency of the proposed technology, the efficiency of the Flyback PFC and the efficiency of the Flyback DC-DC respectively. Using equation 7, one may note that if 87% efficiency has been achieved by the Flyback DC-DC, the proposed technology can achieve 0.985 Eff_{PFC} efficiency, which is very close to the efficiency a comparable conventional Flyback LED driver can achieve.

B. Low component cost

With both the Flyback PFC output voltage V_{ol} , the Flyback DC-DC output V_{o3} as well as LED current sensed at the primary side, the resulting control circuit can be implemented at primary side. The red box shown in Figure 2 illustrates a integrated primary side control solution. Compared to conventional primary side controlled Flyback LED driver, the extra components need to be added in the proposed technology has been shown (marked in red), which include a 5W capacity Flyback transformer T2 and a 20V-1A diode. These two components contribute very trivial costs in a 35W Flyback LED driver.

IV. EXPERIMENTAL RESULT

A 35W (50V/0.7A) experimental prototype was constructed to verify the proposed technology. In order to conduct an objective evaluation, the performance of a conventional Flyback LED Driver and a conventional twostage (Flyback PFC + Buck DC-DC) LED driver have also been included for comparison. Figure 8 compares the efficiency of the three technologies. The PFCs used in three technologies are identical. The efficiency of Flyback DC-DC in the proposed technology and the second stage DC-DC in the two-stage LED driver have also been indicated.

As it is shown in Figure 8, the efficiency of the proposed technology under 110VAC input is 3% higher than the conventional two-stage LED driver. Under 220VAC input, the proposed technology can still achieve 2% higher efficiency than the conventional two-stage LED driver. Since only 10% of output power is handled by the Flyback DCDC in the proposed technology, the structural advantage is very obvious and it is more easier to achieve higher efficiency than two-stage LED driver.

The THD and power factor performance of the proposed technology has also been presented in Figure 9 and Figure 10.

Almost identical power factor and THD performance has been achieved with the proposed technology compare to the conventional Flyback LED driver.



Figure 8 Efficiency comparison between conventional technology and the proposed technology



Figure 9 THD comparison between the proposed technology and the conventional Flyback LED driver



Figure 10 Power Factor comparison between the proposed technology and the conventional Flyback LED driver

Figure 11 shows the ripple voltage sensing result of the Flyback PFC output V_{o1} and the Flyback DC-DC output V_{o3} . High fidelity low frequency ripple information has been retrieved at primary side with the proposed voltage sensing method.



Figure 11 Voltage sensing at primary side

Figure 12 shows the low frequency ripple current performance comparison between the proposed technology and conventional Flyback LED driver. Two LED drivers are connected with 470uF output storage capacitor. Because the low frequency ripple voltage is greatly cancelled in the proposed technology, almost DC LED current can be achieved. The Low frequency ripple current with the conventional LED driver goes up to 200mA pk-pk while the low frequency ripple current has been reduced to 20mA pk-pk with the proposed technology.



Figure 12 Low frequency ripple current performance comparison (a)The proposed technology (b)The conventional Flyback LED driver

The waveform of LED current sensing at primary side has been shown in Figure 13 and the sampled result has been shown in Figure 14.



Sampled peak switch on current switch on current switch on current in 1.00 V %Ch2 5.00 V M4.00ms A Ch3 ≠ 900mV Ch3 1.00 V % Figure 14 Primary side current sensing result

V. CONCLUSIONS

This paper has proposed an innovative primary side controlled Flyback LED driver with low frequency ripple cancellation. The power stage of the novel design is constructed by a Flyback PFC and a Flyback DC-DC. By connecting the output voltage of Flyback PFC output and the output voltage of the Flyback DC-DC in series, A DC LED voltage can be achieved and also a DC LED current.

The Flyback PFC and Flyback DC-DC output voltages are sensed at primary side by extra windings. LED current is also sensed at primary side of Flyback DC-DC. Since all required information to achieve ripple cancellation and LED current regulation are available at primary side, the entire control circuit can be built at primary side and further be integrated into a single package. Besides, the opto-coupler and secondary side control circuit can also be eliminated. This is an very attractive primary side LED driver solution with ripple cancellation.

An experimental prototype has been built to verified the proposed technology. The low frequency ripple current with the proposed technology is 20mA pk-pk, which is ten times lower compared to 200mA pk-pk ripple current in the conventional Flyback LED driver. Since 90% of the output power is delivered by the Flyback PFC directly and has only been converted once, the overall efficiency of the proposed technology is very close to the efficiency of the conventional

Flyback LED driver while much higher than the conventional two-stage counterpart. The experimental prototype has achieved up to 86% efficiency which is 3.5% higher than the conventional two-stage LED driver. Satisfactory power factor and THD performance has also been achieved with the proposed technology.

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