An Electrolytic Capacitor-Free Single Stage Buck-Boost LED Driver and its Integrated Solution

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***Abstract*—For a conventional offline Buck-Boost LED driver, significant low frequency ripple current is produced when a high power factor has been achieved. In this paper, an innovative LED driver technology based on the Buck-Boost topology has been proposed. The featured configuration has greatly reduced the low frequency ripple current without compromising power factor performance. High efficiency and low component cost features have also been retained from conventional Buck-Boost LED driver. A 10W, 50V-0.2A experimental prototype has been constructed to verify the performance of the proposed technology.**

I. INTRODUCTION

Buck-Boost LED drivers are a very attractive candidate for low power LED lighting applications which must be low-cost and which not require electrical isolation. They can additionally achieve high efficiency with low component costs and simple designs. Offline LED driver reference designs based on Buck-Boost topology are widely available. However, like any other single stage LED driver solutions, significant low frequency ripple current is generated in the conventional Buck-Boost LED driver.

A significant low frequency ripple current presents as a flicker in lighting output. For these AC connected lighting fixtures, the flicker frequency is twice that of the AC line frequency. According to [1], human retina can respond to flicker frequencies upwards of 200Hz. Long time exposure to 100/120Hz flicker has been demonstrated to cause malaise, headache and visual impairment in some test subjects.

One method to reduce flickering is to increase the output capacitor value. However, bulky output capacitors are cost ineffective and require excessive PCB space. Various solutions have been proposed to solve undesirable flicker with a single stage power structure. In [4-7], the front power factor stage and second DC-DC stage have been combined. There is a lot of constraints on operating shared power components in order to achieve power factor correction and DCDC conversion at the same time. In [8-11], active energy storage has been proposed. A bi-directional converter has been used to replace the bulky storage capacitor. The drawback of this solution is that approximately 32% of the output power has been converted three times before being delivered at the output. The technology in [12-13] proposes a design trade-off between power factor and the required output capacitance. However, this solution sacrifices input current harmonic levels and power factor performance. In [14], a offline Flyback LED driver with ripple cancellation had been proposed. Tight regulated LED current and high power factor had been achieved with only single power stage. As a further development of this technology, a 10W offline LED driver based on Buck-Boost power topology has been proposed in this paper. As a additional advantage, high level component integration can be achieved since there is no isolation barrier standing between AC input side and LED driver output side. The integrated solution of the proposed technology has been discussed in detail. Because of the ripple cancellation technology, electrolytic capacitors have also been eliminated in the design. The lifespan of the LED driver will not be limited by the life of electrolytic capacitor anymore.

This paper is organized as follows: Section II discusses the operating principle of the proposed topology. The advantages of the proposed solutions are analyzed in section III. Section IV covers the detailed design considerations. The integrated solution of the proposed technology is discussed in section V. Experimental results are shown in VI and section VII is the conclusion.

II. OPERATING PRINCIPLE

In section II, the operating principle of the proposed technology is discussed. The power stage structure, operation of Ripple Cancellation Converter (RCC) as well as LED current regulation will be discussed in detail.

A. The Power Stage Structur

Figure 1 shows the comparison between conventional Buck-Boost LED drivers topology and the proposed LED driver topology. In Figure 1(b), a Ripple Cancellation Converter has been added and is indicated in red. The RCC is implemented with a Buck topology in order to achieve high efficiency and low component costs. The PFC output, $V_{o1,}$ and the RCC output, $V_{o3,}$ are connected in series to achieve a DC LED voltage output.

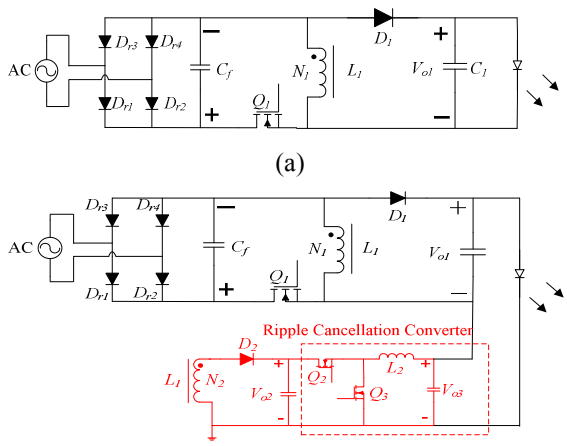

Figure 1 Power stage of Buck-Boost LED Driver (a) Conventional topology; (b) The proposed topology

Figure 2 shows the high level power structure of the proposed Buck-Boost LED driver. The PFC output voltage contains a significant low frequency ripple component. The voltage V_{o1} can be described by (1):

$$V_{o1} = V_{o1\_dc} + V_{o1\_rip}(t) \tag{1}$$

In (1), V_{o1_dc} represents the DC component of V_{o1} while V_{o1_rip}(t) represents its low frequency ripple component. The Ripple Cancellation Converter output, V_{o3}, also contains a significant low frequency ripple component and is described by (2):

$$V_{o3} = V_{o3\_dc} + V_{o3\_rip}(t) \tag{2}$$

The DC component V_{o3_dc} is needed to keep V_{o3} above zero. The purposes of connecting voltages V_{o1} and V_{o3} in series is to have their ripple components cancel. This way, their sum, V_{out} , is a DC value which can be described by (3):

$$\begin{aligned} V_{out} &= V_{o1} + V_{o3} \\ &= (V_{o1\_dc} + V_{o3\_dc}) + [V_{o1\_rip}(t) + V_{o3\_rip}(t)] \end{aligned} \tag{3}$$

In order to achieve total ripple cancellation, the following equation must be satisfied:

$$V_{o1\_rip}(t) + V_{o3\_rip}(t) = 0 \tag{4}$$

Equation (4) implies that V_{o1_rip}(t) and V_{o3_rip}(t) are of equal value but with opposite sign. In the proposed technology, V_{o1_rip}(t) is the master signal and V_{o3_rip}(t) is its dependent follower.

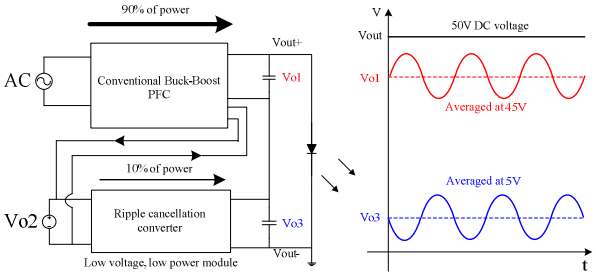

Figure 2 The proposed LED driver structure

B. *Operation of the Ripple Cancellation Converter*

Figure 3 shows the concept implementation of the Ripple Cancellation Converter. As demonstrated in Figure 2, V_{o1} is a differential output pair with respect to the ground potential of the Ripple Cancellation Converter. Firstly, V_{o1} is sensed and converted to the single end signal V_{o1_S}. The DC component of signal V_{o1_S} is then blocked, allowing only the low frequency ripple component, $V_{o1\_S\_rip}$, to pass. $V_{o1\_S\_rip}$ is then inverted and provided an offset. The resulting V_{o3_ref} becomes the reference voltage for the Ripple Cancellation Converter. This way, the Ripple Cancellation Converter's output voltage V_{o3} contains a ripple component which can fully cancel the low frequency ripple voltage from V_{o1}. In the practical circuit implementation, a signal travelling in Figure 3 will need to be properly scaled in order to meet the voltage rating requirements of the OpAmps. Detailed circuit implementation is available in Figure 18.

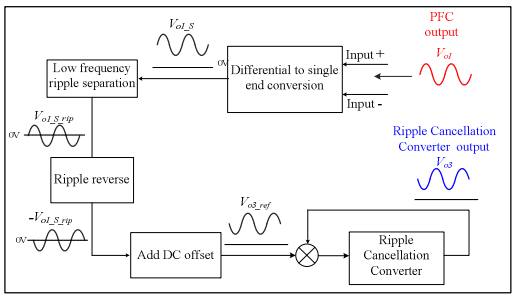

Figure 3 Operation of the Ripple Cancellation Converter

C. *LED current regulation*

Figure 4 shows a diagram of how LED current regulation is achieved. The Ripple Cancellation Converter is configured to cancel the low frequency ripple voltage only, and is not implicated in LED current regulation. LED current regulation is achieved with LED current feedback loop. This feedback loop sense LED current and automatically adjusts the PFC output voltage V_{o1} and further LED current accordingly.

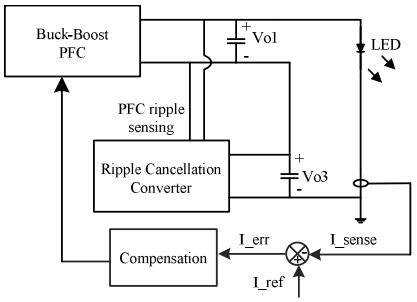

Figure 4 LED current regulation

III. THE ADVANTAGE OF THE PROPOSED TECHNOLOGY

Various technologies [4-13] have been proposed to achieve the low ripple current performance as two-stage LED driver while also maintaining the high efficiency and low component cost as single stage LED driver. However, these technologies have also encountered new issues without

sufficient advantage. The proposed technology contains the collective advantages from both single-stage and two-stage LED drivers while avoid their drawbacks. More importantly, no new disadvantages have arisen. This section discusses the advantages of the proposed system in great detail.

A. High efficiency

As demonstrated in Figure 2, the averaged voltages of V_{o1} and V_{o3} are 45V and 5V respectfully. 90% of the output power is delivered by Buck-Boost PFC directly while 10% of the output power is delivered by the Ripple Cancellation Converter, with the power delivered by Buck-Boost PFC being converted only once. As the input voltage of the Ripple Cancellation Converter is another output of Buck-Boost PFC, the power delivered by the Ripple Cancellation Converter is processed twice. Since the majority of power delivered to the LED Load has only been converted once, the overall efficiency of the proposed technology is very close to that of conventional Buck-Boost LED drivers. The following equation describes the efficiency performance achievable by the proposed technology.

$$Eff_{pos} = \frac{1}{\frac{0.9}{Eff_{PFC}} + \frac{0.1}{Eff_{PFC} \times Eff_{RCC}}} \tag{5}$$

In (5), Eff_{pos}, Eff_{PFC} and Eff_{RCC} represent the overall efficiency of the proposed technology, the efficiency of Buck-Boost PFC and the efficiency of Ripple Cancellation Converter respectively. Using equation 5, one may note that if 90% efficiency has been achieved by the Ripple Cancellation Converter, the proposed technology can achieve $0.99Eff_{PFC}$ efficiency, which is nearly the same efficiency a comparable conventional Buck-Boost LED driver can achieve.

B. Electrolytic capacitor-free

When high power factor has been achieved with single stage LED driver, there is an energy imbalance between the input and output ends of the LED driver. A significant output storage capacitor is necessary to accommodate this energy difference. The required capacitance can only be achieved using an electrolytic capacitor. However, electrolytic capacitors greatly limit the lifespan of an LED fixture. Eliminating electrolytic capacitors is highly desirable in LED driver design, and has been achieved in this proposed design.

Figure 5 demonstrates the energy imbalance between the input and output sides of the proposed LED driver in a half-line cycle. This energy imbalance presents itself as a low frequency voltage ripple on the PFC output. Approximating that all of the LED's power is delivered by V_{o1} , then the relationship between the energy imbalance and the voltage fluctuation becomes:

$$\begin{aligned} E_{imbalance} &= \frac{1}{2} C V_{o1\_\max}^2 - \frac{1}{2} C V_{o1\_\min}^2 \\ &= \frac{1}{2} C (V_{o1\_\max} + V_{o1\_\min})(V_{o1\_\max} - V_{o1\_\min}) \end{aligned} \tag{6}$$

In (6) , $E_{imbalance}$ is the energy imbalance in a half-line cycle. V_{o1_max} and V_{o1_min} represent the maximum and minimum values of V_{o1} in a half-line cycle period. C is the output capacitor of V_{o1}. The required capacitance to achieve a certain output voltage fluctuation becomes:

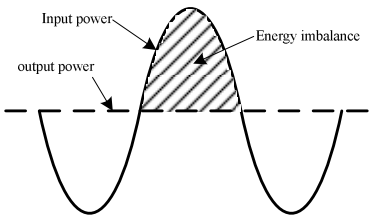

Figure 5 Input and output power waveform

$$C = \frac{E_{imbalance}}{\frac{(V_1 + V_2)}{2}(V_1 - V_2)} \tag{7}$$

For a 10W output power application with a 60Hz input line frequency, the energy imbalance, $E_{imbalance}$, in a half-line cycle is 0.0273J. With a 9V pk-pk low frequency ripple voltage allowed on $V_{o1,}$ the required output capacitance for V_{o1} can be as low as $55uF$. This capacitance can be achieved with a ceramic capacitor en lieu of an electrolytic. In the experimental prototype, three $20uF$ ceramic capacitor have been connected to the PFC output voltage V_{o1}.

C. Cost effective solution

The input voltage and output voltage of the Ripple Cancellation Converter is in the vicinity of 10V. An integrated circuit which includes MOSFETs, gate driver, and controllers is widely available implement the Ripple Cancellation Converter. Thus, cost of the Ripple Cancellation Converter is minor compared to the overall component cost of a comparable Buck-Boost LED Driver. Combining PFC controller and the Ripple Cancellation Converter into a single integrated circuit package will further reduce component costs and the design complexity. Section V examines this point in further detail

IV. DETAIL CIRCUIT DESIGN CONSIDERATION

Low power level Buck-Boost PFC operating under Constant On Time Discontinues Conduction Mode (COTDCM) can inherently achieve high power factor and reduces switching loss. Figure 6 shows the input current waveform of a Buck-Boost PFC working under COTDCM.

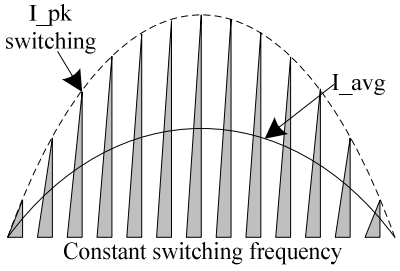

Figure 6 Input current of Buck-Boost PFC working under COTDCM

The following equations demonstrate why high power factor can be achieved when Buck-Boost PFC operate under COTDCM.

The peak input current in a switching cycle:

$$I_{in\_pk} = \frac{V_{in} \times T_{on}}{L} \tag{8}$$

The averaged input current in a switching cycle:

$$I_{in\_ave} = \frac{I_{in\_pk} \times T_{on}}{2T_s} = \frac{V_{in} \times T_{on}^2}{2L \times T_s} \tag{9}$$

It can be shown from (8) and (9) that the averaged input current is proportional to the input voltage, hence achieving a high power factor.

The inductor current discharge time must be calculated to achieve DCM operation and optimized switching frequency. This calculation is straightforward for single output PFC where only one output has an effect on the current discharge time. However, the calculation for two PFC outputs is more complex. One must analyze how two outputs have effect on the current discharge time.

For a multiple-windings derived multiple-outputs DC-DC converter, the reflected voltages (based on their turns ratios) are equal for all outputs. Looking from the input side, the collective effect of all outputs is like a single one. However, the case for multiple outputs PFC is complicated.

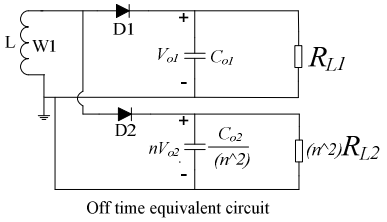

Figure 7 Two outputs Buck-Boost PFC off time equivalent circuit

Compared to Figure 1(b), the circuit connected to winding *W2* has now been equivalently reflected to main winding *W1* in Figure 7. The turn ratio between the two windings *W1:W2* is *n*. In a half AC line cycle, the output waveforms of V_{o1} and nV_{o2}, as well as how current flows in the two outputs have been shown in Figure 8.

To have a clear understanding of how the current discharge time is affected, the waveform relationship between V_{o1} and V_{o2} has been analyzed. Parasitic components and diode forward drop voltages have been neglected in the analysis and the following symbols have been defined:

E_{in1}: Inductor energy transfer to output voltage V_{o1} during off time in a switching cycle

E_{in2}: Inductor energy transfer to output voltage V_{o2} during off time in a switching cycle

E_{o1}: Energy deliver to load by V_{o1} in a switching cycle

E_{o2}: Energy deliver to load by V_{o2} in a switching cycle

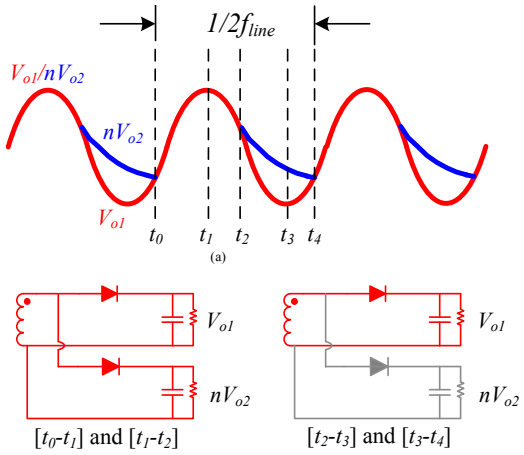

Figure 8 Output voltages and timing of current flow

As demonstrated in Figure 8, there are four distinctive operation conditions for this two-output Buck-Boost PFC during the switching off period.

Interval $[t_0\text{-}t_1]$

This interval begins at t_0. Two voltages V_{o1} and nV_{o2} are equal and rise simultaneously. During this time interval, the following relationship exists:

$$\begin{aligned} E_{in1} &> E_{o1} \\ E_{in2} &> E_{o2} \\ V_{o1} &= nV_{o2} \end{aligned} \tag{10}$$

For each output, the energy transferred from the inductor is higher than the energy that is being delivered to the load. The two voltages V_{o1} and nV_{o2} must be equal. Otherwise, the inductor current will only flow to the lesser voltage of the two, and eventually they will be equal.

Interval $[t_1\text{-}t_2]$

This time interval begins at t_1. Both output voltages reach peak value before falling. The following relationship exists:

$$\begin{aligned} E_{in1} &< E_{o1} \\ E_{in2} &< E_{o2} \\ V_{o1} &= V_{o2} \end{aligned} \tag{11}$$

In this interval, the inductor energy transferred to each output is less than the energy that V_{o1} and V_{o2} deliver to the load (Hence why both output voltages fall). The inductor energy is distributed in such a way that both voltages can be kept equal.

Interval $[t_2\text{-}t_3]$

This time interval begins at t_2. The waveforms of two output voltage start splitting, with the following trigger:

$$
\begin{aligned}
&E_{in1} < E_{o1} \\
&E_{in2} = 0 \\
&E_{o1} - E_{in1} = \frac{1}{2}C_1 V_{o1}^2 - \frac{1}{2}C_1 (V_{o1} - \Delta V_{o1})^2 \\
&E_{o2} = \frac{1}{2}C_2 (nV_{o2})^2 - \frac{1}{2}C_2 (nV_{o2} - \Delta V_{o2})^2 \\
&\Delta V_{o1} > \Delta V_{o2}
\end{aligned} \tag{12}
$$

The condition that two output voltages are equal can no longer be maintained. Since V_{o1} is much more heavily loaded than nV_{o2} with respect to their connected capacitors, V_{o1} will fall at a greater rate than nV_{o2} even if all energy from the inductors is dedicated to V_{o1}. This results in diverging waveforms. In the remaining time of this interval, V_{o1} is always lower than nV_{o2}. All inductor energy flows entirely to V_{o1}. V_{o1} continues decreasing until time t_3, when the inductor energy transfer to output V_{o1} is equal to the energy that V_{o1} provides to the load.

Interval [t_3-t_4]

This time interval begins at t_3. Again, the output voltage V_{o1} starts rising, with the following relationship:

$$
\begin{aligned}
&E_{in1} > E_{o1} \\
&E_{in2} = 0
\end{aligned} \tag{13}
$$

Since voltage V_{o1} is still lower than nV_{o2}, all inductor energy is still dedicated to V_{o1}. nV_{o2} continues to fall within this time interval. This relationship ends at t_4 when V_{o1} and nV_{o2} cross, completing the operating cycle.

The above analysis has formulaically described the relationship between V_{o1}, nV_{o2} , as well as demonstrating how the inductor current flows through each output. This information has additionally been summarized below in Table 1.

Table 1 voltage across inductor during switch off period

Time interval	Voltage across inductor
t_0-t_1	V_{o1} or nV_{o2}
t_1-t_2	V_{o1} or nV_{o2}
t_2-t_3	V_{o1}
t_3-t_4	V_{o1}

To reiterate, there are four distinctive operation conditions for this two-output Buck-Boost PFC, where the effective output voltage across inductor during switching off period is always V_{o1}. When calculating the current discharge time, only V_{o1} need be considered.

V. Ripple Cancellation Converter Integration

It has been discussed in section II that the Ripple Cancellation Converter can be implemented by a single package voltage regulator. In order to further reduce component costs and to simplify the engineering design, an analysis on how to achieve PFC controller and the Ripple Cancellation Converter integration has been done.

Figure 9 shows the integrated solution of the proposed technology. Inside the blue box, the PFC controller and the Ripple Cancellation Converter circuitry have been combined. Compared to conventional Buck-Boost LED drivers, very few components have been added (marked in red). The overall cost of the proposed design is therefore comparable to that of a conventional Buck-Boost LED Driver.

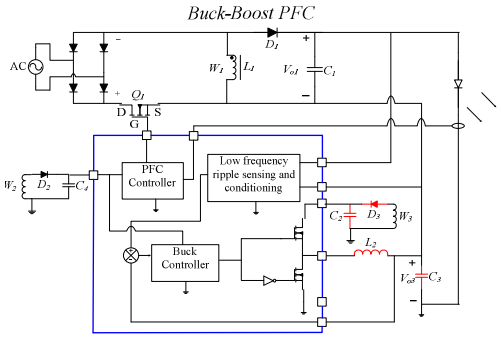

Figure 9 Integrated solution for the proposed technology

However, one issue with this integrated solution is an insufficient gate driving voltage for the MOSFET Q_1. In Figure 9, the ground level of the PFC controller and the Buck controller . In this structure, the source terminal of Q_1 is lifted by the Ripple Cancellation Converter output V_{o3}. The gate driving voltage of Q_1 can be described by (14):

$$
V_{gs} = V_g - V_s = V_{DD} - V_{o3} \tag{14}
$$

In (14), V_{DD} is the supply voltage of the PFC controller, which is also the gate voltage when the output logic is high. A numerical example can interpret the severity of this issue. Given that the output voltage V_{o3} swings from 0.5V to 9.5V in the experimental prototype, if the supply voltage V_{DD} for PFC controller is 14V, then the minimum gate driving voltage for Q_1 becomes 4.5V, which is very marginal to turn on Q_1 or leave Q_1 with high on-resistance. Increasing the supply voltage for the PFC controller can alleviate this issue. However, this is a compromised solution since the static power consumption for PFC controller and Buck controller will both increase.

In order to solve this insufficient gate driving issue, a gate driver circuit is required. A conventional gate driver circuit using bootstrap technology cannot work in this situation. The voltage presenting on the source terminal of Q_1 is not a pulsating voltage. Therefore, a dedicated gate driver circuit has been designed for the experimental prototype. Figure 10 illustrates the working principle of this gate driver.

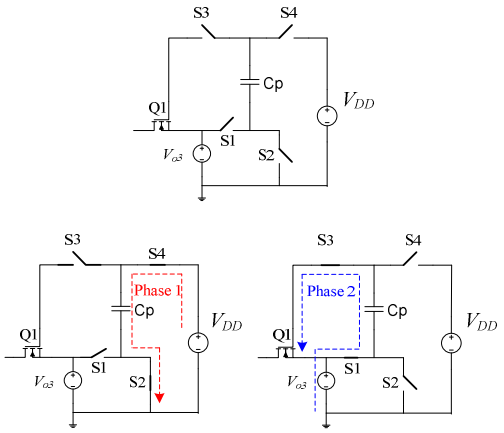

Figure 10 Dedicated designed gate driver for the proposed integrated

The Ripple Cancellation Converter output V_{o3} and the PFC controller supply voltage V_{DD} have been shown in Figure 10. The source terminal of Q_1 is connected to V_{o3}. There are two phases of operations associated with the switches in Figure 10. Table 2 shows the states of each switch in both phases.

Table 2 Switches states table for the gate driver

Phase 1	Phase 2
S1 open	S1 closed
S3 open	S3 closed
S2 closed	S2 open
S4 closed	S4 open

In phase 1, switches S_2 and S_4 are closed and the pumping capacitor C_p will be charged by V_{DD}. In phase 2, S_1 and S_3 are closed and pumping capacitor C_p is placed on top of V_{o3}. MOSFET Q1 will be turned on during phase 2. This way, the voltage applied to the gate terminal of Q_1 during turn on become:

$$V_g = V_{DD} + V_{o3} \tag{15}$$

So the voltage level on the gate terminal of Q_1 has also been increased by V_{o3}. The effective V_{gs} for Q_1 becomes independent of V_{o3}.

VI. EXPERIMENTAL RESULTS

A 10W Buck-Boost LED driver with low frequency ripple cancellation has been built to verify the proposed technology. The circuit diagram is shown in Figure 11 and the circuit parameters are summarized in Table 3.

Table 3 Circuit parameter

Input voltage range	Universal AC input
LED driver output	50V
Buck-Boost PFC output (DC)	45V
Buck-Boost PFC output (120Hz Ripple)	-4.5V to +4.5V
Ripple Cancellation Converter output (DC)	5V
Ripple Cancellation Converter output (120Hz Ripple)	-4.5V to +4.5V
Coupled inductor W1	985uH
Coupled inductor W2	82uF
Buck-Boost PFC output capacitor	60uF
Ripple Cancellation Converter input capacitor	20uF
Ripple Cancellation Converter output capacitor	10uF

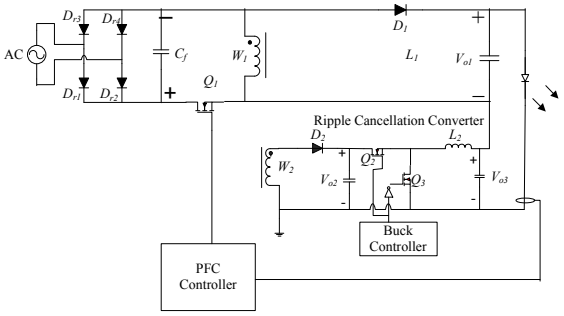

Figure 11 Circuit diagram of the experimental prototype

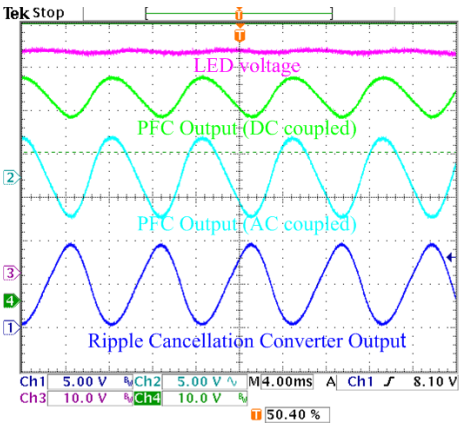

Figure 12 Ripple cancellation between PFC and RCC output

Figure 12 demonstrates the low frequency cancellation between the PFC output V_{o1} and the Ripple Cancellation Converter output V_{o3}. The original ripple from V_{o1} is up to 9V pk-pk. After ripple cancellation, the ripple voltage presenting on LED string has been greatly reduced to only 0.75V.

In order to make an objective evaluation on the proposed technology, comparisons of the ripple current and efficiency have been made between a conventional Buck-Boost LED driver and the proposed technology. The Buck-Boost PFC inside both technologies are identical and are connected to a 60uF output capacitor.

As it is shown in Figure 13, the ripple current with a conventional Buck-Boost LED driver is as high as 250mA. With ripple cancellation technology, the low frequency ripple current has been reduced to 20mA. The reduction ratio is as great as 12.5 times.

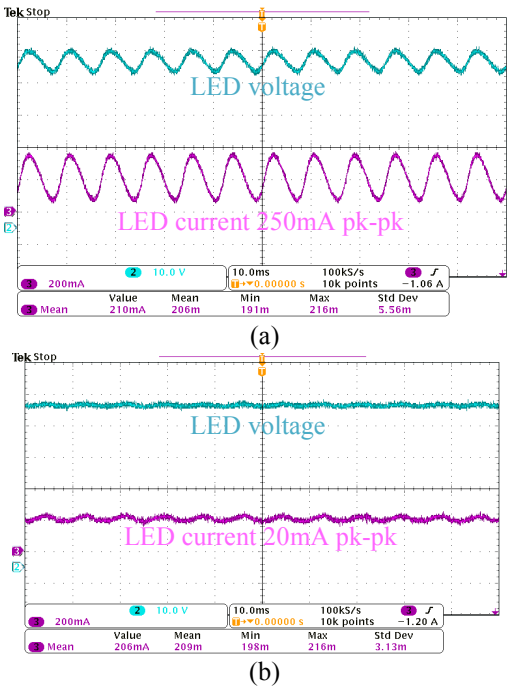

Figure 13 Ripple current comparison (a) The conventional Buck-Boost LED driver; (b) The proposed technology

As the characteristic of LED light in general, there is a linear relationship between LED current to light output. So the low frequency ripple current from LED driver should be linearly reflected as lighting fluctuation. In order to clearly demonstrate the advantage of the proposed technology in the form of light output, a experimental to characterize LED current ripple to LED lighting fluctuation has been done.

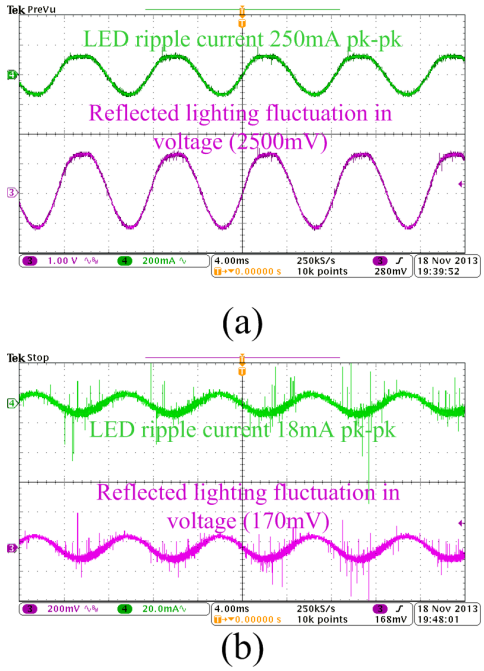

Figure 14 Lighting fluctuation comparison (a) The conventional Buck-Boost LED driver; (b) The proposed LED driver

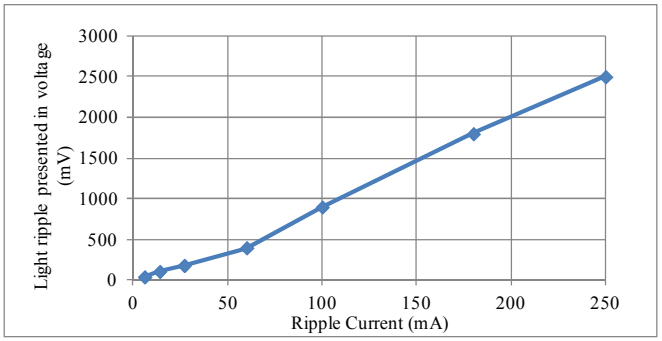

Figure 15 LED Ripple current V.S Lighting fluctuation

A Luminance to voltage conversion device has been made to capture LED light fluctuation. Figure 14 shows the lighting fluctuation comparison when LED string is driven by the proposed LED driver and the conventional Buck-Boost LED driver. In Figure 15, the relationship between LED current ripple and lighting fluctuation has been plotted. The voltage values in Y-axis represent the light ripple. It has demonstrated that a almost linear relationship exist between LED ripple current and LED light fluctuation.

Figure 16 shows the efficiency comparison between the conventional Buck-Boost LED driver and the proposed technology. Since 90% of the output power is delivered by the Buck-Boost PFC and has only been converted once, the overall efficiency of the proposed technology is very close to that of a conventional Buck-Boost LED driver. The efficiency achieved with the proposed technology is only 1% lower than the conventional Buck-Boost LED driver.

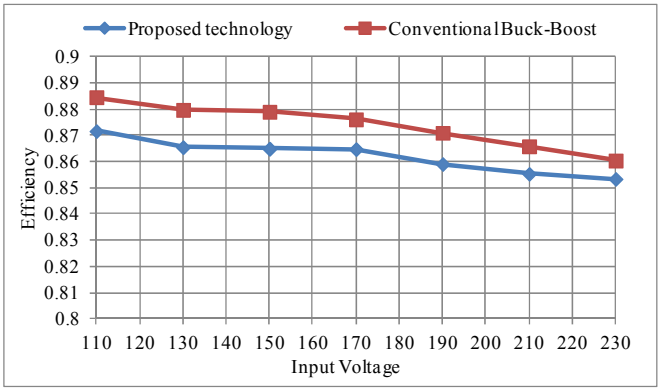

Figure 16 Efficiency comparison between conventional Buck-Boost LED driver and the composed technology

Figure 17 shows the gate driving waveform for MOSFET Q_1. As previously discussed, the dedicated designed gate driver has increased the gate driving signal by the output of the Ripple Cancellation Converter. Thus, the voltage difference between the gate and source terminal of Q_1 is independent of the Ripple Cancellation Converter output voltage.

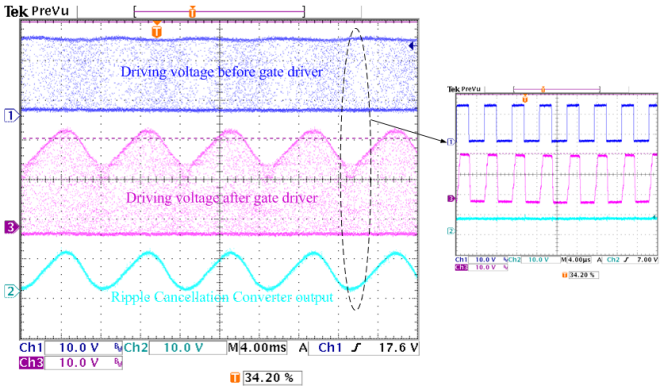

Figure 17 Gate driver waveform

VII. CONCLUSION

This paper has proposed and evaluated an innovative Buck-Boost LED driver with ripple cancellation. The proposed design has achieved high power efficiency, has maintained low component costs, and has enabled a low frequency ripple-free LED current. The lifespan of the LED driver has also been increased through the elimination of an electrolytic output capacitor. This paper has also analyzed an integrated solution in great detail further reducing component costs and simplifying the engineering design. A gate driving issue with integrated solution has been identified and solutions have also been proposed.

A universal input, 10 W output Buck-Boost LED driver prototype has been built and tested to verify the proposed technology. Experimental results strongly support the formulaic analysis. Up to 87.5% efficiency has been achieved in the experimental prototype, which is only 1% lower than the efficiency of conventional technology. Additionally, the electrolytic capacitor has been replaced with a 60uF ceramic capacitor Lastly, the low frequency ripple current has been greatly reduced from 250mA in conventional technology to 20mA in the proposed technology.

APPEDIX

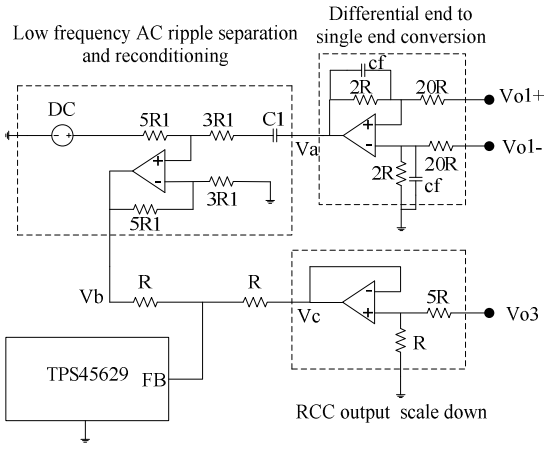

Figure 18 Detail circuit implementation of Ripple Cancellation Converter

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