A Digital Adaptive Discontinuous Current Source Driver for High-Frequency Interleaved Boost PFC Converters

Zhiliang Zhang, *Member, IEEE*, Chuangang Xu, and Yan-Fei Liu, *Fellow, IEEE*

***Abstract*—A digital adaptive current source driver (CSD) is proposed for the interleaved Boost PFC converter. The adaptive drive current is achieved for the CSDs to optimize the switching loss and gate drive loss according to different turn-on and turn-off drain currents in a wide load range. Compared to the adaptive CSDs with the linear regulator, the digital adaptive CSD is able to eliminate the additional loss and cost introduced by the linear regulator. The most important benefit of the digital CSD is that the turn-on and turn-off drive current can be adjusted independently according to the different turn-on and turn-off drain currents. At the same time, the proposed digital CSD is compatible with other advanced digital control technique. The proposed digital CSD is applied to the interleaved Boost PFC converter under critical conduction mode (CRM) to reduce the high turn-off loss and gate drive loss. A 220-V_{AC} input, 380-V/400-W output, two-phase interleaved Boost PFC converter with the switching frequency of 90–500 kHz under CRM was built to verify the functionality and advantages of the digital CSD.**

***Index Terms*—Adaptive drive current, current source driver, digital control, power factor correction, power MOSFET.**

I. Introduction

HIGH switching frequency as a trend can provide faster transient response, smaller passive components' size, and higher power density [1]. However, the frequency-related switching loss and gate drive loss increase if the conventional voltage source drivers (VSDs) are used [2].

Resonant gate drivers (RGDs) have attracted much attention in high-frequency applications [3]–[5]. This technique has been investigated extensively for the power MOSFETs to reduce the gate drive power consumption and usually requires an inductor connected in series with the gate terminal [6]. In [7], the SiC MOSFETs' gate driver circuit that introduced a negative voltage feedback loop to control the on-stage gate voltage to a desired value was proposed to suppress the ringing following a rapid rise in the gate voltage. A resonant gate-drive circuit was proposed in [8] that provided the parallel paths for charging the gate-to-emitter capacitance of the SiC MOSFETs. A resonant inductor path provides the sufficient charging current for the full conduction of the SiC MOSFETs. The remaining current provided by an alternate low loss path charges the gate capacitance to a full gate voltage.

Similarly to the RGDs, the CSD technique has been proposed in the high-frequency, high-current, and low-voltage applications such as voltage regulators (VRs). The basic idea of the CSD technique is to generate the constant drive current to charge and discharge the gate capacitance of the power MOSFETs to accelerate the switching speed and reduce the switching loss. The full-bridge (FB) CSD was proposed for the power MOSFETs to achieve quick turn-on and turn-off interval time to reduce the switching loss and the conduction loss in [9]. In addition, it can recover a portion of CV^2 gate energy that normally dissipated in the conventional VSDs. The current of the current source (CS) inductor is discontinuous in order to minimize the circulating loss of the drive circuit. In [10] and [11], the discontinuous CSD was applied to the Boost converter to verify its advantages of the efficiency improvement over the conventional VSD. To overcome the current diversion problem, the blocking diode was introduced to the CSDs and the fast switching capability was further improved in [12]. The two half-bridge (HB) CSD circuit was used to drive the high-side and low-side MOSFETs independently in a synchronous Buck converter in [13] with different drive currents for the different optimal design objectives. In [14], the FB high-dynamic range current source gate driver (HD-CSD) circuit was proposed to reduce the hard switching loss of the high-side switch in the Buck converters.

However, the aforementioned CSDs drive the power MOSFETs with the constant drive current. When the load condition varies, the constant drive current could hardly achieve optimal design between the switching loss and drive loss anymore. For the CSD technology, higher drive current leads to faster switching speed and reduced switching loss. Meantime, higher drive current also increases the drive circuit loss. Therefore, the "adaptive" concept was proposed. The most important point of the "adaptive" concept is to realize the design tradeoff between the switching loss and drive circuit loss dynamically.

In recent years, it is noted that the adaptive CSDs have also been reported for the Boost PFC converters. The HB adaptive

Manuscript received November 21, 2012; revised February 8, 2013 and March 28, 2013; accepted April 18, 2013. Date of current version September 18, 2013. This work was supported by the Nanjing University of Aeronautics and Astronautics Research Funding 3082013NS2013097. Recommended for publication by Associate Editor C. A. Canesin.

Z. Zhang is with the Jiangsu Key Laboratory of New Energy Generation and Power Conversion, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: zlzhang@nuaa.edu.cn).

C. Xu was with the Jiangsu Key Laboratory of New Energy Generation and Power Conversion, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China. He is now with Bel Power Corporation, Hangzhou, China (e-mail: xucg1988@nuaa.edu.cn).

Y.-F. Liu is with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6 Canada (e-mail: yanfei.liu@queensu.ca).

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Digital Object Identifier 10.1109/TPEL.2013.2260175

continuous CSD was adopted in [15] due to its simple topology and control. In [16] and [17], the FB adaptive continuous CSD was used to eliminate the blocking capacitor in the HB topology to improve its dynamic performance. However, the continuous adaptive CSD has the following disadvantages:

1) the drive current is associated with the switching frequency, the duty cycle, and the drive voltage. Therefore, the continuous CSD is not suitable to the variable frequency applications;
2) the drive current strongly depends on the drive voltage and duty cycle. Therefore, the optimal design and realization of the adaptive drive current is complicated;
3) the turn-on and turn-off drive current can only be the same which reduces the effectiveness of the efficiency improvement in a wide range;
4) the CS inductor current is continuous, which results in high circulating loss in the drive circuit.

To realize the decoupling between the drive current, the duty cycle, and the switching frequency, the control strategy of the HB and FB CSDs is modified in [18] and [19], respectively. The adaptive drive current is adjusted by the drive voltage that is realized by the analog linear regulator. The drive current is only related to the drive voltage. Therefore, the relationship between the adaptive current and the load current is simple and can be easily realized. The CS inductor current is discontinuous, which leads to the reduced circulating loss in the drive circuit. However, the aforementioned discontinuous adaptive CSD is realized by the analog linear regulator which causes high additional loss and cost.

Due to the complexity and loss of the analog realization of the adaptive CSD, the digital controller is adopted. The digital controller owns the advantages over the analog controllers such as the higher level of integration, higher efficiency, smaller volume, faster dynamic response, lower sensitivity to external influences, and more control flexibility [20]. In [21], a digital adaptive slope control was proposed to improve the dynamic response of a current-mode buck converter. In [22], the digital controller was used to set the optimal number of the power switch segments and the gate voltage swing level for the power MOSFETs to realize the tradeoff between the gate drive loss and conduction loss over the full load range. A simple digital implementation was introduced to tune the synchronous rectification (SR) turn-off time and gate driving signals to eliminate the body diode conduction [23]. Due to the applications and advantages of the digital control, the DSP-based digital control was considered in this paper in order to combine the advantages of the digital control and "adaptive" concept.

The objective of this paper is to present a digital adaptive CSD with the discontinuous CS inductor current. Compared to other CSDs proposed in the previous work, the proposed digital adaptive CSD reduces loss caused by the analog regulator and lowers the complexity of the drive circuit. The adaptive drive current is independent of the duty cycle and switching frequency. Therefore, the digital adaptive CSD is suitable to the variable frequency applications. The turn-on and turn-off current can also be realized independently to improve the efficiency further under the different turn-on and turn-off conditions.

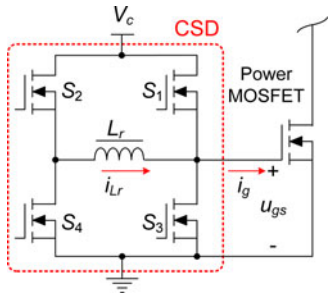

Fig. 1. Topology of an FB CSD.

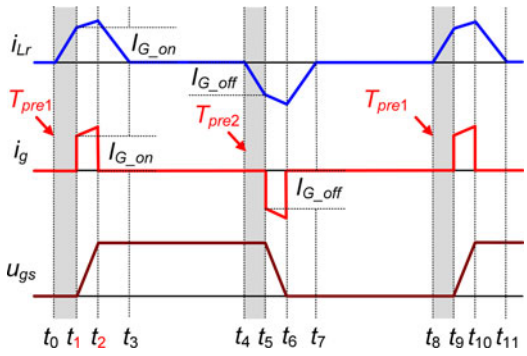

Fig. 2. Key waveforms of the discontinuous CSD.

This paper is organized as follows: Section II presents the principle of the proposed digital adaptive discontinuous CSD. Section III presents the design procedure and implementation. Section IV contains the experimental results and discussion. Section V provides a brief conclusion.

II. Principle of the Proposed Digital Adaptive Discontinuous CSD

A. Topology of the FB CSD

The topology of the digital adaptive CSD is the FB structure as shown in Fig. 1. It consists of four drive switches, S_1-S_4 and a small resonant inductor L_r. V_c is the drive voltage.

Fig. 2 shows the key waveforms of the CSD. The CS inductor current is discontinuous to achieve the lower circulating loss of the drive circuit. From Fig. 2, S_1-S_4 are, respectively, controlled to generate the desired CS inductor current i_{Lr} to provide the nearly constant drive current to turn on and turn off the main power MOSFET. During the turn-on $[t_1, t_2]$ and turn-off $[t_5, t_6]$ interval of the power MOSFET, the turn-on drive current I_{G_on} and the turn-off drive current I_{G_off} can be considered nearly constant to increase the turn-on and turn-off speed to reduce the switching loss.

B. Analysis of the Drive Current

To achieve the adaptive drive current, the turn-on and turn-off intervals are analyzed as follows. The equivalent circuit of the turn-on interval is shown in Fig. 3. C_{gs} is the gate capacitance of the power MOSFET.

Interval [t_0, t_1] [Fig. 3(a)]: This interval is the turn-on precharge interval. Prior to t_0, S_3 is ON. During the precharge

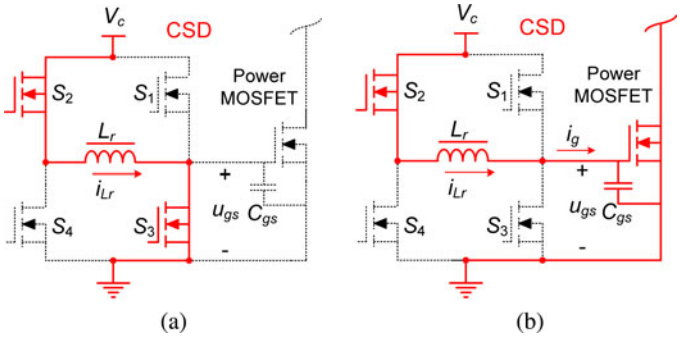

Fig. 3. Equivalent circuit: turn-on interval. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$.

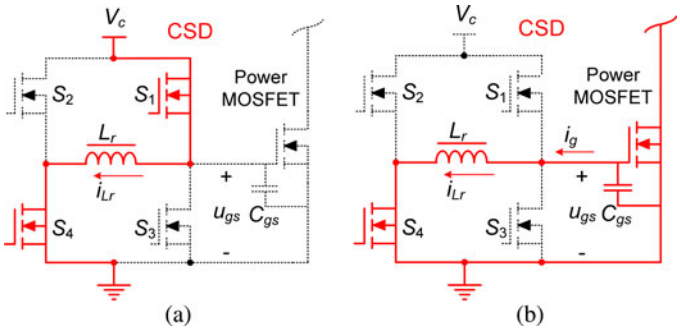

Fig. 4. Equivalent circuit: turn-off interval. (a) $[t_4, t_5]$. (b) $[t_5, t_6]$.

time, S_3 remains ON. At t_0, S_2 turns ON. The CS inductor suffers the forward voltage. i_{Lr} begins to ramp up. At t_1, i_{Lr} reaches the predesigned turn-on drive current value. The turn-on precharge interval ends.

Interval [t_1, t_2] [Fig. 3(b)]: S_2 remains ON during this interval. At t_1, S_3 turns OFF and the CS inductor begins to charge the gate capacitance $C_{\rm gs}$ of the power MOSFET. i_{Lr} ramps up but at a lower slope as the voltage across the gate capacitance increases. The gate-to-source voltage $u_{\rm gs}$ reaches the drive voltage V_c at t_2. The turn-on interval ends.

From the aforementioned analysis and Fig. 3, the turn-on drive current $I_{G\_\rm on}$ can be considered nearly constant as approximately

$$I_{G\_\rm on} = \frac{V_c T_{\rm pre1}}{L_r} \tag{1}$$

where $T_{\rm pre1}$ is the turn-on precharge time of the CS inductor.

The equivalent circuit of the turn-off interval is shown in Fig. 4.

Interval [t_4, t_5] [Fig. 4(a)]: This interval is the turn-off precharge interval. At t_4, the CS inductor suffers the negative voltage; i_{Lr} begins to ramp up negatively until it reaches the pre-designed turn-off drive current value at t_5. The turn-off precharge interval ends.

Interval [t_5, t_6] [Fig. 4(b)]: At t_5, S_1 turns OFF and S_4 remains ON during this interval. The CS inductor begins to discharge $C_{\rm gs}$. i_{Lr} still ramps up negatively at a lower slope as the voltage across the gate capacitance decreases toward zero. At $t_6, u_{\rm gs}$ reaches zero. The turn-off interval ends.

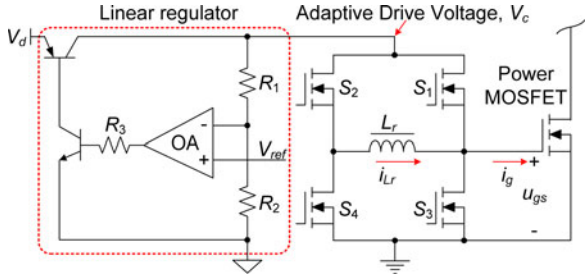

Fig. 5. Linear regulator to realize adaptive drive voltage V_c.

According to Fig. 4 and the above analysis, the turn-off drive current $I_{G\_\rm off}$ is

$$I_{G\_\rm off} = \frac{V_c T_{\rm pre2}}{L_r} \tag{2}$$

where $T_{\rm pre2}$ is the turn-off precharge time of the CS inductor.

From (1) and (2), it is noted that the turn-on drive current $I_{G\_\rm on}$ and turn-off drive current $I_{G\_\rm off}$ are independent of the duty cycle and switching frequency. The drive current can be adjusted by the drive voltage V_c or the CS inductor precharge time $T_{\rm pre1}$ and $T_{\rm pre2}$.

1) Drive Voltage-Based Analog Adaptive CSD: The drive voltage-based adaptive CSD was realized by the analog linear regulator as shown in Fig. 5. V_d is the supply voltage. $V_{\rm ref}$ is the control signal of the adaptive drive voltage. V_c follows the track of $V_{\rm ref}$ to realize the adaptive drive voltage. In this way, the gate drive current can be adjusted. The advantages of using the linear regulator are its simple implementation and fast response. However, the turn-on and turn-off drive current have to be the same which is not suitable for different turn-on and turn-off conditions. In addition, the linear regulator results in the additional loss and high complexity of the drive circuit.

2) Proposed Precharge Time-Based Digital Adaptive CSD: In order to solve the problems of the analog adaptive CSD, the digital adaptive CSD is proposed by adjusting $T_{\rm pre1}$ and $T_{\rm pre2}$ to realize the adaptive turn-on drive current $I_{G\_\rm on}$ and turn-off drive current $I_{G\_\rm off}$.

Fig. 6 illustrates the control gating signals of the four drive switches $S_1 - S_4$, the resonant inductor current i_{Lr}, the drive current i_g, and the power MOSFET gate-to-source voltage $u_{\rm gs}$. $T_{\rm pre1}$ and $T_{\rm pre2}$ are the precharge time of the CS inductor as shown in the shaded area. $I_{G\_\rm on}$ and $I_{G\_\rm off}$ are the turn-on drive current and turn-off drive current, respectively. *VAL*1–*VAL*4 corresponds to the rising edge of S_2, the falling edge of S_3, the rising edge of S_4, the falling edge of S_1, respectively. *VAL*1–*VAL*4 are the pulse width modulation (PWM) register values in the digital controller which are used to control the duty cycle and period of the PWM signals. The basic idea is to adjust the time interval between *VAL*1 and *VAL*2, and the time interval between *VAL*3 and *VAL*4 in the digital controller so that the precharge time $T_{\rm pre1}$ and $T_{\rm pre2}$ can be adjusted accordingly.

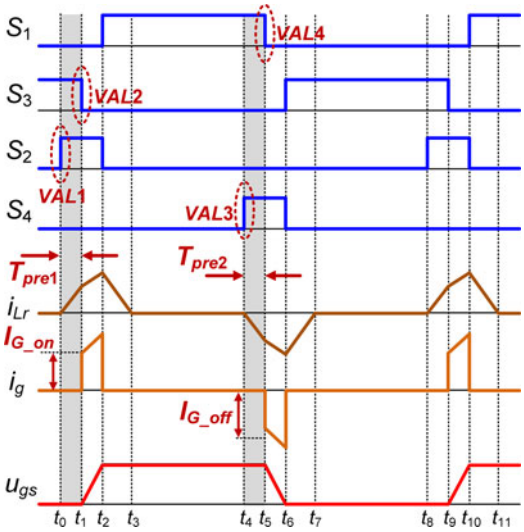

Fig. 6. Key waveforms of the proposed digital adaptive CSD.

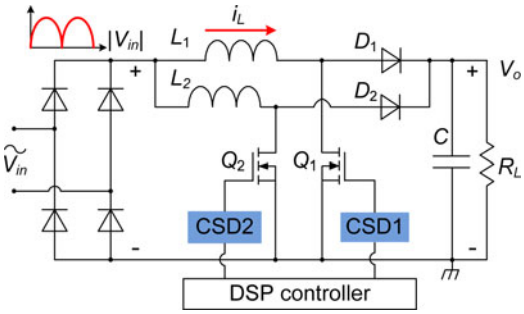

Fig. 7. Two-phase interleaved Boost PFC converter.

III. Design Procedure and Implementation

A. Interleaved Boost PFC Converter Under CRM

In this paper, the proposed digital adaptive CSD was applied to a two-phase interleaved Boost PFC converter under CRM to verify its functionality and advantages. The benefits of the interleaved mode are the reduced current ripple and components current stress, and increased power level [24]. The main power stage is shown in Fig. 7. The reason to choose the CRM mode is that the power MOSFET owes the different turn-on and turn-off conditions.

Fig. 8 gives the boost inductor current i_L and gate-to-source voltage $v_{\mathrm{gs\_mos}}$ during half-line period. When the inductor current crosses zero, the switch turns ON. When the boost inductor current i_L ramps up till it reaches the reference current i_{L_ref}, the switch turns OFF at this instant. Since the current through the boost diode decays to zero before the power MOSFET turns ON, there is no reverse recovery loss in the boost diode [25], [26]. It is noted that the main switching loss under CRM is the turn-off loss because the power MOSFET turns ON at zero current but turns OFF at a high reference current which is twice of the average current i_{L_avg} [27]. Therefore, it is beneficial for the digital adaptive CSD to generate different turn-on and turn-off drive currents individually according to different drain currents in this application.

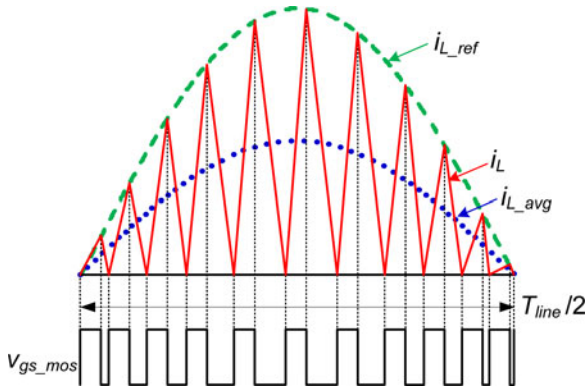

Fig. 8. Boost inductor current and $V_{\mathrm{gs\_mos}}$ of power MOSFET during half-line period.

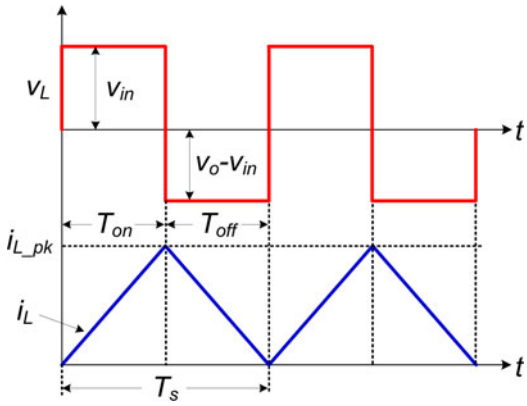

Fig. 9. Voltage and current across the boost inductor.

Due to CRM, the switching frequency of the Boost PFC converter is variable. Therefore, the loss calculation of the variable frequency condition is different to that of the constant frequency condition. The adaptive drive current design is based on the loss analysis. Therefore, for the optimal design of the adaptive drive current, the variable switching frequency is calculated as follows.

Fig. 9 shows the voltage and current across the boost inductor. During a switching period, the peak current across the inductor which equals the turn-off drain current of the power MOSFET is

$$i_{L\_\mathrm{ref}}(t) = \frac{v_{\mathrm{in}}(t)T_{\mathrm{on}}}{L} \tag{3}$$

where L is the boost inductor; $v_{\mathrm{in}}(t)$ is the instantaneous input voltage; and T_{on} is the on time of the power MOSFET during a switching period.

From (3), the instantaneous average input current and the instantaneous input power are, respectively

$$i_{L\_\mathrm{avg}}(t) = \frac{v_{\mathrm{in}}(t)T_{\mathrm{on}}}{2L} \tag{4}$$

$$p_{\mathrm{in}}(t) = v_{\mathrm{in}}(t)i_{L\_\mathrm{avg}}(t) = \sqrt{2}V_{\mathrm{in}}\sin(\omega t) \cdot \frac{\sqrt{2}V_{\mathrm{in}}\sin(\omega t)T_{\mathrm{on}}}{2L} = \frac{V_{\mathrm{in}}^2\sin^2(\omega t)T_{\mathrm{on}}}{L} \tag{5}$$

where $V_{\rm in}$ is the input RMS voltage and ω is the line angular frequency.

From (5), the input energy $W_{\rm in}$ during half-line period is

$$W_{\rm in} = \int_0^{T_{\rm line}/2} p_{\rm in}(t)dt = \frac{V_{\rm in}^2 T_{\rm on} T_{\rm line}}{4L}. \quad (6)$$

The output energy W_o during half-line period is

$$W_o = \frac{V_o^2 T_{\rm line}}{2R_L} \quad (7)$$

where R_L is the load resistance.

Considering the power conversion efficiency η

$$W_o = W_{\rm in}\eta. \quad (8)$$

According to (6)–(8), the on time $T_{\rm on}$ is

$$T_{\rm on} = \frac{2LP_o}{\eta V_{\rm in}^2}. \quad (9)$$

It is noted that the on time $T_{\rm on}$ is a constant value for a given input voltage and load. The off time is

$$T_{\rm off} = T_{\rm on}\frac{v_{\rm in}(t)}{V_o - v_{\rm in}(t)}. \quad (10)$$

From (9) and (10), the switching frequency f_s is

$$f_s = \frac{1}{T_{\rm on} + T_{\rm off}} = \frac{V_o - v_{\rm in}(t)}{V_o T_{\rm on}}. \quad (11)$$

It is observed from (11) that the switching frequency of the Boost PFC converter under CRM varies following the input voltage. From (3) and (11), the relationship between the switching frequency f_s and the turn-off drain current i_D that equals $i_{L\_\rm ref}(t)$ during a switching period is

$$f_s = \frac{V_o - \frac{i_{L\_\rm ref}(t)\cdot L}{T_{\rm on}}}{V_o \cdot T_{\rm on}}. \quad (12)$$

In the experimental verification, the specifications of the two-phase interleaved Boost PFC converter are as follows: 220-$V_{\rm AC}$ input, 380-V/ 400-W output. The boost inductor $L = 220$ μH; the output capacitor $C = 440$ μF. Therefore, the switching frequency f_s of one phase varies from 90 to 500 kHz. The CSD part was built using the discrete components. The FDN335N N-channel MOSFETs were used as the drive MOSFETs. The air core inductor from Coilcraft 1812SMS-R12 was used as the CS inductor [28]. The circuit parameters are summarized in Table I.

TABLE I
CSD DESIGN PARAMETERS

Circuit Parameters	
Switching Frequency, f_s	90 kHz~500 kHz
Gate Drive Voltage, V_c	12 V
Power MOSFET	IPP60R099CPA
Total Gate Charge@V_{gs}=12 V	60 nC
Internal Gate Resistance, R_g	1.3 Ω
Drive switches S_1-S_4	FDN335N
On Resistance, R_{DS_on}	70 mΩ
Total Gate Charge@V_{gs}=5 V	3.5 nC
CS Inductor L_r	1812SMS-R12
Inductor Value	120 nH
CS Inductor Resistance	17.3 mΩ

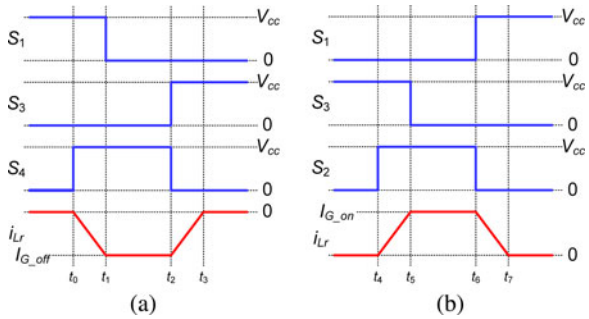

Fig. 10. Gating signals of S_1-S_4 and CS inductor current during switching-transition. (a) Turn-off interval. (b) Turn-on interval.

B. Design Procedure of the Adaptive Drive Current

The adaptive drive current is chosen based on the tradeoff between the drive circuit loss and switching loss. The loss analysis provides the design guideline for the proposed digital adaptive CSD. Although the switching frequency is variable during half-line period, the loss calculation of every switching cycle can be regarded as similar to the constant frequency condition. The basic idea is that the proper drive current is calculated to achieve the lowest total loss during every switching cycle so that the total loss during half-line period can be minimized.

Since the turn-on and turn-off drain current are different, the turn-on drive current $I_{G\_\rm on}$ and turn-off drive current $I_{G\_\rm off}$ are designed, respectively. Compared to the turn-off loss, the turn-on loss is much lower. Considering the tradeoff between the drive circuit loss and turn-on delay, the turn-on drive current $I_{G\_\rm on}$ is chosen as 2 A in this application. The detailed design procedure of the turn-off drive current $I_{G\_\rm off}$ is given as follows.

1) Design of the Turn-Off Drive Current $I_{G\_\rm off}$ During a Switching Period:

1) Turn-off loss of the power MOSFET
The turn-off loss $P_{\rm off\_MOS}$ is

$$P_{\rm off\_MOS}(I_{G\_\rm off}) = \frac{1}{2}V_o \cdot i_D \cdot T_{\rm fcsd} \cdot f_s \quad (13)$$

$$T_{\rm fcsd} = \frac{Q_{\rm pl} - Q_{\rm th} + Q_{\rm gd}}{I_{G\_\rm off}} \quad (14)$$

where $T_{\rm fcsd}$ is the turn-off interval of the power MOSFET; $Q_{\rm pl}$ is the total gate capacitance of the power MOSFET at the beginning of the plateau; $Q_{\rm th}$ is the total gate capacitance at the threshold; $Q_{\rm gd}$ is the gate-to-drain charge; V_o is the output voltage, and i_D is the turn-off drain current through the power MOSFET, which is chosen as the reference signal of the adaptive turn-off drive current.

2) Drive circuit loss of the FB CSD
The drive circuit loss of the FB CSD consists of the conduction loss of S_1-S_4, the gate drive loss of S_1-S_4, and the CS inductor loss during the turn-off interval.
   a) Conduction loss of S_1-S_4
   Fig. 10(a) illustrates the gating signals of the drive switches S_1, S_3, S_4, and CS inductor current during the negative charging interval. Fig. 10(b) illustrates

the gating signals of S_1, S_2, S_3, and CS inductor current during the forward charging interval.

Interval [t_0, t_1]: S_1 and S_4 conduct

The RMS current of the CS inductor current in this interval is

$$I_{\mathrm{RMS\_}t10}(I_{G\_\mathrm{off}}) = I_{G\_\mathrm{off}}\sqrt{\frac{t_{10}f_s}{3}} \tag{15}$$

$$t_{10} = \frac{I_{G\_\mathrm{off}}L_r}{V_c} \tag{16}$$

where I_{G_off} is the turn-off drive current, which can be calculated from (2).

The total conduction loss of S_1 and S_4 is

$$P_{t10}(I_{G\_\mathrm{off}}) = 2\cdot I^2_{\mathrm{RMS\_}t10}\cdot R_{\mathrm{DS\_on}} \tag{17}$$

where $R_{\mathrm{DS\_on}}$ is the on resistance of S_1-S_4, assuming S_1-S_4 are the same.

Interval [t_1, t_2]: only S_4 conducts

The RMS current of the CS inductor current in this interval is

$$I_{\mathrm{RMS\_}t21}(I_{G\_\mathrm{off}}) = I_{G\_\mathrm{off}}\sqrt{t_{21}f_s}. \tag{18}$$

To simply the analysis, it is assumed that the drive current keeps constant during this interval. t_{21} nearly equals the turn-off time T_{fcsd} of the power MOSFET. The conduction loss of S_4 is

$$P_{t21}(I_{G\_\mathrm{off}}) = I^2_{\mathrm{RMS\_}t21}\cdot R_{\mathrm{DS\_on}}. \tag{19}$$

Interval [t_2, t_3]: only S_3 conducts

The RMS current of the CS inductor current in this interval is

$$I_{\mathrm{RMS\_}t32}(I_{G\_\mathrm{off}}) = I_{G\_\mathrm{off}}\sqrt{\frac{t_{32}f_s}{3}} \tag{20}$$

$$t_{32} = \frac{I_{G\_\mathrm{off}}L_r}{V_c}. \tag{21}$$

The conduction loss of S_3 is

$$P_{t32}(I_{G\_\mathrm{off}}) = I^2_{\mathrm{RMS\_}t32}R_{\mathrm{DS\_on}}. \tag{22}$$

The conduction loss during the turn-off interval $P_{\mathrm{con\_off}}$ is

$$P_{\mathrm{con\_off}}(I_{G\_\mathrm{off}}) = P_{t10}(I_{G\_\mathrm{off}}) + P_{t21}(I_{G\_\mathrm{off}}) + P_{t32}(I_{G\_\mathrm{off}}). \tag{23}$$

b) Gate drive loss of S_1-S_4

The gate drive loss of S_1-S_4 is

$$P_{\mathrm{gate}}(I_{G\_\mathrm{off}}) = 4Q_gV_{\mathrm{gs}}f_s \tag{24}$$

where Q_g is the total gate capacitance of a drive MOSFET, V_{gs} is the drive voltage of the four drive MOSFETs which is typically 5 V and f_s is the switching frequency.

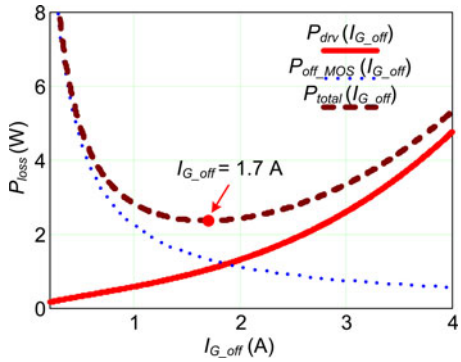

Fig. 11. $P_{\mathrm{drv}}\ (I_{G\_\mathrm{off}}), P_{\mathrm{off\_MOS}}\ (I_{G\_\mathrm{off}}), P_{\mathrm{total}}\ (I_{G\_\mathrm{off}})$ as a function of I_{G_off} with $i_D = 2$ A and $f_s = 210$ kHz.

c) Loss of the CS inductor

The copper loss of the inductor winding during the turn-off interval is

$$P_{\mathrm{copper\_off}}(I_{G\_\mathrm{off}}) = \frac{1}{2}R_{\mathrm{ac}}\cdot I^2_{Lr\_\mathrm{RMS}}(I_{G\_\mathrm{off}}) \tag{25}$$

where R_{ac} is the ac resistance of the inductor winding and I_{Lr_RMS} is the RMS value of the CS inductor current, which can be calculated from (26), as shown at the bottom of the page.

In the proposed digital CSD, the air core inductor is used. Therefore, there is no core loss of the CS inductor.

The drive circuit loss $P_{\mathrm{drv}}\ (I_{G\_\mathrm{off}})$ is

$$P_{\mathrm{drv}}(I_{G\_\mathrm{off}}) = P_{\mathrm{gate}}(I_{G\_\mathrm{off}}) + P_{\mathrm{con\_off}}(I_{G\_\mathrm{off}}) + P_{\mathrm{copper\_off}}(I_{G\_\mathrm{off}}). \tag{27}$$

From (13) and (27), the total loss $P_{\mathrm{total}}\ (I_{G\_\mathrm{off}})$ of the drive circuit loss and the turn-off loss is

$$P_{\mathrm{total}}(I_{G\_\mathrm{off}}) = P_{\mathrm{drv}}(I_{G\_\mathrm{off}}) + P_{\mathrm{off\_MOS}}(I_{G\_\mathrm{off}}). \tag{28}$$

The basic idea is to design proper I_{G_off} to minimize P_{total}. Based on (28), Fig. 11 shows the drive circuit loss P_{drv}, turn-off loss $P_{\mathrm{off\_MOS}}$, and total loss P_{total} as a function of I_{G_off}, where the turn-off drain current i_D is 2 A and the switching frequency is 210 kHz. It is observed that P_{total} is a U-shape curve and the optimized drive current value can be found at the lowest point of this curve. As seen from Fig. 11, the red dot is the optimized drive current value as 1.7 A. It is also noted that the bottom of the total loss curve is smooth and the gate drive current around 1.7 A will not affect P_{total} much.

2) Tendency of the Turn-Off Drive Current I_{G_off} During Half-Line Period: Fig. 12 illustrates the total loss P_{total} as a function of I_{G_off} with different turn-off drain current i_D. In the switching frequency-based loss calculation, f_s is obtained from

$$I_{Lr\_\mathrm{RMS}}(I_{G\_\mathrm{off}}) = \sqrt{2\cdot(I^2_{\mathrm{RMS\_}t10}(I_{G\_\mathrm{off}}) + I^2_{\mathrm{RMS\_}t21}(I_{G\_\mathrm{off}}) + I^2_{\mathrm{RMS\_}t32}(I_{G\_\mathrm{off}}))} \tag{26}$$

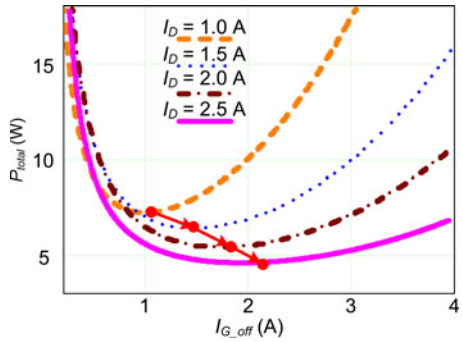

Fig. 12. Object function $P_{\rm total}\,(I_{G\_\rm off})$ as a function of drive current $I_{G\_\rm off}$ under CRM.

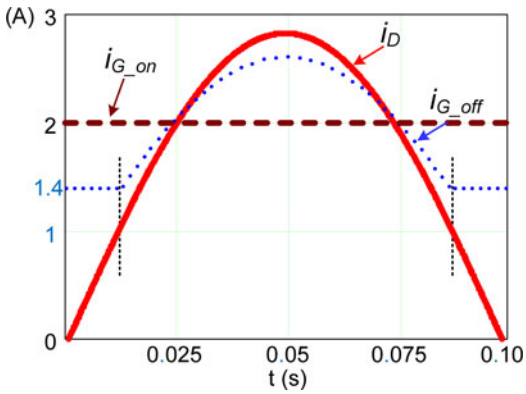

Fig. 13. Turn-off drain current i_D, drive current $i_{G\_\rm on}$, and $i_{G\_\rm off}$ during half-line period.

(12). The red curve gives the tendency of the optimized turn-off drive current with different i_D and f_s. The turn-off drain current i_D increases linearly from 1.0 to 2.5 A, the optimized $I_{G\_\rm off}$ also increases from 1.2 to 2.2 A accordingly. Therefore, the tendency of the red curve can be considered as a linear relationship approximately.

The linear relationship between the turn-off drive current $I_{G\_\rm off}$ and turn-off drain current i_D according to Fig. 12 is approximately

$$I_{G\_\rm off} = 0.7 + 0.7 i_D. \tag{29}$$

In the actual implementation, considering the effect of the turn-off delay, when the turn-off drain current is below the threshold current of 1 A, the turn-off drive current is set constant as 1.4 A. Otherwise, the turn-off drive current is chosen according to (29).

Fig. 13 gives the optimized turn-on and turn-off drive current during half-line period. The turn-on drive current is a constant value as 2 A as designed. As the envelope of the turn-off drain current is a sinusoidal curve during half-line period, the envelope of the optimized turn-off drive current is also nearly a sinusoidal curve. In particular, when the turn-off drain current i_D is lower than the threshold current of 1 A, the gate drive turn-off current $i_{G\_\rm off}$ is chosen as 1.4 A constantly.

According to (1) and (2), the turn-on and turn-off drive current are affected by the drive voltage V_c and CS inductor L_r. Normally, the drive voltage can be controlled in tight range

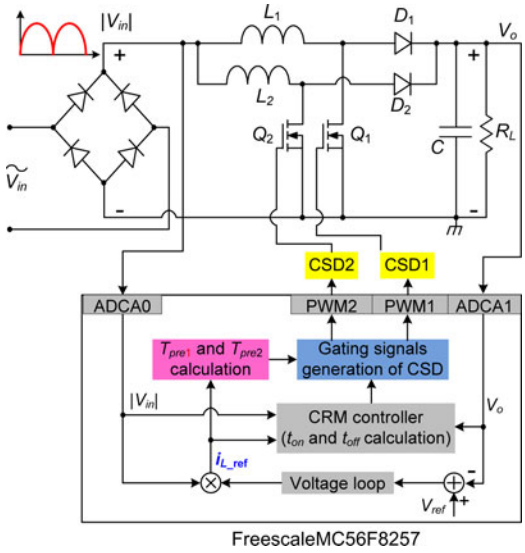

Fig. 14. Two-phase interleaved Boost PFC converter.

(<1%). Owing to the discontinuous current control of the inductor, the inductor value is much reduced and only 120 nH in this case. In the experimental prototype, the air core inductor (Coilcraft 1812SMS-R12) is used. Because the tolerance of the air core inductor is around 2%, the sensitivity to the mismatches caused by the inductor and supply voltage of the digital CSD is relatively low and acceptable.

C. Loss Comparison Between the Constant Drive Current and the Adaptive Drive Current

The efficiency of the PFC stage is determined by the power loss of the input rectifier bridge, the boost inductor, the power MOSFET, the drive circuit, and boost diode. The above loss analysis has been reported in [16] and [29].

Table II gives the loss distribution comparison of the Boost PFC converter with the constant and adaptive drive current. The turn-on and turn-off drive currents of the constant drive current CSD is chosen as 2 A. As shown in Table II, the total loss is reduced by 2.4 W under quarter-load condition, which translates into an efficiency improvement of 2.4%. The total loss is reduced by 3.6 W under full-load condition, which translates into an efficiency improvement of 0.9%. It is noted that the efficiency improvement of the adaptive CSD is more effective under the light-load condition. This is because under the light load condition, the drive circuit loss becomes dominant among the total loss. The adaptive CSD can reduce the drive circuit loss more effectively. The target is to minimize the summation of the switching loss and gate drive loss.

D. Closed-Loop Control of the Interleaved Boost PFC Converter With the Digital Adaptive CSD

The digital adaptive discontinuous CSD is applied to a two-phase interleaved Boost PFC converter to verify its advantages. The interleaved parallel Boost PFC converter under CRM is shown in Fig. 14. The closed-loop control diagram is shown in Fig. 15. The PFC voltage loop is calculated to ensure the

TABLE II
LOSS DISTRIBUTION COMPARISON OF THE BOOST PFC CONVERTER WITH DIFFERENT DRIVE CURRENT TYPES (TWO CHANNELS)

Load	100 W (25%)		200 W (50%)		400 W (100%)	
Drive current type	Constant	Adaptive	Constant	Adaptive	Constant	Adaptive
Switching loss (W)	2.6	2.9	5.1	5.2	11.3	10.9
Drive circuit loss (W)	5.8	3.1	5.8	3.0	5.8	2.6
Conduction loss (W)	0.3	0.3	1.0	1.0	4.0	4.0
Inductor loss (W)	0.3	0.3	1.1	1.1	4.3	4.3
Rectifier bridge loss (W)	1.9	1.9	3.7	3.7	7.2	7.2
Boost diode loss (W)	0.9	0.9	1.9	1.9	3.7	3.7
Total loss (W)	11.8	9.4	18.6	15.9	36.3	32.7
Loss reduction (W)	2.4		2.7		3.6	
Efficiency improvement	2.4%		1.4%		0.9%	

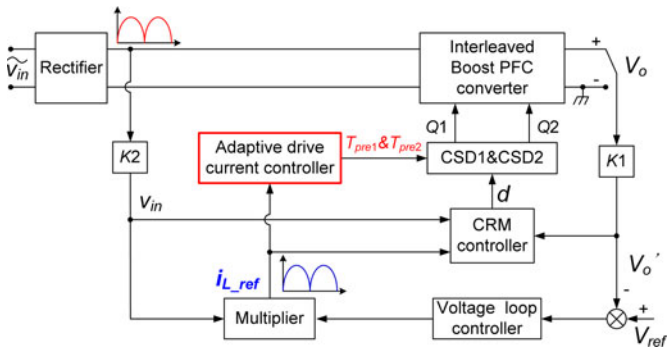

Fig. 15. Closed-loop control diagram of the interleaved Boost PFC converter.

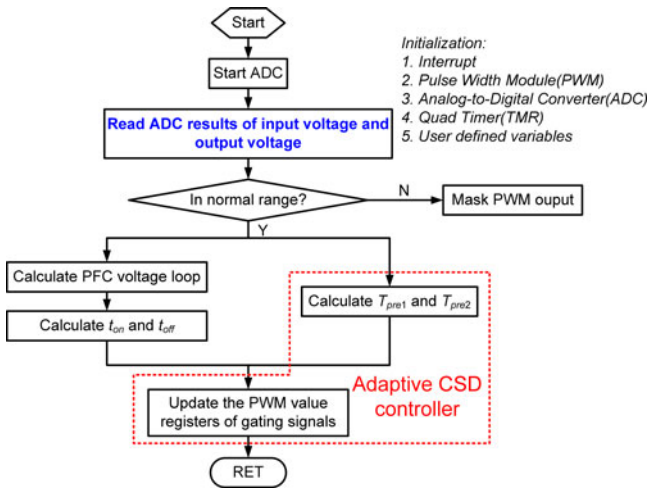

Fig. 16. Flowchart of the Boost PFC converter.

stability of the output voltage. The output of the voltage loop controller multiplied with the input voltage provides the boost inductor current reference i_{L_ref}.

The CRM controller is designed to ensure that the boost inductor current operates under CRM and the input current follows the waveform of the input voltage. In order to reduce the cost, we are using the low-end DSP and a simplified control method is used without sampling the boost inductor current directly. In the CRM controller, the on and off intervals of the main switch can be calculated as

$$t_{\mathrm{on}} = L\frac{i_{L\_\mathrm{ref}}(t)}{v_{\mathrm{in}}(t)} \tag{30}$$

$$t_{\mathrm{off}} = L\frac{i_{L\_\mathrm{ref}}(t)}{V_o - v_{\mathrm{in}}(t)} \tag{31}$$

where v_{in} is the input voltage, V_o is the output voltage, and i_{L_ref} is the boost inductor current reference, which is the output of the multiplier from the voltage control loop.

In the CRM controller, the input voltage, output voltage, and the boost inductor current reference from the output of the multiplier of the voltage loop are read. The on and off intervals of the main switch are calculated according to (30) and (31) in the PWM interrupt [30]. Once t_{on} and t_{off} are obtained, the duty cycle and period of the PWM signal of the main switch can be generated.

Since the sampling of the boost inductor current is avoided, the boost inductor current reference i_{L_ref} is chosen as the reference signal of the adaptive turn-off drive current, which represents the turn-off drain current i_D at the turn-off instant. In the adaptive drive current controller, the turn-on and turn-off precharge times T_{pre1} and T_{pre2} can be calculated according to i_{L_ref} from (1) and (2), respectively. According to $t_{\mathrm{on}}, t_{\mathrm{off}}, T_{\mathrm{pre1}}$, and T_{pre2} calculated in the PWM interrupt, the gating control signals of the CSD drive switches can be generated in real time before a new modulation period.

Fig. 16 shows the flowchart of the master phase of the two-phase interleaved Boost PFC converter. The PWM output functions properly when the ADC results are in the normal range. Otherwise, the PWM output is masked immediately to protect the circuit. In the PFC voltage loop, t_{on} and t_{off} are calculated to realize the PFC function. Meanwhile, the turn-on precharge time T_{pre1} and turn-off precharge time T_{pre2} are calculated according to i_{L_ref}. Then, the PWM register values of the gating signals can be generated. The gating signals of the slave phase are delayed half-period of the master slave.

E. Software Design of the Digital Adaptive CSD

The red dotted border in Fig. 16 is the controller of the adaptive CSD. Once the relationship between the drive current and drain current is determined, the precharge time can be obtained accordingly. The control of the digital CSD is implemented by the Freescale DSP MC56F8257. The detailed general flowchart of the digital adaptive CSD is shown in Fig. 17. The multiplied result of the voltage loop output and input voltage is used as the reference signal i_{L_ref} of the turn-off drive current since i_{L_ref} represents the turn-off drain current i_D at the turn-off instant.

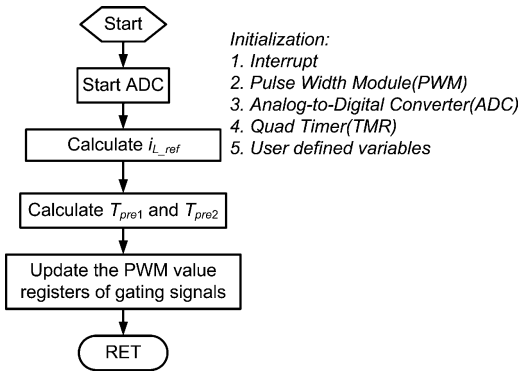

Fig. 17. Flowchart of the adaptive CSD controller.

With i_D, the turn-off drive current can be determined from (29). Then, the turn-on and turn-off precharge interval $T_{\rm pre1}$ and turn-off precharge time $T_{\rm pre2}$ can be calculated according to (1) and (2). After that, the values of *VAL*1–*VAL*4 shown in Fig. 6 can be obtained. With the duty cycle and period of the PWM signals, the control signals of the four CSD switches can be determined. The parameters, respectively, correspond to the PWM value registers in the MC56F8257. The generation method of the PWM is to update the value registers and then output [31]. At the start of the next cycle, the PWM module reloads the corresponding parameters including *VAL*1–*VAL*4 and other PWM parameters.

For the applications requiring higher resolution than a single IPBus clock period, the fractional delay logic of the MC56F8257 can achieve higher resolution on the rising and falling edges of the PWM output. The least fractional delay time is the value of half IPBus clock period dividing 32 which equals 0.251 ns. This is precise enough to realize the precharge interval.

IV. Experimental Results and Discussion

A 220-$V_{\rm AC}$ input, 380-V /400-W output two-phase interleaved Boost PFC converter under CRM was built. The switching frequency varies from 90 to 500 kHz. The specifications are the boost inductor $L = 220$ μH and the output capacitor $C = 440$ μF. The CSD part was built using the discrete components. The FDN335N N-channel MOSFETs were used for the four drive switches $S_1 - S_4$. The Coilcraft 1812SMS air core inductor (120 nH) was used for the CS inductor. The gate drive voltage V_c is 12 V. The Freescale MC56F8257 DSP was used for the digital control of the CSD and PFC control loop. The photo of the prototype is illustrated in Fig. 18.

A. Experimental Results of the Digital Adaptive Discontinuous CSD

Fig. 19 shows the waveforms of the gate drive voltage and CS inductor current when the turn-off drain current $i_D = 1.5$ A. The amplitude of the gate drive voltage is 12 V. The peak value of the turn-on drive current and the turn-off current are 2 and 1.4 A, respectively, which are the optimized values of the drive current.

Figs. 20 and 21 show the zoomed gate drive voltage and CS inductor current during the turn-on interval and turn-off interval.

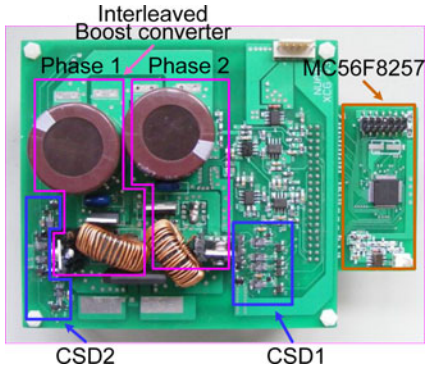

Fig. 18. Photo of the prototype.

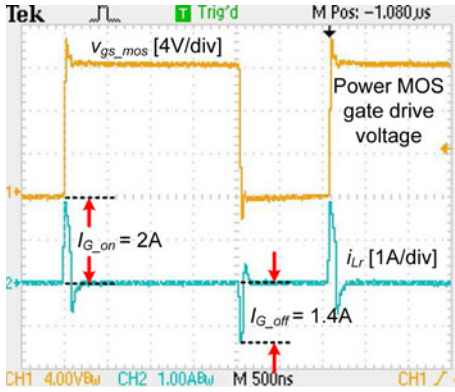

Fig. 19. Gate drive voltage and CS inductor current with $i_D = 1.5$ A.

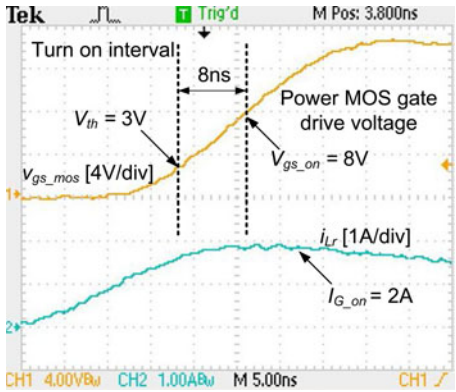

Fig. 20. Zoomed gate drive voltage and inductor current during turn-on interval with $i_D = 1.5$ A.

It is noted that the turn-on interval time and turn-off interval time are 8 and 9 ns, respectively, and fast switching speed is achieved.

Fig. 22 shows the gating signals of drive switches S_2 and S_3, and CS inductor current during the turn-on interval. When S_2 turns ON, the inductor current i_{Lr} starts to ramp up till S_3 turns OFF. Then, i_{Lr} keeps nearly constant to turn ON the power MOSFETs. i_{Lr} ramps down toward zero when S_2 turns OFF. It is observed that the turn-on precharge time is about 30 ns; the peak current is about 2 A.

Fig. 23 gives the turn-off interval waveforms of the drive switches S_1 and S_4. When S_4 turns ON, i_{Lr} ramps up negatively. i_{Lr} keeps nearly constant to turn OFF the power MOSFETs

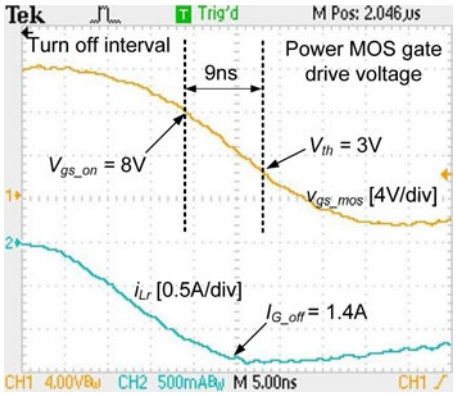

Fig. 21. Zoomed gate drive voltage and inductor current during turn-off interval with $i_D = 1.5$ A.

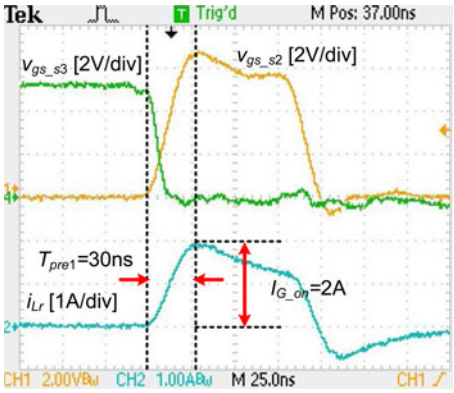

Fig. 22. CS inductor current and gating signals of S_2 and S_3 during turn-on interval with $i_D = 1.5$ A.

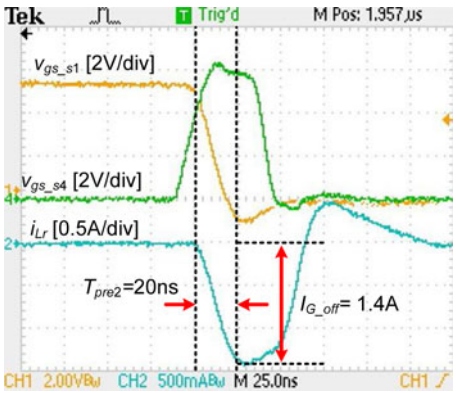

Fig. 23. CS inductor current and gating signals of S_1 and S_4 during turn-off interval with $i_D = 1.5$ A.

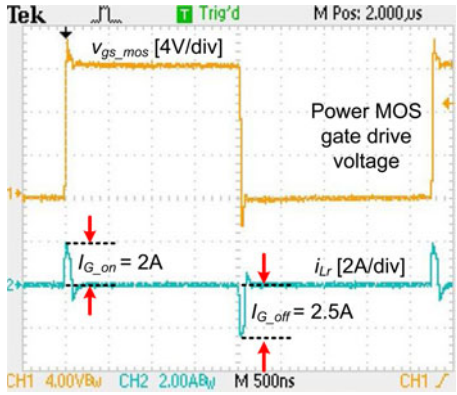

Fig. 24. Gate drive voltage and CS inductor current with $i_D = 2.6$ A.

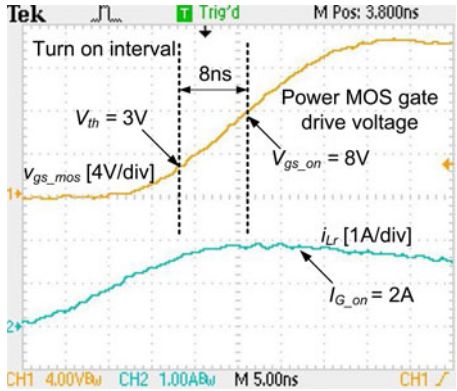

Fig. 25. Zoomed gate drive voltage and inductor current during turn-on interval with $i_D = 2.6$ A.

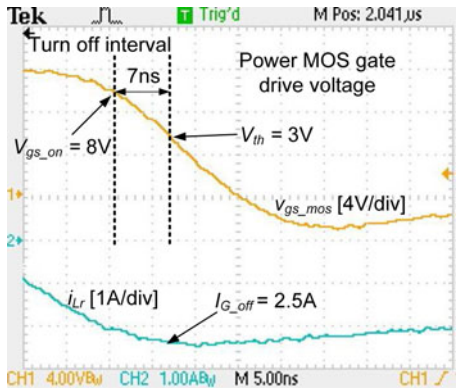

Fig. 26. Zoomed gate drive voltage and inductor current during turn-off interval with $i_D = 2.6$ A.

when S_1 turns OFF. Then, the CS inductor current decays to zero after S_1 turns OFF. The turn-off precharge time is about 20 ns; the peak current is about 1.4 A.

Figs. 24–28 show the detailed waveforms of the CS inductor current, the gate drive voltage, and the drive switches control signals when the turn-off drain current i_D turns into 2.6 A.

From Figs. 22 and 27, the turn-on precharge time and the peak CS inductor current are the same. The drive current is 2 A according to the optimal design. Comparing Fig. 23 with Fig. 28, as the switching current increases from 1.5 to 2.6 A, the precharge time increases to 40 ns and the turn-off drive current increases to 2.5 A adaptively in Fig. 28. From Figs. 20 and 25, it is noted that the turn-on interval time is 8 ns because the turn-on drive current is the same. The turn-off interval time reduces from 9 (seen from Fig. 21) to 7 ns (seen from Fig. 26) (a reduction of 22%) to reduce the turn-off loss.

Fig. 29 shows the drive current and input current during half-line period. As shown in Fig. 29, the turn-on drive current is constant and the envelope curve of the turn-off drive current is nearly a sinusoidal curve during half-line period which are

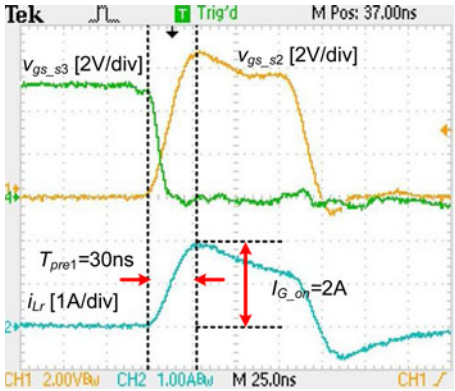

Fig. 27. CS inductor current and gating signals of S_2 and S_3 during turn-on interval with $i_D = 2.6$ A.

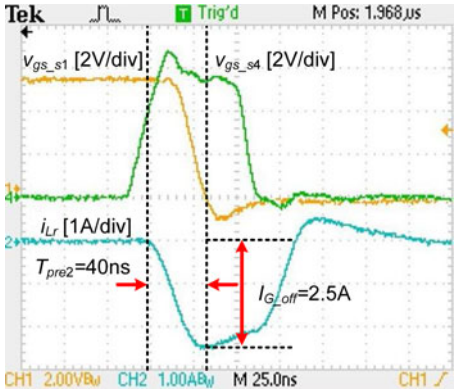

Fig. 28. CS inductor current and gating signals of S_1 and S_4 during turn-off interval with $i_D = 2.6$ A.

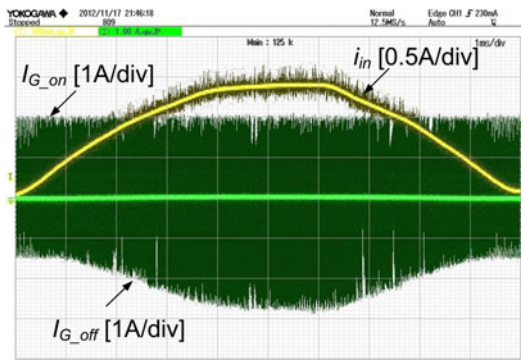

Fig. 29. Input current of one phase and drive current during half-line period.

in accord with the optimal design. The turn-off drive current is adjusted dynamically according to different turn-off drain currents to realize better tradeoff between the turn-off loss and drive circuit loss.

Fig. 30 shows the gating signals of the four drive switches $S_1 - S_4$ of the CSD circuit. They agree with the theoretic waveforms as shown in Fig. 6.

B. Loss Reduction of the Digital Adaptive Discontinuous CSD

Fig. 31 shows the measured efficiency comparison between the digital adaptive CSD and constant one. The turn-on and turn-

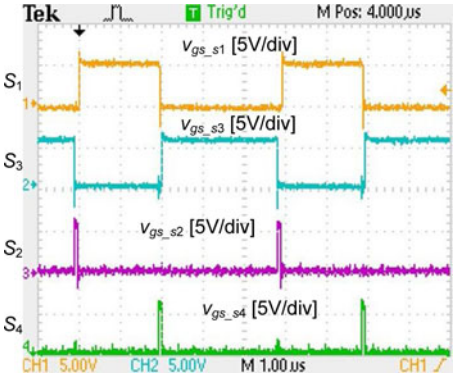

Fig. 30. Gating signals of the four drive switches of the CSD circuit.

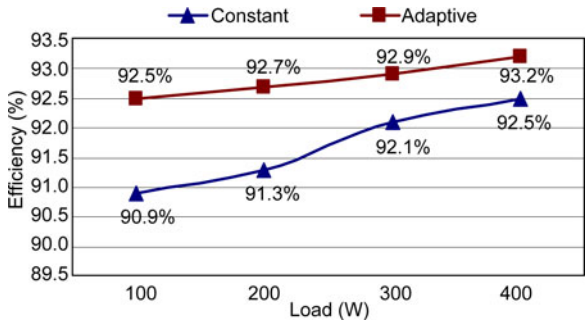

Fig. 31. Efficiency comparison.

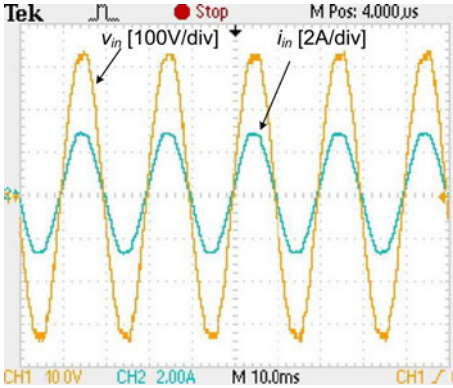

Fig. 32. Input line voltage and current.

off drive current of the constant drive current CSD are chosen as 2 A. As shown in Fig. 31, the Boost PFC with the proposed digital adaptive CSD improves 1.6% over the constant one under the quarter load. An efficiency improvement of 0.7% is achieved over the constant drive current CSD under the full load. The proposed digital CSD achieves a higher efficiency improvement under the light-load condition over the heavy-load condition.

C. Experimental Results of a Digital PFC Converter

Fig. 32 shows the input line voltage and current of the Boost PFC stage. It is observed that the input current is sinusoidal and catching up with the input line voltage so that the high power factor is achieved. The measured PF values are given in Table III under different load conditions. The PF values are above 0.99

TABLE III
MEASURED PF VALUES UNDER DIFFERENT LOAD CONDITIONS

Load conditions (W)	100	200	300	400
PF values	0.992	0.994	0.996	0.999

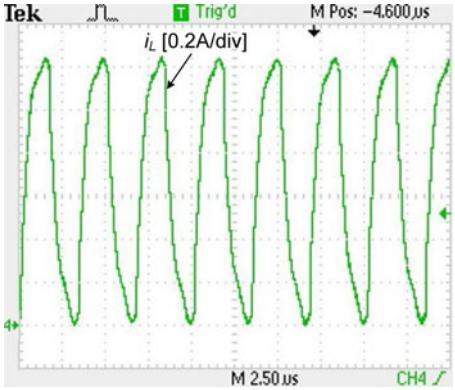

Fig. 33. Zoomed Boost inductor current.

under the different load conditions, which are compatible with the industrial standard.

Fig. 33 shows the zoomed Boost inductor current. It is observed that the Boost inductor current increases from zero and the converter is under the critical conduction mode as designed.

D. Benefits of the Digital Adaptive Discontinuous CSD

The advantages of the proposed digital adaptive CSD are highlights as follows:

1) Loss and Cost Reduction of the Digital Adaptive CSD
The constant drive current CSD can only provide a constant drive current. The switching loss increases proportionally when the drain current increases which reduces the efficiency. The adaptive CSD can adjust the drive current according to the drain current or load to minimize the total loss of the drive circuit loss and switching loss. The proposed adaptive discontinuous CSD is compatible with the digital control. The analog way to realize the adaptive drive current needs the OP amps and BJTs with the additional resistors, and it consumes power continuously. As comparison, the proposed digital method eliminates additional loss and cost, much reducing the complexity of the drive circuit.
2) Optimal Efficiency With the Flexible Control
The proposed digital CSD is compatible with the advanced digital control technique. In this application, the air core inductor is used for the drive circuit and the tolerance of this air core inductor is only around 2–5%, which is quite low. Normally, the drive voltage can be controlled in a tight range. Therefore, the sensitivity to mismatches of the digital CSD is relatively low. However, considering the characterization of the chosen power MOSFETs, the autotuning technique can be accepted with the proposed adaptive CSD concept to eliminate the effect of the parameter variations and further improve the drive performance in other applications.
3) Independent Turn-On and Turn-Off Drive Current
The turn-on and turn-off drive current could be generated independently. The turn-on and turn-off drive current can be designed, respectively. Therefore, the proposed digital CSD offers more design flexibility over the conventional CSD to reduce the losses further when the turn-on and turn-off conditions are different.

V. CONCLUSION

The digital adaptive CSD is proposed and applied to the two-phase interleaved Boost PFC converter. The adaptive function is achieved by the digital controller to adjust the precharge time instead of adjusting the drive voltage with the analog linear regulator. The digital CSD is able to achieve the adaptive drive current in "a free way" since it has strong compatibility with the digital control technique. It eliminates the additional loss and cost introduced by the linear regulator, and reduces the complexity and cost of the circuit significantly. More importantly, the digital adaptive function can offer a more flexible control algorithm to build the different turn-on and turn-off drive currents to achieve the design tradeoff between the switching loss and drive circuit loss, and obtain the optimal efficiency in a wide load range. A 220-V_{AC}, 380-V/400-W Boost PFC converter under CRM was built to verify the advantages. The digital adaptive CSD improves the efficiency from 91.3% to 92.7% (an improvement of 1.4%) under the half-load, and from 92.5% to 93.2% (an improvement of 0.7%) under the full load over the constant drive current CSD. The efficiency improvement verifies the proposed control strategy and the advantages of the digital adaptive CSD.

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Zhiliang Zhang (S'03–M'09) received the B.Sc. and M.Sc. degrees in electrical and automation engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2002 and 2005, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2009.

Since June 2009, he has been an Associate Professor with Aero-Power Sci-Tech Center, Nanjing University of Aeronautics and Astronautics, Nanjing. From June to September 2007, he was a Design Engineering Intern at Burlington Design Center, Linear Technology Corporation. His research interests include high-frequency dc–dc converters, power integrated circuit, digital control techniques for power electronics, and renewable energy conversion system.

Dr. Zhang was the recipient of the Graduate Scholarship through Lite-On Technology Corporation in 2004 and a winner of "United Technologies Corporation Rong Hong Endowment" in 1999.

Chuangang Xu received the B.S. and M.Sc. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2010 and 2013, respectively.

He is currently a Design Engineer at Bel Power Corporation, Hangzhou, China. His research interests include resonant gate driver techniques, power factor correction converters, and dc–dc converters.

Yan-Fei Liu (M'94–SM'97–F'13) received the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

From February 1994 to July 1999, he worked as a Technical Advisor with the Advanced Power System Division of Nortel Networks. Since 1999, he joined Queen's University. Currently, he is a Professor in the Department of Electrical and Computer Engineering. His research interests include digital control technologies for high efficiency, fast dynamic response dcdc switching converter and acdc converter with power factor correction, resonant converters and server power supplies, and LED drivers. He holds 22 US patents and has published more than 130 technical papers in IEEE Transactions and conferences. He is also a principal contributor for two IEEE standards.

Dr. Liu serves as an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS since 2001, Guest Editor-in-Chief for special issue of Power Supply on Chip of IEEE TRANSACTIONS ON POWER ELECTRONICS (September 2013 issue), Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPIC IN POWER ELECTRONICS (JESTPE), as well as technical program co-chair for ECCE 2011. He also serves as chair of Technical Committee of Modeling and Control Core Technology of IEEE Power Electrical Society (PELS).