A Zero-Crossing Noise Filter for Driving Synchronous Rectifiers of *LLC* Resonant Converter

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***Abstract*—A new driving method for synchronous rectifier (SR) in *LLC* resonant converter is presented. By adding a zero-crossing noise filter (ZCNF) to the drain and source of the SR FET, the false-triggering of the SR can be effectively eliminated. Moreover, the resistor and the capacitor in the filter can be used as a compensator to solve the duty-cycle loss issue caused by the trace inductance of the MOSFET package. Only three passive components are needed in the proposed filter, which makes it reliable and easy to implement. Simulation and experimental results show that the ZCNF can significantly improve the reliability as well as the efficiency of the power circuit. A prototype of 400 V to 12 V 600-W half-bridge *LLC* resonant converter is built to verify the advantages of the ZCNF. An efficiency improvement of 0.8% is achieved by the ZCNF.**

***Index Terms*—Dead time control, *LLC* dc–dc converter, resonant converter, synchronous rectifier (SR), zero-crossing noise filter (ZCNF).**

I. Introduction

With the development of computer technology, the demand for the converters with low output voltage (such as 12 or 48 V) and high output current (such as 50 A and up) keeps increasing. Because of its advantages, the *LLC* resonant converter with synchronous rectifier (SR) becomes one of the promising solutions [1]. To achieve high efficiency, the parameters of the *LLC* resonant tank should be optimized [2]. In addition, the driving signal of the SR should be precisely synchronized with the current through the rectifier [3].

Due to the phase shift introduced by the resonant components, the secondary-side currents of the *LLC* resonant converter are not in phase with the switching actions of the primary-side MOSFETs [3], [4]. To generate accurate driving signal for the secondary-side SR, many studies and efforts have been done in the recent years [3]–[13]. All of these schemes can be divided into the current-based method [5]–[10] and the voltage-based method [14], [15].

The current-based method detects the current through the SR to generate the gate drive signal [9], [16]. The main problems of these methods are the large size of the current-sensing transformer (CT), the extra conduction loss of the winding, and the undesired delay that will cause duty-cycle loss of the SR and therefore more conduction loss [5]–[7]. To avoid the aforementioned problems, primary current sensing with magnetizing current cancellation method is proposed in [6]–[8]. The efficiency of the circuit can be improved because of the relatively smaller primary current of the transformer through the CT. However, the CT and the matching circuits of the transformer magnetizing current make the implementation complex. The matching of the magnetizing current with the inductor or the transformer is also difficult.

The voltage-based method detects the voltage across the drain to the source ($v_{\rm DS}$) of the SR to generate the driving signal. Special integrated circuit driving chips have been developed based on this method to simplify the SR driving [14], [15]. However, due to the small $R_{\rm ds\_on}$ of the MOSFET, the detecting threshold voltage is very low, at the millivolt level. Thus, even a very small zero-crossed ringing caused by the parasitic parameters of the circuit may result in the false gate driving signal which causes undesired circulating energy loss. Moreover, the sensed $v_{\rm DS}$ of the MOSFET is actually the sum of the $R_{\rm ds\_on}$ voltage drop and the package as well as the printed circuit board (PCB) trace inductive voltage drop. Although the PCB trace inductance can be minimized by some special layout method such as Kelvin sensing, the lead inductance caused by the bonding wire inside the MOSFET package is inevitable. A nanohenry (nH) inductance will cause a considerable duty-cycle loss [4], [13]. Therefore, the SR will be ON for a much shorter time than required, resulting in extra conduction loss.

In order to eliminate the loss caused by the body diode conduction, in [13] and [17], the authors use the forward voltage drop of the body diode to tune the turnoff time of the SR. But the turn-on of the SR is still synchronous with the primary-side MOSFET. Due to the phase shift mentioned previously, it will cause false-triggering problem at light-load condition.

The conventional DCR (DC resistance of the inductor) current-sensing method is widely used to sense and emulate the current through the inductor in voltage regulators [18]–[20]. The advantages of this method are that it utilizes the parasitic

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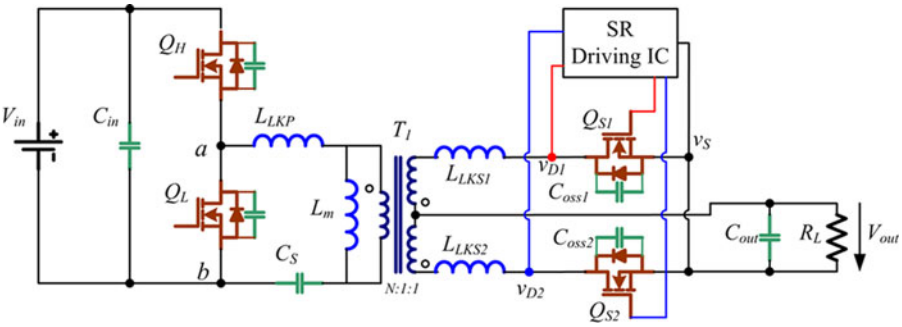


Fig. 1. Typical half-bridge *LLC* resonant converter with SRs.

DCRs of the inductors and is intrinsically lossless [2], [21]. In [4], the authors try to use the DCR current-sensing method to compensate the duty-cycle loss caused by the trace inductance of the MOSFET package. However, there are too many active switches used in the matching circuit that makes the compensator too complicated to implement. In addition, active switches also degrade the reliability of the power circuit. Moreover, the compensator has no filter function such that the false-triggering problem caused by the parasitic ringing cannot be solved.

This paper is an improved version of our ECCE 2010 paper [22], presented in September 2010, where a new driving method for the SR FET based on the $v_{\rm DS}$ sensing scheme is presented. By applying a zero-crossing noise filter (ZCNF) between the drain and the source of the SR, the false triggering can be effectively eliminated. More importantly, the resistor and the capacitor in the filter are also used to compensate the duty-cycle loss introduced by the trace inductance of the MOSFET package. Only three low-power passive components are needed for this filter, which makes the driving scheme reliable and easy to implement and cost effective. Therefore, it has been recommended immediately by leading IC company's application notes, such as [23] published in January 2011 and [24] published in September 2011. More detailed operation conditions are analyzed in this paper and two derivative circuits are proposed to improve the filtering performance of the ZCNF. A 400 V to 12 V/50 A (600 W) half-bridge *LLC* resonant converter prototype is built to validate the theoretical analysis. The organization of this paper is as follows. Section II analyzes in detail the problems of the traditional voltage-sensing SR driving method. Section III introduces the architecture of the proposed ZCNF. Section IV focuses on the parameter calculation of the ZCNF. Experimental results are shown in Section V. Finally, the conclusion is given in Section VI.

II. Problems of the Traditional Voltage-Sensing SR Driving Method

Fig. 1 shows the circuit diagram of the typical half-bridge *LLC* resonant converter with SRs. $L_{\rm LKP}$ is the primary-side leakage inductance of the transformer. $L_{\rm LKS1}$ and $L_{\rm LKS2}$ are the secondary leakage inductances. $C_{\rm oss1}$ and $C_{\rm oss2}$ are the output capacitances of the SRs.

Fig. 2 shows the key waveforms of the *LLC* converter when operated in full-load and light-load conditions. It is observed that the primary-side driving signals cannot be applied to the SRs because they are not in phase, especially at light-load condition. To drive the SRs properly, $v_{\rm DS}$ of the SRs can be used. However, some problems should be solved before applying this method.

A. False-Triggering at the Turn-on of SRs

As shown in Fig. 2, there is a small interval when both the two SR MOSFETs are OFF [t_4–t_6 in Fig. 2(a) and t_4–t_7 in Fig. 2 (b)]. When the SRs turn OFF, $L_{\rm LKP}$, $L_{\rm LKS1}$, and $L_{\rm LKS2}$ resonate with the output capacitance $C_{\rm oss}$ of the SRs. As shown in Fig. 3, voltage $v_{\rm DS1}$ has many high-frequency spikes when Q_{S1} turns OFF. If the voltage spikes reach the SRs turn-on threshold, the SRs will be false-triggered.

Fig. 4 shows the false-turn-on of the SR at light-load condition. This will result in the energy reverse from the output capacitor to the input source, or even worse breakdown of the power circuit.

One possible solution to prevent false-triggering at turn-on of the SRs is to add an *RC* filter to absorb the voltage spikes of $v_{\rm DS}$, as shown in Fig. 5. $v_{\rm filter}$ is used as a substitute for $v_{\rm DS}$ and sensed by the driving IC to generate the gate signal. Fig. 6 shows the experiment results of the *RC* filter scheme. By applying a small time constant (about 100 ns), the false-triggering phenomenon is effectively eliminated.

Unfortunately, it is observed from Fig. 6 that the actual turn-on instant of the SR FET is delayed by $T_{\rm lag}$ and the actual turn-off instant of the SR FET is earlier than needed by $T_{\rm lead}$. During $T_{\rm lag}$ and $T_{\rm lead}$, the body diode of the SR FET will conduct and cause considerable conduction loss. The reason for the delay at SR FET turn-on is that the capacitor, $C_{\rm filter}$, which is charged to two times of the output voltage, has to be discharged through resistor $R_{\rm filter}$. Only when the capacitor voltage is discharged to almost zero, the driving chip will turn ON the SR FET.

Fig. 7(a) shows the equivalent circuits of the SR with *RC* filter during the body diode conduction interval. When the body diode of the SR starts to conduct, as shown in Fig. 7(b), the detected $v_{\rm filter1}$ is larger than the output voltage $V_{\rm out}$ at t_1. During t_1–t_2, the body diode of the Q_{S1} is forward biased and clamps the $v_{\rm DS1}$ to the forward voltage of the body diode $-V_{\rm Fb}$. The voltage,

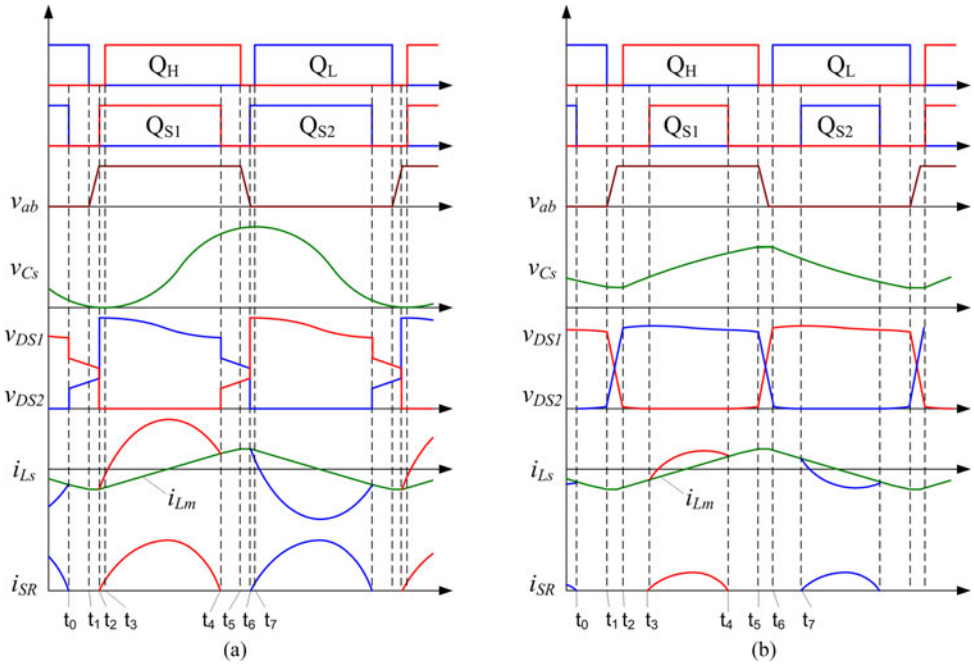


Fig. 2. Key waveforms of the *LLC* converter operated in (a) full-load and (b) light-load condition.

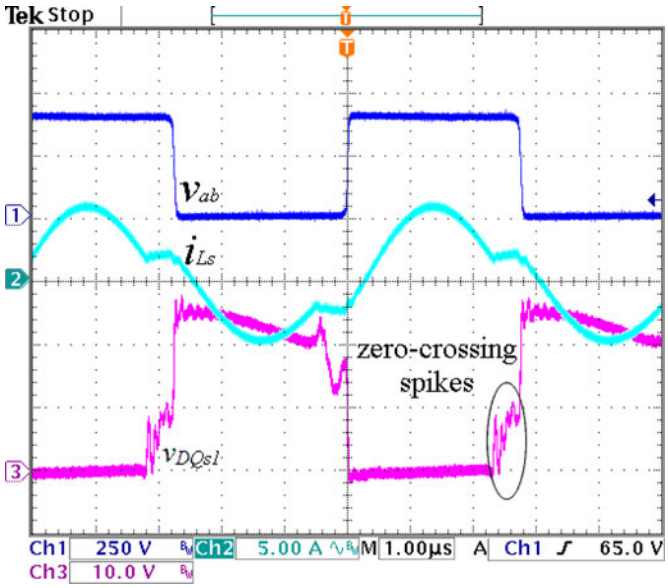


Fig. 3. Parasitic ringing of the $v_{\rm DS}$ when the SRs turned OFF.

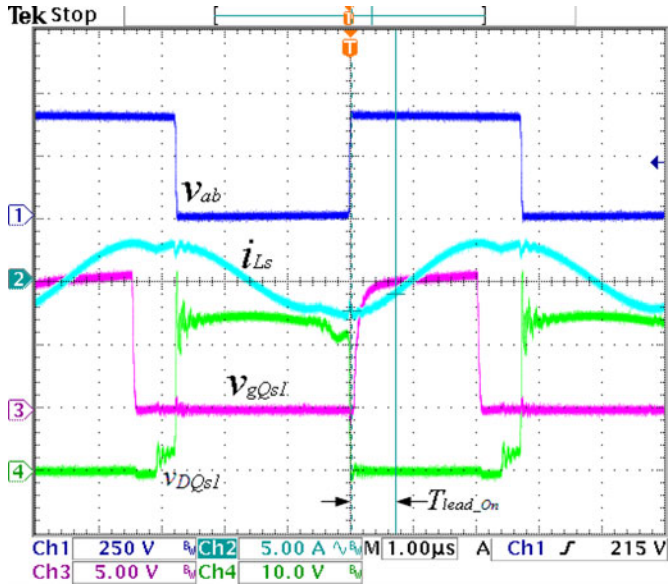


Fig. 4. False-turn-on of SR under light-load condition.

$v_{\rm filter1}$, decreased to zero during t_1 and t_2 based on the time constant of the *RC* filter.

B. Duty-Cycle Loss at the Turn-Off of SRs

When SR FET is ON, the voltage across drain to source is very small. When the trace inductance of the SR package is considered, the equivalent circuit of the SR FET is $R_{\rm ds\_on}$ in series with the trace inductance, as shown in Fig. 5. As the current through the SR is part of a sinusoid waveform with frequency equal to the series-resonant frequency of the resonant tank, the voltage $v_{\rm DS}$ leads the current $i_{\rm SR}$, due to trace inductance. The lead angle and the lead time of the $v_{\rm DS}$ to the $i_{\rm SR}$ can be derived as

$$\theta_{\rm lead} = \tan^{-1}\left(\frac{\omega_0 \cdot L_{\rm lead}}{R_{\rm DS\_on}}\right) \tag{1}$$

$$T_{\rm lead} = \frac{\theta_{\rm lead}}{\omega_0} \tag{2}$$

where ω_0 is the series-resonant frequency of the resonant tank. It is observed that if $v_{\rm DS}$ is used directly to generate the driving signal of SR, the SR FET will be turned OFF while it still carries significant amount of current. Therefore, the duty-cycle loss is inevitable. Fig. 8 shows the lead-turn-off of the SR when $v_{\rm DS}$ of the SR is fed to the driving IC.

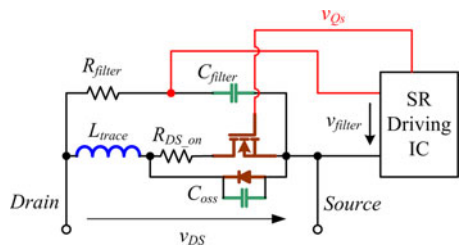


Fig. 5. $v_{\rm DS}$ sensing method with an *RC* filter.

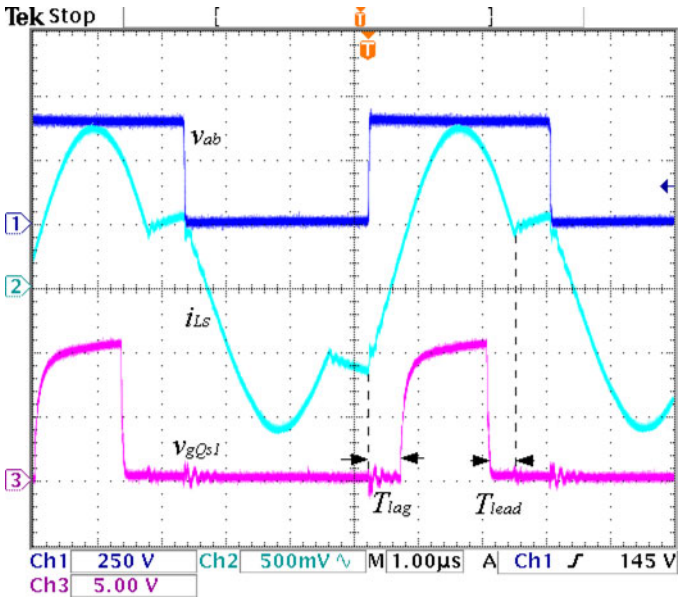


Fig. 6. Experiment result of the triggering signal of the SR with an *RC* filter.

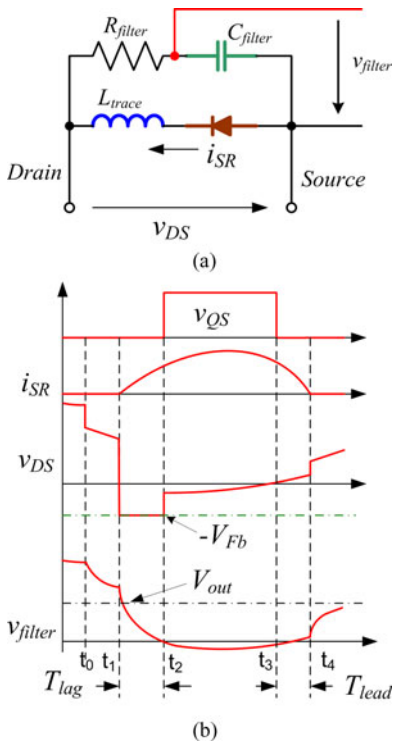


Fig. 7. Operation of the SR with an *RC* filter. (a) Equivalent circuit during body diode conduction. (b) Key waveforms.

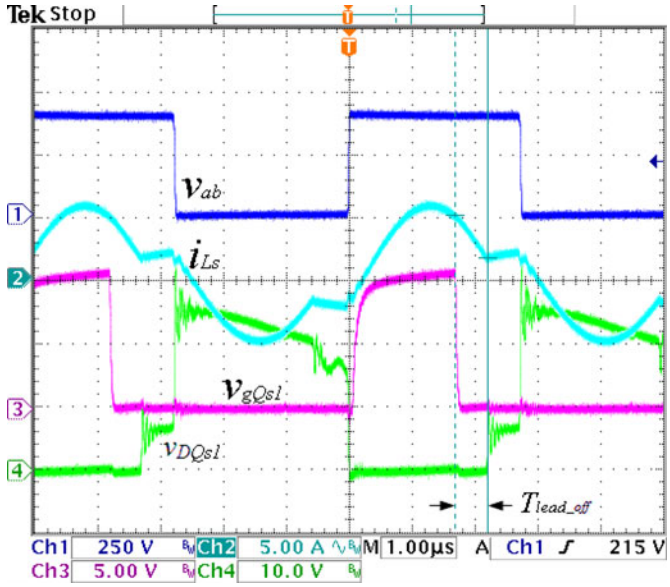


Fig. 8. Lead-turn-off of the SR.

III. ZCNF for SR Gate Drive

To solve the SR FET turn-on delay problem, an antiparallel diode is added to discharge the *RC* filter capacitor quickly. Fig. 9 shows the circuit diagram of the half-bridge *LLC* resonant converter with SRs and ZCNF. In the diagram, v_{f1} and v_{f2} are sensed by the SR driving IC as the substitutes of v_{D1} and v_{D2}.

The equivalent circuit of the SR with ZCNF is shown in Fig. 10 in which the forward voltage of the $D_{\rm filter}$ ($V_{\rm FD}$) should be a little larger than that of the body diode of the SR ($V_{\rm Fb}$). Two diodes need to be connected in series if this condition cannot be met by one diode.

The key waveforms of the SR with ZCNF under different load conditions are illustrated in Fig. 11.

The equivalent circuit diagrams of the SR with the ZCNF of each operation mode are shown in Fig. 12. It is assumed that primary MOSFET Q_H is OFF and Q_L is ON before t_0.

1) Before t_0, all of the SRs are turned OFF. The magnetizing current is discharging the resonant capacitor. At t_0, the primary MOSFET Q_L turns OFF. The voltage across the SR decreases quickly and reaches to the forward voltage drop $V_{\rm Fb}$ of the SR body diode at t_1. At the same time, $C_{\rm filter}$ is discharged through $D_{\rm filter}$ until the voltage across $C_{\rm filter}$ equals to $V_{\rm FD}$–$V_{\rm Fb}$ in which $V_{\rm FD}$ is the forward voltage drop of $D_{\rm filter}$.
2) At t_1, due to the existence of $C_{\rm oss}$ of the SR, the voltage $v_{\rm DS}$ has some high-frequency ringing which has been explained in the previous section.
3) The peak voltage of the ringing is limited by the forward voltage drop $V_{\rm Fb}$ of the SR body diode. Meanwhile, $R_{\rm filter}$ and $C_{\rm filter}$ together work like an *RC* filter and filter out the high-frequency ringing.
4) Before t_2, the body diode of the Q_{S1} is forward biased and clamps $v_{\rm DS}$ to $-V_{\rm Fb}$. At t_2, the voltage across $C_{\rm filter}, v_{\rm filter}$, reaches to the turn-on threshold of the driving chip so the driving signal is generated. During

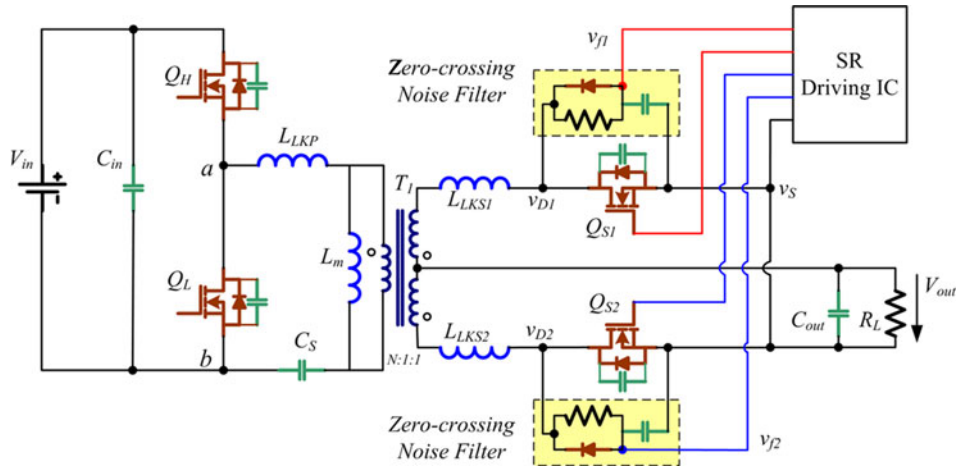


Fig. 9. Circuit diagram of the half-bridge *LLC* resonant converter with SRs and ZCNF.

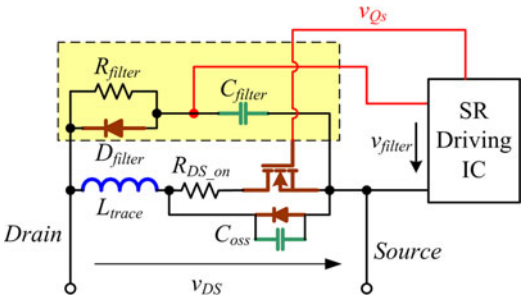


Fig. 10. Equivalent circuit of the SR with the ZCNF.

t_2–t_4, $R_{\rm filter}$ and $C_{\rm filter}$ together work like a traditional DCR current-sensing circuit to emulate the current through the SR. At t_4, the voltage $v_{\rm filter}$ reaches to the turn-off threshold of the driving chip. The SR is turned OFF.

In order to ensure that the voltage across $C_{\rm filter}$ is in same phase with the current through SR FET when the MOSFET and PCB trace inductance cannot be neglected, two conditions should be satisfied. One is that the parameters of the $R_{\rm filter}$ and $C_{\rm filter}$ should be matched to the trace inductance and $R_{\rm DS\_on}$ of the SR, as shown in (5). The other is that the initial condition of the voltage $v_{\rm filter}$ is zero. Due to the deliberately designed parameters of the $R_{\rm filter}$ and $C_{\rm filter}$ as well as the small value between $V_{\rm FD}-V_{\rm Fb}$ and the turn-on threshold, both of these two conditions can be satisfied. In addition, the false-triggering immunity of the ZCNF is still retained. Consequently, the reliability of the circuit is improved and the conduction loss is significantly reduced.

According to the operation modes analyzed before, it is clear that although it looks like a traditional RCD snubber, but the reversely connected diode and the elaborately selected *RC* parameters make the ZCNF work totally different from the traditional snubber [25].

IV. Parameters Selection for the ZCNF

To realize the ZCNF function and the duty-cycle compensation function properly at the same time, the parameters of this filter should be calculated carefully.

A. Parameters Selection for the Duty-Cycle Compensation Function

To compensate for early turn-off of SR FET, the time constant of the $R_{\rm filter}$ and $C_{\rm filter}$ of the ZCNF should be selected to match the time constant of the trace inductance and $R_{\rm DS\_on}$ of the SR. Under this condition, the capacitor voltage is in phase with the voltage across $R_{\rm DS\_on}$, or in phase with the current through SR FET, as shown in Fig. 13. In the figure, the parameters of the filter are chosen specifically to emulate the lead angle $\theta_{\rm lead}$ so that the voltage across $C_{\rm filter}$ can describe $v_{\rm RDS\_on}$ exactly. The parameters of the filter is defined as

$$\tau_{\rm filter}=R_{\rm filter}\cdot C_{\rm filter}=\frac{L_{\rm trace}}{R_{\rm DS\_on}}. \tag{3}$$

Due to the resonant operation, the primary-side current is a sinusoidal waveform. However, because of the existence of the magnetizing current, the current through the SR is not exactly a sinusoidal one. In order to depict the current through the SR, the first thing is to figure out the magnetizing current of the transformer. To simplify the calculation, it is assumed that the resonant tank always operates at the series-resonant frequency f_0.

1) Heavy-Load Condition: At heavy-load condition, from Fig. 2(a), it is distinct that the magnetizing inductor L_m is always clamped by the output voltage. The magnetizing current can be written as

$$i_{Lm}(t)=\frac{N\cdot V_{\rm out}}{L_m}\cdot\left(t-\frac{1}{4f_0}\right) \tag{4}$$

where f_0 is the series-resonant frequency and N is the turns ratio of the transformer: $N=n_p/n_s$. The primary-side resonant

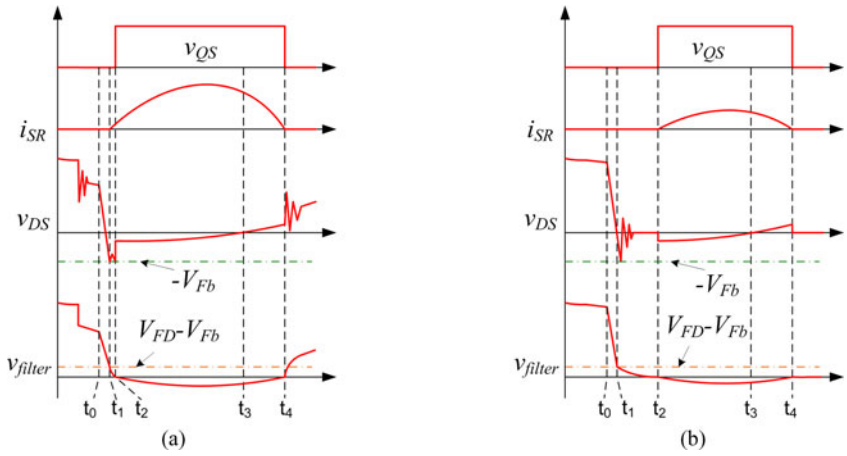


Fig. 11. Key waveforms of the SR with the ZCNF (a) under full-load condition and (b) under light-load condition.

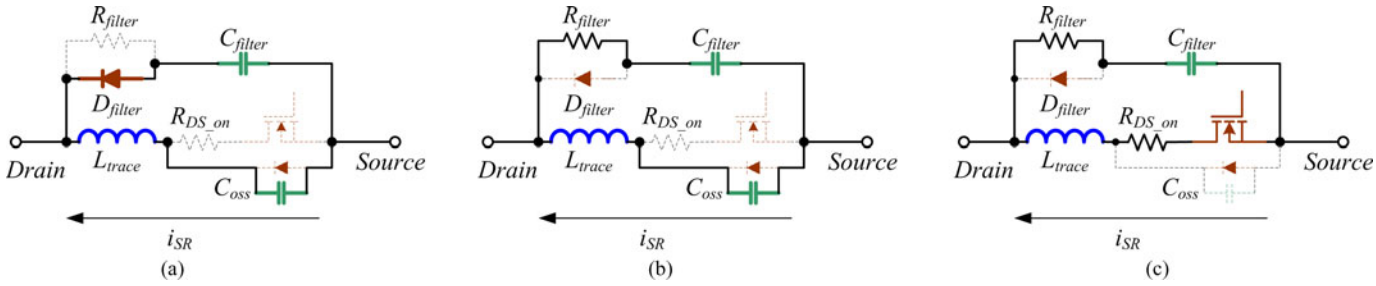


Fig. 12. Operation modes of the SR with the ZCNF: (a) t_0–t_1, (b) t_1–t_2, and (c) t_2–t_4.

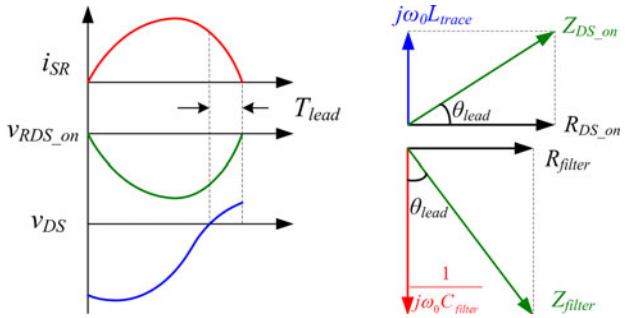


Fig. 13. Voltage matching method for the SR with the ZCNF. (a) Key waveforms of the SR. (b) Vector diagram of voltage matching.

current can be described as

$$i_{Ls}(t) = I_{Ls} \cdot \sin\left(2\pi f_0 t + \arcsin\frac{i_{Lm}(0)}{I_{Ls}}\right) \tag{5}$$

where I_{Ls} is the peak value of the current through the resonant tank. $i_{Lm}(0)$ is the initial value of the magnetizing current. According to the actual experiment, each SR uses two synchronous MOSFET connect in parallel; therefore, the current through each synchronous MOSFET is

$$i_{\mathrm{SR}}(t) = \frac{N \cdot (i_{Ls}(t) - i_{Lm}(t))}{2}. \tag{6}$$

The calculated current waveforms are illustrated in Fig. 14, where i_{Lm} and i_{Ls} have been converted to the secondary side of the transformer.

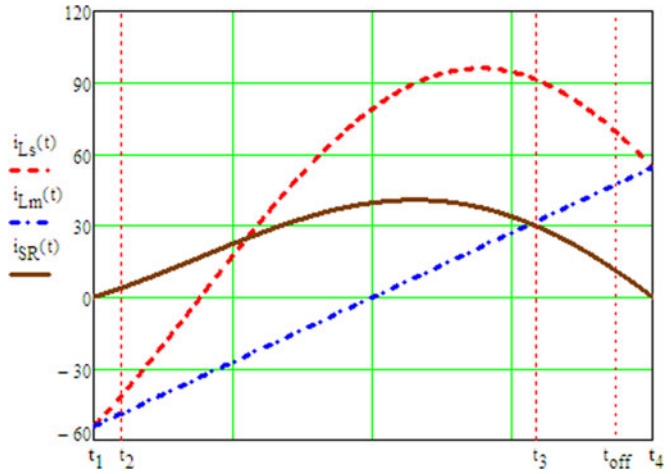


Fig. 14. Calculated current waveforms of i_{Ls}, i_{Lm}, and i_{SR} at heavy-load condition.

V_{DS} of the SR can be deduced as

$$v_{\mathrm{DS}}(t) = i_{\mathrm{SR}}(t) \cdot R_{\mathrm{DS\_on}} + L_{\mathrm{trace}} \cdot \frac{di_{\mathrm{SR}}(t)}{dt}. \tag{7}$$

Before the voltage across the C_{filter} v_{filter} reaches the turn-on threshold of the control chip, the ZCNF takes effects. As shown in Fig. 11(a), v_{filter} decreases slowly from $V_{\mathrm{FD}} - V_{\mathrm{Fb}}$ to $-V_{\mathrm{Fb}}$ as an exponential curve. As soon as v_{filter} reaches the turn-on threshold ($V_{\mathrm{TH\_on}} = 0$ V), the compensation network starts to

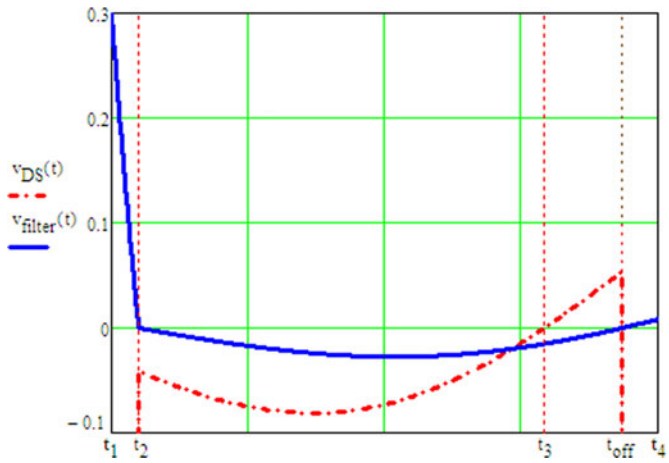


Fig. 15. Calculated voltage waveforms of $v_{\rm DS}$ and $v_{\rm filter}$ at heavy-load condition.

work. $v_{\rm filter}$ can be deduced as

$$v_{\rm filter}=\begin{cases} V_{\rm FD}\cdot e^{-\frac{t-t_1}{\tau_{\rm filter}}}-V_{\rm Fb}, & \text{if } t_1\le t\le t_2 \\ e^{-\frac{t-t_2}{\tau_{\rm filter}}}\cdot\displaystyle\int_{t_2}^{t} v_{\rm DS}(t)\cdot e^{\frac{t-t_2}{\tau_{\rm filter}}}dt, & \text{if } t_2\le t\le t_4. \end{cases} \tag{8}$$

The calculated voltage waveforms are illustrated in Fig. 15, where t_2 is the moment when the SR turns ON, t_3 is the moment when the SR is turned OFF if $v_{\rm DS}$ is detected directly (without ZCNF) and fed to the SR drive chip, and $t_{\rm off}$ is the moment when SR is turned OFF if $v_{\rm filter}$ (after ZCNF) is sensed as a substitute to $v_{\rm DS}$. It is observed that the duty-cycle loss is about one-fourth of the resonant time if $v_{\rm DS}$ is detected directly. This result matches the experimental result as shown in Fig. 8.

It can be observed from the analyses above that ZCNF can significantly reduce the early turn-off of SR FET and will cause a slight turn-on delay for SR FET due to discharging of the filter capacitor. The reduced power loss due to removal of body diode loss at turn-off of SR FET is much more than the added body diode loss due to late turn-on of SR FET. Table I shows the comparison of these two losses for each SR MOSFET with and without ZCNF. Since the current through the diode $D_{\rm filter}$ is very small, in calculation, the forward voltage of $D_{\rm filter}V_{\rm FD}$ is set as a constant value of 1.2 V which is equal to that of two small-signal diodes connected in series. The calculated results show that the proposed ZCNF can work properly at a wide range of the MOSFET body diode forward voltage $V_{\rm Fb}$.

It is noted from the above table that the higher the body diode voltage drop, the higher the loss reduction. It is noted that the forward voltage drop of an SR FET is normally high. For example, the voltage drop of the SR FET used in the prototype in this paper can be as high as 1.1 V. If a more moderate voltage drop of 0.9 V is assumed, the SR FET body diode conduction loss caused by the premature turn-off (or early turn-off) problem is about $P_{\rm loss}=1.52$ W for each synchronous MOSFET at full-load condition. After introducing the ZCNF to the SR drive circuit, although it induces an additional body diode loss before SR FET is turned ON (0.04 W), the body diode loss after SR is turned OFF is reduced to 0.16 W. The total loss reduction is 1.32 W (1.52 – 0.04 – 0.16), which is still significantly lower. This is mainly due to the fact that in the SR turn-on case, the current rises from zero and the conduction loss is small even though the body diode is conducting. On the other hand, in the turn-off case, the SR FET current is still very high when the SR FET is turned OFF earlier and significant conduction loss is introduced.

2) Light-Load Condition: At light-load condition, as shown in Fig. 2(b), the voltage across the resonant capacitor v_{Cs} is almost a constant value and $v_{Cs}\approx {\rm V_{in}}/2$. Therefore, the magnetizing current of the transformer can be described as

$$i_{Lm}(t)=\frac{V_{\rm in}}{2\cdot L_m}\cdot\left(t-\frac{1}{4f_0}\right). \tag{9}$$

When the series resonance starts, the tangent of the resonant current i_{Ls} coincides with the magnetizing current i_{Lm}. Suppose i_{Ls} can be written as

$$i_{Ls}(t)=I_{Ls}\cdot\sin(2\pi f_0 t-\alpha). \tag{10}$$

The point of tangency can be calculated as

$$t_2=\frac{1}{4f_0}-\frac{2L_m\cdot I_{Ls}}{V_{\rm in}}\cdot\sin\left(\arccos\left(\frac{V_{\rm in}}{2\pi f_0\cdot 2L_m\cdot I_{Ls}}\right)\right). \tag{11}$$

And the initial phase angle α can be calculated as

$$\alpha=2\pi f_0 t_2+\arccos\left(\frac{V_{\rm in}}{2\pi f_0\cdot 2L_m\cdot I_{Ls}}\right). \tag{12}$$

Accordingly, the end moment of the series resonance can also be calculated as

$$i_{Ls}(t_4)=i_{Lm}(t_4). \tag{13}$$

The current through each synchronous MOSFET is

$$i_{\rm SR}(t)=\begin{cases}\dfrac{N\cdot(i_{Ls}(t)-i_{Lm}(t))}{2}, & \text{if } t_2\le t\le t_4 \\ 0, & \text{if } t<t_2\vee t>t_4. \end{cases} \tag{14}$$

The calculated current waveforms are illustrated in Fig. 16 in which i_{Lm} and i_{Ls} have been converted to the secondary side of the transformer.

As shown in Fig. 11(b), $V_{\rm filter}$ can be deduced as

$$v_{\rm filter}=\begin{cases} e^{-\frac{t-t_2}{\tau_{\rm filter}}}\cdot\displaystyle\int_{t_2}^{t} v_{\rm DS}(t)\cdot e^{\frac{t-t_2}{\tau_{\rm filter}}}dt, & \text{if } t_2\le t\le t_4 \\ 0, & \text{if } t<t_2\vee t>t_4. \end{cases} \tag{15}$$

The calculated voltage waveforms are illustrated in Fig. 17 in which t_2 is the moment when the SR turns ON, t_3 is the moment when the SR is turned OFF if $v_{\rm DS}$ is detected directly (without ZCNF) and fed to the SR drive chip, and $t_{\rm off}$ is the moment SR is turned OFF if $v_{\rm filter}$ is sensed as a substitute to $v_{\rm DS}$. Compared with Fig. 15, it is apparent that t_4–$t_{\rm off}$, the interval between $t_{\rm off}$ and the moment when the SR current reaches to zero, decreases in accordance with the load reduction. Therefore, the overcompensation might happen at very light load condition. In this case, burst-mode operation or minimum on-time protection

TABLE I
DUTY CYCLE AND BODY DIODE CONDUCTION LOSS VARIATION AT FULL-LOAD CONDITION

V_{Fb} (V)	0.5	0.7	0.9	1.1
Without ZCNF: body diode loss after SR is turned off (W)	0.84	1.18	1.52	1.86
With ZCNF: body diode loss before SR is turned on (W)	0.23	0.12	0.04	0.004
With ZCNF: body diode loss after SR is turned off (W)	0.09	0.13	0.16	0.2
Loss reduction with ZCNF (W)	0.52	0.93	1.32	1.66

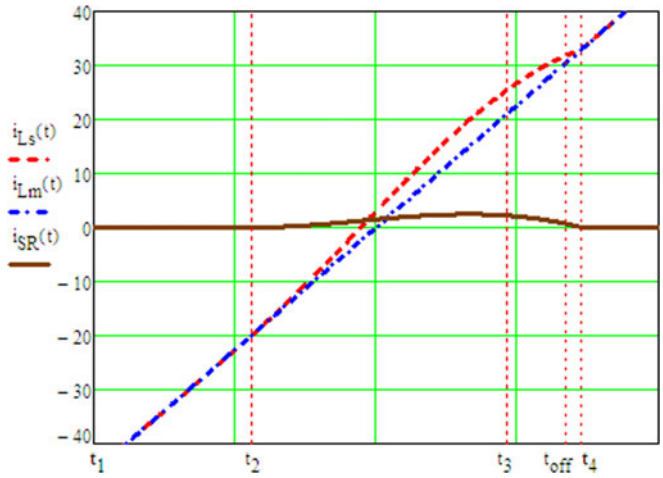


Fig. 16. Calculated current waveforms of i_{Ls}, i_{Lm}, and i_{SR} at light-load condition.

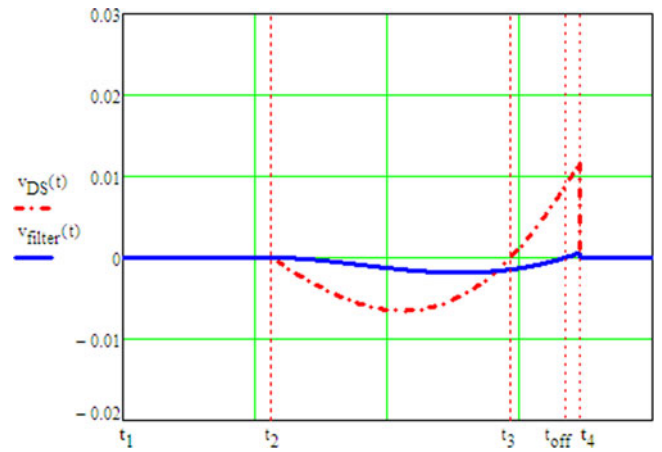


Fig. 17. Calculated voltage waveforms of v_{DS} and v_{filter} at light-load condition.

mode should be adopted to improve the light-load performance and eliminate the overcompensation probability in very light load condition.

For the forward voltage variation of the SR FET body diode, as shown in (15), the forward voltage of the body diode has no effect on the initial value of the v_{filter} at the light-load condition if the precondition $V_{\mathrm{Fb}} < V_{\mathrm{FD}}$ is met. Therefore, the variation of V_{Fb} has no impact on the duty-cycle compensation at the light-load condition.

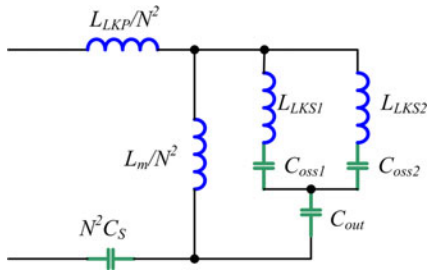


Fig. 18. Equivalent circuit of the parasitic ringing.

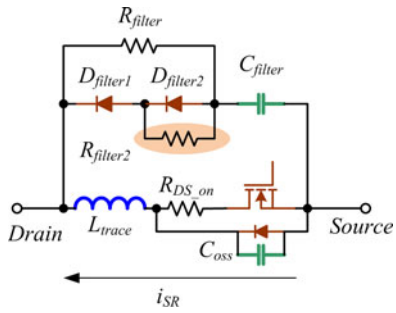


Fig. 19. Reduced time constant for the turn-on noise filter.

B. Parameters Selection for the ZCNF Function

Due to the high-frequency nature of the voltage spikes, the time constant of the noise filter should be very small. According to Fig. 1, the equivalent circuit of the parasitic ringing is deduced in Fig. 18. Comparing the leakage inductance of the transformer with the output capacitance of the SRs, the influences of the magnetizing inductance L_m, the series-resonant capacitor C_S, and the output capacitor C_{out} can be neglected. To simplify the analysis, it is assumed that

$$L_{\mathrm{LKS1}} = L_{\mathrm{LKS2}} = L_{\mathrm{LKS}}$$
$$C_{\mathrm{oss1}} = C_{\mathrm{oss2}} = C_{\mathrm{oss}}. \tag{16}$$

The ringing frequency can be derived as

$$f_{\mathrm{ripple}} = \frac{1}{2\pi \cdot \sqrt{\left(\frac{L_{\mathrm{LKP}}}{N^2} + \frac{L_{\mathrm{LKS}}}{2}\right) \cdot 2C_{\mathrm{oss}}}}. \tag{17}$$

To prevent the false-triggering problem, the time constant of the filter τ_{filter}, as shown in (3). should be selected a little bit larger than the period of the parasitic ringing. Since there is only one time constant in the ZCNF, conflict may happen between the filter function and the duty-cycle compensation function.

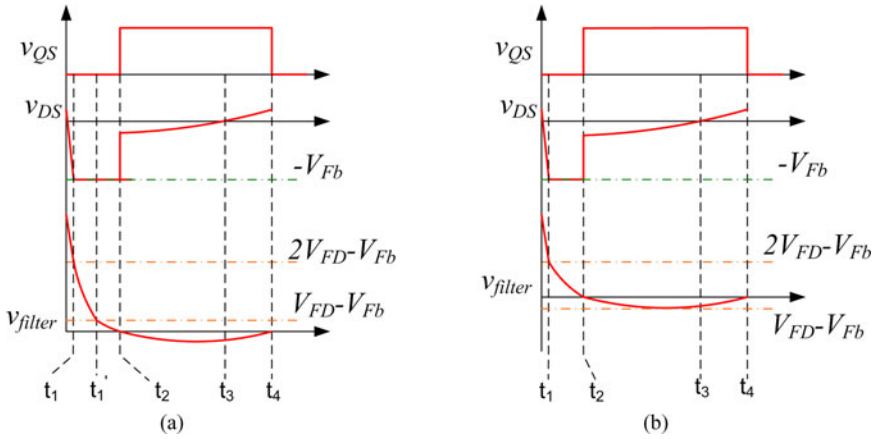


Fig. 20. Key waveforms for the ZCNF with reduced time constant. (a) $V_{\rm Fb} < V_{\rm FD}$. (b) $V_{\rm FD} < V_{\rm Fb} < 2V_{\rm FD}$.

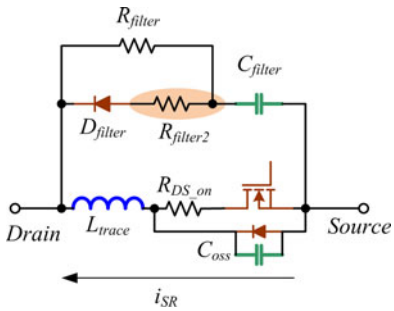


Fig. 21. Increased time constant for the turn-on noise filter.

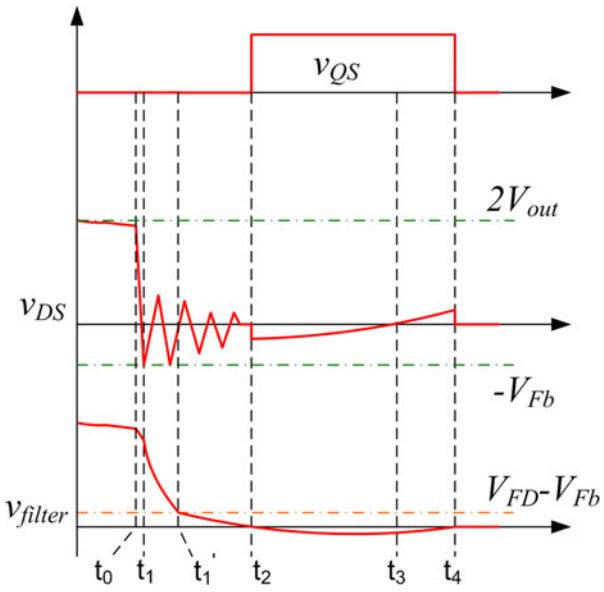


Fig. 22. Key waveforms for the ZCNF with additional time constant.

Suppose the duty-cycle compensation has been finished by the previous section, the following sections will focus on the time constant configuration for the filter function.

1) Solution for the Overfiltering Problem: As shown in Table I, the turn-on duty-cycle loss is inevitable after applying the ZCNF to the SR control circuit. In most situations, this duty-cycle loss caused body diode conduction loss is very small

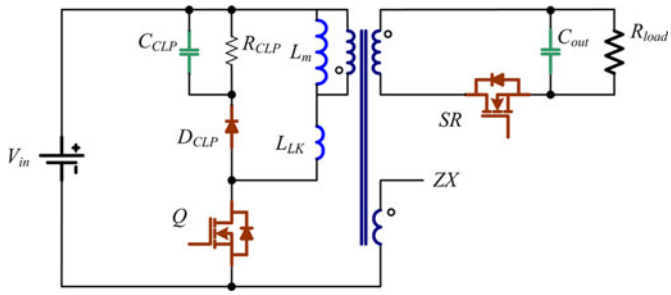


Fig. 23. Circuit diagram of the QR mode Flyback converter with SR.

due to the low current value at the beginning of a switching cycle. However, if this loss is too high to be acceptable, method should be taken to reduce this turn-on duty-cycle loss.

Fig. 19 shows the ZCNF with reduced time constant for the noise filter function. By adding an extra resistor $R_{\rm filter2}$, the time constant for the turn-on noise filter changes from $\tau_{\rm filter}$ to

$$\tau_{\rm filter2} = \frac{R_{\rm filter} \cdot R_{\rm filter2}}{R_{\rm filter} + R_{\rm filter2}} \cdot C_{\rm filter}. \tag{18}$$

Fig. 20 shows the key waveforms of the ZCNF with reduced time constant. Since there are two small-signal diodes connected in series, the total forward voltage of $D_{\rm filter1}$ and $D_{\rm filter2}$ is $2V_{\rm FD}$. If the forward voltage of the MOSFET body diode $V_{\rm Fb}$ is lower than the forward voltage of the small-signal diode $V_{\rm FD}$, $v_{\rm filter}$ will decrease to $V_{\rm FD}$–$V_{\rm Fb}$ first with the time constant of $\tau_{\rm filter2}$ which is shown in (18), and then continue to decrease with a time constant of $\tau_{\rm filter}$ until the turn-on threshold ($V_{\rm TH\_on} = 0$ V) is reached, as shown in Fig. 20(a). Otherwise, if $V_{\rm Fb}$ is higher than $V_{\rm FD}$, $v_{\rm filter}$ will decrease directly to $V_{\rm TH\_on}$ with the time constant of $\tau_{\rm filter2}$, as shown in Fig. 20(b).

2) Solution for the Underfiltering Problem: Usually, the time constant $\tau_{\rm filter}$ is far more than the period of the parasitic ringing. In some circumstances, such as the transformer leakage inductance or the MOSFET output capacitor $C_{\rm oss}$ is very high, $\tau_{\rm filter}$ might be not high enough to filter out the parasitic ringing. In this case, the extra resistor can be placed in series with the small-signal diode $D_{\rm filter}$, as shown in Fig. 21.

In Fig. 21, some details should be clarified.

TABLE II
PARAMETERS OF THE PROTOTYPE

L_m (μH)	100	C_S (nF)	40
L_{LKP} (μH)	6.8	R_{filter} (kΩ)	3.9
L_{LKS} (nH)	15	C_{filter} (pF)	100
D_{filter}	1N4148 (2 in series)		
SR driving IC	IR1168	Q_H, Q_L	IPB50R299CP
Turns ratio	20:1:1	Q_{S1}, Q_{S2}	SIR158DP (2 in parallel)

1) Different from the highlighted resistor in Fig. 19, the resistor $R_{\rm filter2}$ in Fig. 21 will take effect at the whole falling edge of $v_{\rm DS}$ other than the zero crossing area. Therefore, the value of $R_{\rm filter2}$ should be very small to make time constant far less than $\tau_{\rm filter}$; otherwise, it will induce a big body diode conduction loss at the turn-on due to the lag turn-on problem as explained in Section II-A.
2) The total forward voltage of the small-signal diodes $V_{\rm FD}$ is still need to be selected higher than $V_{\rm Fb}$, $V_{\rm FD} > V_{\rm Fb}$; otherwise, it will cause false turn-on problem and reversed energy to the input at the light-load condition.

Key waveforms for the circuit in Fig. 21 are shown in Fig. 22. Since $v_{\rm DS}$ decreases from around $2V_{\rm out}$ to $-V_{\rm Fb}$, the initial value of $v_{\rm filter}$ should also be around $2V_{\rm out}$. Because the time interval t_0–t_1 is very short, t_1–t_1' can be taken as the needed extra filter time $t_{\rm filter\_extra}$:

$$t_{\rm filter\_extra} = \frac{R_f \cdot R_{f2}}{R_f + R_{f2}} \cdot C_f \cdot \ln \frac{2V_{\rm out} + V_{\rm Fb} - V_{\rm FD} \cdot \frac{R_f}{R_f + R_{f2}}}{V_{\rm FD} \cdot \frac{R_{f2}}{R_f + R_{f2}}}. \quad (19)$$

This extra filter time should be at least two times higher than the period of the parasitic ringing to ensure the reliable operation.

C. Extended Application to Other Topology

Due to the intrinsic filtering and compensation ability, the ZCNF can be applied to all the other synchronous rectification applications with zero-current-off characteristic such as the quasi-resonant (QR) mode and discontinuous current mode converter. Taking the QR mode flyback converter for example, the duty cycle of the SR is greatly affected by the lead inductance of the SR and the transformer leakage inductance caused parasitic ringing. The typical circuit of the QR mode flyback converter is shown in Fig. 23 in which ZX is the demagnetizing signal, L_m and $L_{\rm LK}$ are the magnetizing inductance and leakage inductance of the transformer, respectively. As shown in Fig. 24, the leakage inductance of the transformer $L_{\rm LK}$ resonates with parasitic capacitors such as $C_{\rm oss}$ of the primary-side switch Q and the distributed capacitance of the transformer after the SR turns ON. This ringing will be coupled to the lead inductance of the SR by the rectified current and cause the premature turn-off of the SR.

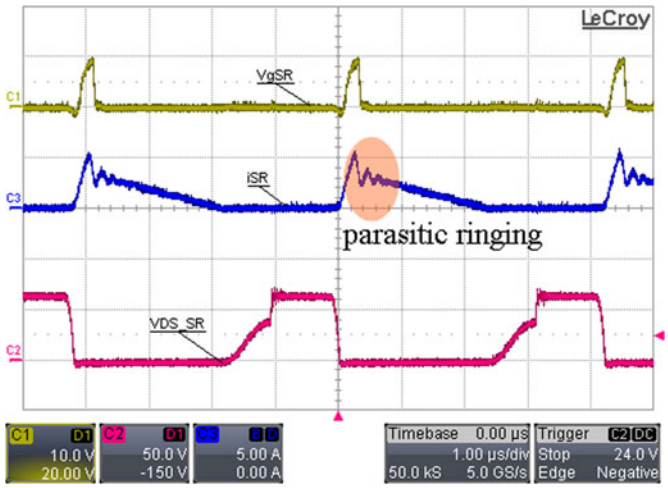


Fig. 24. Parasitic ringing caused premature turn-off.

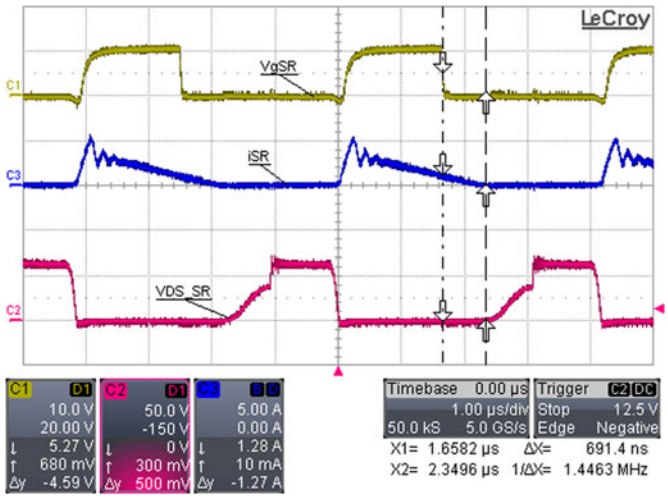


Fig. 25. Lead inductance caused premature turn-off.

Most of the commercial SR controllers have a configurable minimum on-time which can be used to filter out this parasitic ringing after the SR turns ON. However, this function needs to be disabled at some specific operational conditions such as very light load condition to guarantee a safe operation of the SR. Fig. 25 shows the experimental waveform with increased minimum on-time. The parasitic ringing caused false turn-off problem is avoided but the SR lead inductance caused duty-cycle loss still exists. By adding the ZCNF to the SR, both the parasitic ringing caused premature turn-off and the lead

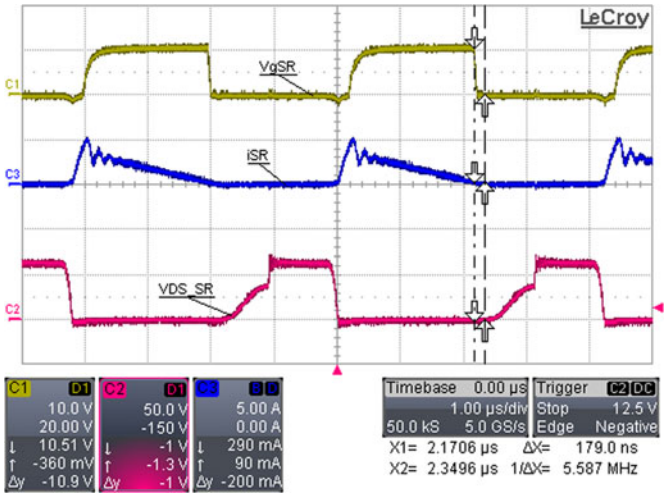


Fig. 26. Experimental waveform of the SR with ZCNF in QR mode Flyback converter.

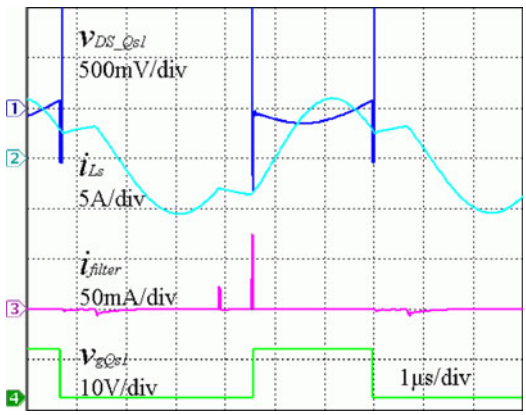


Fig. 27. Simulation results of the $v_{\rm DS}$, i_{Ls}, and the current through the ZCNF.

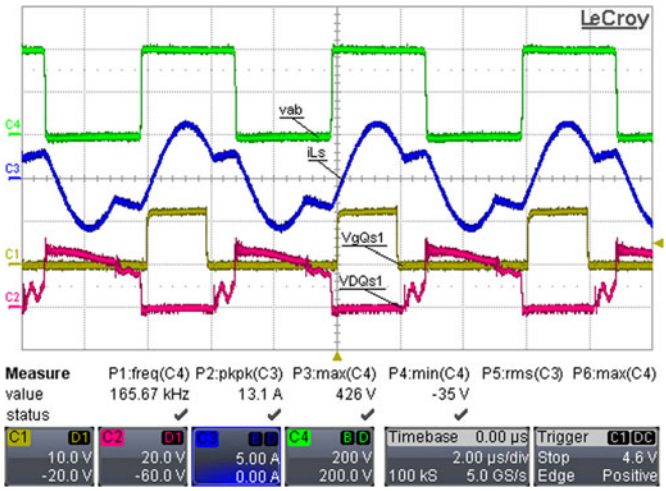


Fig. 28. Experimental waveform of the SR with ZCNF at full-load condition.

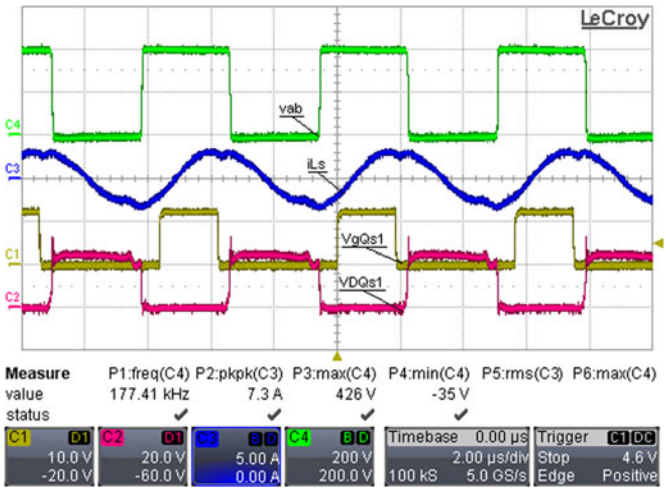


Fig. 29. Experimental waveform of the SR with ZCNF at light-load condition.

inductance caused duty-cycle loss can be effectively removed, as shown in Fig. 26. Because of no minimum on-time limitation, the ZCNF provides safer operation conditions for the SR.

V. Simulation and Experimental Results

To verify the theoretical analysis in the previous section, a prototype of 400 V/12 V 600-W half-bridge *LLC* resonant converter with SRs is built. L6599 from ST Semiconductor is selected as the primary-side controller. The switching frequency is around 170 kHz. The parameters of the circuit are listed in Table II.

Fig. 27 shows the simulation results of $v_{\rm DS}$, the current of the resonant tank, and the current through the ZCNF. It is observed that the extra loss of the ZCNF is tiny. A very short delay at the switch on and a very short lead time at the switch off are added to prevent reverse energy flow from the output capacitor to the source. Because of the small turn-on and turn-off currents of the SR, the conduction loss of the body diode can be neglected.

Figs. 28 and 29 illustrate the experimental waveforms of the SR with ZCNF at full-load and light-load conditions. It is noted that the switching frequency at full load is 165 kHz and the switching frequency at light load is 178 kHz. It shows that the SR with ZCNF can operate properly at any load condition. The turn-on delay and the turn-off lead time match with the theoretical analyses as shown in Figs. 14–17 which verified the theoretical calculations.

Figs. 30–32 show the transient tests of the *LLC* converter with zero-crossing filter. Fig. 30 shows the experiment results from full-load (50 A) to light-load (5 A) condition. Fig. 31 shows the results from light-load (5 A) to full-load (50 A) conditions. All the current slew rates of the step load changes are set as 2.5 A/μs. Fig. 32 shows the converter operating under the burst mode condition (0.5 A). The experiment results demonstrate that the zero-crossing noise can operate under transient condition properly.

Fig. 33 compared the measured efficiency between the prototypes with and without ZCNF at different load condition. It shows clearly that at all load conditions, the proposed ZCNF can effectively improve the efficiency of the *LLC* converter. At full load, the efficiency is improved from 95% to 95.8%. Equivalently, the power loss is reduced by 5.3 W (from 31.6 to 26.3 W), a reduction of 17% which is in accordance with the

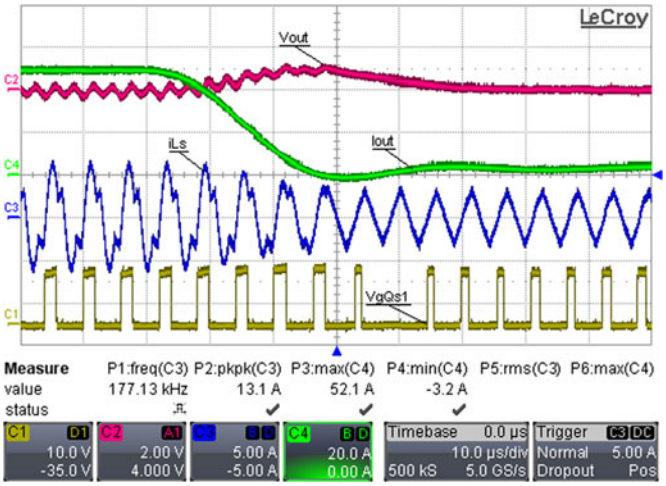


Fig. 30. Load transient test from full-load to light-load condition of the *LLC* converter.

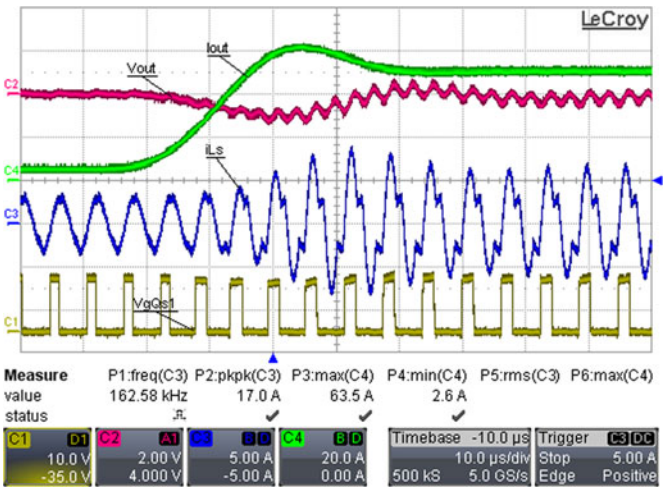


Fig. 31. Load transient test from light-load to full-load condition of the *LLC* converter.

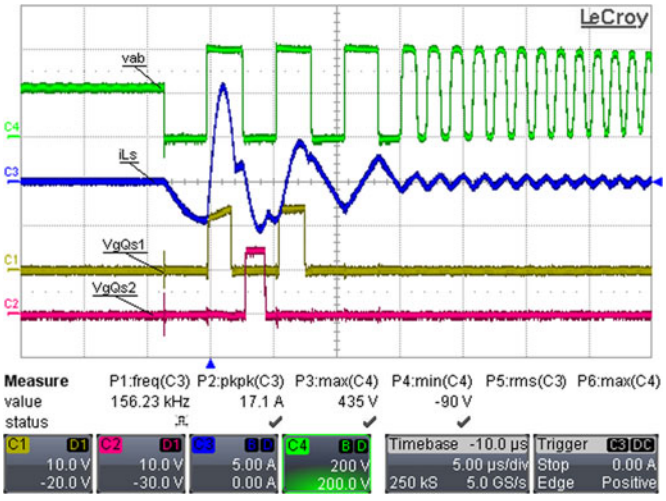


Fig. 32. Burst mode test of the *LLC* converter with ZCNF.

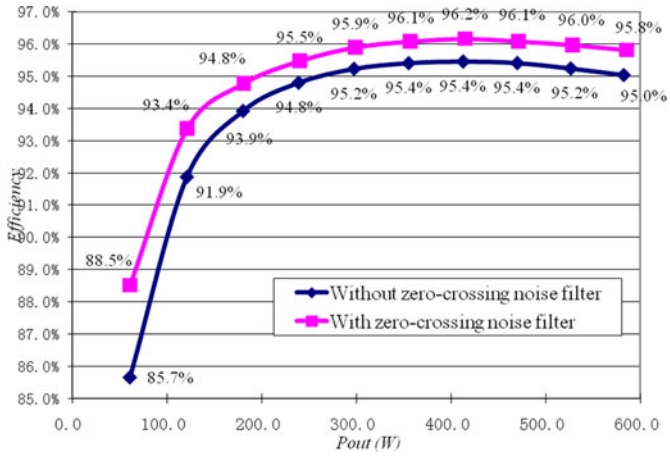


Fig. 33. Efficiency comparison of the circuit with and without the ZCNF.

theoretical analyses in Section IV. The experimental results presented in this section demonstrate that the ZCNF can improve the efficiency of the *LLC* converter and remove the impact of the ringing caused by the parasitic inductance and MOSFET output capacitance.

VI. Conclusion

In this paper, the problems of the existing SR FET driving methods in the *LLC* converter are discussed. A ZCNF is proposed that can remove the impact of the ringing caused by parasitic parameters and can accurately control the turn-on and turn-off of the SR FET. The operation of the ZCNF is analyzed in detail and the selection of filter parameters is presented. A 400 V to 12 V 600 W half-bridge *LLC* resonant converter prototype is built to verify the theoretical analysis and to demonstrate its advantages. Efficiency improvement of 0.8% is achieved with the proposed ZCNF.

References

[1] A. Lokhandwala, M. Salato, and M. Soldano, "Dual SmartRectifier and DirectFET chipset overcomes package source inductance effects and provides accurate sensing for synchronous rectification in DC-DC resonant converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2007, pp. 1559–1562.

[2] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. van Wyk, "Optimal design methodology for LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2006, pp. 533–538.

[3] B. Wang, X. Xin, S. Wu, H. Wu, and J. Ying, "Analysis and implementation of LLC burst mode for light load efficiency improvement," in *Proc. IEEE Appl. Power Electron. Conf.*, 2009, pp. 58–64.

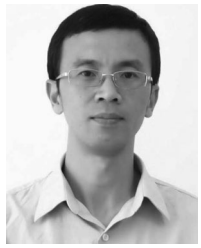
[4] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.

[5] J. Liao, J. Wang, J. Zhang, and Z. Qian, "A novel current driving scheme for LLC resonant converter with Synchronized voltage-doubler rectifier," in *Proc. IEEE Appl. Power Electron. Conf.*, 2011, pp. 566–570.

[6] X. Wu, B. Li, Z. Qian, and R. Zhao, "Current driven synchronous rectifier with primary current sensing for LLC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 738–743.

[7] C. Zhao, B. Li, J. Cao, Y. Chen, X. Wu, and Z. Qian, "A novel primary current detecting concept for synchronous rectified LLC resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 766–770.

[8] X. Wu, G. Hua, J. Zhang, and Z. Qian, "A new current-driven synchronous rectifier for series-parallel resonant (LLC) DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 289–297, Jan. 2011.
[9] G. Zhang, J. Zhang, C. Zhao, X. Wu, and Z. Qian, "LLC resonant DC/DC converter with current-driven synchronized voltage-doubler rectifier," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 744–749.
[10] B. Yuan, M. Xu, X. Yang, and D. Li, "A new structure of LLC with primary current driven synchronous rectifier," in *Proc. IEEE Power Electron. Motion Control Conf.*, 2009, pp. 1266–1269.
[11] J. Wang, J. Zhang, G. Zhang, M. Xu, and Z. Qian, "Research on key application issues of smart synchronous rectifier driver IC in LLC resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2765–2770.
[12] G.-C. Hsieh, C.-Y. Tsai, and W.-L. Hsu, "Synchronous rectification LLC series-resonant converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2007, pp. 1003–1009.
[13] W. Feng, F. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3775–3781, Aug. 2012.
[14] A. Lokhandwala, "Design of secondary-side rectification using IR1168 dual SmartRectifier^{TM} control IC," IR Appl. Note AN-1139, 2008.
[15] "Synchronous rectifier smart driver for LLC resonant converter," ST Datasheet SRK2000 Rev. 1, 2010.
[16] X. Xie, J. C. P. Liu, F. N. K. Poon, and M. H. Pong, "A novel high frequency current-driven synchronous rectifier applicable to most switching topologies," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 635–648, Sep. 2001.
[17] L. Cheng, T. Liu, H. Gan, J. Ying, "Adaptive synchronous rectification control circuit and method thereof," U.S. Patent 7 495 934, 2009.
[18] R. Lenk, "Application bulletin AB20 optimum current-sensing techniques in CPU converters," Fairchild Semiconductor Application Notes, 1999.
[19] E. Dallago, M. Passoni, and G. Sassone, "Lossless current sensing in low-voltage high-current DC/DC modular supplies," *IEEE Trans. Ind. Electron.*, vol. 47, no. 6, pp. 1249–1252, Dec. 2000.
[20] H. P. Forghani-zadeh and G. A. Rincon-Mora, "Current-sensing techniques for DC-DC converters," in *Proc. IEEE Midwest Symp. Circuits Syst.*, 2002, pp. 577–580.
[21] L. Hua and S. Luo, "Design considerations for small signal modeling of DC-DC converters using inductor DCR current sensing under time constants mismatch conditions," in *Proc. IEEE Power Electron. Soc. Conf.*, 2007, pp. 2182–2188.
[22] D. Wang, L. Jia, J. Fu, Y.-F. Liu, and P. C. Sen, "A new driving method for synchronous rectifiers of LLC resonant converter with zero-crossing noise filter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 249–255.
[23] "Secondary-side rectification for an LLC resonant converter featuring the SRK2000," ST Application Note AN-3303 Rev. 1, Jan. 2011.
[24] "Secondary-side rectification for an LLC resonant converter featuring the SRK2000," ST Application Note AN-3303 Rev. 2, Sep. 2011.
[25] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. New York, NY, USA: Wiley, 1995.



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