Electrolytic-Capacitor-Less High-Power LED Driver

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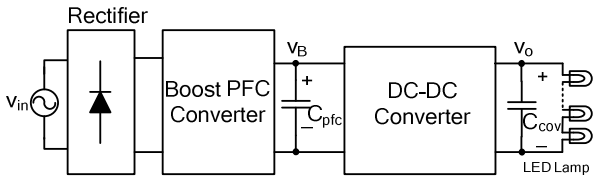
***Abstract*—Conventional topologies for high-power LED drivers with high power factors require large capacitances to mitigate the output current ripples. Electrolytic capacitors are commonly used because they are the only capacitors with sufficient energy density to accommodate high power applications. However, the short life span of electrolytic capacitors significantly reduces the life span of the entire LED lighting fixture, which is undesirable. This paper proposes a single-stage high-power LED driver using ripple compensation concept to minimize the output capacitance requirement, enabling the use of long-life film capacitors. Compared to existing technologies, the proposed circuit achieves zero ripple current through LED lamps and achieves a high power factor and high efficiency. A 100W (150V/0.7A) LED driver prototype was built which demonstrates that the proposed method can achieve the same LED current with only 44μF film capacitors, compared to the 4700μF electrolytic capacitors required in conventional single-stage LED drivers. Meanwhile, the proposed prototype has achieved a peak power efficiency of 92%, benefiting from active clamp technology.**

I. INTRODUCTION

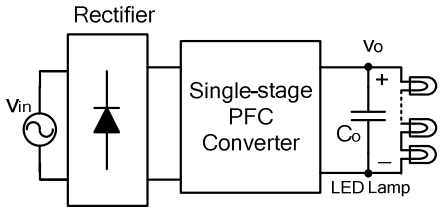
High-power LED drivers are commonly used in outdoor lighting applications. In these applications, a large number of LEDs are connected in series to increase the lumens. This configuration yields a high output voltage and low output current combination, and usually requires isolation.

Conventional LED driver solutions include two categories: (a) two-stage configuration [1-3] and (b) single-stage configuration [4-6]. The two-stage configuration, as shown in Figure 1(a), can achieve high power factor and tight output current regulation, making it a popular choice for high-power LED drivers. However, it exhibits a poor efficiency and low power density. Usually capacitors of high capacitance value are needed at the output of the power factor correction stage to buffer the power difference of the AC input and DC output. The necessary capacitance is generally around 1μF per Watt [7]. The PFC output capacitance can be reduced by increasing the voltage ripple[7]. However, the possible capacitance reduction is limited because the PFC output voltage must be higher than the minimum input line voltage to ensure the normal operation of the boost PFC converter. Therefore, electrolytic capacitors are required.

Conventional single-stage configuration, as shown in Figure 1(b), presents a cost effective and high-efficiency solution, yet the large electrolytic capacitors are still necessary to reduce the double line frequency (120Hz) ripple. Otherwise, the double line frequency current ripple will cause light flickering, which is harmful to human visual system [8-10]. Many solutions have been proposed to reduce this ripple.



(a) Two-stage configuration



(b) Single-stage configuration.

Figure 1 Conventional high-power LED driver configurations.

One method is to inject the harmonics (3rd and 5th) into the input current [11, 12]. This sacrifices the power factor,

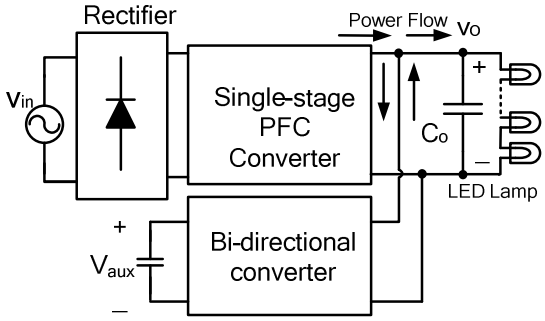


Figure 2 Parallel compensation configuration.

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which is unacceptable for high-power LED drivers. In [13-15], an auxiliary ripple cancellation stage is connected in parallel with the PFC output, as shown in Figure 2. The auxiliary stage must withstand the same high voltage stress equal to the PFC output voltage. Therefore, high voltage-rating components are necessary, which generally have higher cost and lower efficiency than their low-voltage-rating counterparts. In [16, 17], the auxiliary stage is in series with the PFC output, thus the voltage stress can be reduced to the pk-to-pk voltage ripple value. However, the room for capacitance reduction is also limited since the ripple cancellation circuit is unipolar. The auxiliary stage must provide a large DC component to cancel a large PFC output ripple. This increases the stress on the auxiliary circuit, which is also unfavorable to achieve high efficiency.

In this paper, a novel high power single-stage LED driver solution is proposed. The bipolar ripple compensation stage is used to generate a pure AC voltage with zero DC bias which accurately tracks the voltage ripple of the PFC output. With this compensation stage, the PFC output capacitance can be significantly reduced, allowing long-life film capacitors to be used.

The paper is organized as follows: Section II introduces the operation principles of the proposed LED driver configuration. Section III provides the step by step design procedure. Section IV describes the operation modes and advantages of the proposed bipolar ripple compensation stage. Section V provides the experimental results, and Section VI is the conclusion.

II. OPERATION PRINCIPLES OF THE PROPOSED LED DRIVER CONFIGURATION

A. Basic Concept of Proposed LED Driver

Figure 3 shows circuit block diagram of the proposed electrolytic-capacitor-less configuration for high-power LED driver.

This configuration consists of a PFC stage and a bipolar ripple compensation stage (hereafter referred to as the bipolar compensation stage). The main output voltage and the compensation output voltage are connected in series to power the LED lamps. Figure 4 shows the voltage waveforms of the main output, ripple compensation stage output and the LED voltage.

The PFC output voltage, V_{main}, includes both the AC and DC voltage components. The AC voltage ripple is at double line frequency, shown as the upper red dashed line in Figure 4. The expression of the PFC output voltage is in (1).

$$v_{main} = V_{DC} + v_{ripple} \tag{1}$$

where V_{DC} is the DC component of the PFC output voltage, and v_{ripple} is the AC component of PFC output voltage. The output voltage of the compensation stage v_{comp} is a pure AC voltage, shown as the middle blue dotted line in Figure 4 with zero DC voltage. In order to achieve a ripple-free output voltage across the LED lamps, the compensation voltage v_{comp}, must offset the ripple voltage, v_{ripple}, as given in (2).

$$v_{comp}(t) = -v_{ripple}(t) \tag{2}$$

The voltage across the LED lamp is the sum of the PFC output voltage and the compensation voltage, expressed in (3).

$$V_{LED} = v_{main} + v_{comp} \tag{3}$$

Substitution of (1) and (2) into (3) yields (4):

$$V_{LED} = V_{DC} \tag{4}$$

The LED lamp sees only the DC component as shown in the lower brown solid line in Figure 4. It is noted that the peak to peak value of the double line frequency voltage ripple in PFC output V_{ripple} is proportional to the LED output current I_{LED} as well as the PFC output capacitance C_{main}, as shown in (5).

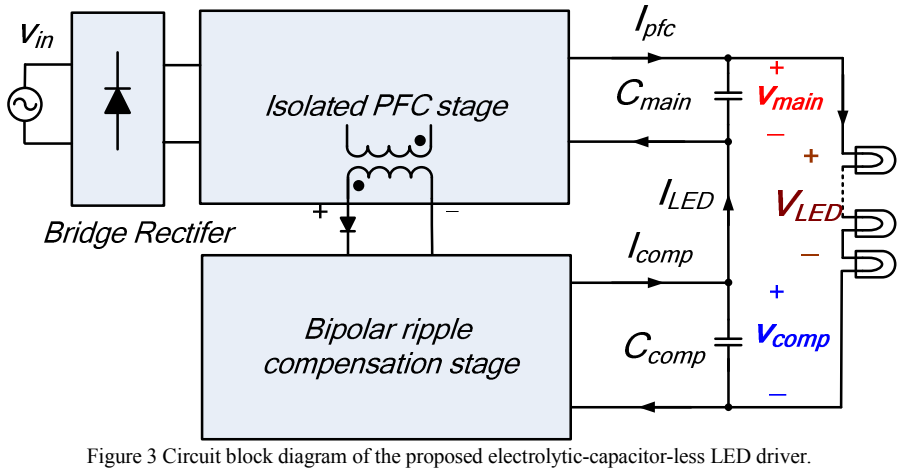


Figure 3 Circuit block diagram of the proposed electrolytic-capacitor-less LED driver.

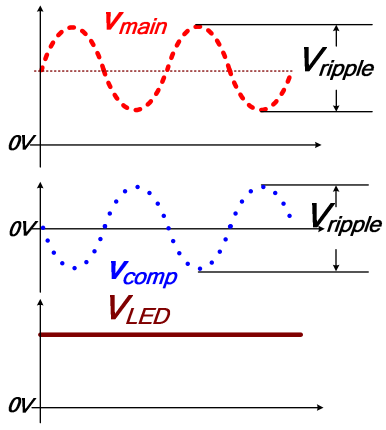


Figure 4 key waveforms of proposed bipolar compensation method

$$V_{ripple} = \frac{P_{in}}{\omega \times C_{main} \times V_{LED}} = \frac{I_{LED}}{2\pi \times f \times C_{main}} \quad (5)$$

A smaller value of C_{main} should be used in order to remove the electrolytic capacitor from the proposed configuration, which will be discussed in Section III (C).

The prototype of the proposed LED driver with a bipolar compensation stage is shown in Figure 5. An active clamped Flyback converter operating in continuous conduction mode (CCM) [18-22] is used to achieve power factor correction. It provides all of the LED driving power as well as a small amount of power to the bipolar compensation stage. According to the experimental results, active clamp technology is able to increase the efficiency of the PFC stage by 2% compared to conventional single-stage PFC technologies using RCD snubbing. The auxiliary serial bipolar compensation stage only compensates the AC voltage ripple.

B. Bipolar Compensation Stage

Figure 6 illustrates the control of the bipolar compensation stage. Firstly, the PFC output voltage v_{main} is sensed and scaled down by a differential amplifier circuit. The sensed signal is expressed as v_{main_s}. Secondly, the DC component of v_{main_s} is blocked by a DC blocking circuit, resulting in an AC reference v_{ref}, which is proportional to the ripple component of the PFC output voltage, v_{main}. Thirdly, the AC component of v_{main} is rebuilt at the output of the bipolar compensation stage, v_{comp}, by forcing the scaled compensation output voltage v_{comp_s} to track the ripple reference, v_{ref}. This is achieved by the conventional PI control in the ripple tracking block. Considering that all of the control circuits in prototype are single-ended powered, a DC bias of the same value is applied to both the voltage reference v_{ref}, and the sensed compensation voltage v_{comp_s}, by level shifters, resulting in a practical positive reference voltage v_{ref_lev} and a positive scaled compensation voltage v_{comp_lev}. This avoids the negative portion of the sensed voltage reference in the circuit. As a result, the bipolar compensation output voltage v_{comp} becomes AC voltage which can fully compensate the double line frequency voltage ripple from v_{main}.

C. LED current regulation

The LED current is regulated and the power factor correction is implemented by the PFC control loop, as shown in Figure 7. The compensation control loop and the PFC control loop operate separately. It is noted that the low frequency voltage ripple, V_{ripple}, is determined by the PFC loop, according to (5).

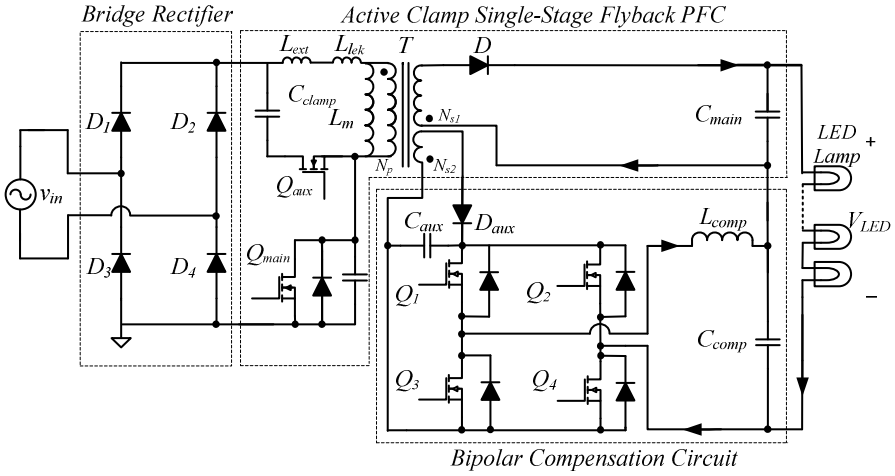


Figure 5 Proposed electrolytic-capacitor-less LED driver architecture.

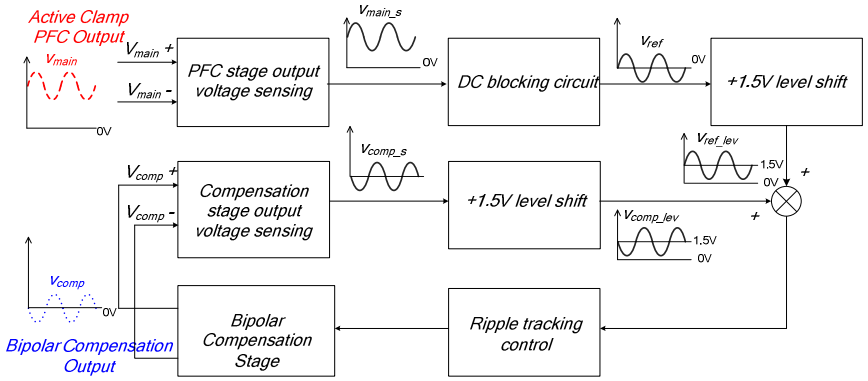


Figure 6 Operation of bipolar compensaiton stage.

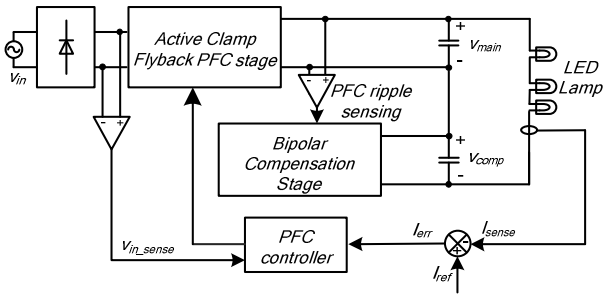


Figure 7 Output current regulation.

III. STEP BY STEP DESIGN PROCEDURE

A. Selection of voltage rating of the compensation stage input capacitor C_{aux}

The compensation stage requires a relatively high input capacitance C_{aux} (over one hundred μF) to buffer the input voltage ripple from the PFC stage transformer winding.

Multi-layer ceramic capacitor is a good choice for the compensation stage input capacitor due to its small size and low cost as compared to film capacitor [23, 24]. However, high-capacitance ceramic capacitors (>10μF) become expensive or even unavailable when the required DC voltage rating is over 50V. Therefore, the design limitation of 50V C_{aux} voltage rating is used in the practical design. The compensation stage switch ratings and the allowable PFC voltage ripple can be decided accordingly.

B. Selection of the compensation stage MOSFETs

The voltage stress of the full bridge switches is the voltage across C_{aux} and is therefore less than 50V, as discussed above. In order to reduce losses, MOSFETs with a low drain-to-source voltage V_{ds}, low $R_{ds(on)}$ and low total gate charge, Q_g, are preferred. In the experimental prototype, MOSFETs with voltage rating of 30V are used. The parameters values and rating of the inductor, L_{comp} and capacitor, C_{comp}, are selected as 47μH and 4.7μF 50V.

C. Selection of PFC stage output capacitance

The following three points must be taken into consideration when selecting the optimal PFC output capacitance:

- The peak voltage of the double line frequency ripple should be limited to be less than the average output voltage of the LED load to ensure a high power factor for the PFC stage, as per (6):

$$\frac{1}{2}V_{ripple} \le V_{LED} \qquad (6)$$

- Although the double line frequency component is removed from the LED output current by the bipolar compensation stage, a high switching-frequency component is introduced. A higher PFC output capacitance helps to dampen this high frequency component.
- Minimizing the PFC output capacitance and limiting the double line frequency voltage ripple is a trade-off, which affects the maximum voltage stress on the PFC output capacitor as expressed in (7) and the voltage stress on the switches in the compensation stages which is discussed in IV.

$$V_{main,\max} = V_{LED} + \frac{1}{2}V_{ripple} \qquad (7)$$

With these factors in mind, the LED driver experimental prototype has been designed to meet the following the specifications as shown in Table 1.

Table 1 Specifications of LED driver

V_{in}	V_{LED}	I_{LED}	P_O	f_{line}
85~265 Vac	≈150 Vdc	700 mA	100 W	60 Hz

With the specified LED current, the amplitude of 120Hz ripple of PFC voltage depends on the output capacitance value, according to (5). It increases dramatically when the output capacitance is less than 100uF as shown in Figure 8:

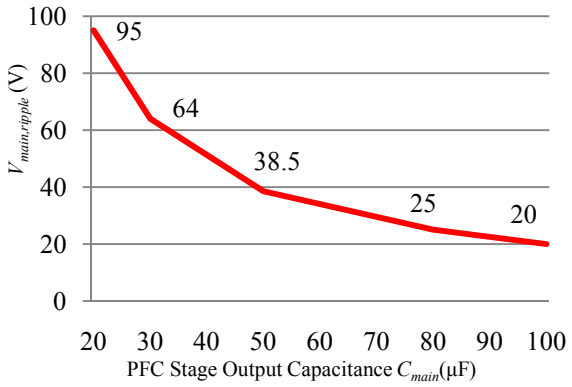


Figure 8 PFC output capacitance vs. PFC output pk-pk ripple

The peak to peak ripple voltage goes to 40V (the peak value is 20V) when the output capacitance is set as 44μF. In the experimental prototype, two 22 μF parallel film capacitors are selected so that the peak voltage of PFC output capacitor is under 200V (150V + 20V = 170V to be exact).

D. Design of active- clamp Flyback PFC stage using conventional methods

In order to enhance the system efficiency of the proposed LED driver, active clamp technology is applied to the PFC stage.

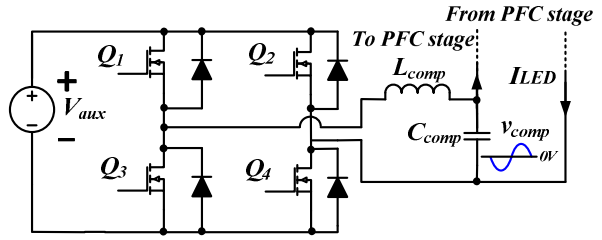
The parameters values are designed based on the selected output capacitor as well as the specifications in

Table 1. The steps should follow the conventional design rules of active-clamp Flyback with PFC mechanism[19].

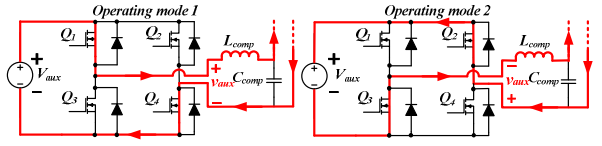
In the experimental prototype, the transformer in Flyback PFC stage is carefully designed with a magnetizing inductance of 1300μH and a leakage inductance of 33uH. This big magnetizing inductance keeps the PFC stage working in current continuous mode (CCM) throughout the whole universal ac input. With an external 15μH inductor connected in series with the transformer, soft switching can be ensured for the most part of line frequency cycle, cycling the energy stored in the lump capacitor of the main MOSFET before it is switched on.

IV. ANALYSIS OF PROPOSED BIPOLAR COMPENSATION STAGE

The proposed compensation circuit features a bipolar output (both positive and negative voltages) as shown in Figure 9(a). However, its output current is the LED current and is a DC current. Two modes of the compensation circuit are shown in Figure 9(b).



(a) Stage prototype.



(b) Operation modes.

Figure 9 Operating modes of bipolar compensation circuit.

From a power flow point of view, the proposed compensation stage is different from the traditional single-phase full bridge inverter in that the circuit does not contribute DC power to the LED load. It instead acts as a reservoir to buffer the power difference and completes an exchange of instantaneous power with the load once every half of a line cycle. The power loss of the bipolar compensation stage is offset via an auxiliary winding from the PFC stage, so that the input voltage of the auxiliary stage is always higher than its output voltage and the compensation can be committed normally.

The four MOSFETs Q_1~Q_4 conduct diagonally to provide paths for the output current I_{LED} as shown in Figure 9(b). According to the electrical features of compensation stage topologies, it sees the peak value as half of the double line frequency ripple, shown in (8).

$$V_{comp,\max} \geq \frac{1}{2} V_{ripple} \tag{8}$$

where $V_{comp,max}$ is the switches' voltage stress in the compensation stage.

The bipolar compensation method also yields a higher efficiency, since the compensation stage does not contribute DC power to the LED load. The processed energy is therefore less than the unipolar solution in [16]. With a bipolar ripple compensation stage, the PFC ripple can be much higher thus significantly reducing the output capacitance.

V. EXPERIMENTAL VERIFICATION

A 100W CCM single-stage Flyback LED driver with bipolar compensation stage has been built. The design specifications are shown in Table 1 and the prototype parameters are below in Table 2.

Table 2 Prototype parameters values

Active Clamp Single-stage Flyback PFC Stage	
Output Capacitor (C_{main})	22 μF×2 (250V Film Cap)
Switches (Q_{main} Q_{aux})	SPP11N80C3
Diode (D)	C3D16060
Turns Ratio (N_p:N_{s1}:N_{s2})	6:5:1
Magnetizing Inductance (L_m)	1300 μH
Leakage Inductance (L_{lek})	33 μH
External Leakage Inductor (L_{ext})	15 μH
Active Clamp Capacitor (C_{clamp})	470 nF (400V Film Cap)
Single-stage PFC Controller	NCP1652A
Proposed Bipolar Compensation Stage	
Switching Frequency (f_{sw})	156 KHz
Input Capacitor (C_{aux})	10 μF×12 (50V 1206 Ceramic Cap)
Output Inductor (L_{comp})	47 μH
Output Capacitor (C_{comp})	4.7 μF×1 (50V 1206 Ceramic Cap)
Full-bridge Switches (Q_1~Q_4)	TPN11003NLLQ×4 (30V, 11mΩ)
SPWM Controller	MC33060A
LED lamp Load	
LED Chip Part Number	XMLEZW-02-0000-0B00T527F×27 connected in series
Forward Voltage/pcs (V_f) Typ	6 V
Max Current (I_{max})	2 A
Luminous Flux/pcs @ 700 mA	270 lm

A. Current ripple compensation performance

The key waveform of the proposed LED driver configuration (C_{main}=44 μF) is shown in Figure 10(a) whose reference polarity is the same in Figure 3. It is noticed that the AC voltage generated by the compensation stage (CH2) mitigates the 120Hz PFC ripple (CH1), resulting in a total flat voltage (CH3) and flat LED current (CH4), the current ripple value @ 120Hz is shown in FFT channel (CHM). The 120Hz PFC voltage ripple is 42V pk-pk before compensation. The LED output current ripple @ 120Hz is 6.2mA RMS after compensation. According to (5), when using conventional single-stage LED drivers, such a small ripple voltage can be only achieved when the output capacitance is increased to 4700μF. Figure 10(b)

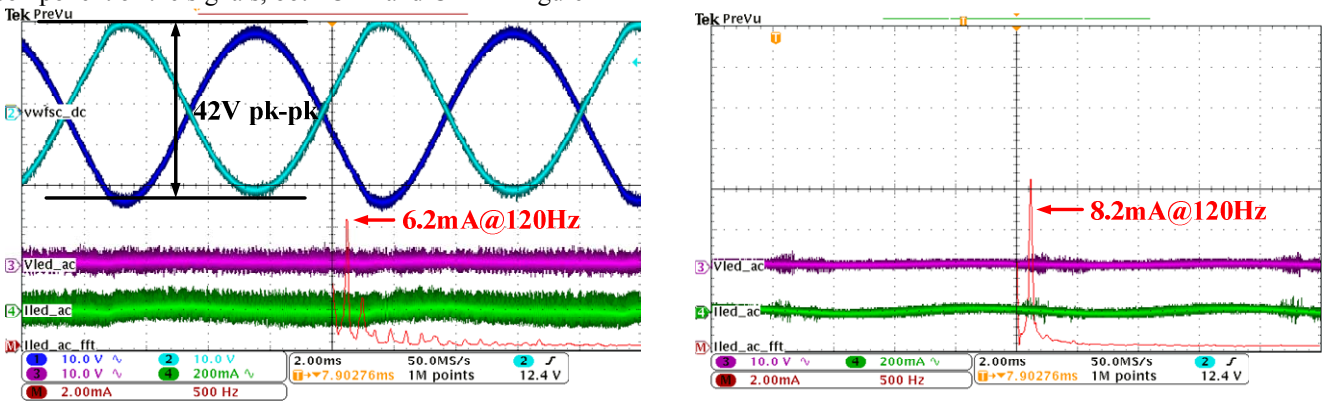
shows the output voltage and LED current of a single-stage LED driver under 4700uF output capacitance with the same power train parameters, the current ripple value is 8.2mA. It is evident that the proposed solution reduces the output capacitance value by 99%!

B. *Light flickering comparsion*

A luminance to voltage conversion device was built to measure the light flickering performance of the proposed method. Figure 11 shows the lighting fluctuation comparison between the LED lamps driven by the proposed LED driver in Figure 11(a) and the conventional single-stage active-clamp Flyback LED driver in Figure 11(b). The proposed LED driver with bipolar compensation shows the superior light flickering reduction ability over the conventional LED driver with 4700 μF output capacitance. In order to highlight the 120Hz component of the signals, both CH1 and CH2 in Figure 11 are AC coupled. As a result, only a small DC component remains in the mathematic channel, as shown in the most left part FFT signal.

C. *Power efficiency and Power Factor performance*

Since the proposed bipolar compensation stage only processes the AC ripple component, the efficiency loss during compensation is minimal. The power efficiency and power factor of the proposed LED driver are shown in Figure 12. The experimental results show that the proposed LED driver has reached 90.6% power efficiency and 0.97 power factor given a universal AC input (110V~220V). The peak efficiency is 92%. The power loss contributed by the compensation is generally very small (<1.5W), as shown in Figure 13. Compared to the major benefit of capacitor value reduction and using film capacitors, the loss is insignificant.

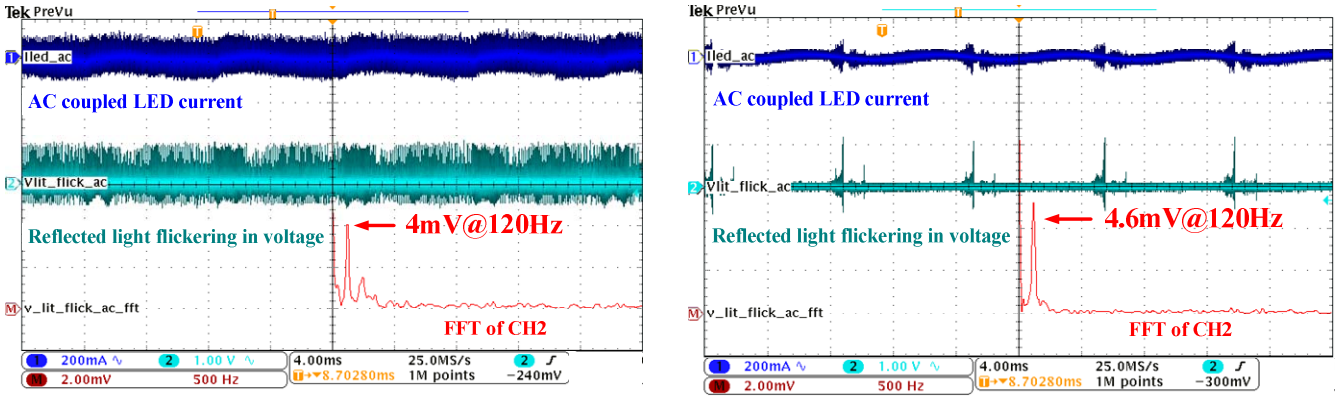


CH1: AC coupled PFC stage output voltage (v_{main}:10V/div) CH2: compensation stage output voltage (v_{comp}:10V/div) CH3: AC coupled LED lamp voltage (V_{LED}:10V/div) CH4: AC coupled LED lamp current (I_{LED}:200mA/div) CHM: FFT of AC coupled LED current (I_{LED_FFT}:2mA/div)

(a) LED driver with proposed bipolar compensation (C_{main}=44μF,C_{aux}=120μF,C_{comp}=4.7μF)

(b) Active-clamp single-stage Flyback LED driver (C_o=4700μF)

Figure 10 Compensation performance of the proposed LED driver, when V_{in}=110 Vac, V_{LED}≈150V, I_{LED}=0.7A, P_o=100W.



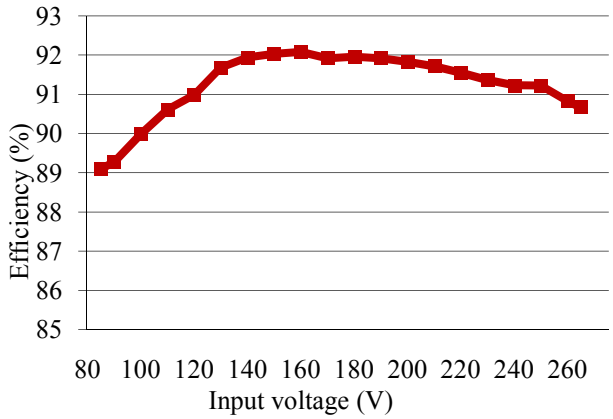
CH1: AC coupled LED current (I_{LED}:200mA/div) CH2: AC coupled reflected light flickering in voltage (v_{lit_flick}:1V/div)

CHM: FFT of reflected light flickering in voltage ($I_{lit\_flick\_FFT}$:2mV/div)

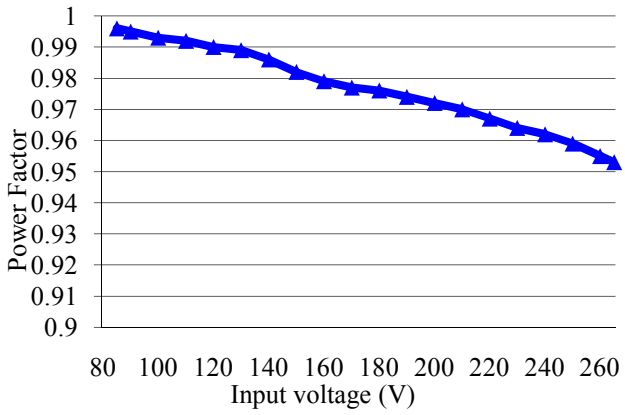
(a) LED driver with proposed bipolar compensation (C_{main}=44μF,C_{aux}=120μF,C_{comp}=4.7μF)

(b) Active-clamp single-stage Flyback LED driver (C_o=4700μF)

Figure 11 Light flickering reduction performance comparison, when V_{in}=110 Vac, V_{LED}≈150V, I_{LED}=0.7A, P_o=100W.



(a) System efficiency.



(b) Power factor.

Figure 12 Performance of proposed LED driver with bipolar compensation, when C_{main}=44μF, V_{LED}≈150V, I_{LED}=0.7A, P_o=100W.

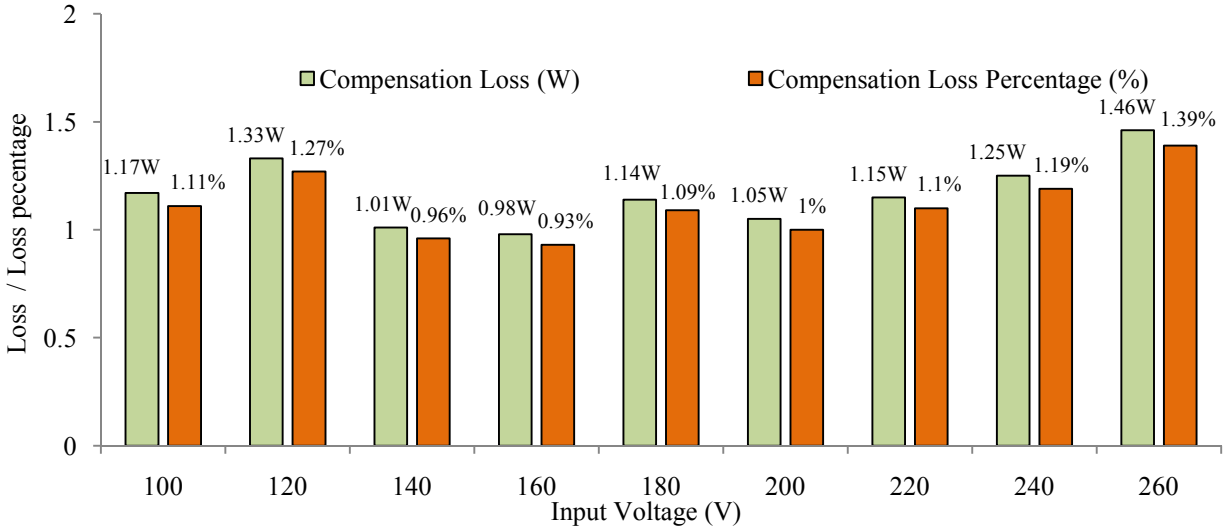


Figure 13 Bipolar compensation stage loss, when C_{main}=44μF, V_{LED}≈150V, I_{LED}=0.7A, P_o=100W.

VI. CONCLUSION

This paper has proposed a high-power LED driver configuration with a bipolar compensation stage. This auxiliary circuit neither impacts the DC output current nor degrades the power factor, compensating only the AC ripple at the PFC output. As a result, the required output capacitor value is significantly reduced and the electrolytic capacitors can be replaced by long-life film capacitors. A 100W (150V/0.7A) experimental prototype was built. The experimental results demonstrate that, using a 44μF output capacitor, the double line frequency LED ripple current can be as low as 6.2mA RMS in the proposed configuration, which would otherwise require over 4700μF outpt capacitance using conventional single-stage LED drivers.

Compared to the existing configurations, the proposed configuration is able to: 1) significantly reduce the PFC output capacitance 2) achieve high efficiency comparable to the conventional single-stage solutions 3) utilize low-voltage-rating components in the compensation stage, thus providing an improved solution for high-power LED drivers.

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