An Interleaved LLC Resonant Converter Operating at Constant Switching Frequency

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***Abstract*—The interleaving technique is necessary for LLC resonant converters to achieve high power level. The advantages include expanded power capacity, lower output ripple current, and higher light-load efficiency by using phase shedding. However, conventional frequency-controlled LLC converters will lose regulation in individual phases if all the phases are operating at the same switching frequency, causing load sharing problem. Existing load sharing solutions for interleaved LLC converters all have limitations. In this paper, a switch-controlled capacitor (SCC) modulated LLC converter (SCC-LLC) is presented to solve the load-sharing problem. With constant switching frequency, interleaving and phase shedding can be achieved. A 600-W, two-phase interleaved constant frequency SCC-LLC prototype is built to verify the feasibility and demonstrate the advantages.**

***Index Terms*—Resonant power conversion, switched-mode power supplies.**

I. Introduction

THE LLC resonant topology is able to achieve high efficiency and is advantageous in front-end dc/dc conversion applications [1]. The related analyses and design methods can be found in [2]–[15]. The development of burst mode and synchronous rectifier can be found in [16]–[18]. The LLC converter has been adopted in many applications such as flat-panel TVs, laptop adapters, and so on. However, it is still absent from high-current applications such as 12-V-output dc/dc power supplies at around 2000 W which can be used in server farms. The major difficulty in this kind of application is the very high-conduction loss caused by the high current on the secondary side. Interleaving technique can be used to solve the high current problem as has been used in voltage regulator applications for CPU. With interleaving technique, the high-RMS current can be split by multiple phases; thus, the conduction loss and component stress will be a fraction of its single-phase counterpart. It also has advantages such as current ripple cancelation and phase shedding, which can shut down unneeded phases to improve light-load efficiency. However, implementing interleaved LLC converters is difficult due the following reasons.

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Interleaving requires all the LLC stages operate at the same switching frequency for current ripple cancelation. However, due to component tolerance among different phases, the voltage gain of each LLC phase will be different at the same switching frequency, and therefore the output current among different LLC stages will be different. [19] demonstrated that with $\pm 10\%$ tolerance for the resonant capacitors only, one phase may supply all the output current while another phase may not output any current at all.

Previous studies on interleaved LLC converters all had limitations. The topologies in [20], [21] are multiphase LLC converters but are not interleaved. The studies in [22]–[25] are interleaved LLC converters but did not consider the load sharing problem caused by the component tolerances. The load sharing method in [26] requires an additional power stage to regulate the output voltage and it cannot work for more than two interleaved phases. The structure in [27] divides down the input voltage by the number of phases, therefore cannot increase the load capacity, and it also has difficulties with phase shedding. The topology proposed in [19] also has difficulties to realize phase shedding.

In this paper, an improved switch-controlled capacitor (SCC) technology is used to control the output voltage by controlling the equivalent resonant capacitance of each LLC stage, and thus modulating the resonant frequency. The switching frequency is constant. As a result, the voltage regulation is achieved in individual LLC phases while the switching frequencies of all phases are the same. This advantage enables a simple interleaving structure and simple load-sharing and phase-shedding implementations. The output power/current capacity can be expanded by paralleling an arbitrary number of phases. Section II describes the improved SCC and the proposed SCC-LLC topology; Section III analyzes the characteristics of the constant switching frequency LLC and provides a design procedure; Section IV analyzes the characteristics of SCC and provides a design procedure as well; Section V gives a design example and simulation results; Section VI demonstrates experimental results of a 600-W prototype; and Section VII concludes the paper.

II. The Improved SCC and the Proposed SCC Modulated LLC Converter

As was discussed in [2]–[4], the gain of an LLC converter is modulated by the ratio of the switching frequency and the resonant frequency. Therefore, when switching frequency is constant, resonant frequency can be changed to modulate the gain. This can be achieved by using SCC to modulate the resonant

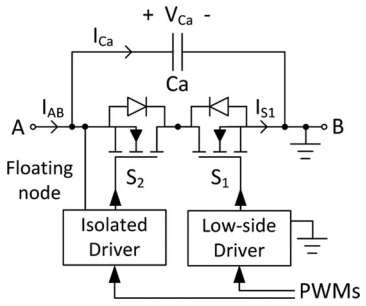

Fig. 1. Structure of SCC.

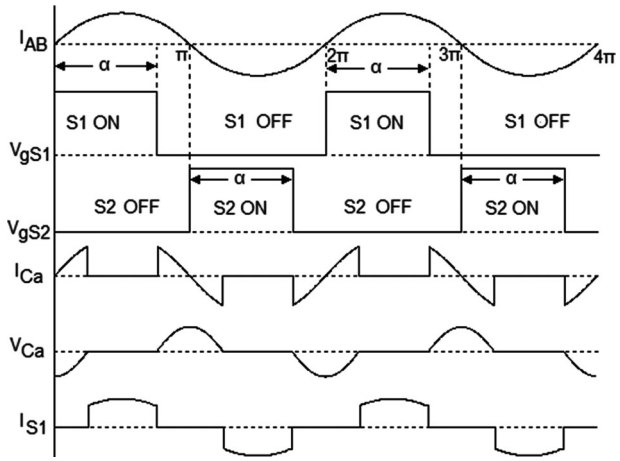

Fig. 2. Waveforms of SCC.

capacitance. In an interleaved SCC-controlled LLC converter (SCC-LLC), the SCC can modulate the gain of individual LLC stages to achieve voltage regulation and load sharing, and the switching frequencies are the same and constant to achieve interleaving operation. As an alternative, variable inductor can be used to control the resonant frequency [28], [29]. However, it requires a dc current source to saturate the inductor; thus, it is less efficient. The proposed SCC-LLC is described as follows.

A. The Improved SCC

The SCC technology was first proposed in [30]. It has been used in various types of resonant topologies to obtain constant frequency operation. In [31], it is used in a Class-E resonant converter; in [32]–[34], it is used in Class-D resonant converters; in [35], it is used in series resonant and LCC resonant converters; in [36], it is used in a Class-D inverter, and in [37], it is used in a charge-pump type electronic ballast.

The original SCC in [30] has the source nodes of both MOSFETs connected to a floating node in the middle; therefore, both MOSFETs require isolated driving. In this paper, one of the MOSFETs can have the source connected to ground; therefore, the driving is simpler, as shown in Fig. 1. The improved SCC consists of two drain-to-drain connected MOSFETs S_1 and S_2, and a parallel capacitor C_a. The electric charge of C_a can be controlled by S_1 and S_2; therefore, the equivalent capacitance can be modulated. The operation waveforms are in Fig. 2 and are described as follows.

When a sinusoidal current I_{AB} is applied to an SCC, the current zero-crossing points are at angle *0,* π*,* 2π, ...etc. For a positive half-cycle where the current flows from A to B, S_2 is turned ON to prevent body diode from carrying current; the gating signal of S_1 is synchronized at $2n\pi$ $(n \in N)$, and it turns OFF S_1 at angle $2n\pi + \alpha$, where $\pi/2 < \alpha < \pi$. The current then flows from A to B via C_a and charges C_a until the angle $(2n + 1)\,\pi$. At the angle $(2n + 1)\,\pi$, the current reverses the direction, and begins to discharge C_a. After C_a is fully discharged, the negative current flows from B to A via S_1's body diode. At the next sync point $(2n + 2)\,\pi$, S_1 is turned ON, and then is turned OFF again at angle $(2n + 2)\,\pi + \alpha$. S_2 controls the negative half-cycle and has the same procedure, except the sync point is at $(2n + 1)\,\pi$. Because the source node has higher potential than the drain node at turn-on points which causes the body diode to clamp the drain-to-source voltage at -0.6 V, and also because the C_a voltage is always zero at turn-off points, S_1 and S_2 are switched both ON and OFF at ZVS conditions. The voltage amplitude of C_a can be designed to be very low, thus, low voltage-rating MOSFETs can be used, whose on-resistance is usually also low; thus, the power loss in the SCC is at minimum.

The equivalent capacitance of an SCC $C_{\rm SC}$ is modulated by the turn-off angle α, given in (1) [30]

$$C_{\rm SC} = \frac{C_a}{2 - (2\alpha - \sin 2\alpha)/\pi}. \tag{1}$$

B. The Proposed SCC Modulated LLC Converter

The proposed SCC-LLC topology is shown in Fig. 3. An SCC is connected in series with the resonant tank in order to modulate the equivalent resonant capacitance C_r, and thus to control the resonant frequency. The resonant frequency in turn controls the voltage gain. The control variable of SCC-LLC is the turn-off delay angle α instead of the switching frequency. Therefore, two or more SCC-LLC converters can be connected in parallel and operate at interleaving mode. The current sharing among each SCC-LLC phase can be achieved by modulating the angle α in each phase which controls the equivalent resonant frequency. For example, if the current in one phase is lower than that of other phases, its control angle α should be decreased to increase its voltage gain, and, therefore, it can provide more current, and current sharing can be achieved.

The design of the proposed SCC-LLC consists of two parts: (a) design of constant switching frequency LLC converters; and (b) design of an SCC. The first part determines inductance values and the required resonant frequency range; the second part determines the capacitors' values according to the required resonant frequency range. They are discussed in the following sections.

III. Analysis and Design Procedure of Constant Switching Frequency LLC Converters

This section analyzes the characteristics of constant switching frequency LLC converters. A design procedure follows.

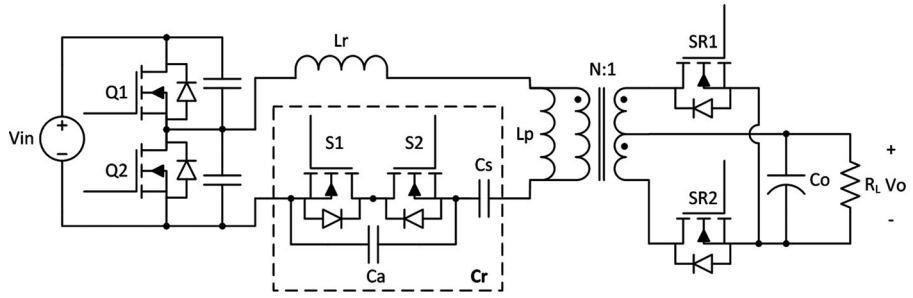

Fig. 3. Topology of the proposed SCC-LLC.

A. Analysis of Constant Switching Frequency LLC Converter

When analyzing the voltage gain of SCC-LLC converter operating at constant switching frequency, the series capacitance C_s and the SCC are considered together as one equivalent resonant capacitance C_r, as shown in Fig. 3. Similar to conventional LLC converters, the gain expression of SCC-LLC converters can be derived using Fundamental Harmonic Approximation (FHA) method. However, since the resonant frequency is variable and the switching frequency is constant, the resonant frequency is normalized at the switching frequency. This is different from conventional LLC analyses. The resultant gain expression is shown in (2)

$$M(\omega_n) = \frac{1}{\sqrt{\left(\frac{\omega_n^2-1}{K}-1\right)^2 + \frac{\pi^4\omega_s^2 L_p^2}{64N^4R_L^2}\left(\frac{\omega_n^2-1}{K}\right)^2}} = \frac{1}{\sqrt{\left(\frac{\omega_n^2-1}{K}-1\right)^2 + Q^2\left(\frac{\omega_n^2-1}{K}\right)^2}} \tag{2}$$

$$N = \frac{N_p}{N_s},\ M = \frac{NV_o}{V_{\text{in}}/2},\ \omega_n = \frac{\omega_r}{\omega_s},\ K = \frac{L_p}{L_r}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}},\ \omega_s = 2\pi f_s \tag{3}$$

where N is the transformer turns ratio, M is the voltage gain of the resonant tank of a half-bridge LLC converter, ω_n is the resonant frequency normalized at the switching frequency, L_p is the parallel inductance, K is the ratio of the parallel inductance and the series resonant inductance, and R_L is the load resistance. Above definitions are listed in (3) for easy reference. Q factor is defined in (4), where R_{ac} is the load resistance reflected to the primary side

$$Q = \frac{L_p\omega_s}{R_{\text{ac}}} = \frac{\pi^2 L_p\omega_s}{8N^2R_L}, R_{\text{ac}} = \frac{8N^2R_L}{\pi^2}. \tag{4}$$

By introducing an intermediate variable X, defined in (5), (2) can be rewritten in (6)

$$X = \frac{\omega_n^2 - 1}{K} \tag{5}$$

$$M(X) = \frac{1}{\sqrt{(X-1)^2 + Q^2X^2}} = \frac{1}{\sqrt{(1+Q^2)X^2 - 2X + 1}}. \tag{6}$$

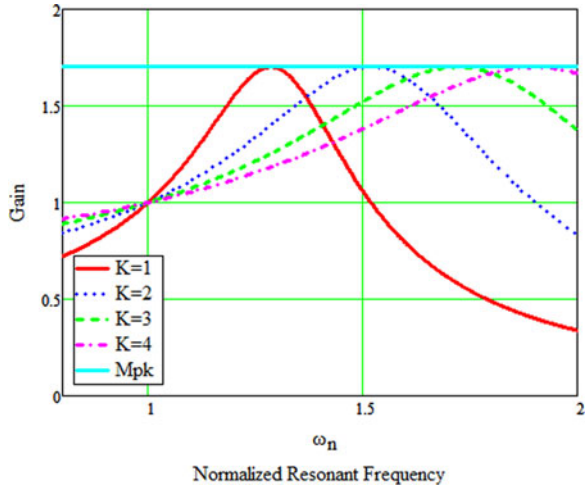

Fig. 4. Gain plot of constant switching frequency LLC, obtained by varying K.

The denominator of (6) includes a parabolic function; therefore, the peak value of M, M_{pk} (peak voltage gain), has a closed-form solution, as expressed in (7)

$$M_{\text{pk}} = \sqrt{\frac{1}{Q^2} + 1} \text{ at } X = \frac{1}{1+Q^2}. \tag{7}$$

Equation (7) reveals that the peak gain of the SCC-LLC is determined by Q and is independent from K. Recall (4), because the switching frequency ω_s, the transformer turns ratio N, and the load resistance R_L are known design parameters, Q is only a function of L_p. Therefore, the peak gain M_{pk} is solely determined by the parallel inductance L_p. This property is different from conventional frequency-controlled LLC converters.

Equation (8) is derived from (5) and (7). It reveals that K only affects the resonant frequency at which the peak gain occurs

$$\omega_{n\text{PK}} = \sqrt{K + 1 - \frac{K}{M_{\text{pk}}^2}} \tag{8}$$

where $\omega_{n\text{PK}}$ is the normalized resonant frequency at which the peak gain occurs.

The above properties of constant switching frequency LLC converters can be illustrated by the gain plots drawn using (2), shown in Fig. 4 and Fig. 5. In Fig. 4, Q is fixed, and varying K only changes the slope of the gain curves, whereas the peak gain amplitude remains the same. Fig. 5 illustrates that when K

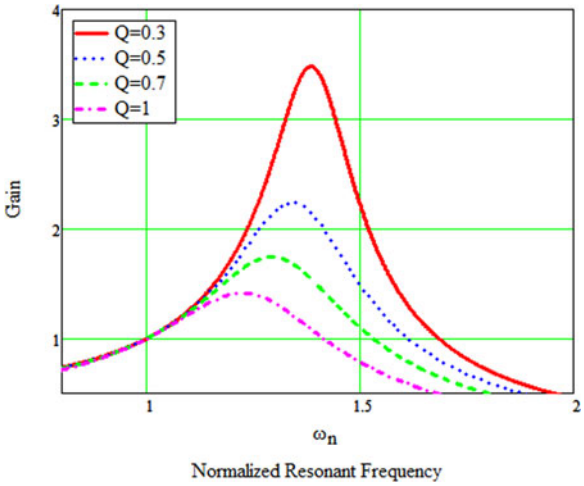

Fig. 5. Gain plot of constant switching frequency LLC, obtained by varying Q.

is fixed, the peak gain increases as Q decreases. According to (4), the decrement of Q can be contributed by either a smaller parallel inductance or a larger load resistance.

Since the input/output voltages and the full-load resistance are known design parameters, the parallel inductance L_p should be determined by the peak gain requirement, using (9), which is derived from (4) and (7)

$$L_p = \frac{8N^2 R_{L,\mathrm{FL}}}{\pi^2 \omega_s \sqrt{M_{\mathrm{pk}}^2 - 1}}. \tag{9}$$

where $R_{L,\mathrm{FL}}$ is the load resistance at the full load condition.

However, in addition to (9), there is another constraint for the L_p value: the full-load ZVS condition. Different from variable switching frequency LLC converters, the worst-case ZVS condition in constant switching frequency LLC converters occurs at full-load scenario because of the following reasons. The ZVS condition is associated with the L_p current at switching points. At full load, the resonant frequency is the highest; thus, the resonance time, during which energy transfers from the primary to the secondary side, and also the L_p current builds up linearly, is the shortest. After the resonance time, the L_p current will remain approximately unchanged, or even slightly decrease in the worst case. At lighter load, the resonant frequency is lower, thus the resonance time is longer, resulting in higher L_p current at switching points. Therefore, the smallest L_p current at switching points happens at full- load scenario, which is the worst case for ZVS. If ZVS can be achieved at full load, ZVS in lighter load conditions is guaranteed.

The derivation for the full-load ZVS constraint is as follows.

Let I_{ZVS} be the L_p current at the switching point and ω_{FL} be the resonant frequency at full load. Assuming the L_p current builds up from $-I_{\mathrm{ZVS}}$ to I_{ZVS} linearly during the resonance time π/ω_{FL}, and remains approximately unchanged until the switching point, the following equation can be derived:

$$I_{\mathrm{ZVS}} = \frac{NV_o\pi}{2L_p\omega_{\mathrm{FL}}}. \tag{10}$$

I_{ZVS} must be sufficient to discharge the MOSFET junction capacitance C_j within the dead time t_d; thus

$$I_{\mathrm{ZVS}} \geq \frac{2V_{\mathrm{in}}C_j}{t_d}. \tag{11}$$

Combine (10) and (11) and get

$$L_p \leq \frac{t_d\pi NV_o}{4\omega_{\mathrm{FL}}V_{\mathrm{in}}C_j}. \tag{12}$$

Equation (12) defines the required L_p for the full-load ZVS condition.

Therefore, according to above analysis, the L_p value must meet both constrains set by (9) and (12). Usually the peak gain requirement is more restrictive, but for applications that only require a low peak gain, the full-load ZVS condition can be a more restrictive constraint. The designer must calculate L_p for both constraints, and select the smaller value.

The ω_{FL} in (12) can be derived as follows.

Recall (6), with a given gain M, the X can be solved as

$$X = \frac{1 \pm \sqrt{\frac{1+Q^2}{M^2} - Q^2}}{1+Q^2}. \tag{13}$$

Then, the expression of ω_n can be derived from (13) and (5)

$$\omega_n = \sqrt{KX+1} = \sqrt{\frac{K \pm K\sqrt{\frac{1+Q^2}{M^2} - Q^2}}{1+Q^2} + 1}. \tag{14}$$

As shown in (14), the ω_n has two roots for a given gain M, which is also shown in Fig. 5, where two resonant frequencies can yield the same gain: one is in ZVS region; the other is in ZCS region. The smaller root is chosen because it is in the ZVS region. Equation (14) is a general equation to calculate the normalized resonant frequency according to given conditions M and Q. Thus, the normalized resonant frequency at full load $\omega_{n\mathrm{FL}}$ can be calculated by (15), where Q_{FL} is the Q calculated in (4) using the full-load load resistance $R_{L,\mathrm{FL}}$

Then, the ω_{FL} in (12) can be obtained by unnormalizing the $\omega_{n\mathrm{FL}}$ value calculated in (15).

The K value in (15) can be selected based on the following considerations:

1) From Fig. 4, it is observed that, the smaller the K, the steeper the gain slope; thus, the less the resonant frequency deviates from the switching frequency. Usually this is preferred in conventional LLC design. However, in constant switching frequency LLC converters, a smaller K does not result in lower primary RMS current. This is because the switching period is fixed; thus, the L_p current does not notably vary with the selection of *K*. Nevertheless, the secondary RMS current will be higher at larger K value. Therefore, from the RMS current point of view, it is still advantageous to use the smallest possible K value.
2) Since L_p is determined beforehand by the peak gain and ZVS requirements, a small K means a large L_r. If magnetic integration is desired, the designer must consider whether the large L_r can be implemented using the transformer's leakage inductance. In many situations, large leakage inductance can be only achieved with large air

gap, which causes excessive loss due to fringing effect. Therefore, a larger K is desired from magnetic design point of view.

3) As discussed above, a small K means a large L_r, which in turn means a small C_r. A resonant tank with a small C_r has high quality factor thus high voltage stress thereof. Since SCC bears a portion of the total C_r voltage stress, the SCC MOSFETs must have higher voltage rating; whereas high-voltage rating MOSFETs usually have higher Rds(on) which in turn increase the conduction loss. Therefore, a reasonably large K value is sometime better than the minimum K value in improving the overall efficiency.

With above considerations in mind, different K values can be tested in (16) to estimate the peak resonant capacitor voltage. The worst case is usually $V_{\rm in} = V_{\rm in.min}$, $\omega_n = \omega_{n\rm PK}$, but may also be $V_{\rm in} = V_{\rm in.nom}$, $\omega_n = \omega_{n\rm FL}$

$$v_{Cr,\max} = \left[\frac{V_o\pi}{R_L N\omega_s} + \frac{NV_o}{2L_p}\cdot\frac{\pi}{\omega_n\omega_s}\left(\frac{\pi}{\omega_s} - \frac{3\pi}{4\,\omega_n\omega_s}\right)\right] \cdot \frac{(\omega_n\omega_s)^2 L_p}{2K} + \frac{V_{\rm in}}{2}. \tag{16}$$

In summary, the K value should be determined by magnetic design, resonant capacitor voltage stress, and $R_{\rm ds(on)}$ of the available MOSFET devices. Simulation or other numerical methods are suggested as FHA analysis is not accurate in calculating above parameters near peak gain point, which defines the worst-case stress. It is found that $K = 5\sim7$ is a reasonable tradeoff. Smaller K values can slightly reduce the secondary RMS current but significantly increase resonant capacitor voltage. The detailed discussion is provided in Section V.

After K is selected, (15) can be used to determine $\omega_{\rm FL}$, then (12) can be used to determine L_p for the full-load ZVS requirement. The resultant L_p value is compared with that from (9), and the smaller value is the selected L_p value.

B. Design Procedure of Constant Switching Frequency LLC Converter

In light of the analysis discussed earlier, the design procedure of constant switching frequency LLC converter is summarized as follows:

1) Determine the switching frequency ω_s and the transformer turns ratio, N. The turns ratio is selected such that the required gain of the LLC resonant tank is slightly above unity during normal operation. The nominal gain required for the nominal input voltage is calculated in (17), where η is the estimated efficiency, the factor 2 is due to half-bridge configuration

$$M_{\rm nom} = \frac{NV_o}{\eta V_{\rm in,nom}/2}. \tag{17}$$

The peak gain required for the minimum input voltage scenario is calculated in (18).

$$M_{\rm pk} = \frac{NV_o}{\eta V_{\rm in,min}/2}. \tag{18}$$

2) Use (9) to calculate L_p according to the peak gain constraint.
3) Choose a K, use (8) and (15) to calculate $\omega_{n\rm PK}$ and $\omega_{n\rm FL}$, respectively.
4) Plug the K value selected in Step 3 into (15) to calculate $\omega_{n\rm FL}$, then un-normalize it to $\omega_{\rm FL}$, and then use (12) to calculate L_p according to the full-load ZVS constraint. Compare the resultant L_p value to that obtained in Step 2, and select the smaller one as the L_p value.
5) If the selected L_p is computed from (12), repeat Step 3 and Step 4 to find a proper K.
6) Use L_p and K to calculate L_r.
7) Use (16), plug in two sets of values, $V_{\rm in} = V_{\rm in.nom}$, $\omega_n = \omega_{n\rm FL}$ and $V_{\rm in} = V_{\rm in.min}$, $\omega_n = \omega_{n\rm PK}$, respectively, to calculate the peak capacitor voltage. If the capacitor voltage stress is not satisfactory, try a different K values in Step 3 and iterate Steps 4—7.

It is noted that the equations derived from FHA are less accurate when the resonant frequency is further deviated from the switching frequency. This is because FHA assumes sinusoidal current, which is not true when the resonant frequency deviates too much from the switching frequency. As a result, the L_p calculated from (9) tends to provide a higher peak gain than calculated, hence in reality, the resonant frequency at the required peak gain point will be lower than that calculated in (8), and therefore the component stress will be lower than that given by (16). This inaccuracy results in a tendency of over-design, but nevertheless provides some useful margins for component tolerances. In order to find out the capacitor voltage stress more accurately, simulation approach is recommended in Step 7.

$$\omega_{n\rm FL} = \sqrt{\frac{K - K\sqrt{\frac{1+Q_{\rm FL}^2}{M_{\rm nom}^2} - Q_{\rm FL}^2}}{1+Q_{\rm FL}^2} + 1}. \tag{15}$$

IV. Analysis and Design Procedure of Switch-controlled Capacitor in Constant Frequency LLC Converters

A. Analysis of Switch-controlled Capacitor

As shown in Fig. 3, the SCC is connected in series with a series capacitor C_s in order to modulate the equivalent resonant capacitance C_r. The SCC equivalent capacitance $C_{\rm SC}$ is given in (1). The total equivalent resonant capacitance C_r is derived in

$$C_r = \frac{C_{\rm SC}C_s}{C_{\rm SC}+C_s} = \frac{\pi C_a C_s}{\pi C_a + 2\pi C_s - 2\alpha C_s + C_s\sin(2\alpha)} \tag{19}$$

where α is turn-off delay angle and $\frac{\pi}{2} \le \alpha \le \pi$.

Substitute (19) and the definition of ω_n in (3) into (2), and the SCC-LLC's gain expression as a function of the control angle α is derived in (20), as shown at the bottom of the next page.

In order to determine the values of C_s and C_a, the required minimum and maximum C_r must be determined first. The minimum C_r is determined by the resonant frequency at which the

peak gain is achieved

$$C_{r,\min} = \frac{1}{\left(\omega_s \omega_{n\mathrm{PK}}\right)^2 L_r}. \tag{21}$$

The maximum C_r is determined by the lowest resonant frequency, which is at light load and just before burst mode is triggered. Generally speaking, the SCC-LLC enters into burst mode when load current is less than a threshold level. The triggering level is determined by the designers, which is normally 5%–15% of the full load. Once the triggering level is defined, the minimum resonant frequency is derived from (14) and written in (22)

$$\omega_{n,\min} = \sqrt{\frac{K - K\sqrt{\frac{1+Q_{\mathrm{burst}}^2}{M_{\mathrm{nom}}^2} - Q_{\mathrm{burst}}^2}}{1+Q_{\mathrm{burst}}^2} + 1} \tag{22}$$

where $Q_{\mathrm{burst}} = \frac{\pi^2 L_p \omega_s}{8N^2 R_{L,\mathrm{burst}}}$.

Then, the maximum C_r can be calculated in (23)

$$C_{r,\max} = \frac{1}{\left(\omega_s \omega_{n,\min}\right)^2 L_r}. \tag{23}$$

The maximum and the minimum control angle of the SCC also need to be determined in order to solve for the values of C_s and C_a. Ideally, the angle α is from 0.5π to π. Then, the values of C_s and C_a can be calculated using (24) and (25), derived from (19)

$$C_s = C_{r,\max} \tag{24}$$

$$C_a = \frac{C_s C_{r,\min}}{C_s - C_{r,\min}}. \tag{25}$$

However, in order to ensure reliable operation of the driving scheme, it is suggested to make $\alpha_{\max}$ slightly below π and $\alpha_{\min}$ slightly above $0.5\,\pi$. As was discussed earlier, the design procedure of constant switching frequency LLC based on FHA tends to provide an over design of the peak gain, which automatically leaves some margin for $\alpha_{\min}$. Therefore, $\alpha_{\min} = 0.5\,\pi$ can be considered has margin already, and only $\alpha_{\max}$ needs additional margin from the theoretical maximum value π.

A plot of the control angle α versus the equivalent resonant capacitance C_r is drawn using (19), shown in Fig. 6, in which the C_r curve becomes flat when α is beyond $0.9\,\pi$. This characteristic is true for most reasonably designed C_s and C_a values. Hence, because the flat C_r curve indicates a reduction of the loop gain, it is suggested to place $\alpha_{\max}$ below 0.9π in order to ensure the dynamic performance.

Then the values of C_s and C_a can be solved by substituting two sets of values, $C_{r,\max}$, $\alpha_{\max}$ and $C_{r,\min}$, $\alpha_{\min}$, into (19),

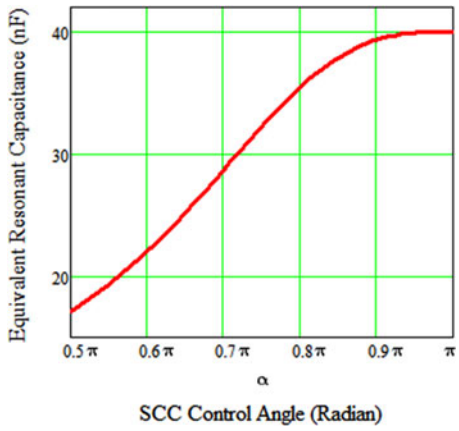

Fig. 6. SCC Control Angle versus Equivalent Resonant Capacitance.

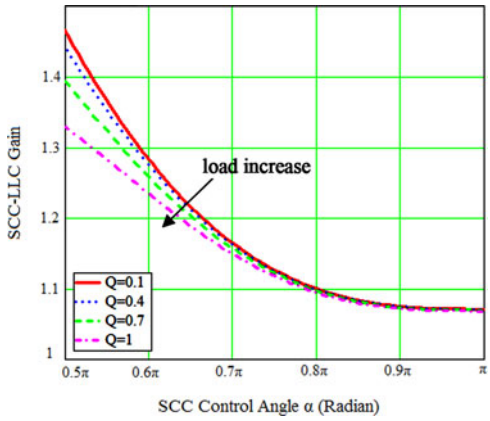

Fig. 7. SCC Control Angle versus SCC-LLC Gain.

respectively, derived in (26) and (27)

$$C_a = \frac{\begin{array}{c}[\sin(2\alpha_{\min}) - \sin(2\alpha_{\max}) \\ +2\alpha_{\max} - 2\alpha_{\min}]C_{r,\min}C_{r,\max}\end{array}}{(C_{r,\max} - C_{r,\min})\pi}. \tag{26}$$

$$C_s = \frac{\begin{array}{c}[\sin(2\alpha_{\min}) - \sin(2\alpha_{\max}) \\ +2\alpha_{\max} - 2\alpha_{\min}]C_{r,\min}C_{r,\max}\end{array}}{\begin{array}{c}[2\alpha_{\max} - \sin(2\alpha_{\max}) - 2\pi]C_{r,\max} \\ +[\sin(2\alpha_{\min}) - 2\alpha_{\min} + 2\pi]C_{r,\min}\end{array}}. \tag{27}$$

Finally, an example of the SCC control angle versus the SCC-LLC gain is plotted using (20), shown in Fig. 7. The adopted parameter values are: $C_s = 36$ nF, $C_a = 30$ nF, $L_r = 12\ \mu$H, $K = 7$, and $f_s = 200$ kHz. The change in Q reflects the change in load.

It is desired to limit the peak SCC voltage below 100 V as MOSFETs rated below 100 V exhibit significantly lower $\mathrm{R_{ds(on)}}$ than those above 100 V. The peak C_a voltage is estimated as follows.

$$M(\alpha) = \frac{K}{\sqrt{\left(\frac{\pi C_a + 2\pi C_s - 2\alpha C_s + C_s \sin(2\alpha)}{\omega_s^2 L_r \pi C_a C_s} - K - 1\right)^2 + Q^2\left(\frac{\pi C_a + 2\pi C_s - 2\alpha C_s + C_s \sin(2\alpha)}{\omega_s^2 L_r \pi C_a C_s} - 1\right)^2}} \tag{20}$$

TABLE I
DESIGN SPECIFICATION

Input voltage	400*V* nominal / 300*V* minimum
Output voltage	12*V*
Output power	Maximum load: 300*W* (I_o = 25*A*) Minimum load: 30*W* (I_o = 2.5*A*)
Switching frequency	200 *kHz* (constant)
MOSFET junction capacitance	0.5 nF
Dead time	200 ns

The maximum C_a voltage occurs at $\alpha = 0.5\ \pi$ in which case C_a is considered always connected in series with C_s. Thus, the voltage on C_a is proportional to the ac portion of the peak resonant capacitor voltage, which is calculated in (16). Therefore, the peak C_a voltage is estimated by (28)

$$v_{Ca,\max} = \frac{C_s}{C_s + C_a}\left(v_{Cr,\max} - \frac{V_{\text{in}}}{2}\right). \tag{28}$$

If the estimated peak C_a voltage is higher than 100 V, then iteration of the LLC design procedure discussed in Section III may be required to lower the total resonant capacitor voltage.

B. Design Procedure of SCC

In light of the analysis discussed earlier, the design procedure of SCC is summarized as follows:

1) use (21), (22) and (23) to determine the objective minimum and maximum C_r;
2) determine the maximum and the minimum control angle α. For example, $\alpha_{\max} = 0.9\pi$, $\alpha_{\min} = 0.5\pi$;
3) use (26) and (27) to solve for C_a and C_s;
4) use (28) to check the peak C_a voltage. If it is not satisfactory, return to Step 3 of the constant switching frequency LLC design procedure discussed in Section III and choose a different K value.

V. DESIGN EXAMPLE AND SIMULATION RESULTS

A. Design Example

The design procedures of constant frequency LLC and SCC are given in Sections III and IV, respectively. In this section, a design example is provided. The design specification for one SCC-LLC phase is shown in Table I.

It is expected that when the output power is below the minimum load, burst mode operation is used to regulate the output voltage down to zero load.

The design steps are as follows:

1) Determine turns ratio, nominal gain and peak gain.
   Assume 0.1 V drop of synchronous rectifiers, N = 400 V/2/12.1 V = 16.5
   Choose $N = 18$ to leave some margin to ensure stable SR operation and for component tolerance.
   Therefore the gain required for nominal input is calculated by (17)

$$M_{\text{nom}} = \frac{NV_o}{V_{\text{in,nom}}/2} = \frac{18 \times 12.1}{200} = 1.09$$

   Assuming 95% efficiency, choose $M_{\text{nom}} = 1.15$.

   The gain required for the lowest input is given by (18)

$$M_{\text{pk}} = \frac{NV_o}{V_{\text{in,min}}/2} = \frac{18 \times 12.1}{150} = 1.452$$

   Assuming 95% efficiency, choose $M_{\text{pk}} = 1.53$.

2) Calculate L_p according to the peak gain constraint using (9)

$$R_{L,\text{FL}} = \frac{V_o^2}{P_o} = \frac{(12\ \text{V})^2}{300\ \text{W}} = 0.48\ \Omega$$

$$L_p = \frac{N^2 R_{L,\text{FL}}}{\omega_s \frac{\pi^2}{8}\sqrt{M_{\text{pk}}^2 - 1}} = \frac{18^2 \times 0.48\ \Omega}{2\pi \times 200\ \text{kHz} \times \frac{\pi^2}{8} \times \sqrt{1.53^2 - 1}} = 86.6\ \mu\text{H} \approx 86\ \mu\text{H}$$

3) Select K, and then use (8) and (15) to calculate $\omega_{n\,\text{PK}}$ and $\omega_{n\,\text{FL}}$
   In this step, K is selected to be 7. Other K values are also used for comparison purposes, as discussed in the following sections:

$$\omega_{n\text{PK}} = \sqrt{K + 1 - \frac{K}{M_{\text{pk}}^2}} = \sqrt{7 + 1 - \frac{7}{1.53^2}} = 2.238$$

$$\omega_{n\text{FL}} = \sqrt{\frac{K - K\sqrt{\frac{1+Q_{\text{FL}}^2}{M_{\text{nom}}^2} - Q_{\text{FL}}^2}}{1 + Q_{\text{FL}}^2} + 1} = \sqrt{\frac{7 - 7 \cdot \sqrt{\frac{1+0.857^2}{1.15^2} - 0.857^2}}{1 + 0.857^2} + 1} = 1.404$$

   where $Q_{\text{FL}} = \frac{\pi^2}{8}\frac{L_p\omega_s}{N^2 R_{L,\text{FL}}} = 0.857$

4) Use (12) to calculate L_p according to the full-load ZVS constraint

$$L_p \le \frac{t_d \pi N V_o}{4\omega_{n\text{FL}}\omega_s V_{\text{in,nom}} C_j} = \frac{200\ \text{ns} \cdot \pi \cdot 18 \cdot 12\ \text{V}}{4 \cdot 1.422 \cdot 2\pi \cdot 200\ \text{kHz} \cdot 400\ \text{V} \cdot 0.5\ \text{nF}} = 95\ \mu\text{H}$$

5) Determine L_p based on both constraints.
   The L_p value of 95 μH given by the ZVS constraint is larger than that of 86 μH given by the peak gain constraint, which means if the smaller value of 86 μH is selected, both ZVS and peak gain constrains will be fulfilled. Therefore $L_p = 86\ \mu$H is chosen. No iteration is needed.
6) Calculate L_r according to (3)

$$L_r = \frac{L_p}{K} = \frac{86\ \mu\text{H}}{7} \approx 12\ \mu\text{H}$$

TABLE II
DESIGN RESULTS COMPARISON

Design Iteration	Case #1		Case #2		Case #3		Case #4	
Design Parameters	L_p=86μH K=2 N=18		L_p=86μH K=5 N=18		L_p=86μH K=7 N=18		L_p=90μH K=7 N=20	
Design Method	Calculated	Simulated	Calculated	Simulated	Calculated	Simulated	Calculated	Simulated
$C_{r,max}$ at 400V/min load	12 nF	13.4 nF	23 nF	28.5 nF	28 nF	36 nF	20 nF	24.5 nF
$C_{r,min}$ at 300V/full load	6 nF	9.4 nF	9 nF	14.9 nF	10 nF	16.5 nF	8 nF	13.3 nF
Designed C_s	13 nF	14 nF	24 nF	29 nF	29 nF	37 nF	21 nF	25 nF
Designed C_a	12 nF	32 nF	15 nF	31 nF	16 nF	31 nF	14 nF	29 nF

TABLE III
COMPONENT STRESS COMPARISON

Design Iteration	Case #1		Case #2		Case #3		Case #4	
Design Parameters	L_p=86μH K=2 N=18		L_p=86μH K=5 N=18		L_p=86μH K=7 N=18		L_p=90μH K=7 N=20	
Input Voltage Condition	400 V	300 V	400 V	300 V	400 V	300 V	400 V	300 V
Primary RMS Current Stress	2.7 A	2.7 A	2.6 A	2.6 A	2.6 A	2.5 A	2.5 A	2.5 A
Secondary RMS Current Stress	30 A	33 A	30 A	35 A	32 A	36 A	33 A	39 A
Total Capacitor Voltage Stress	437 V	482 V	313 V	339 V	292 V	319V	320 V	359 V
C_s Voltage Stress	411 V	381 V	301 V	248 V	282	230V	316 V	263 V
C_a Voltage Stress	26 V	101 V	12 V	91 V	10V	89 V	4V	96 V

TABLE IV
SIMULATION PARAMETERS IN LARGE TOLERANCES CONDITION

Switching frequency	200kHz
Input Voltage	400V
Output Voltage	12V
Output Current	50A × 2
Transformer Turns Ratio	20:1
Parallel Inductance	86μH × 115% (Phase1) 86μH × 85% (Phase2)
Series Inductance	12μH × 115% (Phase1) 12μH × 85% (Phase2)
Series Capacitance	36nF × 108% (Phase1) 36nF × 92% (Phase2)
SCC Capacitance	30nF
Output Capacitance	4mF

7) Use (16) to calculate the peak resonant capacitor voltage. This is the total voltage across C_s and C_a

$$v_{Cr,\max,\mathrm{pk}} = \left[\frac{V_o\pi}{R_{L,\mathrm{FL}}N\omega_s} + \frac{NV_o}{2L_p}\cdot\frac{\pi}{\omega_{n\mathrm{PK}}\omega_s}\left(\frac{\pi}{\omega_s} - \frac{3\pi}{4\omega_{n\mathrm{PK}}\omega_s}\right)\right] \cdot \frac{\left(\omega_{n\mathrm{PK}}\omega_s\right)^2 L_p}{2K} + \frac{V_{\mathrm{in,min}}}{2} = 282\ \mathrm{V_{ac,pk}} + 150\ \mathrm{V}_{dc} = 432\ \mathrm{V}$$

$$v_{Cr,\max,\mathrm{FL}} = \left[\frac{V_o\pi}{R_{L,\mathrm{FL}}N\omega_s} + \frac{NV_o}{2L_p}\cdot\frac{\pi}{\omega_{n\mathrm{FL}}\omega_s}\left(\frac{\pi}{\omega_s} - \frac{3\pi}{4\omega_{n\mathrm{FL}}\omega_s}\right)\right] \cdot \frac{\left(\omega_{n\mathrm{FL}}\omega_s\right)^2 L_p}{2K} + \frac{V_{\mathrm{in,nom}}}{2} = 116\ \mathrm{V_{ac,pk}} + 200\ \mathrm{V}_{dc} = 316\ \mathrm{V}$$

8) Use (21), (22) and (23) to determine the maximum and minimum C_r

$$C_{r,\min} = \frac{1}{\left(\omega_s\omega_{n\mathrm{PK}}\right)^2 L_r} = \frac{1}{\left(2\pi\cdot 200\ \mathrm{kHz}\cdot 2.238\right)^2 12\ \mu\mathrm{H}} \approx 10\ \mathrm{nF}$$

According to the design specification, the SCC-LLC enters burst mode at 30 W load, then

$$\omega_{n,\min} = \sqrt{\frac{K - K\sqrt{\frac{1+Q_{\mathrm{burst}}^2}{M_{\mathrm{nom}}^2} - Q_{\mathrm{burst}}^2}}{1+Q_{\mathrm{burst}}^2} + 1} = \sqrt{\frac{7 - 7\sqrt{\frac{1+0.086^2}{1.15^2} - 0.086^2}}{1+0.086^2} + 1} = 1.383$$

where $Q_{\mathrm{burst}} = \dfrac{\pi^2 L_p\omega_s}{8N^2 R_{L,\mathrm{burst}}} = 0.086$

$$C_{r,\max} = \frac{1}{\left(\omega_s\omega_{n,\min}\right)^2 L_r} = \frac{1}{\left(2\pi\cdot 200\ \mathrm{kHz}\cdot 1.383\right)^2\cdot 12\ \mu\mathrm{H}} \approx 28\ \mathrm{nF}$$

9) Determine the maximum and minimum control angle. Based on the discussion in Section IV, the control angle range is determined below

$$\alpha_{\max} = 0.9\pi$$
$$\alpha_{\min} = 0.5\pi.$$

10) Use (26) and (27) to determine C_a and C_s

$$C_s = \frac{\left[\sin(2\alpha_{\min}) - \sin(2\alpha_{\max}) + 2\alpha_{\max} - 2\alpha_{\min}\right]}{\begin{array}{c}C_{r,\min}C_{r,\max}\\ \hline \left[2\alpha_{\max} - \sin(2\alpha_{\max}) - 2\pi\right]C_{r,\max}\\ +\left[\sin(2\alpha_{\min}) - 2\alpha_{\min} + 2\pi\right]C_{r,\min}\end{array}} = \frac{\left[\sin(2\cdot 0.5\pi) - \sin(2\cdot 0.9\pi) + 2\cdot 0.9\pi - 2\cdot 0.5\pi\right]}{\begin{array}{c}\cdot 10\ \mathrm{nF}\cdot 28\ \mathrm{nF}\\ \hline \left[2\cdot 0.9\pi - \sin(2\cdot 0.9\pi) - 2\pi\right]\cdot 28\ \mathrm{nF}\\ +\left[\sin(2\cdot 0.5\pi) - 2\cdot 0.5\pi + 2\pi\right]\cdot 10\ \mathrm{nF}\end{array}} = 29\ \mathrm{nF}$$

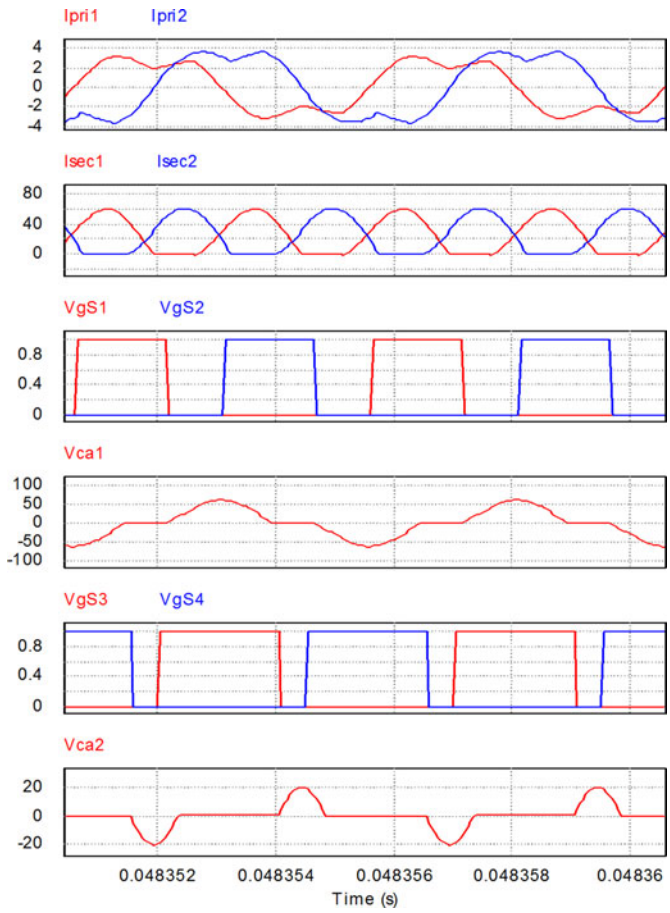

Fig. 8. Simulation results in large tolerances condition.

C_s is the series capacitor, as shown in Fig. 3

$$C_a = \frac{[\sin(2\alpha_{\min}) - \sin(2\alpha_{\max}) + 2\alpha_{\max} - 2\alpha_{\min}]\, C_{r,\min} C_{r,\max}}{(C_{r,\max} - C_{r,\min})\pi}$$

$$= \frac{[\sin(2\cdot 0.5\pi) - \sin(2\cdot 0.9\pi) + 2\cdot 0.9\pi - 2\cdot 0.5\pi] \cdot 10\text{ nF}\cdot 28\text{ nF}}{(28\text{ nF} - 10\text{ nF})\pi}$$

$$= 16\text{ nF}$$

C_a is the SCC capacitor connected in parallel with auxiliary MOSFETs.

11) Use (28) to calculate the SCC voltage stress

$$v_{Ca,\max,\text{pk}} = \frac{C_s}{C_s + C_a}\left(v_{Cr,\max,\text{pk}} - \frac{V_{\text{in,min}}}{2}\right)$$

$$= \frac{29\text{ nF}}{29\text{ nF} + 16\text{ nF}}\left(432\text{ V} - \frac{300\text{ V}}{2}\right)$$

$$\approx 182\text{ V}.$$

The aforementioned result shows the peak voltage across C_a is 182 V, and the SCC MOSFETs should be selected accordingly. However, as was discussed in the last paragraph of Section III, above formulae are derived based on FHA, which has an over-design tendency. The minimum equivalent resonant capacitance in actual circuit can be larger; thus, the C_a value can be larger, and the voltage stress can be lower. Therefore, in order to achieve design optimization, simulation is recommended to substitute Steps 7 and 8. The simulation can be carried out by using one equivalent resonant capacitor; thus, the model is simple to build. The C_s and C_a values can be calculated based on maximum and minimum C_r values obtained from simulation.

If the resultant SCC voltage stress from Step 11 is satisfactory, the design procedure is completed. Otherwise, iteration from Step 3 is needed.

B. Design Comparison and Discussion

The design steps described earlier are performed for different N and K values, and are then verified against simulation results. The calculated results and simulated results are compared in Table II.

From Table II, the following facts are observed:

1) The C_r values obtained from simulation are larger than the calculated values. It means the actual resonant frequency required to achieve a certain gain are lower than the calculated value, which confirms the over-design tendency discussed in Section III.
2) The over design effect significantly affects the C_a value. The C_a values based on simulated C_r values are more than twice of that based on the calculated C_r values, thus the voltage stress of SCC can be in fact much lower than the calculated value. Therefore, for optimal design so as to choose the lowest possible voltage rating MOSFET, simulation tool should be used.

C. Component Stress Study

The current stress and voltage stress of the above design examples are studied using simulation approach. The results are shown in Table III. The discussions on how to trade-off N and K values are further below.

From Table III, the following trade-offs are observed:

1) Comparing Design #3 and Design #4, the secondary-side RMS current and resonant capacitor voltage at $N = 20$ are notably higher than that at $N = 18$; therefore a lower transformer turns ratio is preferred to reduce RMS current and capacitor voltage stress.
2) Comparing Design #1, #2, and #3, when the K value increases from 2 to 7, the primary-side RMS current almost doesn't change.
3) Comparing Design #1, #2, and #3, when the K value increases from 2 to 7, the secondary-side RMS current at 400 V input is only increased by 2 A (or 7%), but the peak resonant capacitor voltage at 300 V input is reduced by 159 V (or 33%). The capacitor voltage reduction is more significant than the RMS current increase, therefore Design #2 and #3 (with larger K value) are better trade-offs than Design #1.
4) The voltage stress of C_a slightly decreases as K increases. Among the four designs, Design #3 has the lowest C_a voltage stress in the worst-case scenario (89 V at 300 V/full load).

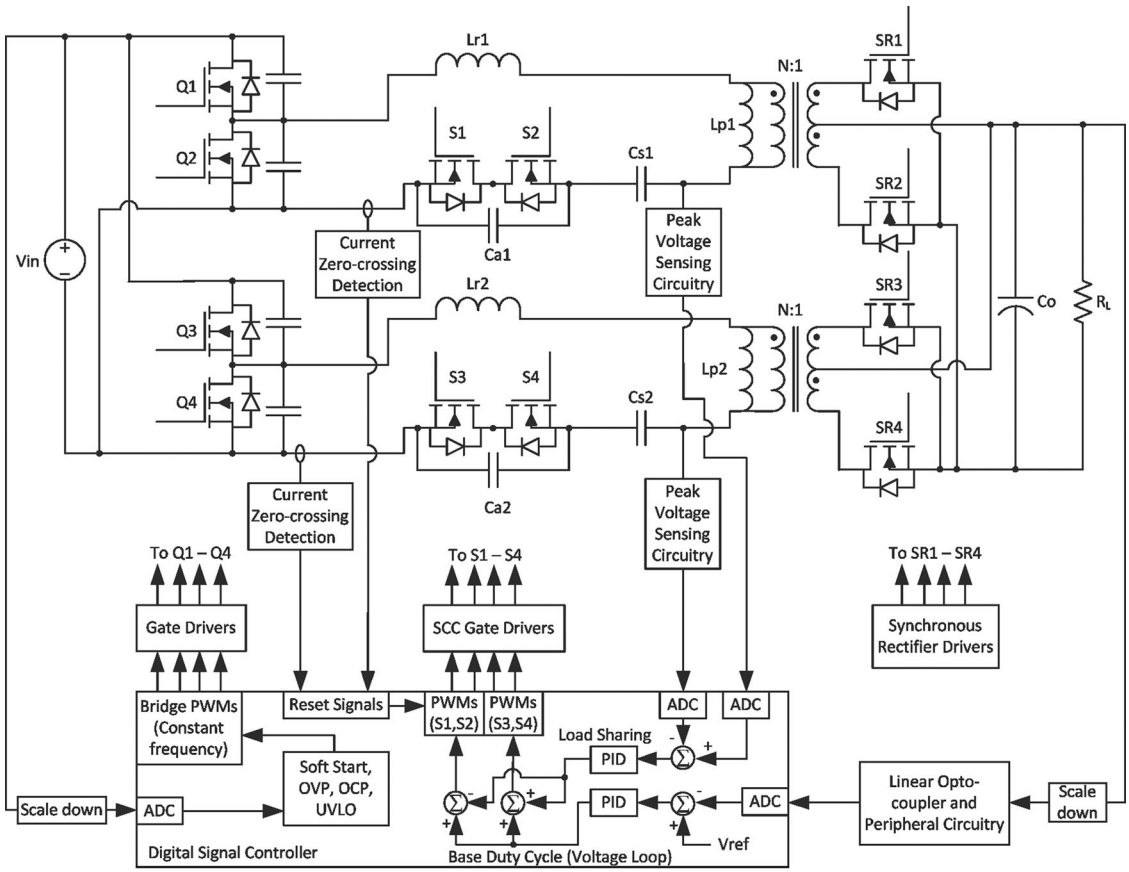

Fig. 9. Diagram of the prototype two-phase interleaved SCC-LLC.

D. Tolerance Considerations

In an interleaved SCC-LLC converter, the component tolerances cause the output voltage gain of each phase different at the switching frequency. Different control angle α values will be needed in each phase to achieve load sharing. Since the output current is entirely controlled by SCC from light load to full load, there is no performance limitation of the load sharing as long as all the SCC-LLC phases are capable of delivering the rated power level. However, if the tolerance is too large, the power train is no longer the one that was originally designed, therefore the output current capacity in some phases may be lower than the design specification. In this case, the below-specification phases will be incapable of matching the output current of other phases at heavy load. This is a design margin issue faced by all types of resonant converters. Therefore, the component tolerances should be within a reasonable range. Usually the design margin provided by the FHA design approach should be sufficient. However, if the component tolerances are particularly large, simulation is necessary to confirm the design margin.

In order to prove the proposed SCC-LLC is able to achieve load sharing even with very large tolerance as long as the power stage is capable of delivering such power level, simulation is performed with 30% variation of resonant inductance and 15% variation of resonant capacitance. The simulation uses the parameters listed in Table IV.

The simulation results are shown in Fig. 8, where Ipri1 and Ipri2 are primary-side resonant current in Phase 1 and 2, respectively; Isec1 and Isec2 are secondary-side output current of Phase 1 and 2, respectively; VgS1 and VgS2 are SCC gating signals of Phase 1; VgS3 and VgS4 are SCC gating signals of Phase 2; Vca1 and Vca2 are SCC capacitor voltages of Phase 1 and 2, respectively.

Fig. 8 shows that even with very large tolerances, the output current of the two phases are very well balanced. The resonant component values in Phase 1 are significantly larger than those in Phase 2; therefore the SCC control angle α in Phase 1 is much smaller than that in Phase 2 in order to reduce the equivalent resonant frequency.

VI. Experiment Results

A 600-W two-phase interleaved SCC-LLC converter is implemented to verify the feasibility and to demonstrate the advantages of the proposed method. The diagram of the prototype is shown in Fig. 9, and the parameters are in Table V.

The resonant inductors are implemented using the transformers' leakage inductance. They are intentionally made nonidentical in order to verify the prototype's load sharing performance. The two SCC-LLC phases have 90° phase shift for ripple cancelation.

The Design #3 is chosen to implement. The implemented capacitor values are close to the designed values as much as

TABLE V
PROTOTYPE PARAMETERS

Switching frequency	200kHz
Input Voltage	400V nominal/300V minimum
Output Voltage	12V
Output Power	300W × 2
Transformer Turns Ratio	20:1, Center tapped
Magnetizing Inductance	87μH(Phase1) 85μH(Phase2)
Resonant Inductance	12μH(Phase1) 14μH(Phase2)
Series Capacitance	36nF±5% (12nF× 3, Polypropylene Film)
SCC Capacitance	30nF±3% (10nF× 3, Polypropylene Film)
Output Capacitance	1790μF (100μF× 8 + 330μF× 3)
Half-bridge MOSFET	Infineon IPB60R190C6
SCC MOSFET	Infineon BSC060N10NS3 G (100V, 6mΩ)
SR MOSFET	Infineon BSC011N03LS

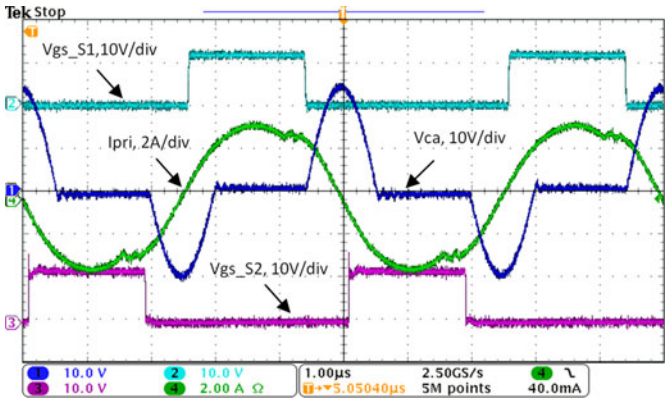

Fig. 10. SCC operation. $V_{\rm in} = 400$ V, $V_o = 12$ V, $I_o = 40$ A (20 A per phase), $\alpha = 131°$.

possible. The transformer turns ratio is later changed to 20:1 because the magnetic cores used in this prototype are relatively large for the designed power level, therefore increasing the transformers' turns to reduce the core loss in order to obtain a higher overall efficiency can be justified in this particular case.

A Microchip DSC dsPIC33FJ32GS606 is used to implement the digital controller. A linear opto-coupler is used to transmit output voltage signal to the primary side. The output voltage signal is sampled by an ADC, and then subtracted from a reference voltage value to create an error value. The error value is processed by a voltage-loop control law and becomes a base duty cycle for both SCC PWMs. Two other ADCs are used to sample the peak resonant capacitor voltage of each phase which reflects the output current level. The peak voltage sensing circuitry is adopted from [38]. The error between the two peak voltage values is processed by a load-sharing control law and becomes adjustment values of the base duty cycle. The adjusted duty cycle values are then used to control the SCC PWMs. Each SCC PWM is synchronized with the zero-crossing points of the primary-side current of the corresponding phase. The zero-crossing detection is implemented using a current transformer and a comparator. The synchronization is implemented using the DSC's External PWM Reset (XPRES) function, which allows a logic signal from the current zero-crossing detection circuit to reset the digital PWM.

Fig. 10 and Fig. 11 show the measured waveforms of SCC modulation. $V_{\rm ca}$ is the voltage across C_a; V_{gs_S1} is the gating signal of S_1; V_{gs_S2} is the gating signal of S_2; $I_{\rm pri}$ is the primary current. Fig. 10 shows 40 A (20 A × 2 phases) load current scenario; the control angle α is 131°. Fig. 11 shows 20 A load current scenario (10 A × 2 phases); the control angle α is 136°.

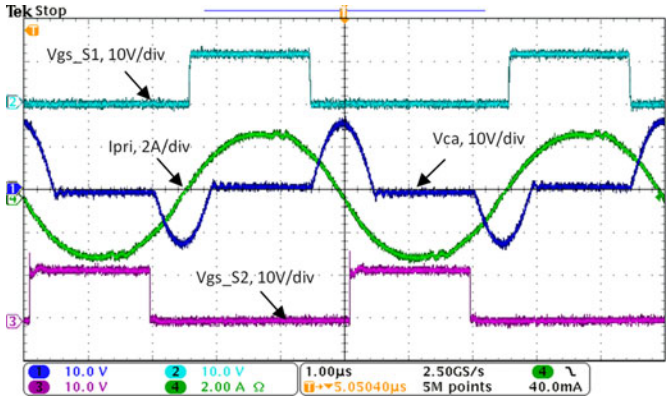

Fig. 11. SCC operation. $V_{\rm in} = 400$ V, $V_o = 12$ V, $I_o = 20$ A (10 A per phase), $\alpha = 136°$.

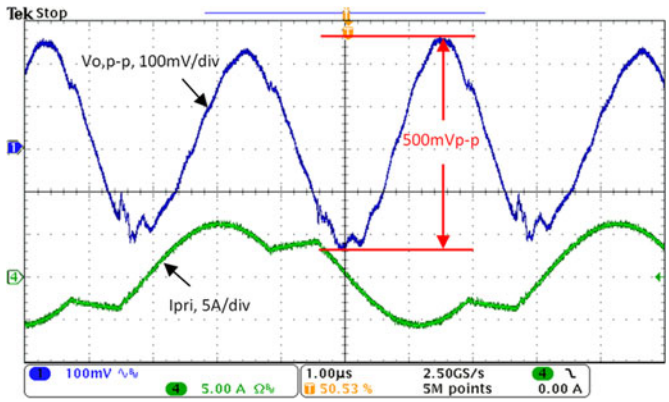

Fig. 12. Output voltage ripple, $V_{\rm in} = 400$ V, $V_o = 12$ V, $I_o = 50$ A, single-phase LLC.

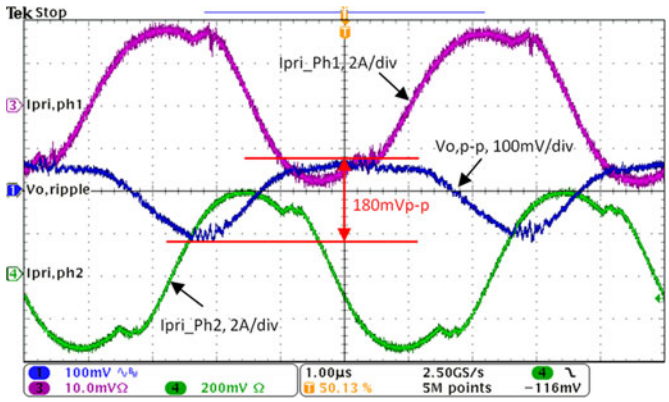

Fig. 13. Output voltage ripple, $V_{\rm in} = 400$ V, $V_o = 12$ V, $I_o = 50$ A, two-phase interleaved SCC-LLC.

Fig. 12 and Fig. 13 show the effectiveness of the current ripple cancellation and the load sharing of the proposed SCC-LLC converter. A separate single-phase LLC converter with the same input/output specification and output capacitance has been built for the purpose of comparison.

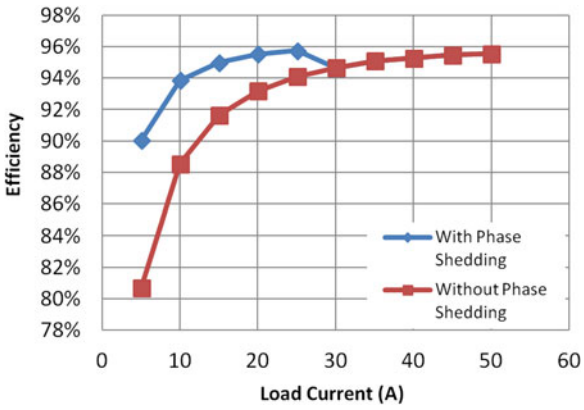

Fig. 14. Efficiency comparison.

Fig. 15. Prototype photo.

Fig. 12 shows waveforms of the single-phase LLC converter with 12 V, 600-W output, with identical output capacitance used in the prototype SCC-LLC. The output voltage ripple is 500 mV peak to peak at 50 A load current.

Fig. 13 shows waveforms of the proposed two-phase interleaved SCC-LLC converter. The output voltage ripple at 50 A load is reduced to 180mV peak to peak. The ripple cancelation can perform even better if external resonant inductors are used, which will make the resonant inductance of the two half-switching cycles better symmetrical. Fig. 13 also shows that the output current of the two phases are very well balanced. Given that the SCC MOSFETs have only 6-mΩ on-resistance, and the primary-side RMS current is only 2.5-A per phase, the total conduction loss in SCC MOSFETs is negligible. There is no switching loss as all the SCC MOSFETs have ZVS turn-on and turn-off.

Fig. 14 shows the efficiency curves of the two-phase interleaved SCC-LLC with and without phase shedding. It is shown that the heavy load efficiency approaches 96%; and with phase shedding, the 5-A load efficiency is significantly improved from 81% to 90%.

Fig. 15 shows a photo of the prototype board.

VII. Conclusion

A SCC modulated LLC converter (SCC-LLC) is proposed in this paper to achieve constant switching frequency operation. The proposed SCC-LLC uses SCC to modulate resonant frequency, thus, to modulate voltage gain. This is favorable for interleaved operation because all the SCC-LLC stages can operate at the same switching frequency for ripple cancellation, and each phase still has independent control to achieve load sharing. The output power capacity can be easily expanded by interleaving multiple SCC-LLC stages, and the light-load efficiency can be improved by using phase shedding technique. Analyses show that the proposed constant frequency SCC-LLC converter has different characteristics from conventional variable switching frequency LLC converters; therefore, a design procedure is developed. A design example is provided, and a group of design results are compared against simulation results in order to provide insights into the calculation accuracy and the design tradeoffs. A two-phase 600-W SCC-LLC prototype is built to prove the feasibility of the proposed method. The prototype shows good load sharing performance and light-load efficiency improvements, as well as current ripple cancelation.

References

[1] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. Appl. Power Electron. Conf. Expo.*, 2002, vol. 2, pp. 1108–1112.

[2] Y. Zhang, D. Xu, M. Chen, Y. Han, and Z. Du, "LLC resonant converter for 48 V to 0.9 V VRM," in *Proc. Power Electron. Spec. Conf.*, 2004, vol. 3, pp. 1848–1854.

[3] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. van Wyk, "Optimal design methodology for LLC resonant converter," in *Proc. Appl. Power Electron. Conf. Expo.*, 2006, p. 6 pp.

[4] S. De Simone, C. Adragna, C. Spini, and G. Gattavari, "Design-oriented steady-state analysis of LLC resonant converters based on FHA," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom., Motion*, 2006, pp. 200–207.

[5] H.-S. Choi, "Design consideration of half-bridge LLC resonant converter," *J. Power Electron.*, vol. 7, 2007.

[6] D. Fu, B. Lu, and F. C. Lee, "1 MHz high efficiency LLC resonant converters with synchronous rectifier," in *Proc. Power Electron. Spec. Conf.*, 2007, pp. 2404–2410.

[7] J. Jee-hoon and K. Joong-gi, "Theoretical analysis and optimal design of LLC resonant converter," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.

[8] C. Adragna, S. De Simone, and C. Spini, "A design methodology for LLC resonant converters based on inspection of resonant tank currents," in *Proc. Appl. Power Electron. Conf. Expo.*, 2008, pp. 1361–1367.

[9] K. Bong-Chul, P. Ki-Bum, K. Chong-Eun, L. Byoung-Hee, and M. Gun-Woo, "LLC resonant converter with adaptive link-voltage variation for a high-power-density adapter," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2248–2252, Sep. 2010.

[10] P. Drgona, M. Frivaldsky, and A. Prikopova, "Optimal design of digital control system for LLC resonant converter," in *Proc. Int. Conf. Appl. Electron.*, 2010, pp. 1–4.

[11] D. Fu, F. C. Lee, and W. Shuo, "Investigation on transformer design of high frequency high efficiency dc-dc converters," in *Proc. Appl. Power Electron. Conf. Expo.*, 2010, pp. 940–947.

[12] C. Oeder, A. Bucher, J. Stahl, and T. Duerbaum, "A comparison of different design methods for the multiresonant LLC converter with capacitive output filter," in *Proc. Workshop Control Modeling Power Electron.*, 2010, pp. 1–7.

[13] G. Ivensky, S. Bronshtein, and A. Abramovitz, "Approximate analysis of resonant LLC DC-DC converter," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3274–3284, Nov. 2011.

[14] X. Fang, H. Hu, Z. J. Shen, and I. Batarseh, "Operation mode analysis and peak gain approximation of the LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1985–1995, Apr. 2012.

[15] X. Fang, H. Hu, F. Chen, U. Somani, E. Auadisian, J. Shen, and I. Batarseh, "Efficiency-Oriented optimal design of the LLC resonant converter based on peak gain placement," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2285–2296, May 2013.
[16] B. Wang, X. Xin, S. Wu, H. Wu, and J. Ying, "Analysis and implementation of LLC burst mode for light load efficiency improvement," in *Proc. Appl. Power Electron. Conf. Expo.*, 2009, pp. 58–64.
[17] D. Wang, L. Jia, J. Fu, Y.-F. Liu, and P. C. Sen, "A new driving method for synchronous rectifiers of LLC resonant converter with zero-crossing noise filter," in *Proc. Energy Convers. Congr. Expo.*, 2010, pp. 249–255.
[18] W. Feng, F. C. Lee, and P. Mattavelli, "Optimal trajectory control of burst mode for LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 457–466, Jan. 2013.
[19] E. Orietti, P. Mattavelli, G. Spiazzi, C. Adragna, and G. Gattavari, "Current sharing in three-phase LLC interleaved resonant converter," in *Proc. Energy Convers. Congr. Expo.*, 2009, pp. 1145–1152.
[20] E.-S. Kim, K.-H. Yoon, S. Phum, S. Meas, J.-S. Won, S.-J. Oh, and Y.-S. Bae, "Operation characteristics of two-stage DC/DC converter for photovoltaic system," in *Proc. Appl. Power Electron. Conf. Expo.*, 2012, pp. 681–685.
[21] E.-S. Kim, Y.-J. No, S.-M. Lee, B.-G. Chung, J.-S. Lee, M.-S. Park, and D.-Y. Huh, "A low profile LLC resonant converter using novel planar transformer," in *Proc. Appl. Power Electron. Conf. Expo.*, 2012, pp. 1307–1312.
[22] T. Jin and K. Smedley, "Multiphase LLC Series Resonant Converter for Microprocessor Voltage Regulation," in *Proc. Ind. Applicat. Conf.*, 2006, pp. 2136–2143.
[23] K.-H. Yi, B.-C. Kim, and G.-W. Moon, "A simple and novel two phase interleaved LLC series resonant converter employing a phase of the resonant capacitor," in *Proc. Energy Convers. Congr. Expo.*, 2009, pp. 754–757.
[24] B.-R. Lin, W.-R. Yang, J.-J. Chen, C.-L. Huang, and M.-H. Yu, "Interleaved LLC series converter with output voltage doubler," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 92–98.
[25] M. Kim, "Two-phase interleaved LLC resonant converter with phase shedding control," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 1642–1645.
[26] H. Figge, T. Grote, N. Froehleke, J. Boecker, and P. Ide, "Paralleling of LLC resonant converters using frequency controlled current balancing," in *Proc. Power Electron. Spec. Conf.*, 2008, pp. 1080–1085.
[27] B.-C. Kim, K.-B. Park, C.-E. Kim, and G.-W. Moon, "Load sharing characteristic of two-phase interleaved LLC resonant converter with parallel and series input structure," in *Proc. Energy Convers. Congr. Expo.*, 2009, pp. 750–753.
[28] S. Ben-Yaakov and M. M. Peretz, "A self-adjusting sinusoidal power source suitable for driving capacitive loads," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 890–898, Jul. 2006.
[29] J. M. Alonso, M. A. Dalla Costa, M. Rico-Secades, J. Cardesin, and J. Garcia, "Investigation of a new control strategy for electronic ballasts based on variable inductor," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 3–10, Jan. 2008.
[30] W.-J. Gu and K. Harada, "A new method to regulate resonant converters," *IEEE Trans. Power Electron.*, vol. 3, no. 4, pp. 430–439, Oct. 1988.
[31] W. J. Gu and K. Harada, "A circuit model for the class E resonant DC-DC converter regulated at a fixed switching frequency," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 99–110, Jan. 1992.
[32] J.-H. Cheng, A. F. Witulski, and J. L. Vollin, "Dynamic analysis of the Class-D converter at fixed frequency using amplitude and phase modulation," in *Proc. Power Electron. Spec. Conf.*, 1998, vol. 1, pp. 387–393.
[33] J.-H. Cheng, A. F. Witulski, and J. L. Vollin, "A generalized DC model and low-frequency dynamic analysis for the Class-D converter at fixed frequency," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1212–1220, Nov. 2000.
[34] C. Jung-Hui, A. F. Witulski, and J. L. Vollin, "A small-signal model utilizing amplitude modulation for the class-D converter at fixed frequency," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1204–1211, Nov. 2000.
[35] L. Huber and M. M. Jovanoviae, "Evaluation of AC VRM topologies for high-frequency power distribution systems," in *Proc. Appl. Power Electron. Conf. Expo.*, 2001, vol. 1, pp. 160–166.
[36] Y.-T. Chen, W.-M. Lin, and Y.-H. Liu, "Analysis and design of a dimmable electronic ballast controlled by a switch-controlled capacitor," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1564–1572, Dec. 2005.
[37] H.-J. Chiu and S.-J. Cheng, "Single-Stage voltage source charge-pump electronic ballast with switched-capacitor dimmer for multiple fluorescent lamps," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2915–2918, Oct. 2007.
[38] STMicroelectronics, "High-voltage resonant controller," L6599 datasheet, 2006.

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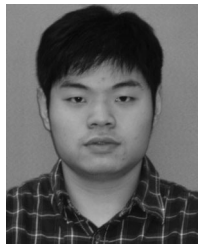

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