A Control Strategy and Design Method for Interleaved LLC Converters Operating at Variable Switching Frequency

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***Abstract*—LLC converters face challenges in high-current applications, where the high conduction loss limits the maximum load capacity and reduces efficiency. Interleaving technique can be used to solve this problem, but the component tolerances of the resonant tanks will cause severe load sharing problem. The SCC–LLC converter was proposed to solve the load sharing problem. However, due to its constant switching frequency operation, it has some limitations over complete line and load variation compared to conventional LLC converters. In this paper, a new control strategy is proposed for the SCC–LLC converter, which enables variable switching frequency operation; thus, it provides uncompromised performance while achieving interleaved operation. Analyses and a design method are provided, and a 600-W two-phase interleaved SCC–LLC prototype is built to verify the feasibility.**

***Index Terms*—Interleaving, load sharing, resonant power conversion, switched-mode power supply.**

I. Introduction

TODAY'S power converters are required to deliver more power and achieve high efficiency in a wide load range. These requirements are sometimes contradictive, because when the current is high, the conduction loss is dominant, then the efficiency is likely to suffer. To solve this problem, interleaving and phase-shedding techniques have been developed, and they have the following advantages: 1) in heavy load condition, multiple phases can split the total current, thus mitigate the I^2R loss and other associated losses; 2) in light load condition, unneeded phases can be shut down, thus the light-load efficiency can be improved; and 3) output ripple current are cancelled by the interleaved phases, thus the output capacitor size can be smaller.

The LLC resonant topology [1]–[4] has been popularly adopted in flat panel TVs [5], laptop adaptors [6], [7], LED lighting [8], [9], computer [10], battery charger [11], renewable energy [12]–[15], transportation [16]–[18], and so on. The below-resonance region of the LLC converters has advantages such as zero-voltage switching (ZVS) for main switches, zero-current switching (ZCS) for output rectifiers, narrow frequency variation range, etc., resulting in high efficiency. However, interleaving LLC converters has a difficulty: when interleaved, all the LLC stages must operate at the same switching frequency; whereas due to the components' tolerances, individual LLC stages may have different resonant frequencies, thus the output currents will be different. Simulation results in Section IV will show that the normal component tolerances can cause severe load sharing problem.

Previous studies on interleaved LLC converters all have limitations. The interleaved LLC converters in [19]–[22] did not consider the load sharing problem caused by the component tolerances. The load sharing method in [23] needs an additional power stage to regulate the output voltage and does not work for more than two phases interleaved. The structure in [24] divides down the input voltage by the number of phases; therefore, the load capacity is still limited and it has difficulties with phase shedding. The topology in [25] also has difficulties with phase shedding. The variable inductor method in [26] requires a controlled dc current source to saturate the inductor, thus is less efficient.

The switch-controlled capacitor (SCC)–LLC converter was proposed in [27]. It uses an SCC [28] in each LLC power stage to control the resonant frequency. Therefore, output voltage regulation is achieved with constant switching frequency operation, which provides a simple solution for interleaving, load sharing, and phase shedding. However, the constant switching frequency operation also imposes some limitations over complete line and load variation compared to conventional LLC converters with switching frequency control.

In this paper, a new control strategy is proposed for the SCC–LLC converter. It achieves variable switching frequency operation and interleaving at the same time. Section II reviews the constant switching frequency SCC–LLC converter; Section III proposes the new control strategy; Section IV provides analyses and a design method of the new control strategy; Section V shows the experimental results; and Section VI is the conclusion.

II. Review of Constant Switching Frequency SCC–LLC Converter

The concept of SCC was proposed in [28] and has been applied in various applications to obtain constant switching frequency operation [29]–[34]. It includes the full-wave SCC and

Manuscript received August 4, 2013; revised October 31, 2013; accepted January 2, 2014. Date of current version March 26, 2014. Recommended for publication by Associate Editor R.-L. Lin.

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Digital Object Identifier 10.1109/TPEL.2014.2300165

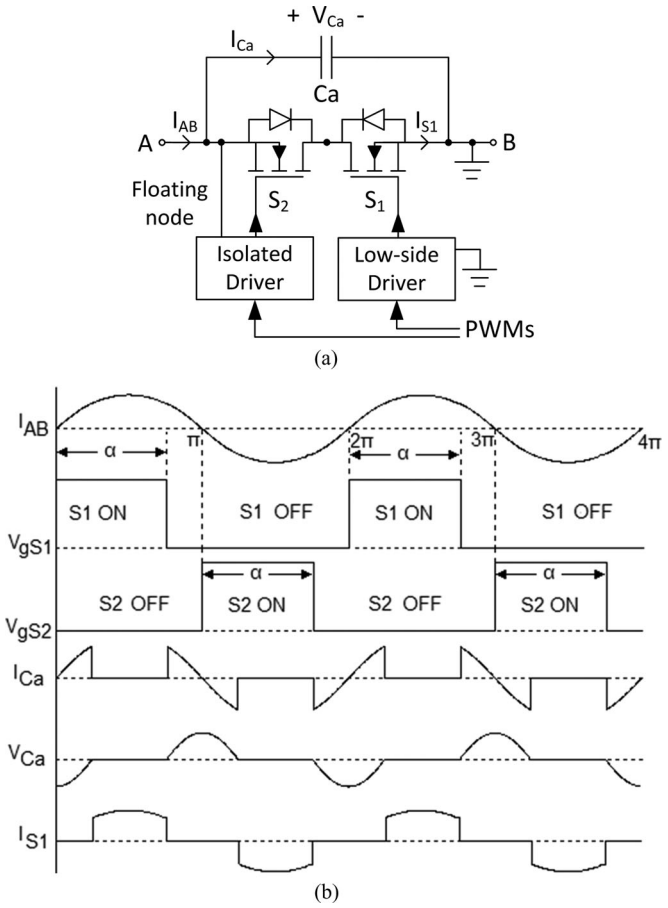

Fig. 1. Structure and waveforms of full-wave SCC. (a) Structure of full-wave SCC. (b) Waveforms of full-wave SCC.

the half-wave SCC. Both structures consist of a capacitor in parallel with one or two switches. When the switches are turned ON, the current bypasses the capacitor, thus the circuit behaves noncapacitive. When the switches are turned OFF, the current flows through the capacitor, thus the circuit behaves capacitive. The equivalent capacitance of SCC, $C_{\rm SC}$, can be modulated by the turn-off angle of the switches.

Fig. 1 shows the structure and waveforms of a full-wave SCC. The equivalent capacitance of the full-wave SCC, $C_{\rm SC,FW}$, is modulated by the angle α ($\pi/2 < \alpha < \pi$), given in (1) [28]. The angle α is synchronized at the zero-crossing points of the resonant current

$$C_{\rm SC,FW} = \frac{C_a}{2-(2\alpha-\sin 2\alpha)/\pi}. \tag{1}$$

The previously proposed constant switching frequency SCC–LLC converter [27] is illustrated in Fig. 2. A full-wave SCC is connected in series with the resonant tank in order to modulate the resonant capacitance. The equivalent resonant capacitance, C_r, is derived as follows:

$$C_r = \frac{C_{\rm SC}C_s}{C_{\rm SC}+C_s}. \tag{2}$$

The operation principle of the constant switching frequency SCC–LLC converter is described as follows.

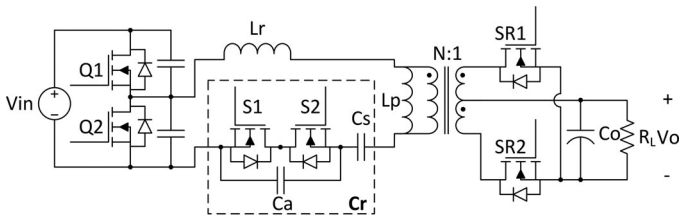

Fig. 2. Topology of the constant switching frequency SCC–LLC converter.

The switching frequency is constant. The SCC's turn-off angle α controls the equivalent resonant capacitance C_r, which in turn controls the resonant frequency, and thus, the output voltage gain of the SCC–LLC converter. In an interleaved multiphase SCC–LLC converter, all the phases are operating at the same constant switching frequency with shifted phase angles to facilitate the ripple cancellation. Each phase uses an SCC to regulate the output voltage and to achieve load sharing. For example, when the controller detects that one phase is providing more output current than other phases, it slightly increases the control angle α of the corresponding phase, which increases the resonant capacitance C_r and lowers the resonant frequency, and thus reduces the output current until it reaches the balanced point. Different phases may use different α angles to achieve load sharing because the component tolerances are usually different.

The aforementioned constant switching frequency SCC–LLC converter solves the load sharing problem for the interleaved LLC topology, and enables this highly efficient topology to be applied in high-current applications. However, as disclosed in [27], the constant switching frequency SCC–LLC converter exhibits different characteristics than conventional LLC converters, because it uses resonant frequency modulation (FrM) instead of switching frequency modulation (FsM). The differences of the two modulation methods are discussed as follows.

The voltage gain expression of an LLC resonant tank is derived in (3) using the fundamental harmonic approximation (FHA) method. The definitions are in (4) for quick reference. M is the gain of the resonant tank, where the factor 2 is due to the half-bridge configuration. N is the transformer turns ratio. L_p is the parallel inductance. K is the inductance ratio. R_L is the load resistance. ω_s is the switching frequency in radians ω_r is the resonant frequency in radians

$$M = \frac{K}{\sqrt{\left[\left(\frac{\omega_r}{\omega_s}\right)^2 - K - 1\right]^2 + \frac{\pi^4\omega_s^2 L_p^2}{64N^4R_L^2}\left[\left(\frac{\omega_r}{\omega_s}\right)^2 - 1\right]^2}} \tag{3}$$

$$M = \frac{NV_o}{V_{\rm in}/2},\ N = \frac{N_p}{N_s},\ K = \frac{L_p}{L_r},\ \omega_s = 2\pi f_s,\ \omega_r = \frac{1}{\sqrt{L_rC_r}}. \tag{4}$$

For a given set of values of L_p, K, R_L, and N, the gain curves resulted from FrM and FsM are plotted using (3), respectively, shown in Fig. 3. When plot the FrM curve, ω_s is fixed and ω_r is variable; the normalized frequency is defined as ω_r/ω_s. When

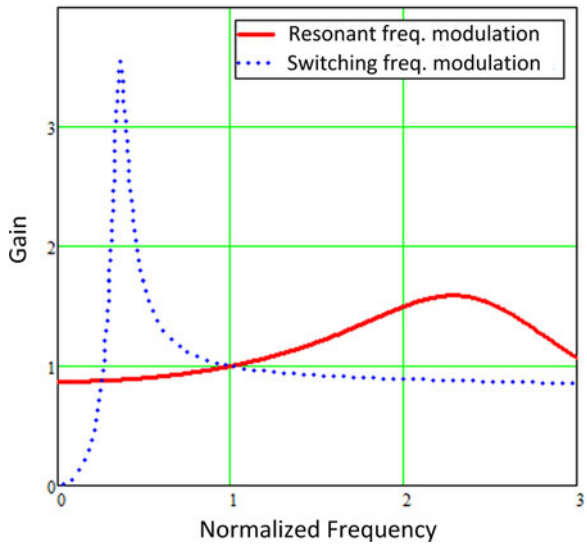

Fig. 3. Comparison of FsM and FrM.

plot the FsM curve, ω_r is fixed and ω_s is variable; the normalized frequency is defined as ω_s/ω_r. It is evident that the FsM provides a higher peak gain within a narrower frequency variation range than the FrM does. This phenomenon can be understood from the impedance point of view: the FsM modulates the impedance of all the resonant components, whereas the FrM only modulates the impedance of the resonant capacitance, thus is less effective.

The aforementioned analysis reveals that the previously proposed constant switching frequency SCC–LLC converter makes compromises in terms of peak gain range and normalized frequency variation range compared to conventional LLC converters. In order to take full advantage of the LLC topology, FsM is preferred.

In addition, Fig. 1 shows that, the full-wave SCC uses two MOSFETs and requires isolated driving. This increases the circuit complexity and the conduction loss. Half-wave SCC is more desirable if it can be used.

III. Proposed Variable Switching Frequency Control Strategy

A. Variable Switching Frequency SCC–LLC Converter

It is noted that the interleaving operation only requires that the switching frequency of all the interleaved phases be the same, yet the switching frequency of all the phases can change together in different operating conditions. It is also noticed that the FsM is more effective than the FrM. Therefore, a new control strategy is proposed as follows:

1) All the interleaved SCC–LLC phases operate at the same but variable switching frequency. The output voltage is controlled by the switching frequency.
2) The gate driving signals of all phases are interleaved so that the output current of all phases is interleaved for ripple cancellation.
3) The load sharing among different phases is achieved by changing the equivalent resonant capacitance using the SCC technology.

In this way, the peak gain range and the frequency variation range of the SCC–LLC converter are the same as conventional LLC converters. The ZVS condition of the half-bridge switches is also the same as conventional LLC converters. The required capacitance variation range for the SCC is much smaller because it is only responsible for compensating the component tolerances to achieve load sharing; therefore, half-wave SCC can be used.

The new control strategy can be applied in the topology in Fig. 2, but the full-wave SCC is unnecessary and can be reduced to a half-wave SCC. The modified topology suitable for the new control strategy is shown in Fig. 4.

B. Comparison of Full-Wave SCC and Half-Wave SCC

Fig. 5 shows the structure and waveforms of a half-wave SCC. The control scheme is similar to that of the full-wave SCC, except that there is only one MOSFET, and the control angle α is from 0 to π.

In order to reduce the power loss on the MOSFET's body diode, in this paper, the SCC MOSFET is turned ON as soon as the C_a voltage is discharged to zero. From the C_a voltage zero-crossing point to the resonant current zero-crossing point, the MOSFET acts like a synchronous rectifier. It has no impact on the equivalent capacitance modulation.

The equivalent capacitance of the half-wave SCC, $C_{\mathrm{SC,HW}}$, is given in [33], and is rewritten in (5) after rearrangement

$$C_{\mathrm{SC,HW}} = \frac{2C_a}{2-(2\alpha-\sin 2\alpha)/\pi}. \tag{5}$$

The comparison of the full-wave SCC and the half-wave SCC includes the following aspects:

1) *Cost.* The half-wave SCC has only one MOSFET and does not require isolated driving; therefore, its cost is lower than that of the full-wave SCC.
2) *Power loss.* The half-wave SCC has only one MOSFET; therefore, its conduction loss and gate driving loss are lower than that of the full-wave SCC. Both the full-wave and the half-wave SCCs have ZVS conditions at turn-on and turn-off; therefore, there is no switching loss.
3) *Capacitance regulation capacity.* The control angle α of a full-wave SCC is from $\pi/2$ to π. Substituting α into (1) gives that the resultant capacitance regulation range is from C_a to infinity. Likewise, the control angle α of a half-wave SCC is from 0 to π. Substituting α into (5) gives that the resultant capacitance regulation range is also from C_a to infinity. Therefore, the half-wave SCC and the full-wave SCC have the same capacitance regulation capacity. This analysis result can be understood by considering the two extreme cases: when the control angle α is minimum ($\pi/2$ for full-wave SCC, and 0 for half-wave SCC), the capacitor C_a is always connected in the resonant circuit, therefore its equivalent capacitance is C_a; when the control angle α is maximum (π for both full-wave and half-wave SCCs), the capacitor C_a is always shorted by the MOSFET, therefore its equivalent capacitance is infinite.
4) *Symmetry.* The full-wave SCC can perform modulation when the resonant current is in both directions; therefore,

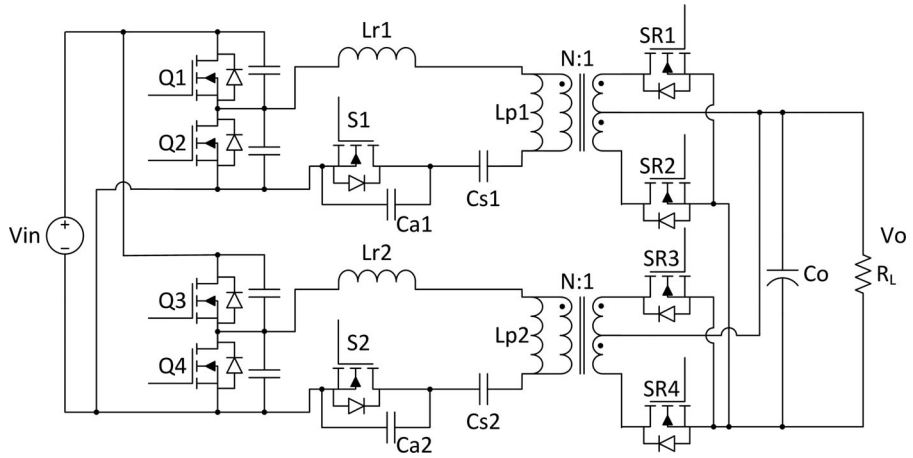

Fig. 4. Modified SCC–LLC converter suitable for the variable switching frequency control strategy.

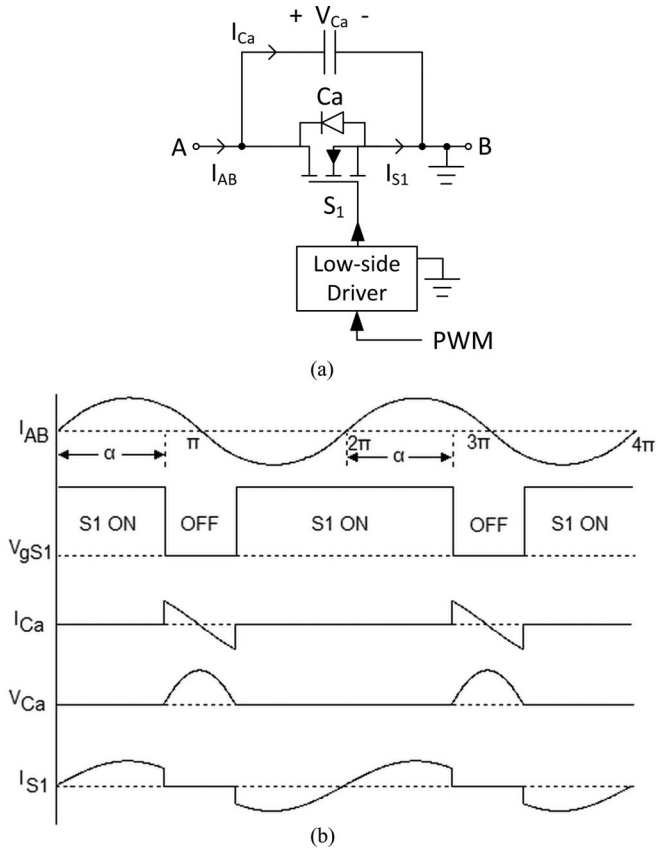

Fig. 5. Structure and waveforms of half-wave SCC. (a) Structure of half-wave SCC. (b) Waveforms of half-wave SCC.

the SCC voltage waveform is symmetrical in both half-cycles. This is favorable for LLC converter because the output current in both half-cycles will be the same. The half-wave SCC can perform modulation only in one direction; therefore, the SCC's waveforms will be asymmetrical, causing the output current of the two half-cycles nonidentical. This effect can be observed in Fig. 16. In order to restrict the asymmetrical effect within an acceptable level, the SCC voltage amplitude should be kept low, which means the capacitance variation range should be small. As a result, half-wave SCC is not desirable in constant switching frequency SCC–LLC converters, because the resonant capacitance needs to vary significantly in different operating conditions. However, half-wave SCC is suitable in variable switching frequency SCC–LLC converters, because the resonant capacitance only needs to vary by a small amount to compensate the component tolerances.

To sum up aforementioned analyses, the half-wave SCC has lower cost, lower power loss, the same capacitance regulation capacity, but asymmetrical waveforms compared to the full-wave SCC. Because the proposed control strategy only requires a small capacitance variation range for the SCC, the asymmetrical effect can be managed within an acceptable level. Therefore, the half-wave SCC is the best tradeoff between the cost and the performance in the proposed control strategy.

IV. Analysis and Design Method

The proposed control strategy uses the switching frequency to regulate the output voltage; therefore, the design procedure is the same as in conventional LLC converters, which is available in many literatures [4], [35]–[38]. The only unknown parameter is the SCC capacitor value C_a. This section studies the load sharing characteristics of multiphase LLC converters, and then provides a design method to select the value of C_a according to component tolerance values.

A. Load Sharing Characteristics

Due to components' tolerances, the resonant frequencies of interleaved LLC stages are slightly different from each other, resulting in different output-current-versus-switching-frequency curves. A set of such curves are obtained from simulation and plotted in Fig. 6. In this example, $\pm 7\%$ tolerances are assumed for inductors, and $\pm 5\%$ tolerances are assumed for capacitors. The specification is: $V_{\text{in}} = 300$ V-400 V, $V_o = 12$ V. Reasonable power train parameters are used: transformer turns ratio is 20:1; nominal component values of C_s, L_r, and L_p are 40 nF, 12 μH, and 86 μH, respectively. The peak output current

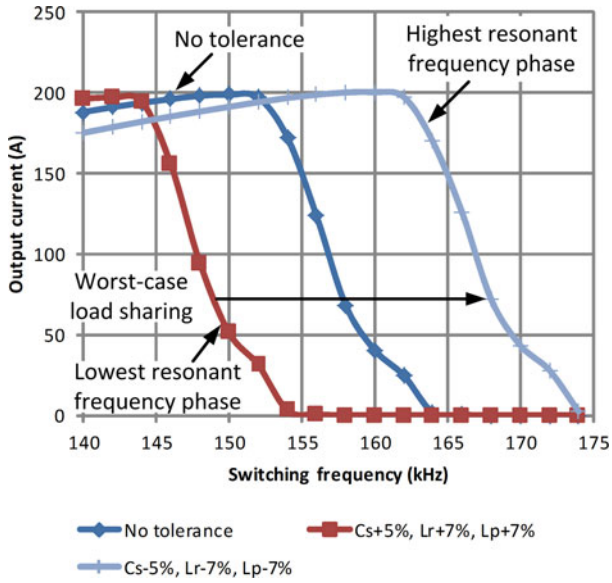

Fig. 6. Output current versus switching frequency curves at different tolerances. Input voltage is 400 V. Output voltage is 12 V. Transformer turns ratio is 20:1.

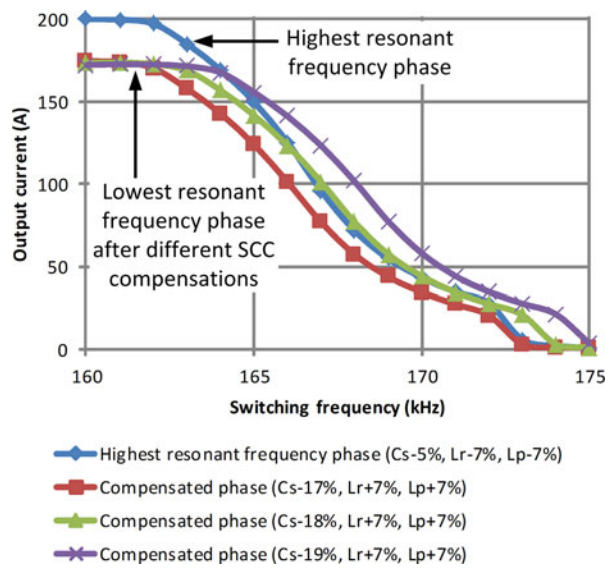

Fig. 7. Output current versus switching frequency curves after compensation. Input voltage is 400 V. Output voltage is 12 V. Transformer turns ratio is 20:1.

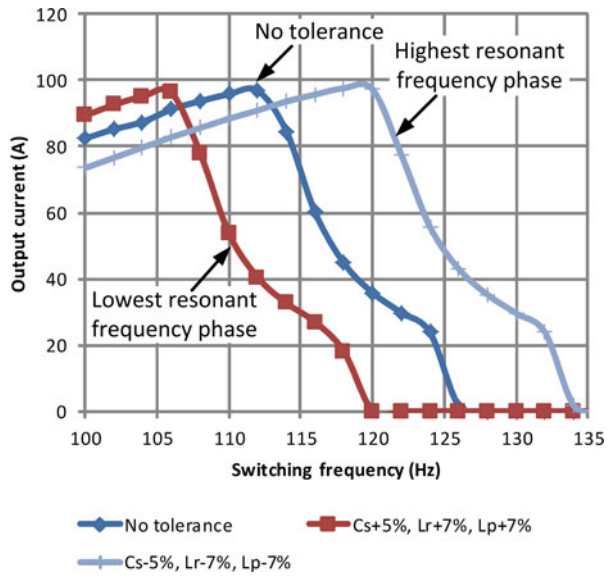

Fig. 8. Output current versus switching frequency curves at different tolerances. Input voltage is 300 V. Output voltage is 12 V. Transformer turns ratio is 20:1.

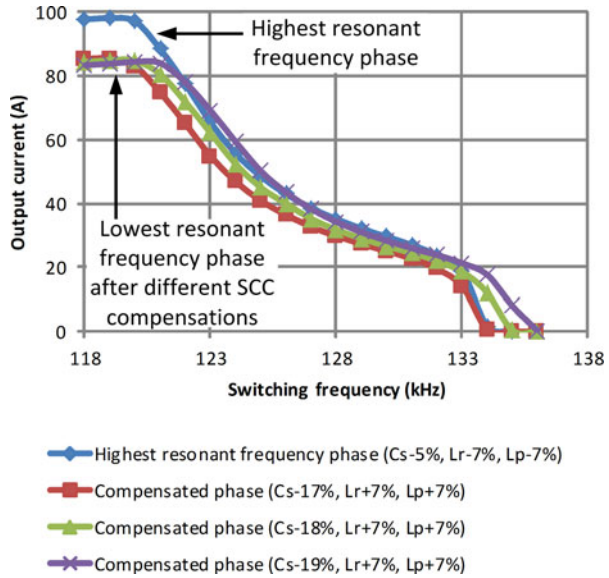

Fig. 9. Output current versus switching frequency curves after compensation. Input voltage is 300 V. Output voltage is 12 V. Transformer turns ratio is 20:1.

obtained by simulation are the theoretical maximum capacity of such a resonant tank.

In Fig. 6, the rightmost curve represents the relation between output current and switching frequency when the resonant components are at their minimum tolerance values. The leftmost curve represents the relation between the output current and the switching frequency when the resonant components are at their maximum tolerance values. The middle curve represents the relation between output current and switching frequency with nominal resonant component values. This plot demonstrates that when two LLC converters are connected in parallel, in the worst case, no current sharing can be achieved. For example, at 170 kHz switching frequency, the output current of the aforementioned two phases are 50 and 0 A, respectively.

In order to achieve load sharing, SCC can be used to reduce the equivalent resonant capacitance of the lower output current phase, so that its output current will increase and match the higher output-current phase. Note that the SCC can only increase the resonant frequency, but not decrease; therefore, the highest resonant frequency phase in an interleaved SCC–LLC converter automatically becomes the reference phase. All the lower resonant frequency phases must be compensated by the SCC and match to the reference phase. The worst case for load sharing is to have these two extreme tolerance cases in the same interleaved SCC–LLC converter. In this scenario, the leftmost curve must be moved toward the rightmost curve until the two curves are matched. The compensation results are shown in Fig. 7.

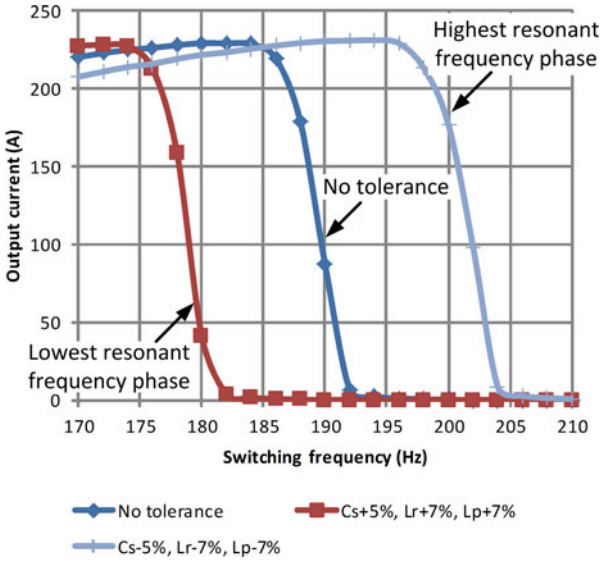

Fig. 10. Output current versus switching frequency curves at different tolerances. Input voltage is 400 V. Output voltage is 12 V. Transformer turns ratio is 18:1.

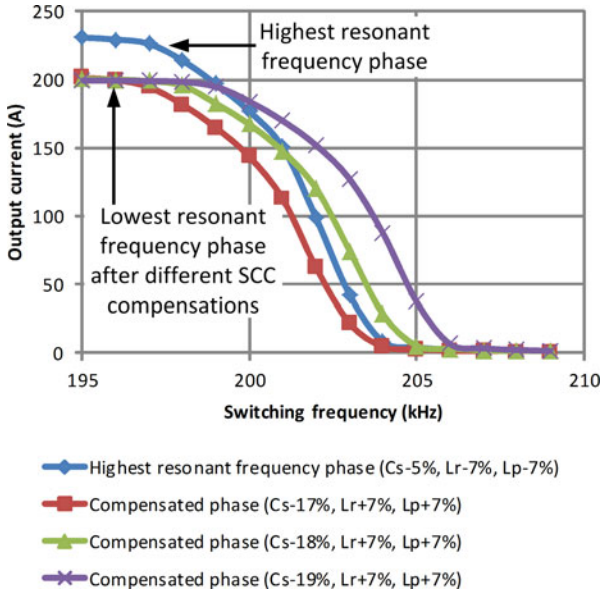

Fig. 11. Output current versus switching frequency curves after compensation. Input voltage is 400 V. Output voltage is 12 V. Transformer turns ratio is 18:1.

Fig. 7 reveals that, from no load to heavy load, the required reduction of C_s to achieve load sharing is almost invariant. In this example, across the entire load range, 17% reduction of C_s always results in lower output current than the highest resonant frequency phase; 18% reduction of C_s results in the closest match of the output currents; and 19% reduction of C_s provides the best match at heavy load. Therefore, in this example, the worst case for SCC design is to achieve 19% reduction of the ideal C_s value.

Above simulation studies are repeated for 300 V input condition and 18:1 turns ratio, respectively. The simulation results are shown in Figs. 8–11. They show that with the same component tolerance values, the required resonant capacitance to achieve load sharing are both 19% reduction from C_s for either 300 V input condition or 18:1 turns ratio, identical to the case studied in Figs. 6 and 7. Therefore, the worst case of SCC design is only affected by the component tolerances, and does not change with input condition and turns ratio.

The aforementioned case studies illustrated the characteristics of load sharing by varying the resonant capacitance. A design method is developed in the next section.

B. Design of Resonant Capacitance Variation Range

The expression of output current can be obtained from (3), and is shown in (6), at the bottom of the page.

Coefficients a, b, and c are defined as the ratios of the actual and ideal component values of L_p, L_r, and C_s, respectively, shown in (7), where the subscript 0 stands for ideal values without tolerances

$$a = \frac{L_p}{L_{p0}},\ b = \frac{L_r}{L_{r0}},\ c = \frac{C_s}{C_{s0}}. \tag{7}$$

Then the inductance ratio becomes

$$K_0 = \frac{L_{p0}}{L_{r0}},\ \text{and}\ K = \frac{L_p}{L_r} = \frac{aL_{p0}}{bL_{r0}} = \frac{a}{b}K_0. \tag{8}$$

And the resonant frequency and switching frequency become

$$\omega_{r0} = \frac{1}{\sqrt{L_{r0}C_{s0}}},\ \text{and}\ \omega_r = \frac{1}{\sqrt{L_rC_s}} = \frac{1}{\sqrt{bL_{r0}\cdot cC_{s0}}} = \frac{1}{\sqrt{bc}}\omega_{r0} \tag{9}$$

$$\omega_s = \omega_n \cdot \omega_{r0} \tag{10}$$

where ω_n is the switching frequency normalized at the ideal resonant frequency ω_{r0}.

Substitute (8), (9), and (10) into (6), then I_o can be expressed as a function of ω_n, a, b, and c, shown in (11), at the bottom of the page. Equation (11) shows that the output current of a

$$I_o = \frac{8V_oN^2\sqrt{2\omega_r^2K\omega_s^2M^2 + 2\omega_r^2\omega_s^2M^2 - \omega_r^4M^2 - \omega_s^4M^2 - K^2\omega_s^4M^2 - 2K\omega_s^4M^2 + K^2\omega_s^4}}{\pi^2\left(\omega_r + \omega_s\right)\left(\omega_r - \omega_s\right)\omega_sL_pM} \tag{6}$$

$$I_o(\omega_n, a, b, c) = \frac{8V_oN^2\sqrt{2aK_0\omega_n^2M^2c - M^2 - \omega_n^4M^2b^2c^2 + 2\omega_n^2M^2bc - a^2K_0^2\omega_n^4M^2c^2 - 2aK_0\omega_n^4M^2bc^2 + a^2K_0^2\omega_n^4c^2}}{\pi^2\omega_{r0}\omega_n aL_{p0}M\left(1 - \omega_n^2bc\right)} \tag{11}$$

given LLC stage is determined by the switching frequency and the component tolerances.

With a good SCC design, after compensating the tolerance of resonant components, the output current of the highest resonant frequency phase and the lowest resonant frequency phase should be the same. Equation (12) can describe such a relation. The left-hand side of (12) is the output current of the highest resonant frequency phase; the right-hand side of (12) is the output current of the lowest resonant frequency phase after SCC compensation. The coefficient q is the ratio of the required equivalent resonant capacitance, C_r, and the ideal series capacitor value, C_{s0}. As shown in Fig. 7, the required q value slightly varies in different load conditions. The minimum value of $q, q_{\min}$, is the worst case scenario for the SCC design, which happens when the corresponding SCC control angle α is minimum.

$$I_o(\omega_n, a_{\min}, b_{\min}, c_{\min}) = I_o(\omega_n, a_{\max}, b_{\max}, q) \qquad (12)$$

where $q = \frac{C_r}{C_{s0}}$ due to SCC modulation.

The expression of q can be derived from (11) and (12). Then its values can be calculated at different switching frequency points. The minimum value of q can be identified accordingly. However, this approach could result in severe overdesign. This is because the equation is based on FHA, which assumes sinusoidal waveforms; but when the LLC converter operates near the peak gain point, the switching frequency is far below the resonant frequency, thus the waveforms are no longer sinusoidal, and consequently, large errors are resulted [37], [39], [40]. Because the $q_{\min}$ always happens at the peak gain point, the FHA approach is less than ideal.

Nevertheless, the FHA-based equation provides good accuracy at a lower gain region. Therefore, the q value at light load condition can be accurately estimated using the FHA-based equations. Also, according to the observations made in the previous section, the required resonant capacitance to achieve load sharing only varies a little from light load to heavy load. Therefore, after the light-load q value is obtained from the FHA-based equation, it is observed by the authors that the heavy load q value can be estimated by subtracting 0.02 from the light load q value for the worst case SCC design. Using the idea described earlier, a visual-assisted design method is proposed as follows.

Still considering the example in Fig. 7, output current curves with different q values are plotted using (11), and shown in Fig. 12. The solid line represents the output current of the highest resonant-frequency phase, which is the reference curve for the SCC compensations.

The first step is to try different q values in (11) and plot output current curves, and then identify the undercompensated curve that is the closest to the reference curve. Fig. 12 shows that when $q = 0.83$, the resultant output current curve is always below the reference curve, meaning that it is undercompensated; whereas the next curve ($q = 0.82$) intersects the reference curve, meaning that it is a critically compensated curve. Above two curves suggest that $q = 0.83$ (C_s-17%) is the undercompensated curve that is the closest to the reference curve. This result is in accordance with the observation made in Fig. 7.

Next, in order to guarantee sufficient SCC compensation at heavy load, $q_{\min} = 0.81$, which corresponds to series capacitance reduction of -19%, is chosen to be the worst case SCC design, which has additional 2% reduction of the series capacitance value based on the undercompensated curve. This result is also in accordance with Fig. 7. Fig. 12 also suggests that the heavy-load compensation curve intersects the reference curve at $\omega_n = 0.71$ (or 164 kHz), which also agrees with the simulation results in Fig. 7.

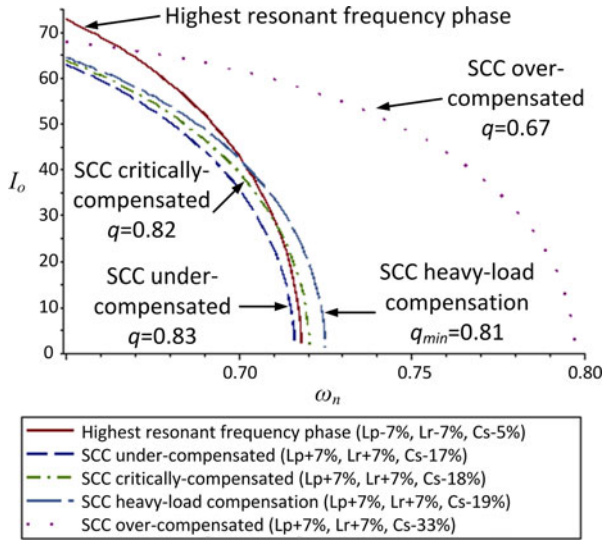

Fig. 12. Visual assisted design method to find $q_{\min}$.

Fig. 12 also provides the output current curve at $q = 0.67$ (C_s-33%), which is obtained by solving (12) directly. It is very far from the reference curve and it is very much overcompensated. This comparison demonstrates the accuracy advantage of the proposed visual-assisted design method.

Above steps derived the resonant capacitance variation range for worst case SCC design. The SCC capacitor value, C_a, is calculated in the next section.

C. Design of Half-Wave SCC Capacitor Value

The half-wave SCC is in series with C_s, therefore the equivalent resonant capacitance is derived by substituting (5) into (2), given in the following equation:

$$C_r = \frac{2C_aC_s\pi}{2C_a\pi + 2C_s\pi - 2C_s\alpha + C_s\sin(2\alpha)}. \qquad (13)$$

The control angle α is from *0* to π, which modulates the resonant capacitance from $C_{r,\min}$ to $C_{r,\max}$. $C_{r,\max}$ occurs at $\alpha = \pi$, which means the SCC MOSFET is always turned ON and the current always bypasses C_a. Therefore, $C_{r,\max}$ equals to C_s. $C_{r,\min}$ occurs at $\alpha = 0$, which means the SCC MOSFET is always turned OFF, and the current always flow through C_a. Therefore, $C_{r,\min}$ equals to C_s and C_a connected in series.

According to the discussion in the previous section, $C_{r,\min}$ must be equal to or smaller than $q_{\min}C_{s0}$ so that it is able to achieve load sharing in the worst case scenario. If $C_{r,\min}$ is smaller than $q_{\min}C_{s0}$, the SCC is overdesigned: the C_a value will be smaller than necessary, and the C_a peak voltage will be higher, and thus the asymmetrical effect discussed in Section

III-B will be severer. For an optimal design of SCC, $C_{r,\min}$ should equal to $q_{\min}C_{s0}$.

In the worst case scenario, C_s has the largest possible tolerance, thus $C_s{=}C_{s0}{\cdot}c_{\max}$. Substituting $C_r{=}q_{\min}C_{s0}, \alpha = 0$, and $C_s{=}C_{s0}{\cdot}c_{\max}$ into (13) gives

$$q_{\min}C_{s0} = \frac{C_a C_{s0} c_{\max}}{C_a + C_{s0} c_{\max}}. \tag{14}$$

Then solving (14) gives the expression of C_a

$$C_{a0} = C_{s0}\frac{c_{\max}q_{\min}}{c_{\max} - q_{\min}} \tag{15}$$

where C_{a0} is the ideal value of C_a.

Considering that the C_a capacitor also has tolerance, the rated C_a capacitor value should be chosen such that its maximum possible value is still smaller than the designed C_{a0} value in (15). Therefore, the implemented C_a capacitor value should be selected according to the following equation:

$$C_{a,\text{rated}} \le \frac{C_{a0}}{e_{\max}} \quad \text{where} \quad e = \frac{C_a}{C_{a,\text{rated}}} \tag{16}$$

where $e_{\max}$ is the maximum ratio of actual C_a value and ideal C_a value due to the component tolerance.

D. Design Procedure

The design procedure of the variable switching frequency half-wave SCC–LLC converter is summarized as follows:

1) Design the LLC power train parameters using existing methods. It is prudent to design the maximum output current higher than the specification. For example, if the required capacitance reduction to achieve load sharing is -20% (as will be obtained in Step 3), the designed maximum output current should be about 20% higher than the specification.
2) Identify the tolerances of the resonant components.
3) Visual-assisted design method: Use (11) to plot the output current curve of the highest resonant frequency phase (reference curve). Still use (11), but substitute the tolerance ratio c with the compensation value q, and plot the compensated output current curve of the lowest resonant frequency phase. Try different q values and visually identify the undercompensated curve that is the closest to the reference curve. Then subtracting a few percent (e.g., 0.02) from the undercompensated q value will give a good estimation of the heavy-load compensation q value, $q_{\min}$.
4) Use (15) and (16) to calculate the implemented C_a capacitor value.

V. Experimental Results

A 600-W two-phase interleaved variable switching frequency half-wave SCC–LLC converter is implemented to verify the feasibility and the advantages of the proposed control strategy. The system block diagram is shown in Fig. 13. The parameters are inTable I.

The resonant inductors are implemented with the transformers' leakage and are intentionally made nonidentical in order to test the load sharing performance. Because Phase 1's inductances are intentionally made smaller, its resonant frequency is higher than Phase 2; therefore, only Phase 2 needs a half-wave SCC to modulate the output current to match Phase 1. Two values of the SCC capacitor are tested in the circuit in order to show the effects of SCC overdesign. The gate driving signals of these two LLC converters operate at 90° phase shift for current ripple cancellation.

A Microchip DSC dsPIC33FJ32GS606 is used to implement the digital controller. A linear optocoupler is used to transmit output voltage signal to the primary side. The output voltage signal is sampled by an ADC, and then subtracted from a reference voltage value to create an error value. The error value is processed by a voltage-loop PI controller and becomes the switching period for both the half-bridge pulse-width modulation (PWM) and the SCC PWM. The phase shift between the two half-bridges is adjusted according to the switching period to maintain 90° phase shift. Two other ADCs are used to sample the resonant capacitor voltage, which reflects the output current level. The load sensing method can be adopted from either [41] or [42]. The load current error between the two phases is processed by a load-sharing PI controller and becomes the duty cycle of the SCC PWM. The SCC duty cycle is multiplied by the switching period and becomes the duty cycle period. The SCC PWM is synchronized with the zero-crossing points of the primary-side resonant current. The zero-crossing detection is implemented using a current transformer and a comparator. The synchronization is implemented using the DSC's external PWM reset function, which allows a logic signal from the current zero-crossing detection circuit to reset the digital PWM. An SCC gating logic circuit is used to turn ON the SCC MOSFET at the SCC voltage zero-crossing points, in order to eliminate the power loss in its body diode [43].

Fig. 14 shows the operation of the half-wave SCC. The SCC MOSFET is turned ON as soon as the SCC voltage returns to zero in order to prevent the MOSFET body diode from carrying current. The SCC MOSFET is always turned ON and OFF at ZVS condition, therefore the switching loss is negligible.

Figs. 15, 16, and 17 demonstrate the effectiveness of current ripple cancellation and load sharing. Small ripple indicates good load sharing performance. A separate 600-W single-phase LLC converter with the same input/output specification and output capacitance has been built for the purpose of comparison.

Fig. 15 shows waveforms of the single-phase LLC converter at 50-A load. The output voltage ripple is 500 mV peak to peak.

Fig. 16 shows waveforms of the SCC–LLC converter with the proposed control strategy at 50-A load. With the same output capacitance, the output voltage ripple is reduced to 210 mV peak to peak. From the resonant current waveforms, it can be seen that the output currents of the two phases are well balanced even though the resonant tanks are intentionally made different. This waveform is obtained when the C_a is 30 nF. It is noticeable that the resonant current of the two half-cycles in Phase 2 are slightly asymmetrical due to the half-wave SCC modulation.

Fig. 17 shows waveforms of the SCC–LLC converter with the proposed control strategy at 50-A load, with the SCC capacitance increased to 155 nF. It is observed that when C_a is larger,

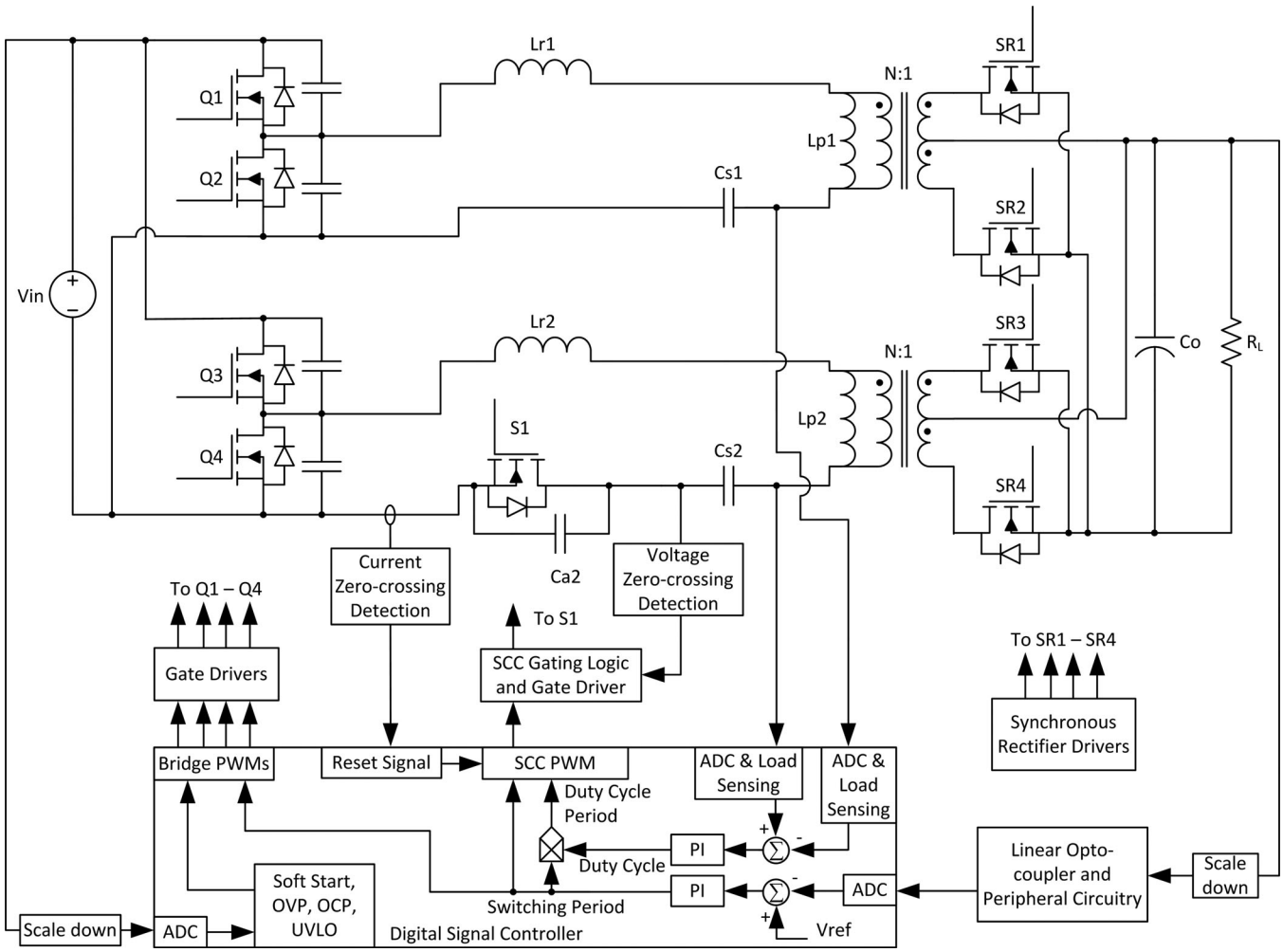

Fig. 13. Implemented two-phase interleaved SCC–LLC converter with the proposed control strategy.

TABLE I
PROTOTYPE PARAMETERS

Switching frequency	Variable around 200kHz
Input Voltage	400V nominal/300V minimum
Output Voltage	12V
Output Power	600W (300W × 2 phases)
Transformer Turns Ratio	20:1, Center tapped
Magnetizing Inductance	87μH(Phase1) 85μH(Phase2)
Resonant Inductance	12μH(Phase1) 14μH(Phase2)
Series Capacitors	36nF±5%
SCC Capacitors	30nF±3% (over-design case) or 155nF±5% (optimal case)
Output Capacitance	1790μF (100μF× 8 + 330μF× 3)
Half-bridge MOSFET	IPB60R190C6
SCC MOSFET	BSC060N10NS3G(100V,6mΩ)
SR MOSFET	BSC011N03LS

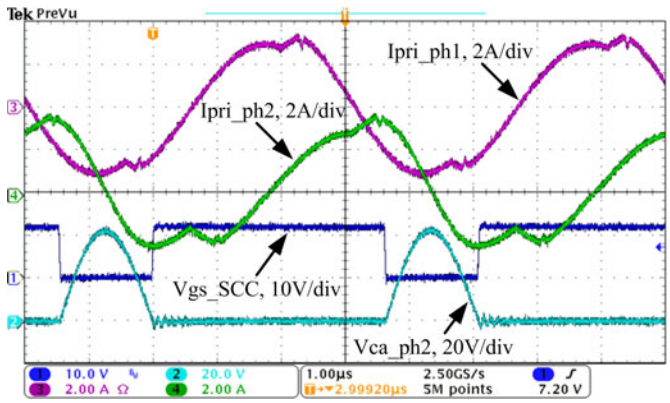

Fig. 14. Operation of half-wave SCC.

the α angle is smaller to achieve the same load sharing task. The SCC voltage amplitude is also significantly lower. As a result, the asymmetrical effect of the resonant current is mitigated, and is almost invisible. The output voltage ripple is further reduced to 130 mV peak to peak. As discussed in Section IV-C, for optimal performance, the C_a value should be as large as possible, but still sufficiently small to achieve load sharing in the worst case scenario.

Fig. 18 shows the efficiency improvement using the phase-shedding technique in the proposed SCC–LLC converter. When the load current is below 50%, one phase is shut down. The 25 A (50%) load efficiency is improved from 94% to above 95.5%, and the 5 A (10%) load efficiency is improved from 81% to 90%.

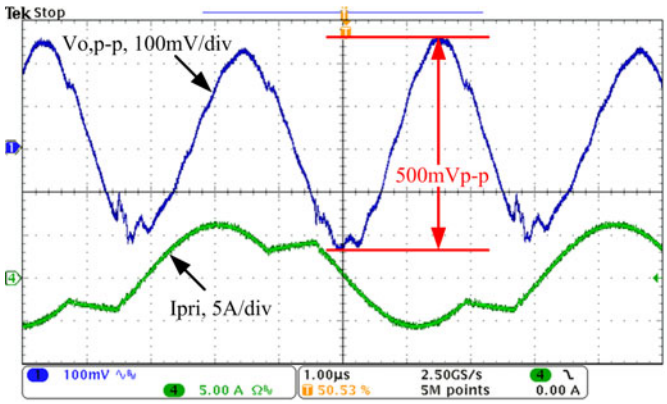

Fig. 15. Output voltage ripple of single-phase LLC converter. $I_o = 50$ A and $C_o = 1790$ μF.

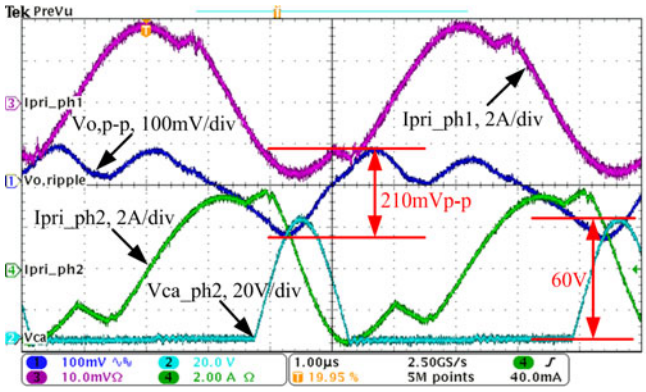

Fig. 16. Output voltage ripple of two-phase interleaved SCC–LLC converter with the proposed control strategy. $I_o = 50$ A, $C_o = 1790$ μF, and $C_a = 30$ nF.

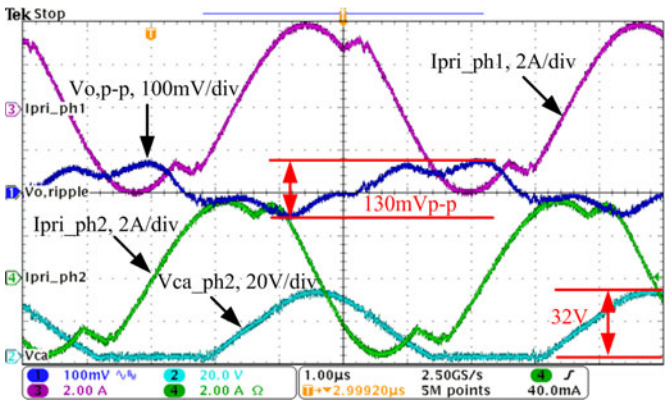

Fig. 17. Output voltage ripple of two-phase interleaved SCC–LLC converter with the proposed control strategy. $I_o = 50$ A, $C_o = 1790$ μF, and $C_a = 155$ nF.

VI. Conclusion

A new control strategy is proposed for interleaved SCC–LLC converters. The switching frequency control is used for voltage regulation; thus, it can provide uncompromised peak gain range and frequency variation range compared to conventional LLC converters. The resonant frequency control is only responsible for load sharing, thus the half-wave SCC can be used to reduce cost and conduction loss. The load sharing characteristic of SCC–LLC converters is studied, and a visual-assisted design method is proposed to determine the optimal SCC capacitance value. A 600-W two-phase interleaved SCC–LLC prototype is built and shows good performances of load sharing, current ripple cancellation, and light-load efficiency improvement.

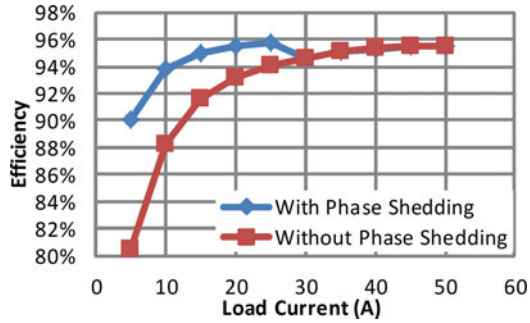

Fig. 18. Efficiency comparison, with and without phase shedding.

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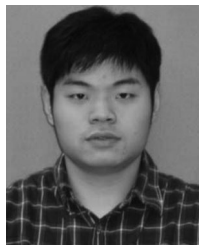

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