Bang–Bang Charge Control for LLC Resonant Converters

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***Abstract*—This paper proposes a Bang–Bang Charge Control (BBCC) method for LLC resonant converters. Instead of switching frequency control, the BBCC method utilizes the series resonant capacitor voltage level to trigger the MOSFETs' switching actions. Advantages of the proposed method include fast dynamic performance and simple implementations. Small-signal analysis shows that the loop bandwidth can achieve around 1/6 of the switching frequency in all operating conditions. Experimental results show that 5 to 25 A load step transients are completed within only seven switching cycles at both 400- and 300-V input-voltage conditions. Practical considerations are also discussed in detail.**

***Index Terms*—Charge control, resonant power conversion, switched-mode power supply, transient response.**

NOMENCLATURE

ABCbits	Number of bits of analog-to-digital converter.
C_j	Charge-equivalent value of MOSFET junction capacitance.
C_o	Output capacitance.
C_s	Series resonant capacitance.
DACbits	Number of bits of digital-to-analog converter.
e	Tolerance of sensing resistors.
$f_{\rm pole}$	Dominant pole frequency of LLC power stage.
f_s	Switching frequency.
F_s	dc operating point of switching frequency.
$\hat{f}_s$	Small-signal variable of switching frequency.
$\rm Gain_{DC}$	dc gain of LLC power stage.
I_o	Load current.
$i_{\rm sec}$	Secondary-side current from output rectifier.
$\hat{i}_{\rm sec}$	Small-signal variable of secondary-side current from output rectifier.
K_a	Partial derivative of $i_{\rm sec}$ with respect to v_o.
K_b	Partial derivative of $i_{\rm sec}$ with respect to $v_{{\rm th}H}$.
K_c	Partial derivative of $i_{\rm sec}$ with respect to f_s.
K_d	Partial derivative of $\hat{f}_s$ with respect to v_o.
K_H	Ratio of minimum $v_{{\rm th}H}$ and sensed $V_{\rm in}$.
$K_{\rm sen}$	Attenuation factor of $V_{\rm in}$ and v_{Cs} in sensing circuit.
K_{Vo}	Sensing gain of output voltage.
L_p	Parallel resonant inductance.
L_s	Series resonant inductance.
N	Transformer turns ratio.
$P_{\rm in}$	Input power.
$q_{\rm DAC}$	Quantization step of digital-to-analog converter.
q_E	Quantization step of per-cycle input energy.
$Q_{\rm net}$	Per-cycle net input charge.
q_Q	Quantization step of per-cycle input charge.
$q_{{\rm th}H}$	Quantization step of BBCC control threshold $v_{{\rm th}H}$.
q_{Vo}	Quantization step of output voltage.
R_L	Load resistance.
s	Laplace variable.
$t_{H\rm off}$	Time point when high-side gate is turned-off.
$t_{L\rm off}$	Time point when low-side gate is turned-off.
$v_{\rm comp}$	Compensated error signal.
v_{Cs}	Series resonant capacitor voltage.
$V_{\rm DAC,max}$	Full-scale range of digital-to-analog converter.
$V_{\rm in}$	Input voltage of LLC converter.
V_o	dc operating point of output voltage.
v_o	Output voltage.
$\hat{v}_o$	Small-signal variable of output voltage.
$V_{\rm ref}$	Reference output voltage in control circuit.
$v_{{\rm th}H}$	BBCC control threshold of high-side gate turn-off point.
$\hat{v}_{{\rm th}H}$	Small-signal variable of $v_{{\rm th}H}$.
$v_{{\rm th}L}$	BBCC control threshold of low-side gate turn-off point.
Z_o	Impedance of output network, including load resistance and output capacitance.

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I. INTRODUCTION

THE LLC resonant topology [1]–[5] emerged in recent years. Its applications now include laptop adaptor [2], [6], flat panel TV [7], [8], LED lighting [9], [10], computer [11]–[13], battery charger [14], photovoltaic energy [15], [16], fuel cell [17], [18], and transportation [19]–[21] among many others. Its main advantages are the high-power efficiency and the integrated magnetic components [22]–[25]. However, the dynamic performance of LLC converters has been unfavorable due to limited bandwidth.

With conventional voltage-mode control, the small-signal characteristics of LLC converters vary with operating conditions. It changes between a first-order system and a second-order system at different gain points [26]–[28]. The second-order scenario puts constraints to the compensator design, and thus limits the loop bandwidth.

Several technologies are proposed to improve the dynamic performance of LLC converters:

Average current-mode control for LLC converters [29], [30] provides constant dynamic performance at different input voltages. However, it only removes the impact of input voltage variation, but does not show significant bandwidth improvement. The maximum achievable bandwidth is limited by two factors: 1) the low-pass filter required by the average resonant current sensing circuit; 2) the current-loop compensator, effectively another low-pass filter.

Sliding-mode control for LLC converters [31] provides fast dynamic performance but sacrifices steady-state performances. It introduces steady-state error and increases output voltage ripple. Also, the method requires sensing ripple current in the output capacitors, which is impractical when the output capacitor bank consists of many distant surface mount capacitors.

Optimal trajectory control [32] based on state-plane analysis can provide very fast dynamic performance for series resonant converters. However, trajectory control for LLC converter is very complicated because of the increased state variables and operation modes. Simplified optimal trajectory control for LLC converters [33] is based on a closed-form solution of the resonance trajectory assuming that the switching frequency equals to the resonant frequency. It provides very fast dynamic performance. However, its limitation is also the resonant frequency assumption, which means at other switching frequencies (e.g., at low-input voltage) the solution is not valid. Also, calculating the optimal trajectory requires the inductor and the load current values; the calculation accuracy is sensitive to the component tolerance and the sensing accuracy. The dc current sensing also causes efficiency loss.

On a different note, charge control is proposed in [34] and [35] as an equivalent of current-mode control. One-cycle control [36] covers a broad range of control methods probably including the charge control. Both methods can be applied to pulse width modulation (PWM) and quasi-resonant converters, but are not suitable for full/half-bridge type resonant topologies. Charge control devices [37], [38] are developed for half-bridge LLC converters. It is a variation of the charge control method, employing a resettable integrator to determine the time length of the first half-cycle, and then making the second half-cycle an equal time length. However, in real world, the resettable integrator implementation is complicated, nonideal, and subject to noise. In addition, during soft start, burst mode, and input voltage fluctuation, the dc component of the resonant capacitor voltage needs to be controlled at $\frac{1}{2}$ of the input voltage for optimal resonance trajectory [33], [39], [40]. Existing charge control methods do not monitor resonant capacitor voltage, thus cannot provide optimal performance.

This paper proposes a Bang–Bang Charge Control (BBCC) method for resonant converters. Instead of switching frequency modulation, the proposed method switches the MOSFETs based on the series resonant capacitor voltage. As will be disclosed later, the series resonant capacitor voltage at the MOSFETs' switching points directly controls the per-cycle input charge. Consequently, the resonant power stage becomes a first-order system, which is favorable to high-bandwidth loop compensation. In addition, the BBCC method forces the resonant tank's trajectory into new steady states within only a few switching cycles, much faster than switching-frequency control methods do, further accelerating the transient response. Comparing to existing control methods, the proposed BBCC method has the following advantages: 1) provides very fast dynamic response in all operating conditions; 2) does not require current sensing, current loop, resettable integrator, or algorithm, thus is simple and suitable for IC integration; 3) does not sacrifice performance, such as steady-state error, output voltage ripple, efficiency, and so on.

Half-bridge LLC resonant converter is used as an example in this paper; but the proposed BBCC method can be extended to other topologies that include a series capacitor. The following sections are organized as follows: Section II explains the operation theory and the control mechanism; Section III provides small-signal analysis; Section IV discusses considerations in digital implementation; Section V demonstrates the experimental results; and Section VI concludes the paper.

II. Proposed BBCC

The proposed BBCC method is based on the physics that the input electric quantity of each switching cycle can be derived from the series resonant capacitor voltage level at the switches' turn-off points. The theory is proposed in [41], and is summarized below. The control mechanism of the proposed BBCC method is described further below in this section.

A. Review of Relationship Between Input Charge and Series Resonant Capacitor Voltage

The series resonant capacitor voltage is an integral of resonant current. In half-bridge topologies, the resonant current is also the input current during the first half-switching-cycle. Therefore, the change of the series capacitor voltage during the first half-cycle reflects the per-cycle input charge. As discussed in [41], the per-cycle input charge can be derived from the series capacitor voltage at the turn-off points of high-side and low-side switches, plus the contribution of the junction capacitances. The relation is expressed in (1), and the consequent input power is derived in (2)

$$Q_{\rm net} = C_s\left[v_{Cs}(t_{H\rm off}) - v_{Cs}(t_{L\rm off})\right] + 2C_j V_{\rm in} \quad (1)$$

$$P_{\rm in} = V_{\rm in} C_s f_s\left[v_{Cs}(t_{H\rm off}) - v_{Cs}(t_{L\rm off})\right] + 2C_j f_s V_{\rm in}^2 \quad (2)$$

where $Q_{\rm net}$ is the net input charge of a switching period, C_s is the series resonant capacitor value, C_j is the junction capacitance, $v_{Cs}(t_{H\rm off})$ is the series capacitor voltage at the high-side switch turn-off point, and $v_{Cs}(t_{L\rm off})$ is the series capacitor voltage at the low-side switch turn-off point. The C_j is a charge-equivalent value of the MOSFET junction capacitance, which can be derived from the MOSFET datasheet. It is the average value of the $C_{\rm oss} - V_{\rm DS}$ curve from 0 V to $V_{\rm in}$ [42].

Because the C_s voltage waveform is symmetrical to $\frac{1}{2}$ of the input voltage, $v_{Cs}(t_{H\rm off})$ and $v_{Cs}(t_{L\rm off})$ have a relation described in (3)

$$\frac{V_{\rm in}}{2} - v_{Cs}(t_{L\rm off}) = v_{Cs}(t_{H\rm off}) - \frac{V_{\rm in}}{2}$$
$$\Rightarrow v_{Cs}(t_{L\rm off}) = V_{\rm in} - v_{Cs}(t_{H\rm off}). \quad (3)$$

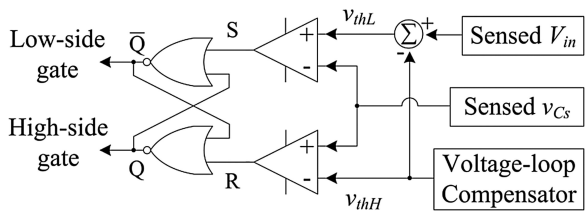

Fig. 1. Simplified structure of the BBCC.

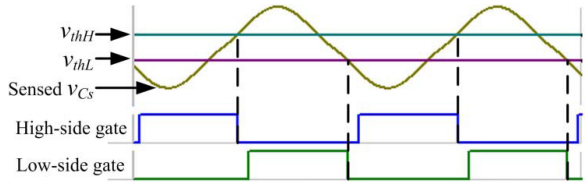

Fig. 2. Operation waveforms of a BBCC-controlled LLC converter.

B. Proposed BBCC Control Method

In order to achieve fast dynamic response, the objective is to control the cycle-by-cycle input charge, so that the resonant power stage can be reduced to a first-order system, favorable for high-bandwidth loop compensation. As discussed previously, the per-cycle input charge is determined by the series resonant capacitor voltage at the switches' turn-off points, namely, $v_{Cs}(t_{H\text{off}})$ and $v_{Cs}(t_{L\text{off}})$. The proposed BBCC method controls two voltage thresholds in the control circuitry, $v_{\text{th}H}$ and $v_{\text{th}L}$, to define the desired $v_{Cs}(t_{H\text{off}})$ and $v_{Cs}(t_{L\text{off}})$ levels. The v_{Cs} waveform is scaled down to signal voltage level, and is then compared with two thresholds. When the sensed v_{Cs} exceeds either threshold, the corresponding switch is turned OFF and the complementary switch is turned ON. As a result, the per-cycle input charge is directly controlled by the thresholds. The simplified structure of the BBCC controller is illustrated in Fig. 1. The operation waveforms are shown in Fig. 2. The description is as follows.

V_{in} and v_{Cs} are both scaled down by the same attenuation factor, K_{sen}, before connected to the BBCC control circuitry. The two thresholds, $v_{\text{th}H}$ and $v_{\text{th}L}$, are generated by the BBCC control circuit. The $v_{\text{th}H}$ is generated by the voltage loop compensator. Because the two thresholds are symmetrical to $\frac{1}{2}$ of V_{in}, the $v_{\text{th}L}$ is generated by subtracting $v_{\text{th}H}$ from the sensed input voltage according to (3). By definition, $v_{\text{th}H}$ and $v_{\text{th}L}$ have the following relation with $v_{Cs}(t_{H\text{off}})$ and $v_{Cs}(t_{L\text{off}})$, respectively:

$$v_{Cs}(t_{H\text{off}}) = K_{\text{sen}} v_{\text{th}H} \tag{4}$$

$$v_{Cs}(t_{L\text{off}}) = K_{\text{sen}} v_{\text{th}L}. \tag{5}$$

Both $v_{\text{th}H}$ and $v_{\text{th}L}$ are compared to the sensed v_{Cs} using two comparators. When the sensed v_{Cs} is below $v_{\text{th}L}$, the set–reset latch (SR latch) is SET, thus the low-side gate is turned off and the high-side gate is turned on. When the sensed v_{Cs} is above $v_{\text{th}H}$, the SR latch is RESET, thus the high-side gate is turned off and the low-side gate is turned on. When the sensed v_{Cs} is between $v_{\text{th}L}$ and $v_{\text{th}H}$, both comparators output logic LOW, and the SR latch maintains the previous state. It is noted that with BBCC control, the switching actions of the LLC converter are triggered by voltage thresholds instead of a controlled switching frequency.

A full diagram of a BBCC-controlled LLC converter is shown in Fig. 3. The input signals include the input voltage, the resonant capacitor voltage, and the output voltage. Comparing to the simplified BBCC controller in Fig. 1, two mono-stable blocks and two AND gates with an inverting input are placed between the comparators and the SR latch. The reasons of adding such elements are discussed below.

C. Practical Issues

1) Light-Load Operation: As discussed in [41], the MOSFETs' junction capacitance has a fixed contribution to the total input charge, which is represented by the second term on the right-hand side of (1). Therefore at light load, when the desired net input charge is less than the fixed input charge contributed by the junction capacitance, the first term on the right-hand side of (1) should be a negative value. This means $v_{\text{th}H}$ must be smaller than $v_{\text{th}L}$—effectively reversing the extra charge back to the source. In this scenario, when the sensed v_{Cs} is between the two thresholds, it is above $v_{\text{th}H}$ and below $v_{\text{th}L}$ at the same time. Then, both comparators will output logic HIGH, causing illegal input combination of the SR latch, and the circuit will malfunction. In order to avoid this problem, mono-stable blocks are placed between the comparators and the SR latch, converting the comparators' positive level signals into positive pulses. The SET pulses and RESET pulses will not happen at the same time. The waveforms of light-load operation are shown in Fig. 4.

2) Robust Operation in Fast Transient and Burst Mode: Even with the mono-stable blocks in place, however, during large transients, when the thresholds and the v_{Cs} are fast changing, a set/reset pulse may be missed due to several reasons, causing the bang–bang operation to stop. For example, when the sensed v_{Cs} is already above the $v_{\text{th}H}$ threshold, but the high-side turn-off pulse is missed, the high-side switch will be kept ON, then the sensed v_{Cs} will run away and never fall below $v_{\text{th}L}$ to trigger the next switching action.

A similar runaway problem happens in burst mode, as illustrated in Fig. 5. During burst-off, $v_{\text{th}H}$ is lower than $v_{\text{th}L}$. The sensed v_{Cs} may be above the $v_{\text{th}H}$ threshold and oscillates around $v_{\text{th}L}$. Each time when the v_{Cs} falls below $v_{\text{th}L}$, it triggers a SET pulse to the SR latch. As a result, when the LLC converter enters burst-on mode, the high-side switch will be turned ON first. Then the sensed v_{Cs} will increase further above the $v_{\text{th}H}$ threshold, and can never fall back and trigger a RESET pulse to turn OFF the high-side switch. Consequently, the switching operation will stop.

In order to ensure robust operation, the two AND gates, along with their inverting inputs, are used to reinforce the input state of the SR latch as shown in Fig. 3: when the sensed v_{Cs} is above both thresholds, the lower AND gate outputs a steady RESET signal to force the high-side switch to turn OFF; and when the sensed v_{Cs} is below both thresholds, the upper AND gate outputs a steady SET signal to force the low-side switch to turn OFF. An illustration of the mechanism is in Fig. 6. During

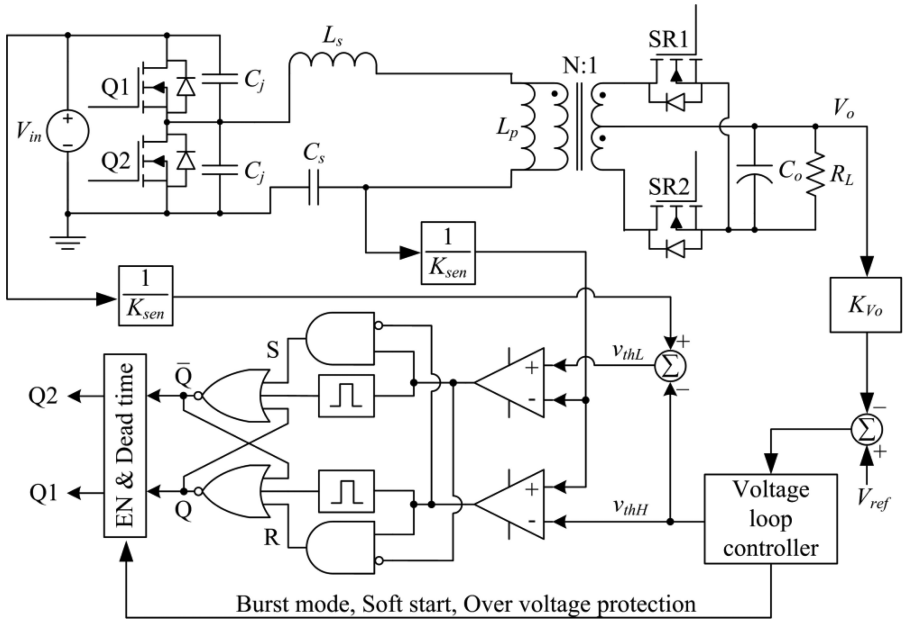

Fig. 3. System diagram of the proposed BBCC control.

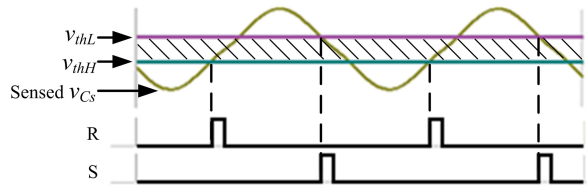

Fig. 4. Light-load operation. When sensed v_{Cs} is within the shadow area, both comparators output logic high.

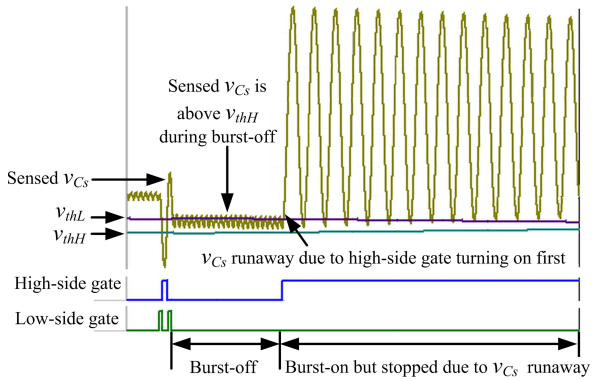

Fig. 5. v_{Cs} runaway problem during burst mode.

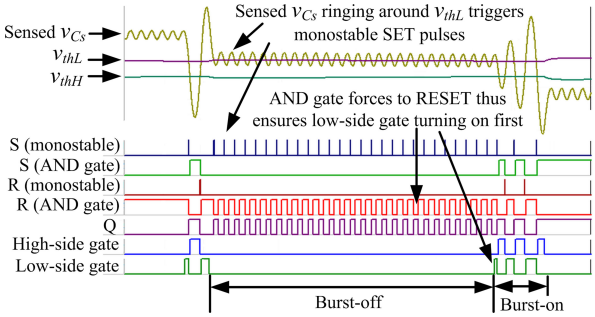

Fig. 6. v_{Cs} runaway problem solved by adding AND gates.

burst-off, the sensed v_{Cs} oscillates around $v_{\mathrm{th}L}$, which generates a series of SET pulses to set the SR latch. However, the AND gate generates a RESET signal once the sensed v_{Cs} is above $v_{\mathrm{th}L}$ (it is always above $v_{\mathrm{th}H}$). This mechanism makes sure that, if the sensed v_{Cs} is above both thresholds when the LLC converter enters burst-on mode, the low-side gate will be turned ON first, and thus the v_{Cs} will decrease instead of run away.

The same mechanism can correct any unexpected output state of the SR latch, thus keeping the switching operation going. With the aforementioned arrangements, the BBCC operation is robust and reliable.

III. Small-Signal Analysis

A. Derivation of Small-Signal Model

The BBCC method directly controls the input charge from the input voltage source in each switching cycle. This is equivalent to programming the input power. Assuming 100% efficiency, the output power equals to the input power; also, the output power is a product of the output voltage, v_o, and the average secondary-side current (the current from the output rectifier to the output capacitor), i_{sec}. Therefore, the large-signal average secondary-side current can be expressed in (6).

After the small-signal expression of i_{sec} is derived, the small-signal expression of the output voltage can be derived using (7), where Z_o is the output network's impedance, as defined in (8). In (8), C_o is the output capacitor, and R_L is the load resistance. From (7), the control-to-output transfer function can be further derived

$$i_{\mathrm{sec}} = \frac{P_{\mathrm{in}}}{v_o} \tag{6}$$

$$\hat{v}_o = Z_o \hat{i}_{\mathrm{sec}} \tag{7}$$

$$Z_o = \frac{R_L}{1 + sC_o R_L}. \tag{8}$$

The aforementioned energy conversion relation is similar to that in boundary-conduction mode Flyback converter, in which the input power is programmed, and the secondary-side current is a function of the input power and the output voltage. Its small-signal analysis is discussed in [43]. A similar approach can apply to BBCC-controlled resonant converters. The derivation process is as follows.

Substituting (2), (3), and (4) into (6), the average secondary-side current can be expressed in (9)

$$i_{\rm sec} = \frac{V_{\rm in} C_s f_s \left(2K_{\rm sen} v_{{\rm th}H} - V_{\rm in}\right) + 2C_j f_s V_{\rm in}^2}{v_o}. \tag{9}$$

When deriving control-to-output transfer function, the input voltage is treated as a constant. Then, the secondary-side current $i_{\rm sec}$ is only affected by $v_o, v_{{\rm th}H}$, and f_s. Its small-signal model can be obtained by linearization around the steady state operation point [43], as derived in (10)

$$\hat{i}_{\rm sec} = K_a \hat{v}_o + K_b \hat{v}_{{\rm th}H} + K_c \hat{f}_s \tag{10}$$

where K_a, K_b, and K_c are partial derivatives defined as follows:

$$K_a = \frac{\partial i_{\rm sec}}{\partial v_o} = -\frac{V_{\rm in} C_s F_s \left(2K_{\rm sen} V_{{\rm th}H} - V_{\rm in}\right) + 2C_j F_s V_{\rm in}^2}{V_o^2} \tag{11}$$

$$K_b = \frac{\partial i_{\rm sec}}{\partial v_{{\rm th}H}} = \frac{2V_{\rm in} C_s F_s K_{\rm sen}}{V_o} \tag{12}$$

$$K_c = \frac{\partial i_{\rm sec}}{\partial f_s} = \frac{V_{\rm in} C_s \left(2K_{\rm sen} V_{{\rm th}H} - V_{\rm in}\right) + 2C_j V_{\rm in}^2}{V_o} \tag{13}$$

where $V_o, V_{{\rm th}H}, F_s$ are the dc operation points of $v_o, v_{{\rm th}H}$, and f_s, respectively.

The output voltage v_o is a function of the switching frequency f_s. Therefore, in small-signal model, f_s can be mathematically expressed as a function of v_o

$$\hat{f}_s = K_d \hat{v}_o. \tag{14}$$

K_d is the partial derivative of f_s with respect to v_o. It takes into account the slight switching frequency variation with respect to the output voltage fluctuation. This amount is related to the resonant tank property, namely, the frequency-versus-gain curve.

It is possible to derive the expression of the frequency-versus-gain curve using fundamental harmonic approximation (FHA) approach, and then further derive the value of K_d. However, the result would be inaccurate if the switching frequency is distant from the resonant frequency [44], [45]. In order to demonstrate the accuracy of the proposed small-signal model, K_d is measured in simulation in this paper.

Substituting (14) and (10) into (7), the small-signal expression of the output voltage is derived in (15)

$$\hat{v}_o = Z_o \hat{i}_{\rm sec} = Z_o \left(K_a \hat{v}_o + K_b \hat{v}_{{\rm th}H} + K_c K_d \hat{v}_o\right). \tag{15}$$

From (15), the small-signal transfer function from $v_{{\rm th}H}$ to v_o is derived in (16)

$$\frac{\hat{v}_o}{\hat{v}_{{\rm th}H}} = -\frac{Z_o K_b}{K_c K_d Z_o + K_a Z_o - 1}. \tag{16}$$

TABLE I
SIMULATION PARAMETERS

Topology	Half-bridge LLC resonant
Input voltage (V_{in})	400V – 300V
Output voltage (V_o)	12V
Transformer turns ratio	20:1
Parallel inductance (L_p)	86 μH
Series inductance (L_s)	12 μH
Series capacitance (C_s)	36 nF
Junction capacitance (C_j)	1 nF
Output capacitance (C_o)	4 mF
Attenuation factor (K_{sen})	125
Switching frequency (f_s)	120kHz – 170 kHz

Substituting (11), (12), (13), and (15) into (16) gives (17)

$$\begin{aligned}\frac{\hat{v}_o}{\hat{v}_{{\rm th}H}} = \frac{2V_o K_{\rm sen} F_s C_s V_{\rm in} R_L}{&-2C_s K_d K_{\rm sen} R_L V_{\rm in} V_o V_{{\rm th}H} - 2C_j K_d R_L V_{\rm in}^2 V_o \\ &+C_s K_d R_L V_{\rm in}^2 V_o + 2C_s K_{\rm sen} R_L V_{\rm in} V_{{\rm th}H} F_s \\ &+2C_j R_L V_{\rm in}^2 F_s - C_s R_L V_{\rm in}^2 F_s + V_o^2 + sC_o R_L V_o^2.\end{aligned} \tag{17}$$

Equation (17), although appears complicated at first glance, only has one pole in the denominator. It reveals that the BBCC-controlled resonant power stage is a first-order system regardless the input voltage and the load current conditions. The pole frequency (in Hz) is derived in (18), and the dc gain (absolute) is derived in (19)

$$\begin{aligned}f_{\rm pole} = \frac{&-2C_s K_d K_{\rm sen} R_L V_{\rm in} V_o V_{{\rm th}H} - 2C_j K_d R_L V_{\rm in}^2 V_o \\ &+C_s K_d R_L V_{\rm in}^2 V_o + 2C_s K_{\rm sen} R_L V_{\rm in} V_{{\rm th}H} F_s \\ &+2C_j R_L V_{\rm in}^2 F_s - C_s R_L V_{\rm in}^2 F_s + V_o^2}{2C_o R_L V_o^2 \pi}\end{aligned} \tag{18}$$

$$\begin{aligned}{\rm Gain}_{\rm DC} = \frac{2V_o K_{\rm sen} F_s C_s V_{\rm in} R_L}{&-2C_s K_d K_{\rm sen} R_L V_{\rm in} V_o V_{{\rm th}H} - 2C_j K_d R_L V_{\rm in}^2 V_o \\ &+C_s K_d R_L V_{\rm in}^2 V_o + 2C_s K_{\rm sen} R_L V_{\rm in} V_{{\rm th}H} F_s \\ &+2C_j R_L V_{\rm in}^2 F_s - C_s R_L V_{\rm in}^2 F_s + V_o^2.\end{aligned} \tag{19}$$

B. Verification of Small-Signal Model

SIMPLIS simulation software is used to verify the above small-signal model. The parameters used in simulation are summarized in Table I.

Open-loop Bode plots for heavy load ($R_L = 0.48\ \Omega$) and light load ($R_L = 2\ \Omega$) at 400- and 300-V input conditions are shown in Fig. 7. As predicted by (17), the transfer function is a first-order system in all operating conditions. The phase delay is 90° up to near the switching frequency, reassuring it is a first-order system. A double-pole is observed at the switching frequency, which is not included in the derived small-signal model. The related discussion is further below in this section. Since the double-pole stays at the switching frequency, it does not impose complexity in loop compensation.

In order to verify the accuracy of the derived small-signal model, the calculated Bode plots using (17) is shown in Fig. 8. Comparisons of calculated and simulated dc gains and pole frequencies are summarized in Table II and Table III. When using (17), (18), and (19) for calculation, the dc operation points of f_s and K_d are obtained from simulation. The dc point of $v_{{\rm th}H}$

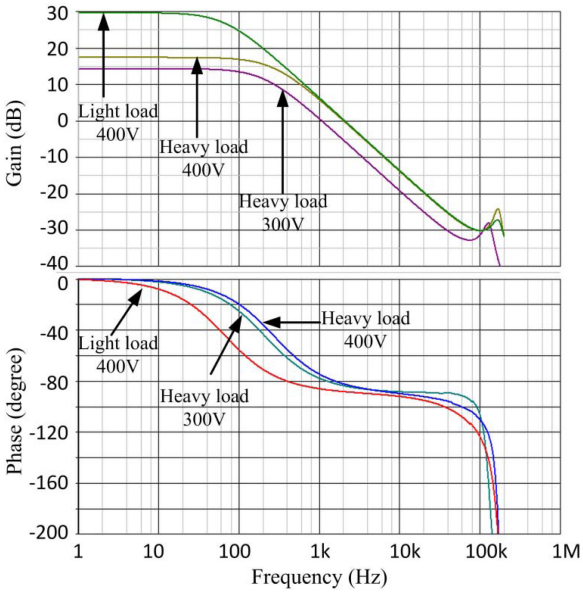

Fig. 7. Simulated Bode plots of BBCC-controlled LLC converter from $v_{\mathrm{th}H}$ to v_o.

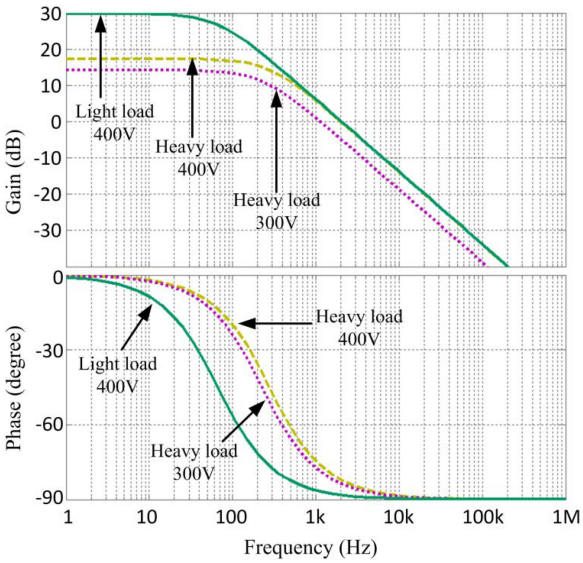

Fig. 8. Calculated control-to-output Bode plots using (17).

TABLE II
COMPARISON OF CALCULATED AND SIMULATED DC GAINS

	DC gain	
Operating condition	***Calculation***	***Simulation***
400V light load	29.8 dB	29.5 dB
400V heavy load	17.3 dB	17.3 dB
300V heavy load	14.2 dB	14.2 dB

TABLE III
COMPARISON OF CALCULATED AND SIMULATED POLE FREQUENCIES

	Pole frequency	
Operating condition	***Calculation***	***Simulation***
400V light load	66.3 Hz	67.2 Hz
400V heavy load	276.7 Hz	270.1 Hz
300V heavy load	226.1 Hz	207.7 Hz

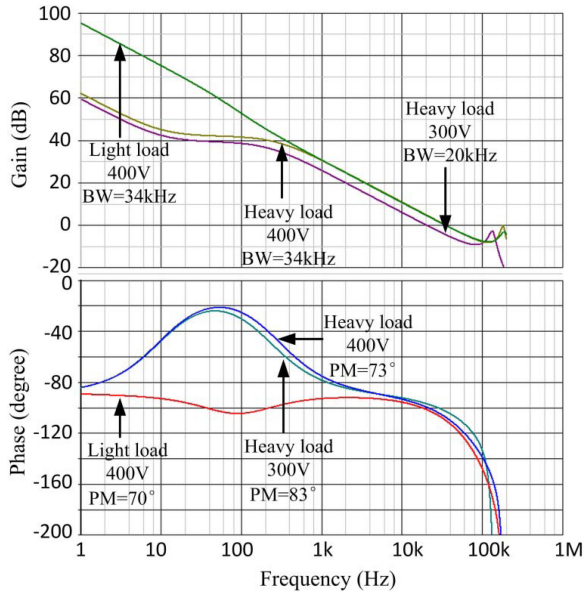

Fig. 9. Simulated Bode plots of BBCC-controlled LLC converter after compensation.

can be measured in simulation as well, or calculated from (20)

$$V_{\mathrm{th}H} = \frac{1}{K_{\mathrm{sen}}}\left(\frac{V_o^2}{2R_L F_s V_{\mathrm{in}} C_s} + \frac{V_{\mathrm{in}}}{2} - \frac{C_j}{C_s}V_{\mathrm{in}}\right). \quad (20)$$

Fig. 8, Table II, and Table III demonstrate that the derived small-signal model is highly consistent with the simulation results; only the double-pole at the switching frequency is neglected.

C. Compensator Design

From the Bode plots, it is observed that the gain and phase curves in all operating conditions are very close to each other from kilo-hertz frequency range to the adjacency of the switching frequency. If the cross-over frequency is placed in this window, optimal loop compensation can be achieved for all operating conditions.

Taking advantage of the first-order system, a simple Type-2 or a PI controller is sufficient to compensate the BBCC controlled resonant converter. The compensation zero should be placed to compensate the lowest pole frequency as the worst-case scenario. The Bode plots of the compensated system using Type-2 compensation are simulated using SIMPLIS software and shown in Fig. 9. In this example, the compensation zero is placed at 10 Hz. A high-frequency pole is placed at 400 kHz, which is intentionally left outside the frequency-of-interest to mimic the behavior of a PI controller.

The compensation results in Fig. 9 are summarized in Table IV. It shows that the maximum bandwidth can achieve 34 kHz at 400-V input condition, and 20 kHz at 300-V input condition. In both cases, the bandwidths have achieved 1/6 of their switching frequencies, respectively. Also, the gains at 100 Hz are above 40 dB in all conditions, which is sufficient to attenuate input voltage ripple from the upstream PFC stage.

TABLE IV
COMPENSATION RESULTS SHOWN IN FIG. 9

Operating condition	Bandwidth	Phase margin
400V light load	34 kHz	70°
400V heavy load	34 kHz	73°
300V heavy load	20 kHz	83°

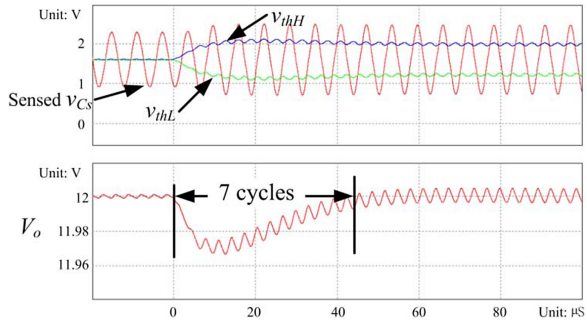

Fig. 10. Load step from 5 to 25 A (400-V input).

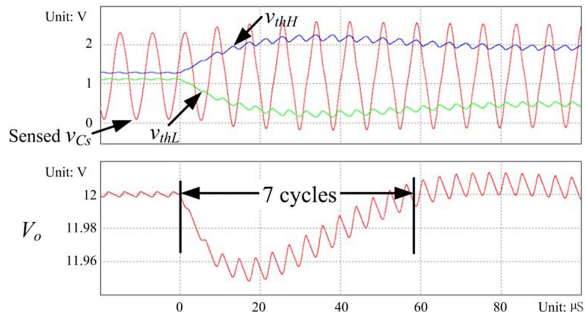

Fig. 11. Load step from 5 to 25 A (300-V input).

Transient responses simulated at 400- and 300-V input voltages are shown in Fig. 10 and Fig. 11. The output voltage is recovered within seven switching cycles in both cases (44 and 58 μs, respectively) using the same compensator. It demonstrates that the BBCC control can provide very fast dynamic performance across the entire input voltage range (300 V–400 V). The ripples on the threshold signals are due to the output voltage ripple feeding into the high-bandwidth compensator. It can be removed if use synchronized sampling (digital sampling or analog sample-and-hold).

D. Discussions on Resonant Tank Behavior

It is noted that, the small-signal model derived in this section is not topology-specific. It does not include the resonant component values except C_s. Also, it does not include the high-order behavior of the resonant tank, which is the double-pole observed in Fig. 7. The reason is discussed as follows.

Although all the resonant components are state variables, the end result is the output power. The BBCC method directly controls the input energy in every switching cycle. Because the resonant components are not energy transfer components and they operate in resonance mode, their total stored energy only changes a little at different operating conditions. If the energy variation in the resonant tank is neglected, the input power always equals to the output power. Therefore, when the BBCC

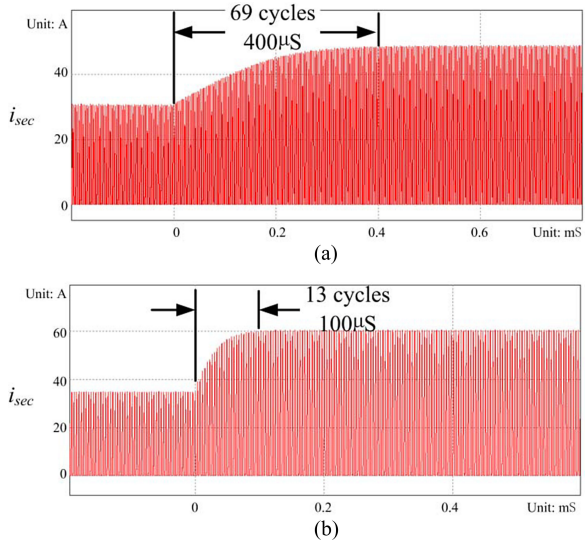

Fig. 12. Step response of switching-frequency control, resulting in average secondary-side current changing from 10 to 20 A. $V_o = 12$ V. (a) $V_{\rm in} = 400$ V. f_s changes from 171 482 to 171 321 Hz; (b) $V_{\rm in} = 300$ V. f_s changes from 132 573 to 131 596 Hz.

method controls the cycle-by-cycle input energy, the resonant power stage delivers approximately the same amount of power to the output port, even before the resonant tank enters steady state. Therefore, from output power point of view, the resonant tank disappears from the small-signal transfer function in low-medium frequency range. Consequently, the energy transfer relation in (9) dominates the low-medium frequency response, which is not topology specific.

In comparison, switching frequency modulation does not guarantee per-cycle output energy. The output power depends on the resonant tank state. After a step change of the switching frequency, the resonant tank takes many switching cycles to reach the desired output power level. The transition time is long, and notably varies in different operating conditions. This long transition time is topology-related, and affects the low-frequency dynamic response.

Simulation waveforms in Fig. 12 and Fig. 13 can illustrate the aforementioned insights.

Figs. 12 and 13 show open-loop step responses of switching-frequency controlled and BBCC-controlled LLC converters, respectively. The same power train parameters in Table I are used in simulation. A step change is applied to the control signals such that the average secondary-side current is changed from 10 to 20 A. The output voltage is set to 12 V. Fig. 12 shows that with switching-frequency control, the average secondary-side current takes 69 and 13 cycles to reach 20 A, at 400 and 300-V input voltages, respectively. Fig. 13 shows that with BBCC control, although it takes six and five cycles to enter steady state at 400- and 300-V input voltages, respectively, the average secondary-side current immediately reaches 20 A after the step change.

Above simulation studies reveal that, the BBCC-controlled LLC converter can be seen as a fast programmed power source up to high frequency range (close to switching frequency), thus

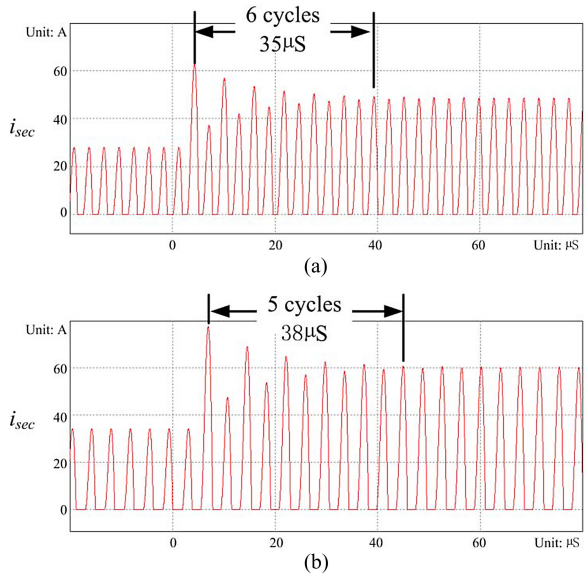

Fig. 13. Step response of BBCC control, resulting in average secondary-side current changing from 10 to 20 A. $V_o = 12$ V. (a) $V_{\rm in} = 400$ V. $v_{{\rm th}H}$ changes from 1.703 to 1.898 V; (b) $V_{\rm in} = 300$ V. $v_{{\rm th}H}$ changes from 1.465 to 1.807 V.

the high-order resonant tank property is not shown in the low-medium frequency small-signal model.

In addition to the charge control advantage discussed previously (i.e., equivalent to a fast programmed power source), the BBCC method also inherently features trajectory control advantage: the control thresholds $v_{{\rm th}H}$ and $v_{{\rm th}L}$ also define the steady-state operation of the resonant capacitor voltage. The time durations of the two half-cycles are not necessarily identical during dynamic operation. By controlling the resonant capacitor voltage at the MOSFETs' turn-off points, the BBCC method forces the resonant tank to enter the new steady state via a much shorter trajectory than the switching-frequency control methods do. The comparison in Figs. 12 and 13 can illustrate the aforementioned insight: the BBCC method takes only six and five switching cycles to settle in the new steady state, whereas the switching-frequency control method takes 69 and 13 cycles to settle. The fast transition time of BBCC also makes the resonant tank disappear in the low-medium frequency small-signal model.

Comparing to the simplified optimal trajectory control method in [33], the BBCC method only provides a suboptimal trajectory, because the controller does not calculate the new steady state. However, it uses a fast feedback loop to approach the new steady state; in return it does not need to sense the load current, or to know the component value. More importantly, it is applicable to the entire switching frequency range.

E. Discussions on Impact of MOSFET Junction Capacitance

The junction capacitance value C_j is an estimated value. It contributes a fixed amount of power as described in (2). Therefore, it is of interest to understand its impact on the system performance. A case study based on quantitative analysis is provided as follows.

TABLE V
COMPARISON OF CALCULATED DC GAINS WITH AND WITHOUT C_j TERM

	DC gain		
Operating condition	***Accurate Calculation***	***Assume Cj=0***	***Difference***
400V light load	29.8 dB	36.2 dB	6.4 dB
400V heavy load	17.3 dB	18.5 dB	1.2 dB
300V heavy load	14.2 dB	14.6 dB	0.4 dB

TABLE VI
COMPARISON OF CALCULATED POLE FREQUENCIES WITH AND WITHOUT C_j TERM

	Pole frequency		
Operating condition	***Accurate Calculation***	***Assume Cj=0***	***Difference***
400V light load	66.3 Hz	31.6 Hz	34.7 Hz
400V heavy load	276.7 Hz	241.8 Hz	34.9 Hz
300V heavy load	226.1 Hz	215.1 Hz	11.0 Hz

When $C_j = 1$ *n*F, at 200-kHz switching frequency and 400-V input voltage, the C_j related input power is

$$P_{Cj} = 2C_j f_s V_{\rm in}^2 = 2 \cdot 1\ n{\rm F} \cdot 200\ {\rm kHz} \cdot (400\ {\rm V})^2 = 64\ {\rm W}. \tag{21}$$

Therefore, when the load is below 64 W, the $v_{{\rm th}H}$ threshold must be lower than the $v_{{\rm th}L}$ threshold, as discussed in Section II-C.

Comparisons of calculated dc gains and pole frequencies with and without the C_j term can reveal its impact on system performance. The comparisons are based on the same parameters in Table I. The comparison results are summarized in Tables V and VI.

The comparisons in Tables V and VI show that the light-load performance is notably affected by the C_j value, but not so at low-input voltage and heavy load. However, even though the impact is notable, the errors of 6-dB dc gain and 35-Hz pole frequency would have little impact to the compensator design and system stability. Besides, if the MOSFET datasheet is available, the estimation will be very good. As a conclusion of the case study, the estimation of the C_j value will have notable impact to the light-load performance, but it can be easily resolved.

F. Input Voltage Step Response

In practice, the input source of a LLC converter is usually a large dc-link capacitor. Therefore, a real input voltage step cannot happen in reality. For completeness, simulated dynamic responses to input voltage step are provided below. Figs. 14 and 15 show 400- to 300-V input voltage step at 5- and 25-A load conditions, respectively. The power train parameters are the same in Table I. The simulation results demonstrate that, with such a drastic input voltage step change, the output voltage generally recovers in 100 μs (or 13 cycles), and the resonant tank settles in the new steady state within 200 μs (or 26 cycles). The output voltage deviation is about 20 mV (0.17%) at light-load condition and 50 mV (0.42%) under heavy load condition. The fast response is due to the high bandwidth of the BBCC control loop.

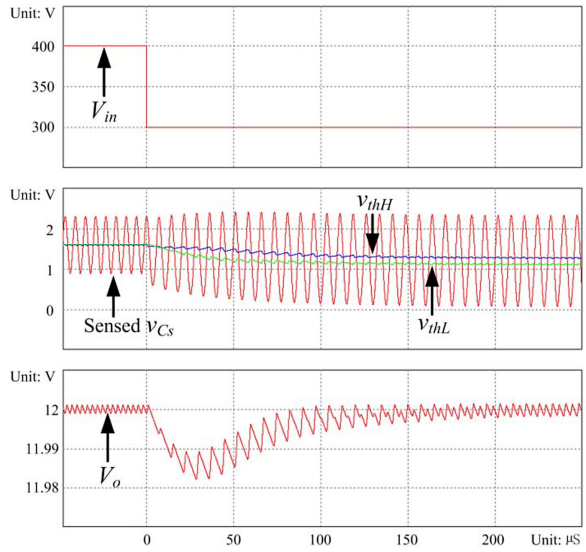

Fig. 14. Input voltage step from 400 to 300 V (5-A load).

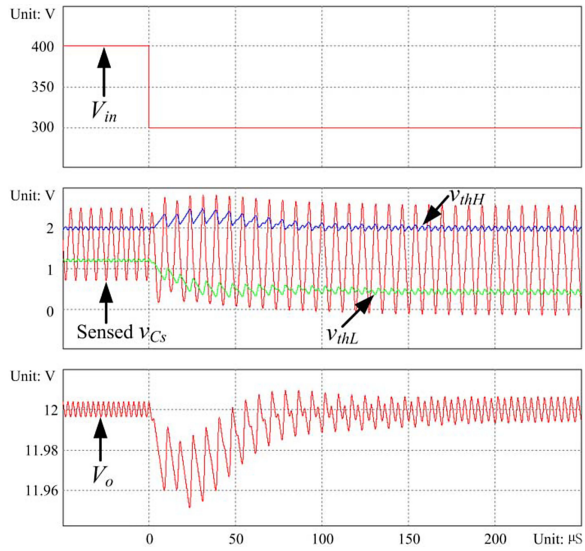

Fig. 15. Input voltage step from 400 to 300 V (25-A load).

IV. Considerations in Digital Implementation

The proposed BBCC method is suitable for both digital and analog circuit implementations.

The digital implementations are better suitable for relatively low switching frequency applications (several hundred kHz). When the control loop bandwidth is very high with respect to the switching frequency, the compensator does not provide sufficient attenuation for noise signals at the switching frequency; thus, the output voltage ripple signal will appear on the compensated error signal, degrading the performance. Digital control has advantages in sampling synchronization and oversampling which can easily remove the ripple. However, special considerations are needed due to the limited resolution and computing speed.

Analog implementations are better suitable for high switching frequency applications (MHz range). Analog controllers have unlimited resolution and can work well beyond MHz range. With a reasonable output capacitor size, the output voltage ripple can be made small at high switching frequency, thus it may not need treatment. Besides, analog sample-and-hold is also available to solve the ripple problem.

In this section, considerations in DSP-based BBCC implementations are discussed.

The diagram of the proposed digital BBCC controller is in Fig. 16. The operation and design considerations are discussed as follows.

A. Design of Amplifier Circuit

The DSP uses a digital-to-analog converter (DAC) to convert the PI calculation result into an analog voltage signal. The DAC output voltage range is from 0 to its reference voltage. However, the minimum $v_{\mathrm{th}H}$ voltage, $V_{\mathrm{th}H,\min}$, is near $\frac{1}{2}$ of the sensed V_{in}. Therefore, in order to maximize the utilization of the DAC quantization levels, the $v_{\mathrm{th}H}$ voltage is derived from summing $V_{\mathrm{th}H,\min}$ and the DAC output voltage, v_{comp}, as shown in Fig. 16. This way, all the DAC quantization levels can be utilized.

The $V_{\mathrm{th}H,\min}$ corresponds to zero input charge. It can be derived as follows.

At no load, the expression of input power can be derived from (2), (3), and (4), shown in (22)

$$P_{\mathrm{in}} = 0 = V_{\mathrm{in}} C_s f_s \left(2K_{\mathrm{sen}} V_{\mathrm{th}H,\min} - V_{\mathrm{in}}\right) + 2C_j f_s V_{\mathrm{in}}^2. \tag{22}$$

Then, the $V_{\mathrm{th}H,\min}$ can be derived in (23)

$$V_{\mathrm{th}H,\min} = \frac{V_{\mathrm{in}}(C_s - 2C_j)}{2K_{\mathrm{sen}} C_s} = K_H \frac{V_{\mathrm{in}}}{K_{\mathrm{sen}}}$$
$$\text{where } K_H = \frac{C_s - 2C_j}{2C_s} = \frac{1}{2} - \frac{C_j}{C_s}. \tag{23}$$

The coefficient K_H is the ratio of $V_{\mathrm{th}H,\min}$ and the sensed V_{in} voltage. The sensed V_{in} voltage is available in the control circuit. The $V_{\mathrm{th}H,\min}$ voltage can be generated by a resistor divider.

B. Attenuation Factor K_{sen}

The selection of K_{sen} should maximize the utilization of DAC quantization levels. The maximum swing range of $v_{Cs}(t_{H\mathrm{off}})$ should be identified by simulation or by (24)

$$V_{\mathrm{th}H,\max} K_{\mathrm{sen}} = \frac{P_{o,\max} - 2V_{\mathrm{in},\min}^2 C_j f_{s,\min}}{2V_{\mathrm{in},\min} f_{s,\min} C_s} + \frac{V_{\mathrm{in},\min}}{2} \tag{24}$$

where $P_{o,\max}$ is the maximum output power; $V_{\mathrm{in},\min}$ is the minimum input voltage; $f_{s,\min}$ is the lowest switching frequency.

The maximum swing range of v_{comp} can be expressed in (25)

$$V_{\mathrm{comp},\max} = V_{\mathrm{th}H,\max} - \frac{V_{\mathrm{in}}}{K_{\mathrm{sen}}} K_H. \tag{25}$$

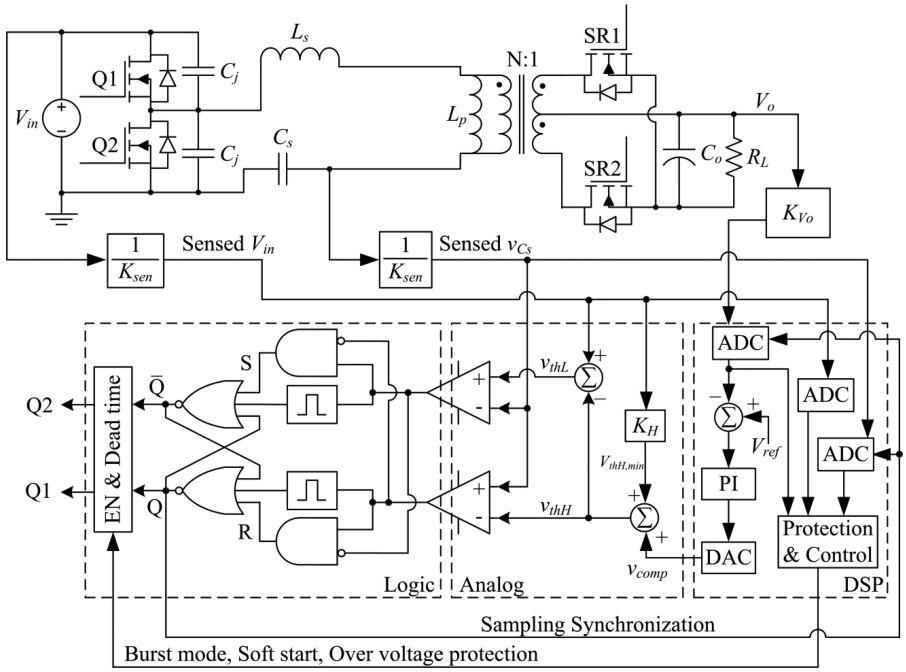

Fig. 16. Digital implementation of the proposed BBCC controller.

Combining (24) and (25) gives

$$K_{\rm sen} = \frac{1}{V_{\rm comp,max}} \left(\frac{P_{o,\max} - 2V_{\rm in,min}^2 C_j f_{s,\min}}{2V_{\rm in,min} f_{s,\min} C_s} + \frac{V_{\rm in,min}}{2} - V_{\rm in,min} K_H \right). \quad (26)$$

Substitute $V_{\rm comp,max} = V_{\rm DAC,max}$ in to (26), which means the $v_{\rm comp}$ voltage range is equal to the DAC full-scale range, then all the DAC quantization levels can be utilized. The $K_{\rm sen}$ value can be calculated accordingly. This is the minimum value for $K_{\rm sen}$. If smaller, the DAC cannot provide enough modulation range for the rated power. If larger, the DAC quantization levels are not fully utilized.

In addition to maximizing the DAC resolution, the $K_{\rm sen}$ should be large enough to scale down all the voltage signals into the range of the analog circuit.

C. DAC Resolution to Avoid Limit-Cycle Oscillation

The control signal, $v_{\rm comp}$, is quantized by DAC, and the output voltage is quantized by analog-to-digital converter (ADC). One criterion to avoid limit-cycle oscillation is that, the DAC controlled output-voltage quantization step must be finer than the ADC sampled output-voltage quantization step [46].

The required output voltage accuracy is usually defined by the design specification, which in turn determines the required ADC resolution. Consequently, the DAC must provide a finer resolution to control the output voltage. However, the DAC only controls input charge; for the same input charge, the input energy is determined by input voltage; and for the same amount of energy, the output voltage is determined by the load current. Therefore, the DAC controlled output voltage quantization step varies with input voltage and load current. The worst-case scenario happens at minimum load current and maximum input voltage. The following derivation calculates the required DAC resolution.

The required output voltage resolution is given by the design specification. The ADC resolution and the sensing gain should be selected accordingly to meet or exceed the specification. Once the ADC and the sensing gain are selected, the output voltage quantization step can be calculated accordingly

$$q_{Vo} = \frac{V_{\rm ADC,max}}{2^{\rm ADCbits} K_{Vo}} \quad (27)$$

where q_{Vo} is the quantization step of the output voltage; K_{Vo} is the sensing gain of V_o; $V_{\rm ADC,max}$ is the ADC full-scale range.

To provide the aforementioned output voltage quantization step in the worst case (at the minimum output current), the per-cycle energy quantization step is determined by

$$q_E = \frac{q_{Vo} I_{o,\min}}{f_{s,\max}} \quad (28)$$

where q_E is the quantization step of the per-cycle energy; $I_{o,\min}$ is the minimum load current before entering burst mode; $f_{s,\max}$ is the switching frequency corresponding to $I_{o,\min}$, which is also the maximum switching frequency of the converter.

To provide the aforementioned per-cycle energy quantization step in the worst case (at the maximum input voltage), the per-cycle input charge quantization step is determined by

$$q_Q = \frac{q_E}{V_{\rm in,max}}. \quad (29)$$

To provide the aforementioned per-cycle input charge quantization step, the quantization step of $v_{{\rm th}H}$ is determined by

$$q_{{\rm th}H} = \frac{q_Q}{2C_s K_{\rm sen}}. \quad (30)$$

The DAC quantization step should be finer than the $q_{\mathrm{th}H}$ value to avoid limit-cycle oscillation, therefore

$$q_{\mathrm{DAC}} = \frac{q_{\mathrm{th}H}}{2}. \tag{31}$$

Then, the required DAC bits can be calculated by (32)

$$\mathrm{DACbits} = \mathrm{ceil}\left(\log_2\left(\frac{V_{\mathrm{DAC,max}}}{q_{\mathrm{DAC}}}\right)\right) \tag{32}$$

where $V_{\mathrm{DAC,max}}$ is the DAC full-scale range.

D. Sensing Resistor Precision

The same attenuation factor K_{sen} is used to scale down both the input voltage and the C_s voltage. The purpose of sensing the input voltage, in addition to the input over/under-voltage protections, is to derive the $v_{\mathrm{th}L}$ threshold based on the $v_{\mathrm{th}H}$ threshold, such that the two thresholds are always symmetrical to the dc component of the C_s voltage. If the two sensing gain blocks have a small mismatch, the two control thresholds will not be perfectly symmetrical. The result is slightly unbalanced output current of the two half-cycles. Therefore, the required sensing resistor precision must be investigated.

The sensing gain blocks utilize resistive dividers, which consists of two resistors. The upper arm is defined as R_a, and the lower arm is defined as R_b. Then, K_{sen} can be expressed as

$$K_{\mathrm{sen}} = \frac{R_a + R_b}{R_b}. \tag{33}$$

From (33), R_a can be expressed as a function of R_b

$$R_a = R_b\left(-1 + K_{\mathrm{sen}}\right). \tag{34}$$

Assuming the resistors have a tolerance of $\pm e$, the worst-case mismatch of the two sensing gain blocks happens when

$$K_{\mathrm{sen1}} = \frac{R_a(1+e) + R_b(1-e)}{R_b(1-e)} \tag{35}$$

$$K_{\mathrm{sen2}} = \frac{R_a(1-e) + R_b(1+e)}{R_b(1+e)} \tag{36}$$

where K_{sen1} and K_{sen2} are nonideal attenuation factors of the sensing gain blocks.

The ratios of the nonideal K_{sen} and the ideal K_{sen} are

$$\frac{K_{\mathrm{sen1}}}{K_{\mathrm{sen}}} = \frac{R_a\left(1+e\right) + R_b\left(1-e\right)}{\left(1-e\right)\left(R_a + R_b\right)} \tag{37}$$

$$\frac{K_{\mathrm{sen2}}}{K_{\mathrm{sen}}} = \frac{R_a\left(1-e\right) + R_b\left(1+e\right)}{\left(1+e\right)\left(R_a + R_b\right)}. \tag{38}$$

Substituting (34) into (37) and (38) gives

$$\frac{K_{\mathrm{sen1}}}{K_{\mathrm{sen}}} = -\frac{K_{\mathrm{sen}}e - 2e + K_{\mathrm{sen}}}{\left(-1+e\right)K_{\mathrm{sen}}} \tag{39}$$

$$\frac{K_{\mathrm{sen2}}}{K_{\mathrm{sen}}} = -\frac{K_{\mathrm{sen}}e - 2e - K_{\mathrm{sen}}}{\left(1+e\right)K_{\mathrm{sen}}}. \tag{40}$$

Considering that surface mount resistors usually have less than $\pm 1\%$ tolerance, thus $K_{\mathrm{sen}} \gg e$. Therefore, the aforementioned equations can be simplified to

$$\frac{K_{\mathrm{sen1}}}{K_{\mathrm{sen}}} = -\frac{1+e}{-1+e} \tag{41}$$

$$\frac{K_{\mathrm{sen2}}}{K_{\mathrm{sen}}} = -\frac{-1+e}{1+e}. \tag{42}$$

Then, the mismatch of the two sensing gain blocks is

$$\frac{K_{\mathrm{sen1}}}{K_{\mathrm{sen2}}} = \frac{\left(1+e\right)^2}{\left(-1+e\right)^2}. \tag{43}$$

If choose resistors with $\pm 1\%$ tolerance, substituting $e = 0.01$ into (43) gives

$$\frac{K_{\mathrm{sen1}}}{K_{\mathrm{sen2}}} = 1.04. \tag{44}$$

It means that the two sensing blocks will have a maximum mismatch of 4%. When input voltage is 400 V, the low-side gate turn-off point could be as high as 16 V off the desired value. This asymmetrical threshold will cause notable unbalanced current in the two half-cycles.

If choose resistors with $\pm 0.1\%$ tolerance, substituting $e = 0.001$ into (43) gives

$$\frac{K_{\mathrm{sen1}}}{K_{\mathrm{sen2}}} = 1.004. \tag{45}$$

It means that the worst-case mismatching is only 0.4%. When input voltage is 400 V, the low-side gate turn-off point will be 1.6 V off the desired value. The asymmetry effect is negligible.

Based on the aforementioned analysis, sensing resistors with $\pm 0.1\%$ tolerance are recommended.

If implemented in integrated circuits, these sensing resistors can be made by the same process, deposited on the same substrate, and trimmed to the same value to achieve optimal matching.

E. Comparator Hysteresis

The hysteresis of the comparators creates a fixed offset to the threshold voltages $v_{\mathrm{th}H}$ and $v_{\mathrm{th}L}$. Their effects are discussed as follows.

If the two comparators have the same hysteresis, the offset voltage becomes a part of the threshold voltage, and is automatically compensated by the closed-loop feedback system, thus has no impact to the system performance. It is recommended to have the two comparators in a single package, thus the two comparators have closely matched hysteresis.

If the two comparators have different hysteresis, the offset voltages on the thresholds $v_{\mathrm{th}H}$ and $v_{\mathrm{th}L}$ will be different. Consequently, they will be imperfectly symmetrical to the DC component of the v_{Cs}. However, calculation shows that the effect of the hysteresis is negligible.

For example, Linear Technology LT1712 contains two comparators in a single package. The hysteresis is 0.5 mV typical. Assuming the DAC full-scale range is 1.6 V, the hysteresis voltage only counts for 0.5 mV/1600 mV = 0.03% of the control signal range. This is completely negligible.

Even if use a low-cost comparator with typically 6-mV hysteresis, comparing to the 1.6-V DAC output voltage range, the

hysteresis voltage only counts for 6 mV/1600 mV $= 0.38\%$ of the control signal range. The mismatch between the two comparators will be even smaller. Therefore, it is again negligible.

In conclusion, the comparator hysteresis has no impact to the system performance if the two comparators are matched; and has negligible impact if the two comparators are not matched. For the best performance, matched, low-hysteresis comparators are recommended.

F. Devices' Speed Limits

As discussed at the beginning of this section, digital BBCC and analog BBCC are suitable for different switching frequency ranges. Therefore, it is of interest to estimate the limits of both solutions.

1) Speed of Digital Devices: The DSP consumes the longest time during the loop execution. Taking Microchip dsPIC33F family DSCs as an example:

The maximum CPU speed is 50 MIPS. Assuming the routine PI algorithm and monitoring functions have 50 instructions, the total computing time is 1 μs.

The successive approximation ADC (SAR) takes two-ADC clock cycles for sampling and 14-ADC clock cycles for analog-to-digital conversion. An ADC clock cycle is 35.8 ns minimum. Therefore, the ADC consumes approximately 0.6 μs.

The DAC takes 0.65 μs to settle a swing from 50% to 75% of the full-scale range.

Summing up the aforementioned time lengths gives 2.25-μs processing time. Therefore, even if all other components are ideal, the DSP can only execute a control loop routine up to 444 thousand iterations per second. Increasing the switching frequency beyond 444 kHz does not bring improvement in control loop bandwidth.

The time consumptions of other logic devices are negligible. For example, the 74LVC family logic gates have around 4-ns propagation delay; Altera MAX II CPLDs have around 200-ps combinational path delay. Because the proposed BBCC logic is very simple, the total propagation delay time is no more than a few nanoseconds.

2) Speed of Analog Devices: Today's comparators and op-amps can work well beyond MHz range. Thus, they do not impose limitations to neither digital nor analog BBCC solutions.

For example, Linear Technology LT1711 and Texas Instruments TLV3502 comparators have only 4.5-ns propagation delay. For a BBCC-controlled LLC converters operating at 1.2-MHz switching frequency, assuming the loop bandwidth is 200 kHz, the delay time only causes 4.5 ns/5000 ns $\times$ 360° $= 0.3°$ phase delay.

Linear Technology LTC6240 and LT1358 op-amps have 1-MHz and 11.7-MHz full power bandwidth, respectively. They are suitable for the analog circuits in the proposed BBCC circuit.

MOSFET gate drivers usually have 100 to 200-ns propagation delay time. In the aforementioned example of 200-kHz loop bandwidth, it will cause 200 ns/5000 ns $\times$ 360° $= 14.4°$ phase delay. Thus, it will become a concern in high switching frequency applications; but the problem is also faced by all types of control methods.

In conclusion, the speed limit of digital BBCC solutions is imposed by the DSP processing time; the speed limit of analog BBCC is possibly imposed by MOSFET gate drivers' propagation delay.

G. Soft Start Operation

The simplest method for soft start is with analog BBCC controller, where the soft start can be simply implemented using burst mode and closed-loop control. The reference voltage slowly rises from zero. The feedback loop tries to regulate output voltage according to the reference voltage. When the output voltage is very low, the resonant current tends to have very large amplitude, thus the secondary-side current is very large, causing the output voltage to rise faster than the reference voltage. In this case, the controller enters burst mode, disabling the operation immediately. This burst mode is the same as in light-load operation. It has two functions during soft start: 1) cut out the resonant current to prevent damage; 2) regulate the output voltage to follow the reference voltage. As the output voltage increases, the resonant current amplitude will decrease. Eventually, the BBCC control will operate continuously to reach the rated output voltage.

However, the aforementioned method is not suitable for digital control. In digital control, the output voltage is sampled at intervals, thus the burst mode may not disable the operation in time to cut out the large resonant current. Instead, frequency sweep is easy to implement in DSPs. The switching frequency is swept from high to low as in conventional control methods. When the soft start is near completion, an ADC takes samples of the v_{Cs} at the switch turn-off points, and then use the sampled values to initialize the PI controller. The PI controller will generate voltage thresholds according to the sampled values; thus the BBCC logic operation is synchronized with the resonant tank. Then, the BBCC controller can smoothly take over.

H. Maximum and Minimum Switching Frequency Limits

Maximum and minimum switching frequency limits are practical issues for conventional switching-frequency control methods. These limits ensure proper operation of the LLC converters. The BBCC method does not control the switching frequency; but the proposed control mechanism naturally limits the switching frequency range.

The maximum switching frequency happens at maximum input voltage and light load. Same as in conventional frequency-controlled LLC converters, the maximum switching frequency can be limited by introducing burst-mode operation [39], [47], [48]. When the BBCC control threshold, $v_{\mathrm{th}H}$, is lower than a predefined level, it indicates the light-load condition, which triggers the burst-mode operation. As a result, the switching frequency will not further increase.

The minimum switching frequency happens at minimum input voltage and full load. It is determined by the power train design, not by the BBCC controller. Nevertheless, the BBCC control logic inherently ensures that the operation is always in the zero-voltage switching (ZVS) region, thus it needs not to set

a minimum frequency as in conventional LLC controllers. The mechanism is explained as follows.

In the ZVS region, the resonant current zero-crossing points are lagging the MOSFET switching points. The current zero-crossing points are also the peak resonant capacitor voltage points, thus the resonant capacitor voltage reaches the peak after the MOSFET switching points. As a result, referring to Fig. 2, to trigger the low-side gate to turn-off, the resonant capacitor voltage must be descending and cross the $v_{\mathrm{th}L}$ threshold; the ascending cross of the $v_{\mathrm{th}L}$ signal is ignored by the logic. To trigger the high-side gate to turn-off, the resonant capacitor voltage must be ascending and cross the $v_{\mathrm{th}H}$ threshold; the descending cross of $v_{\mathrm{th}H}$ signal is ignored by the logic.

In the zero-current switching (ZCS) region, the logic is the opposite. The peak resonant capacitor voltage points are leading the MOSFET switching points. Therefore, the two signals that are ignored in the ZVS region should be used to trigger the MOSFET switching in the ZCS region, and the other two signals that are used in the ZVS region should be ignored in the ZCS region.

The proposed BBCC control logic is designed for the ZVS region. Referring to Fig. 1, the SR latch ignores the ascending cross of $v_{\mathrm{th}L}$ and the descending cross of the $v_{\mathrm{th}H}$ signals. As a result, it will never operate in the ZCS region.

For the sake of completeness, the BBCC method can be also designed for the ZCS region, by simply swapping the input polarities of the comparators in Fig. 1. In this case, it will always operate in the ZCS region, and never enter the ZVS region.

Instead of limiting the minimum switching frequency, the BBCC method should limit the maximum $v_{\mathrm{th}H}$ threshold. This is because the maximum sensed v_{Cs} voltage happens at the peak gain point; if the $v_{\mathrm{th}H}$ threshold rises above this level, the sensed v_{Cs} voltage cannot reach the thresholds, and the switching operation will stop. In fact, if K_{sen} is selected according to (26), the DAC output voltage range naturally limits the maximum $v_{\mathrm{th}H}$ voltage. If K_{sen} is selected greater, the maximum $v_{\mathrm{th}H}$ voltage can be calculated from (24).

I. Over-Current Protection

The power train of the BBCC-controlled LLC converter is identical to the conventional frequency-controlled LLC converters. Therefore, the same over-current protection techniques can apply.

One commonly used method is monitoring the peak resonant capacitor voltage. When over load/short-circuit condition happens, the peak resonant capacitor voltage will surge, which triggers the over-current protection procedure, in which case the operation will either stop or enter soft start. This technique also applies to the BBCC-controlled LLC converters.

V. Experimental Results

The experiment is carried out using a half-bridge LLC converter. The BBCC method does not change the steady state operation of the LLC power train, thus conventional design methods for LLC converters also apply to BBCC-controlled LLC converters. The power train parameters are listed in Table VII. The system diagram is the same as in Fig. 16. A Microchip dsPIC33F DSC is used to implement the ADC, PI controller, soft start, and protections. The BBCC logic is implemented in an Altera MAX II CPLD. It uses only 37 logic elements. In order to exploit the potential of the BBCC control, a high-speed linear opto-coupler circuit [49] is used to transmit output voltage signal to the primary side, so that the isolator is not a bottleneck of the loop bandwidth.

TABLE VII
Prototype Parameters

Topology	Half-bridge LLC resonant
Input voltage (V_{in})	400V – 300V
Output voltage (V_o)	12V
Transformer turns ratio	20:1, Center tapped
Parallel inductance (L_p)	86 µH
Series inductance (L_s)	12 µH
Series capacitance (C_s)	36 nF
Output capacitance (C_o)	1790 µF (100µF× 8 + 330µF× 3)
Attenuation factor (K_{sen})	100

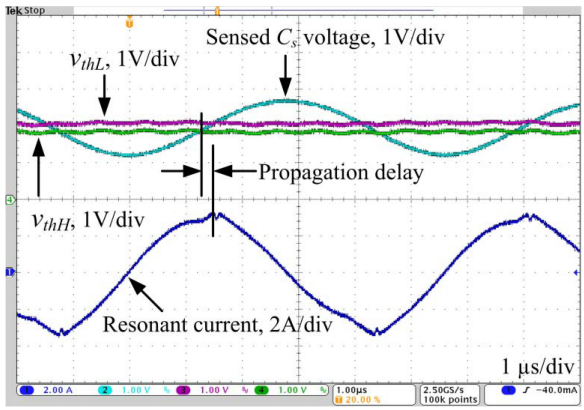

Fig. 17. Steady state at 400-V input and 5-A load.

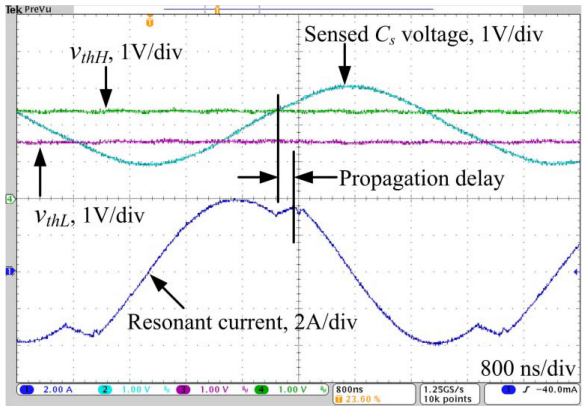

Fig. 18. Steady state at 400-V input and 25-A load.

The steady state waveforms at 5- and 25-A load conditions are shown in Fig. 17 and Fig. 18, respectively. A 200-ns propagation delay can be observed from the waveforms, which is mainly contributed by the gate driver. Note in Fig. 17, the threshold $v_{\mathrm{th}H}$ is lower than $v_{\mathrm{th}L}$. This is predicted in Section II, meaning that the output power is lower than that contributed by the junction capacitance.

Figs. 19 and 20 show 5- to 25-A load step at 400- and 300-V input voltage, respectively. In both cases, the output voltage is recovered within 7 switching cycles. This is an outstanding

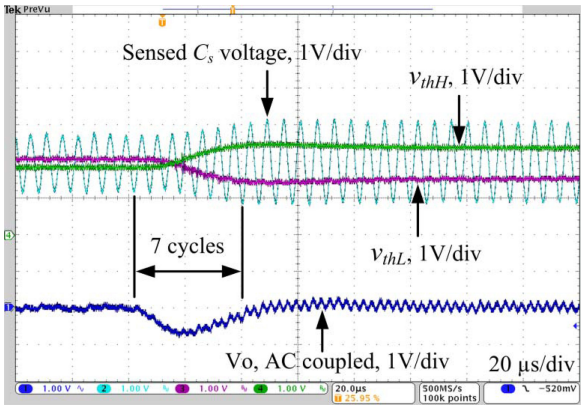

Fig. 19. Load step from 5 A to 25 A (400-V input).

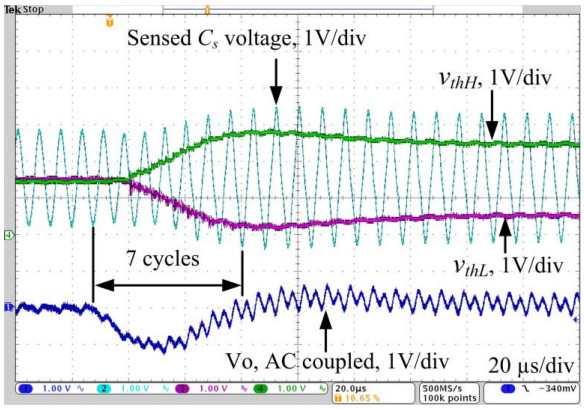

Fig. 20. Load step from 5 A to 25 A (300-V input).

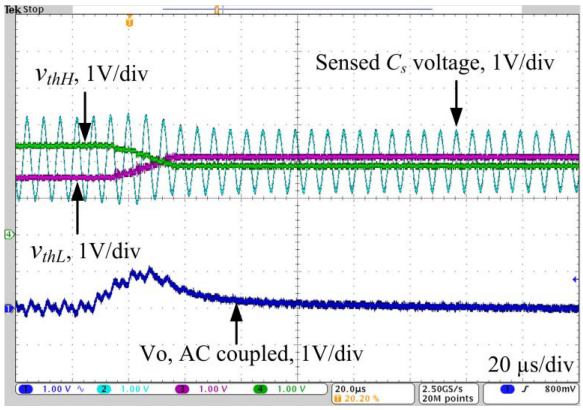

Fig. 21. Load step from 25 A to 5 A (400-V input).

performance provided by a simple PI controller, and the same fast response is achieved at both 400- and 300-V input voltage. This result is also highly consistent with the simulation results in Figs. 10 and Fig. 11.

Figs. 21 and 22 show 25- to 5-A load step at 400- and 300-V input voltage, respectively. The output voltage is also recovered within only a few switching cycles.

The above experimental results demonstrate the effectiveness of the proposed BBCC control method, as well as the fast dynamic performance at both 400- and 300-V input voltages. If

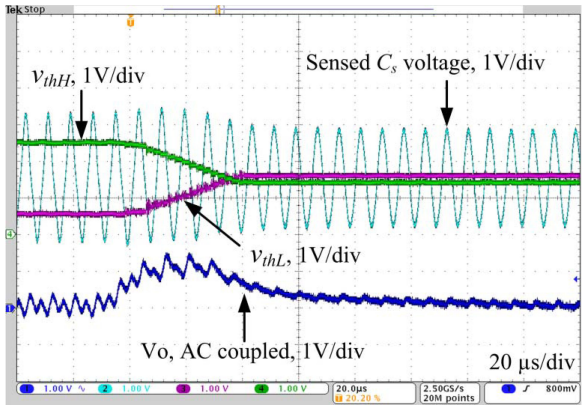

Fig. 22. Load step from 25 A to 5 A (300-V input).

we use conventional control methods, the load transient would normally take tens of, or even over a hundred switching cycles.

VI. Conclusion

A BBCC method is proposed for LLC resonant converters. Instead of conventional switching-frequency control, the BBCC method utilizes the series resonant capacitor voltage and a pair of voltage thresholds to determine the MOSFETs' switching points. The essence of such a control scheme is charge control plus trajectory control; therefore, it provides very fast dynamic performance in all operating conditions.

Small-signal analysis reveals that the BBCC-controlled LLC converter is a clean first-order system in all operating conditions, favorable to achieving high-loop bandwidth. Simulation results are highly consistent with the derived small-signal model, and show that the compensated loop bandwidth can achieve 1/6 of the switching frequency in all operating conditions. A digital implementation of the BBCC controller is presented, and practical design considerations are discussed in detail. Experimental results demonstrate its feasibility and the very fast dynamic performance at both 400 and 300-V input voltages, which are also consistent with simulation results.

The proposed BBCC method is simple: it does not require current sensing, current control loop, resettable integrator, or algorithm; and it simplifies the high-order resonant topology into a first-order system, thus the control loop design is made simple. For these reasons, the BBCC method is suitable for IC integration, in either analog or digital controllers. Its applications can be extended to other topologies that include a series capacitor.

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