

A Novel Asymmetrical Three-Level BUCK (ATL BUCK) Converter for Point-of-Load (POL) Application

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Abstract—This paper presents a novel, non-isolated step-down converter for the application of point-of-load (POL) voltage regulation. The new converter can achieve higher power density by utilizing a much smaller inductor compared with Buck converter in the POL application. A smaller inductor is achieved by increasing the effective operating frequency applied to the inductor by a factor of 4 and at the same time reducing the voltage applied to the inductor while maintaining the same switching frequency of control switches. The new converter uses two groups of interleaving switches to increase the effective operating frequency on the inductor and a flying capacitor to reduce the voltage across the inductor. The new switch topology is adopted because inductors take up much more space than active switches in a high power density power module [1][2]. A 12V-to-1V/1A prototype demonstrates that the proposed topology can use an inductor that is 77% less inductance than a conventional Buck Converter (i.e. only 23% of Buck's inductance is used in the prototype). Since two groups of switches are interleaved, the RMS (Root Mean Square) current in each group of control switches is reduced to half and the hotspot on the control switches is split into two.

Keywords—DC-DC; Non-isolated Converter; Point-of-load; Three-Level Buck; PWM

I. INTRODUCTION

The non-isolated DC-DC converters are widely used in any modern electronic piece of equipment. These converters are directly built right next to the load and are also called point-of-load (POL) power supplies. With the increasing demand to miniaturize the voltage regulators for computers and telecommunication products, high power density POL converter topologies are highly desirable in satisfying this trend. The conventional Buck converter has been the dominant method for implementing non-isolated DC-DC POL power supplies, but the inductor of Buck occupies a large portion of a Buck converter's footprint. It is difficult to reduce the size and weight of the Buck inductor. For example, in today's POL power modules, inductors serving as substrates consume the most space and is the biggest barrier in increasing power density[1]-[3]. To solve this problem, two things can be implemented: one is significantly increasing the switching frequency to reduce the size and weight of the inductor (Fig. 1 [4]) and the second is to

integrate magnetic component as the substrate of converter [5].

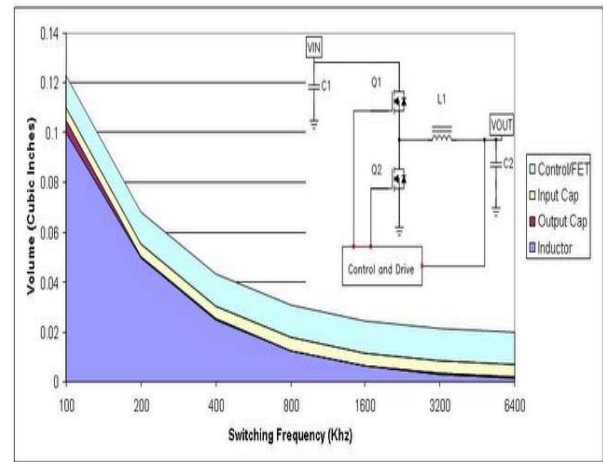


Fig. 1. Power Supply's Components Volume

Increasing the switching frequency is the most common and easiest way in reducing inductance of POL Buck converter. But by simply increasing the switching frequency the power loss will be increased and switch overheat will occur. Also, pushing switching frequency beyond tens of MHz in non-integrated POL Buck converter is impractical since a very small duty cycle is needed to provide very low voltage (0.5 – 1.6V) [6] output for modern microprocessors. A very small duty cycle limits the maximum switching frequency when the switching period is shorter than the turn-on and turn-off time of switches [7]. The conventional Three-Level Buck converter is a potential candidate for replacing the Buck Converter in high power density POL converters because it can increase the effective operating frequency on the inductor by a factor of two [8]. The Three-Level Buck converter can further extend its effective operating frequency by adding more levels of flying capacitors (e.g. Four-Level Buck converter) but the extra capacitor will complicate the operation of converter.

The proposed Asymmetrical Three-Level Buck (ATL Buck) converter is able to extend the effective operating frequency on the inductor to four times that of control switch driving frequency and at the same time, reduce the voltage across the inductor by half. This means that the inductor in ATL Buck converter operates at 4MHz when the switches operate at 1MHz. This has been proved and demonstrated in a 12V-to-1V/1A prototype and also 77% inductance reduction than a conventional Buck converter is achieved. By using two groups of switches in an alternating fashion, the RMS (Root Mean Square) current in each group of control switches is reduced to half. The reduced RMS current will benefit the thermal dissipation in the converter.

This paper is organized in the following manner: Section II describes the topology and operation of the proposed topology; Section III presents the experimental results and Section IV is a conclusion.

II. ASYMETRICAL THREE-LEVEL BUCK (ATL BUCK) CONVERTER

A. Circuit Configuration

Fig. 2 illustrates the configuration of the proposed Asymmetrical Three-Level (ATL) Buck converter. The proposed circuit is composed of four control switches, two synchronous rectifier (SR) switches, a flying capacitor C_f and an LC filter. The flying capacitor voltage V_c is pre-charged to half of the input voltage V_{in} by a pre-charging circuit before starting the converter.

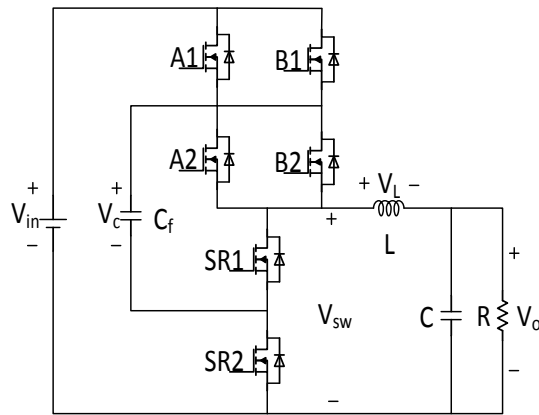


Fig. 2. Schematic of Asymmetrical Three-Level Buck converter

Fig. 3 illustrates the timing diagram for each switch during steady-state. Four control switches A1, A2, B1 and B2 are driven with 90° phase difference, two SR switches are driven complimentary. In one period T_s , each control switch turns on only once but the equivalent operating frequency of supplied voltage V_{sw} to the inductor is four times extended. When either of top control switches A1 or B1 is on, V_{sw} is equal to $V_{in}-V_{C_f}$. When either of lower control switches A2 or B2 is on, V_{sw} is equal to V_c . Since the flying capacitor C_f is pre-charged to half of the input voltage, the magnitude of switch node voltages are all equal to half of the input voltage. Switches in group A and group B are interleaved. In the first

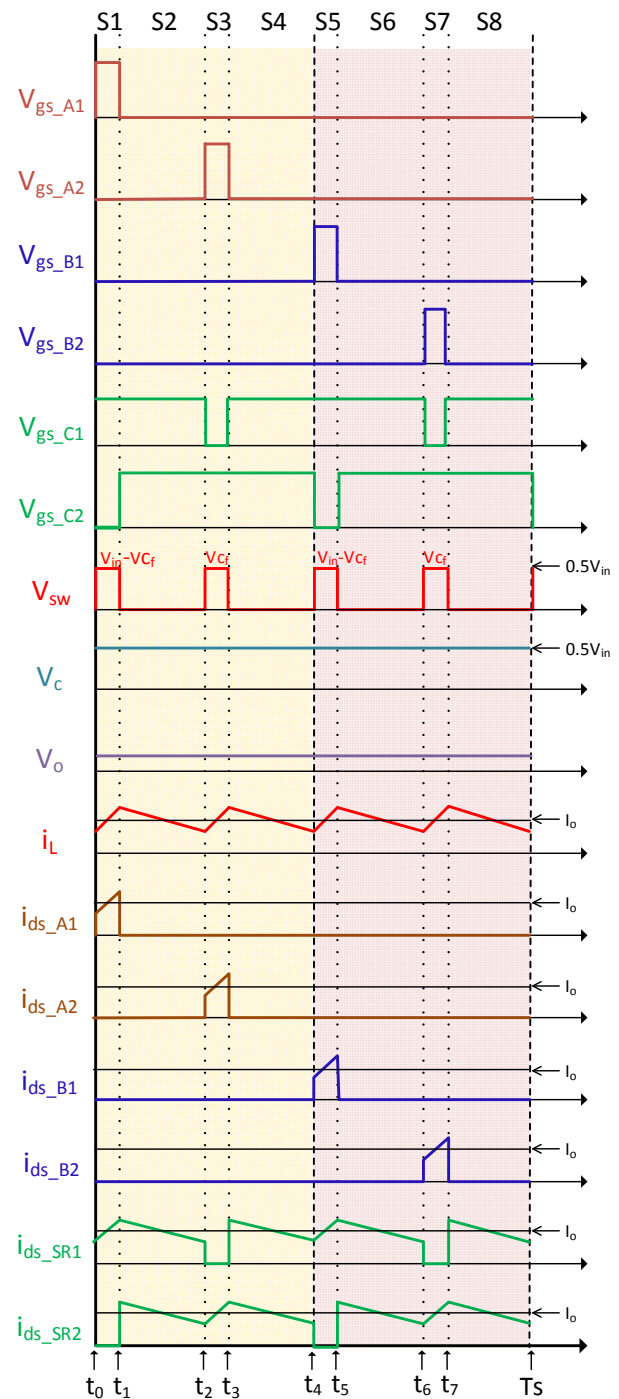


Fig. 3. Key Operation Waveforms of the Proposed Converter

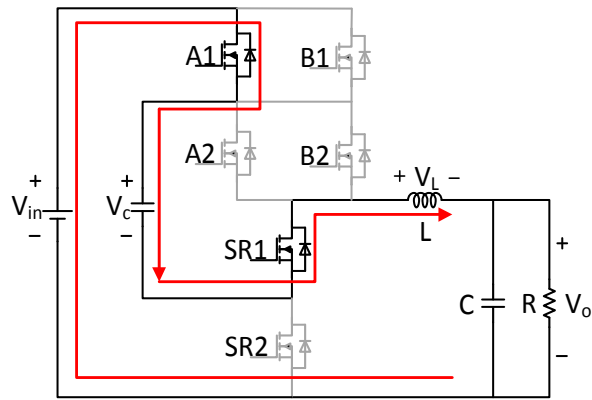
half period (from state 1 to state 4) switch group A is on and switch group B is off. In the last half period (from state 5 to state 8), switch group B is on and switch group A is off.

B. Operating States

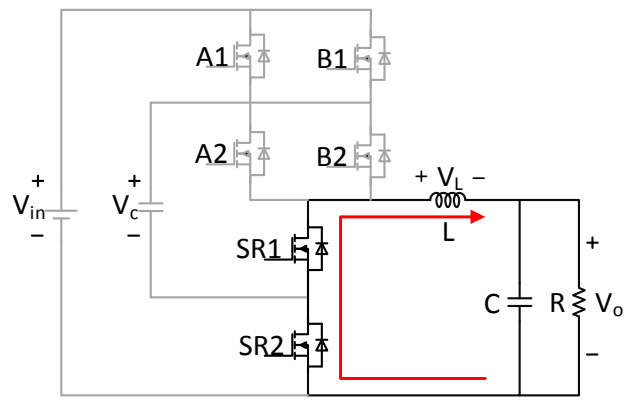
As illustrated in Fig.4, there are eight states in one switching period. During state 1 (t_0-t_1) the control switch A1 and SR switch C1 are on, the supplied voltage to the inductor

is V_{sw} ($V_{in} - V_c = V_{in} - 0.5V_{in}$) which is half of the input voltage V_{in} . The flying capacitor is charged by the voltage

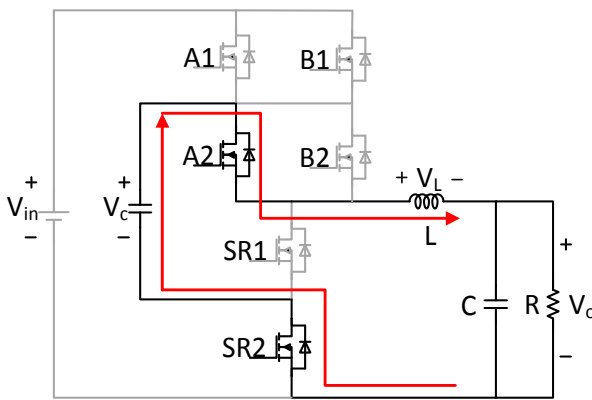
source and the charging current is as same as inductor



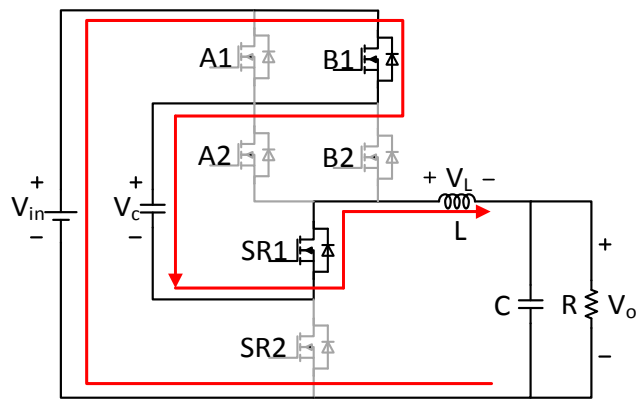
(a) State 1 (t_0-t_1)



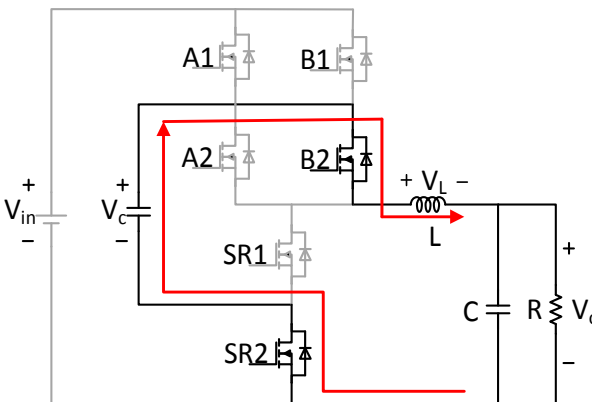
(b) State 2 (t_1-t_2), 4 (t_3-t_4), 6 (t_5-t_6), 8 (t_7-t_8)



(c) State 3 (t_2-t_3)



(d) State 5 (t_4-t_5)



(e) State 7 (t_6-t_7)

Fig. 4. Equivalent Circuits for Eight Operating States

current. At the end of state 1, the flying capacitor voltage V_c is a little higher than half of V_{in} . During state 2 (t_1 - t_2), both SR switches are on and the inductor current freewheels. The flying capacitor is floating and no current flows through it. In state 3 (t_2 - t_3), control switch A2 and SR switch C2 are on, the supplied voltage to the inductor is V_c which is almost half of the input voltage. The flying capacitor is discharged and the discharging current is as same as inductor current. In state 4 (t_3 - t_4), both SR switches are on, the inductor current freewheels and V_c keeps constant.

States 5-8 mirror states 1-4, but control switches B1 and B2 take over for A1 and A2. In state 5 (t_4 - t_5), the control switch B1 and SR switch C1 are on, the supplied voltage to the inductor is V_{sw} ($V_{in} - V_c = V_{in} - 0.5V_{in}$) which is half of the input voltage. The flying capacitor is charged again by the voltage source and the charging current is as same as inductor current. At the end of state 5, the flying capacitor voltage is a little higher than half of V_{in} . In state 6 (t_5 - t_6), both SR switches are on and the inductor current freewheels. The flying capacitor is floating. During state 7 (t_6 - t_7), control switch B2 and SR switch C2 are on, the supplied voltage to the inductor is V_c which is almost half of the input voltage V_{in} and the flying capacitor is discharged again. In state 8 (t_7 - T_s), both SR switches are on and the inductor current freewheels.

C. Extended Equivalent Operating Frequency

As illustrated in Fig. 4, four control switches take turns to turn on only once in one period, and this results in four times input with a magnitude of $0.5V_{in}$ to the inductor. The equivalent operating frequency is four time extended.

The voltage conversion can get from (1). D_{ATL} is the duty cycle of each control switch and it is defined as T_{on}/T_s , where T_{on} is t_1 - t_0 , t_3 - t_2 , t_5 - t_4 and t_7 - t_6 .

$$\frac{V_o}{V_{in}} = 2D_{ATL} \quad (1)$$

D. Reduced RMS Current in Control Switches

To achieve the same equivalent operating frequency with the proposed converter, the conventional Three-Level Buck converter in [8] has to double switching frequency and each control switches will conduct twice. The proposed Asymmetrical Three-level Buck converter has two groups of interleaving control switches. Each control switch conducts only once in one period. Thus, the RMS current of each control switch is reduced by half in the proposed circuit.

E. Inductance and Inductor Volume Reduction

For the given design specification in Table 1, the inductance required in the Buck converter can be designed according to equation (2) [9].

$$L_{BUCK} = \frac{V_L \cdot D}{\Delta i_L \cdot f_s} = \frac{(V_o - \frac{V_o^2}{V_{in}})}{\Delta i_L \cdot f_s} \quad (2)$$

TABLE I. DESIGN SPECIFICATION COMPARISON

	Buck Converter	New Topology
$V_{in} \rightarrow V_o$	12V \rightarrow 1V	12V \rightarrow 1V
I_o	1A	1A
Δi	200mA (20%)	200mA (20%)
Voltage on Inductor	11V	5V
Control Switch(es)	1MHz	1MHz
Driving Frequency	1MHz	1MHz
Equivalent Frequency on the Inductor	1MHz	4MHz
Inductance	4.58uH	1.04uH

In the new topology the supplied input voltage V_{sw} to inductor is almost half of V_{in} in state 1, 3, 5, 7 due to the flying capacitor, so the new conversion ratio is doubled as in (1). Besides, the equivalent operating frequency of the proposed circuit is four times that of the Buck converter, thus the inductance in the ATL Buck converter can be calculated from equation (3).

$$L_{ATL} = \frac{V_{L_ATL} \cdot D_{ATL}}{\Delta i_L \cdot f_{s_ATL}} \quad (3)$$

Substitute $D_{ATL} = \frac{V_o}{2V_{in}}$ from (1) into (3) yields (4).

$$L_{ATL} = \frac{(\frac{1}{2}V_{in} - V_o) \cdot (\frac{V_o}{\frac{1}{2}V_{in}})}{\Delta i_L \cdot (4f_s)} = \frac{(V_o - \frac{2V_o^2}{V_{in}})}{4 \cdot \Delta i_L \cdot f_s} \quad (4)$$

Based on the design specification in Table.1, the inductance of the ATL Buck converter is reduced to 23% (i.e. $L_{ATL}=1.04 \mu\text{H}$) of that of the Buck converter (i.e. $L_{BUCK}=4.58 \mu\text{H}$) in order to achieve same inductor ripple.

The core volume ratio can be obtained by using Area Product concept [10] which is a quantitative estimation method of a core. The core volume can be obtained from (5) [11], where K_v is a constant related to volume factor, W is the maximum energy of the inductor, K_u represents window utilization factor of the core, B_m is the maximum flux density and J_w is the current density in coils.

$$Vol_{core} = K_v \left(\frac{2W}{K_u B_m J_w} \right)^{\frac{3}{4}} \quad (5)$$

The volume ratio can be obtained from (6) when the same core is used for both circuits. The inductor volume of ATL converter only takes 33% of Buck's.

$$\frac{Vol_{ATL}}{Vol_{Buck}} = \left(\frac{W_{ATL}}{W_{Buck}} \right)^{\frac{3}{4}} = \left(\frac{L_{ATL}}{L_{Buck}} \right)^{\frac{3}{4}} = 0.33 \quad (6)$$

F. Flying Capacitor Voltage Ripple

It is also noted that the voltage ripple for ATL Buck converter is smaller because the capacitor current frequency is 4 times of Buck converter's (using (7) [9]).

$$\Delta v = \frac{\Delta i_L}{8C_f \cdot f_s} \quad (7)$$

The value of flying capacitor should be selected based the current flowing through the flying capacitor to guaranty no significant capacitor voltage drop. In one period, the flying capacitor is charged and discharged twice, the charging and discharging time should be balanced to stabilize the flying capacitor voltage in the steady state.

G. Inductance Reduction in Different Output Voltage

For the same switching frequency of control switches, inductance ratio between the ATL Buck converter and Buck Converter is obtained from (8).

$$\text{Inductance Ratio} = \frac{L_{ATL}}{L_{BUCK}} = \frac{\frac{1}{4}(V_o - \frac{2V_o^2}{V_{in}})}{(V_o - \frac{V_o^2}{V_{in}})} \quad (8)$$

This ratio is only related to the input and output voltage. For the application of 12V input voltage, the inductance can be further reduced in higher output voltage. Fig. 5 illustrates the inductance ratio in different output voltage. For the 3.3V output voltage, only 16% of Buck's inductance is needed in the Asymmetrical Three-Level Buck converter to achieve same inductor current ripple.

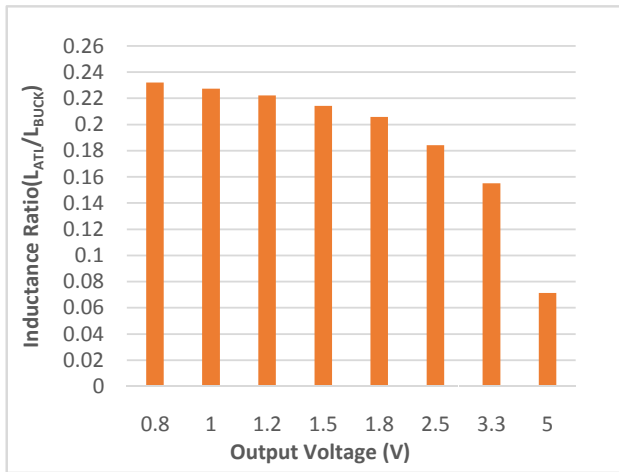
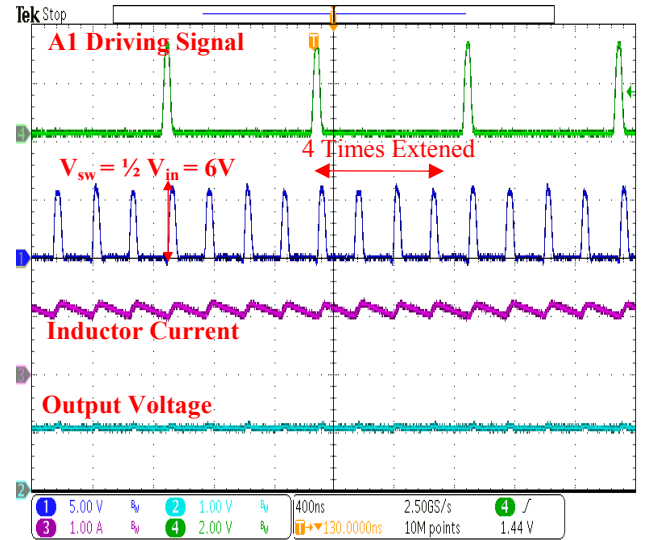


Fig. 5. Inductance Ratio in Different Output Voltage

III. EXPERIMENTAL VERIFICATION

An experimental converter prototype with 12V input and 1V output was built and tested to prove the proposed topology. Experimental waveforms are displayed in Fig. 6. It

is shown that the driving signal of control switch A1 (in channel 4) is 1MHz and the equivalent operating frequency on the inductor (in channel 1) is 4MHz. The inductor current ripple is 20% of the output current as required in the specification (Table. 1) and the output voltage (in channel 2) stabilized at 1V.



CH1: Switching Node Voltage CH2: Output Voltage
CH3: Inductor Current CH4: Switch A1 Driving Signal

Fig. 6. Experimental Waveforms

IV. CONCLUSION

This paper has presented a novel Asymmetrical Three-Level Buck converter for the application of point-of-load. The effective operating frequency of this converter is extended to four times that of the switch driving frequencies. This new topology can significantly reduce the size of the inductor in a point-of-load power module. The inductance in proposed circuit is reduced to 23% that of the Buck converter's inductance as proved in the experimental prototype. Moreover, the core volume can be reduced to 33% of Buck's. The power density of the POL converter is significantly improved. Besides, the interleaved two groups of controls helps reducing the RMS current in each control switch to half compared with the conventional Three-Level Buck converter.

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