# An Average Current Modulation Method for Single-Stage LED Drivers With High Power Factor and Zero Low-Frequency Current Ripple

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***Abstract*— Conventional single-stage light-emitting diode (LED) drivers with a high power factor (PF) contain a significant LED current ripple at twice the ac line frequency, and would require large energy storage capacitors to limit the effect on LED light. Conventional designs and novel control techniques aim to power LED loads with a dc voltage to ensure a limited low-frequency LED current ripple. This paper proposes an average current modulation method that is designed to operate in conjunction with single-stage PF correction (PFC) circuits that contain significant ac voltage ripple, while maintaining zero low-frequency current ripple. This allows the energy storage capacitance of the PFC stage to be reduced, avoiding the need for electrolytic-type capacitors and prolonging the life of the LED driver. The average current modulation circuit requires a single low-voltage MOSFET, a current sense resistor, and a simple control circuit. By requiring no additional magnetic components, the cost of the current modulation circuit is very low and has minimal impact on the efficiency of the overall LED driver. Two experimental prototypes, an 8.75-W system with a buck–boost PFC converter and a 25-W system with a flyback PFC converter, have been built to verify the capability and excellent performance of the proposed driving technique.**

***Index Terms*— Energy efficiency, LED lamps, light-emitting diodes (LEDs), power electronics.**

## I. Introduction

RISING energy prices have significantly increased the demand for high efficiency electronics, and government regulations continually increase standards for grid-tied electronics. With electric lighting consuming 19% of total global electricity production [1], advances in lighting technology result in significant energy savings. As fluorescent lamps offered increased luminous efficacy over traditional incandescent lighting, solid-state lighting now offers numerous benefits that will soon see it overtaking fluorescent lighting as the dominant source of residential and commercial lighting [2], [3]. Light-emitting diode (LED) lamps offer higher luminous efficacy, longer lifetimes (50 000+ h), and contain no hazardous materials (such as mercury). The combined high luminous efficacy and long lifetimes reduce the cost and the environmental impact of lighting.

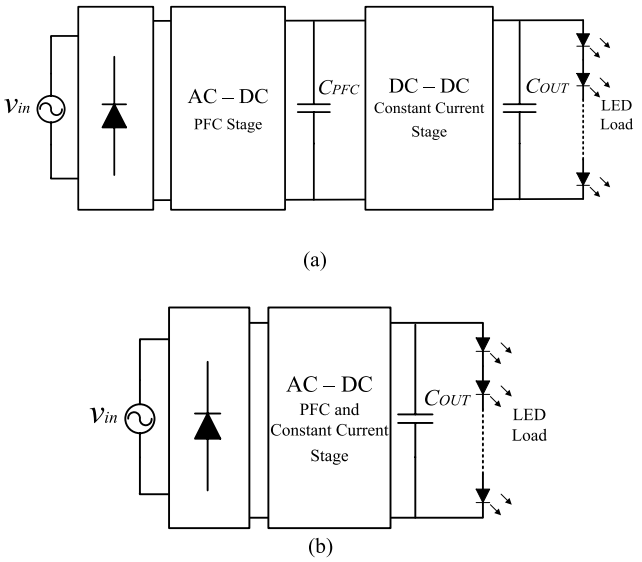


Fig. 1. Conventional LED driver topologies. (a) Two-stage LED driver. (b) Single-stage LED driver.

Residential and commercial lighting, powered directly by the main power grid, must meet certain requirements set by government agencies. High power factor (PF) is desirable to maximize the power transferred over the grid, decrease noise, and ensure stability. Energy Star regulations [4] require residential lighting to achieve 0.7 PF, and commercial lighting to achieve 0.9 PF. Two-stage LED drivers have commonly been used to provide this high performance. These drivers consist of a high-performance ac–dc PF correction (PFC) circuit, followed by a dc–dc converter that provides a constant current to an LED lamp. The block diagram of a two-stage

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LED driver is shown in Fig. 1(a). This configuration requires relatively low energy storage capacitance in the PFC stage, as the dc–dc converter is able to follow a fluctuating input voltage while still providing a constant output current. The two-stage approach, however, suffers from a high component count, which leads to high power loss and high component cost. To reduce the component count, single-stage PFC converters can be employed to power the LED lamps. The block diagram of a single-stage LED driver is shown in Fig. 1(b).

Single-stage PFC LED drivers maintain a high PF while regulating the LED current. Though a high PF can be achieved by a single-stage ac–dc topology, it results in an energy imbalance between the ac input and the dc output. This energy imbalance requires energy storage capacitors to store energy during the zero crossings of the input voltage to maintain a smooth output. If these capacitors are not large enough, the output will contain significant ripple at twice the line frequency. Conventionally, single-stage PFC LED drivers utilize very large capacitors to limit the current ripple within the LED load. This is done to limit the ripple in the light produced by the LEDs. A large capacitance necessitates the use of electrolytic-type capacitors due to their high energy density. Electrolytic capacitors have significantly lower lifespans ($\sim$10 000 h) than the LED chips, and the use of these capacitors in the LED drivers limits the overall life of the resulting LED lamp. As a long lifespan is a key attraction to LED lighting, this is undesirable. It is, therefore, desirable to use an LED driver that has the advantages of a single-stage PFC circuit (high PF and high efficiency), but does not require a large capacitor to provide a low output current ripple.

Numerous novel LED driving techniques to reduce the required energy storage capacitance, thus avoiding electrolytic capacitors were proposed in [5]–[16]. Attempting to maintain simple control techniques, Almeida *et al.* [5] and Alonso *et al.* [6] propose using integrated power converters to merge an ideal ac–dc PFC circuit and a dc–dc circuit into a single topology. Several circuit configurations have been proposed in these papers. The circuits are able to achieve higher efficiency than two-stage designs and demonstrate a reduction in the output capacitance. However, these topologies still suffer from a high component count and carry a significant LED current ripple.

Harmonic current (third and fifth) injection has been proposed in [7] and [8], as a cost-effective means of lowering the peak to average ratio of input power. While injecting current harmonics into the input lowers the amount of storage capacitance required for the PFC stage, the method inherently lowers the PF of the driver and does not substantially limit the LED current ripple.

Significant work has focused on modifying single-stage PFC LED drivers, using auxiliary circuits to condition the energy imbalance rather than using an additional capacitance. These methods aim to avoid processing 100% of the LED power twice, as is the case in two-stage LED drivers. A method of conditioning the twice line frequency current component via a bidirectional converter has been proposed in [9]. The proposed converter stores excess current during the first half cycle, and provides current during the second half cycle to mitigate the energy imbalance. The LED load is supplied by a dc current with a low ripple. In this proposed method, the PFC stage is implemented with a relatively low storage capacitance, facilitating the use of long life capacitors. The drawbacks of this method are significant conversion losses due to converting over a third of the output power twice, and the high voltage stress required of the bidirectional converter's components, which increase the cost.

High-frequency LED pulse current driving techniques are discussed in [17]–[20]. A very high-frequency LED driver is presented in [17], which utilizes the pulsed current for stable control of the LED output and applies pulsewidth modulation (PWM) dimming. A novel ac–dc LED driver with a pulsed output is presented in [18]. The work offers a unique topology to provide high PF with minimal output capacitance at a higher output voltage, though it contains low-frequency current ripple in the LED load. These works discuss the characteristics of driving the LEDs with pulsed current waveforms. Extensive LED flicker and electrothermal analysis are presented in [21], where the role of root mean square (rms) current is discussed. An analysis technique of the LED light output is presented that is able to quantize the luminous ripple. Additional novel LED drivers are detailed in [22]–[28].

Previous proposed works suffer from increased component costs, complicated control techniques, or relatively significant power losses. An average current modulation method is proposed in this paper. The proposed method features a simple control scheme, and requires a single low-voltage MOSFET, rated the same as the LED output voltage. It ensures zero low-frequency current ripple for an LED load, while also offering a reduction in the energy storage capacitor of the PFC stage. The proposed design is configured to work with single-stage PFC designs, and is capable of improving the performance of existing isolated and nonisolated PFC converters. As the proposed modulation method does not interact with the operation of the power switch in the PFC circuit, the PF is unchanged and remains high. The proposed design has been experimentally tested by both buck–boost and flyback prototypes.

This paper is organized as follows. Section II explains the theory and operation of the proposed average current modulator, and discusses its limitations. Section III discusses the relationship between the PFC output voltage and the LED current, and introduces a peak duty cycle control to limit the maximum LED current pulse. Section IV presents two methods to control the peak duty cycle. Section V presents the benefits of the peak duty cycle control and provides a design procedure to minimize the PFC capacitance. Section VI presents the experimental results. Finally, the conclusions are drawn in Section VII.

## II. Operating Principle of Proposed Average Current Modulation Circuit

### A. Average Current Modulation Method

LED drivers based on single-stage ac–dc PFC circuits contain significant output current ripple at twice the ac line frequency. The magnitude of this low-frequency ripple is inversely proportional to the amount of energy storage

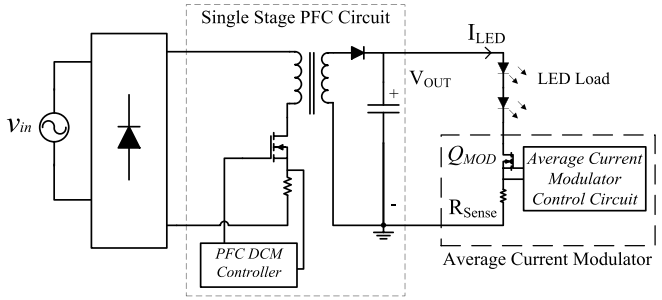


Fig. 2. Placement of average current modulator within single-stage PFC circuit.

capacitance used in the PFC stage. This low-frequency current variation in the LED load produces undesirable ripple in the light produced by the LED load. The proposed average current modulation circuit (current modulator) removes the low-frequency current ripple that is normally generated by the conventional single-stage PFC LED drivers.

Fig. 2 shows the circuit diagram of the average current modulator with a single-stage PFC circuit. The proposed LED current modulator is designed to operate in series with an LED load that is powered by a single-stage PFC converter. The LED current is modulated at a fixed high modulation frequency (∼25 kHz) such that the average current of the LED load is controlled for each modulation cycle. By doing this, the LED current will consist of a dc component and a high-frequency component, at the modulation frequency. This modulation method removes any low-frequency current ripple that would be induced by the voltage ripple of the PFC stage. The resulting high-frequency current will produce light that is proportional to the average LED current, and will appear flicker-free as humans do not notice high-frequency light modulation [29], [30].

By controlling the average current at a high frequency, the current modulator is able to respond to significant low-frequency voltage variation of the PFC output voltage. Therefore, the average current modulator can ensure zero low-frequency LED current from PFC circuits with significant twice line frequency voltage ripple introduced by limited energy storage capacitance. The magnitudes of the LED current pulses will fall within the low-frequency envelope, but the LED current will contain no content at the low frequency, due to the modulator maintaining the average current each modulation cycle.

The PFC circuit utilized could be realized by numerous topologies, with or without electrical isolation. The average current modulator consists of a modulation MOSFET switch ($Q_{\mathrm{MOD}}$), a current sense resistor (that are connected in series with the LED load), and a control circuit that controls the current modulator's operation. There is no need for additional magnetic components, and no change to the PFC circuit is required. The modulation frequency is required to be high enough to push the LED current ripple out of the range of human observers, but it is kept relatively low to minimize switching losses. As the voltage rating for $Q_{\mathrm{MOD}}$ is the same as the LED voltage, which is <60 V in most cases, and the simple control circuit, the cost of the modulator is kept very low. The schematic in Fig. 2 shows the average current modulator control circuit, modulation switch, and current sense resistor connected to the output of a single-stage flyback PFC converter.

The diagram of Fig. 3 shows the operation of the average current modulator by providing key waveforms of the circuit. The waveforms of the PFC circuit output voltage, $V_{\mathrm{OUT}}$, gate signal of the modulation switch, $V_{\mathrm{GS\_MOD}}$, LED load current, $I_{\mathrm{LED}}$, and the control signal that dictates the modulation switch turn-OFF instance, $V_{\mathrm{Control}}$, are shown in Fig. 3. To illustrate the two extreme operating points of the current modulator's operation, the waveforms of Fig. 3 are the zoomed-in view to isolate the behavior at the maximum and minimum values of the PFC output voltage, $V_{\mathrm{OUT\_max}}$ and $V_{\mathrm{OUT\_min}}$, respectively. These two operating points highlight the peak duty cycle, $D_{\mathrm{peak}}$, which occurs at the minimum LED current pulse, $I_{\mathrm{LED\_min}}$, and the minimum duty cycle, $D_{\mathrm{min}}$, which occurs at the maximum LED current pulse, $I_{\mathrm{LED\_max}}$.

The control circuit of the average current modulator is shown in Fig. 4. To obtain a constant average LED current over one modulation cycle, the modulator instigates the modulation switch turn-ON at the beginning of each modulation cycle, via the flip-flop and fixed frequency clock. The LED current is sensed and integrated by the LED current integrator, and once the average current equals the error voltage, the modulation switch is turned OFF by the flip-flop through the current comparator. The error voltage is generated by the error amplifier by comparing the average LED current level, which is generated by filtering the LED current with low-pass filter, LPF $I_{\mathrm{AVG}}$, to the current reference. The control circuit can be realized by two operational amplifiers (op-amps) and a generic PWM controller. The LED current integrator requires one op-amp, and the low-pass filter LPF $I_{\mathrm{AVG}}$ requires one op-amp. The error amplifier, current comparator, fixed frequency clock, and flip-flop are packaged within the PWM controller. The power to turn the modulation switch ON and OFF is supplied by a gate driver that is also packaged within the PWM controller. For simplicity, this gate driver is not drawn as the flip-flop is the component that dictates the turn ON and OFF.

Due to the low-frequency variation of the PFC output voltage, the magnitude of the LED current pulses that drive the LED load also varies at this low frequency. As such, the duty cycle of the modulation switch will vary, peaking at the minimum PFC output voltage and reaching its minimum value at the maximum PFC output voltage.

The varying amplitude of the LED current pulses has minimal effect on the switching frequency ripple of the PFC output voltage. As the switching frequency of the PFC circuit is two to three times larger than the modulation frequency, the behavior at the output capacitor will differ slightly between the switching cycles of the PFC switch. When the output voltage is at the minimum value of the low-frequency (100/120 Hz) variation, the charging and discharging of the output capacitor are very similar to the conventional PFC circuits as the conduction time of $Q_{\mathrm{MOD}}$ is at its highest point. The switching frequency ripple will be relatively low as the PFC circuit is regularly

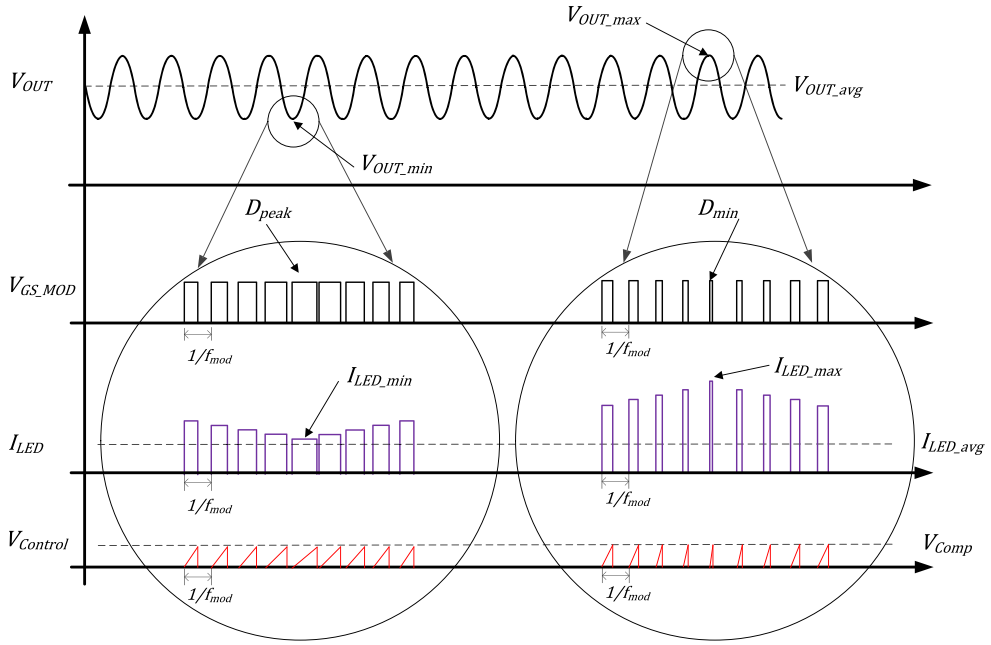


Fig. 3. Operational waveforms of average current modulator.

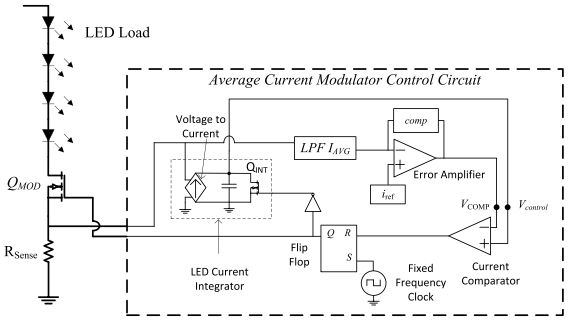


Fig. 4. Schematic of average current modulator control circuit.

charging the capacitor and the LED load is drawing a relatively constant current (due to the high conduction time). When the output voltage is at its maximum value of the low-frequency variation, the charging and discharging of the output capacitor will be more irregular. As the LED current pulse is much larger when the output voltage is low, the capacitor will discharge faster during the shorter conduction time of $Q_{\mathrm{MOD}}$. During the longer OFF time of $Q_{\mathrm{MOD}}$, the PFC circuit will charge the capacitor over multiple switching cycles. This results in a larger switching frequency ripple at the maximum value of the PFC output voltage. As the low-frequency variation of the PFC output voltage is multiple orders of magnitude larger than the switching frequency ripple, the variation of the switching frequency ripple has no effect on the system operation.

### *B. Pulsed Current Limitations of LEDs*

Pulsed LED current is defined by two characteristics: 1) pulse amplitude and 2) pulse duty cycle. Two separate sources are referenced to provide a design guideline for the proposed modulator. The Applications Engineering team at Cree published strict limitations for their XLamp LED series in [31]. They recommend that current pulses do not exceed 100% of the maximum rated current for duty cycles between 51% and 100%, current pulses do not exceed 200% of the rated current for duty cycles between 10% and 50%, and current pulses with <10% duty cycles do not exceed 300% of the rated current. These restrictions are compared with the recommendations from OSRAM [32], and it is found that Cree recommends more conservative guidelines. For this reason, their limitations are used in this paper.

From the guidelines, it is observed that for the LED drivers using the average current modulator, the LED load should be rated for a maximum current twice that of the desired average current. This ensures that if the LED load experiences pulses with amplitudes equal to or above the rated current, the duty cycles of these pulses will be equal to or <50%.

A presentation by Texas Instruments in collaboration with OSRAM [33] states that low-frequency LED current variation does not have a major effect on the color coordinates of the LED light, while it does have a limited effect on luminous efficacy. This is due to the nonlinear relationship between LED forward current and luminous flux, which is illustrated in [32]. Due to the limited effect of this nonlinearity and the control of the average current, it is not expected that the current modulator will be severely affected by these characteristics. The experimental results show that this is true.

As the modulation method drives the LED load with current pulses higher than the average current, the modulation method will cause the rms value of the LED current to be higher than the average LED current. Even though the increased rms LED current will increase the LED junction temperature, the increase will be negligible and not significantly affect the lifetime of the LED.

An equivalent circuit model of an LED is shown in Fig. 5, which equates an LED to an ideal diode, a series resistance, $R_{\mathrm{LED}}$, and a voltage source, $V_{\mathrm{fwd}}$. The power consumed by an LED is largely attributed to the equivalent

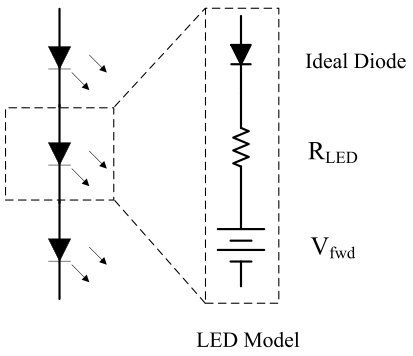


Fig. 5. Equivalent circuit model of an LED.

voltage source, which consumes ~90% of the LED power. The remaining power is dissipated within the equivalent resistance. The power consumed by the equivalent voltage source is proportional to the average value of the LED current, and as the average current is maintained by the modulation method, the associated power loss is unchanged. The power dissipated by the equivalent resistance is proportional to the rms value of the LED current, and causes the rise in junction temperature. Due to the fact that the majority of LED power is associated with the equivalent voltage source, the increase in the LED power due to the modulation method is negligible. Therefore, even though the modulation method increases the rms value of the LED current, the effect on the lifetime of the LED is minimal. The LED power is estimated to increase by ~5%.

## III. PFC Circuit Output Voltage Variation and Peak Duty Cycle Control

With the average current modulator controlling the average LED current by modulating the duty cycle of the LED current, the current pulse amplitudes are not controlled. As high current levels can damage the LED devices, action must be taken to ensure that the maximum current pulse amplitude is limited. This section defines the low-frequency voltage variation of the PFC circuit output and its relation to the LED current pulses. A peak duty cycle control method for the modulation switch is proposed to operate in conjunction with the average current modulation method. The peak duty cycle control ensures that minimal current stress is applied to the LED load.

When coupled with the average current modulator, the single-stage PFC converter will have different control requirements as compared with conventional LED drivers. The dc level of the PFC output voltage does not correspond to the programmed average LED current level. Based on the operating principle of the modulator, each LED current pulse must be larger than the desired average LED current to achieve zero low-frequency current [$I_{\mathrm{LED_{pulse}}}(t) > I_{\mathrm{LED\_avg}}$]. Thus, the PFC output voltage must be high enough to produce current pulses larger than the desired average current at all points during its low-frequency variation. This can be guaranteed if the minimum current pulse ($I_{\mathrm{LED\_min}}$), produced by the minimum PFC voltage ($V_{\mathrm{OUT\_min}}$), is larger than the desired average current. The peak duty cycle of the modulator, which occurs at the minimum LED current pulse, is defined in (1). A general expression is given in (2) for all the LED current pulses

$$\text{Peak Duty Cycle}\% = \frac{I_{\mathrm{LED\_avg}}}{I_{\mathrm{LED\_min}}} \tag{1}$$

$$\text{Duty Cycle}(t)\% = \frac{I_{\mathrm{LED\_avg}}}{I_{\mathrm{LED\_pulse}}(t)} \tag{2}$$

The relationship between the PFC voltage and the LED current pulses is dependent on the characteristics of the LED load, and is expressed in (3). An LED load could consist of several LED chips in combination. The resistance and forward voltage of an LED load are dynamic with the forward current, but can be considered constant for a given average output current

$$I_{\mathrm{LED_{pulse}}}(t) = \frac{V_{\mathrm{out}}(t) - V_{\mathrm{fwd}}}{R_{\mathrm{LED}}} \tag{3}$$

The amplitude of the LED current pulses, $I_{\mathrm{LED_{pulse}}}(t)$, as defined in (3), is the difference between the PFC output voltage, $V_{\mathrm{OUT}}(t)$, and the forward voltage of the LED load, divided by the series resistance of the LED load. As the current modulator's modulation frequency is significantly higher than the low-frequency variation of the PFC output voltage, $V_{\mathrm{OUT}}(t)$ and $I_{\mathrm{LED_{pulse}}}(t)$ can be considered constant for each modulation cycle of the current modulator. Based on the equivalent circuit model of the LED load, the minimum voltage of the PFC output is defined in (4), with its limitation expressed in

$$V_{\mathrm{OUT\_min}} = I_{\mathrm{LED\_min}} \cdot R_{\mathrm{LED}} + V_{\mathrm{fwd}} \tag{4}$$

$$V_{\mathrm{OUT\_min}} \geq I_{\mathrm{LED\_avg}} \cdot R_{\mathrm{LED}} + V_{\mathrm{fwd}} \tag{5}$$

From (3), it is noted that the amplitudes of the LED current pulses vary proportionally to the low-frequency variation of the PFC output voltage, and that from (2), the duty cycle of the modulation switch varies inversely with the PFC output voltage. As the output voltage increases, the duty cycle will decrease, and as the output voltage decreases, the duty cycle will increase. The maximum value of the output voltage, $V_{\mathrm{OUT\_max}}$, produces the maximum LED current pulse amplitude, $I_{\mathrm{LED\_max}}$, as expressed in (6). The maximum output voltage can also be expressed as the minimum output voltage plus the peak-to-peak voltage ripple of the PFC output, $V_{\mathrm{OUT\,pk\text{–}pk}}$, as given in (7). This output voltage ripple is dependent on the energy storage capacitance used in the PFC stage and the average LED current, defined in (8), where $f_{\mathrm{line}}$ is the line frequency (60 Hz for North America) and $C_{\mathrm{out}}$ is the capacitance value [34]

$$V_{\mathrm{OUT\_max}} = I_{\mathrm{LED\_max}} \cdot R_{\mathrm{LED}} + V_{\mathrm{fwd}} \tag{6}$$

$$V_{\mathrm{OUT\_max}} = V_{\mathrm{OUT\_min}} + V_{\mathrm{OUT\,pk\text{–}pk}} \tag{7}$$

$$V_{\mathrm{OUT\,pk\text{–}pk}} = \frac{I_{\mathrm{LED_{avg}}}}{2\pi \cdot f_{\mathrm{line}} \cdot C_{\mathrm{out}}} \tag{8}$$

The voltage ripple of the PFC circuit can be expressed using the maximum and minimum LED current pulses and the resistance of the LED load by combining (4), (6), and (7) to produce (9). By combining (8) and (9), it is possible to define

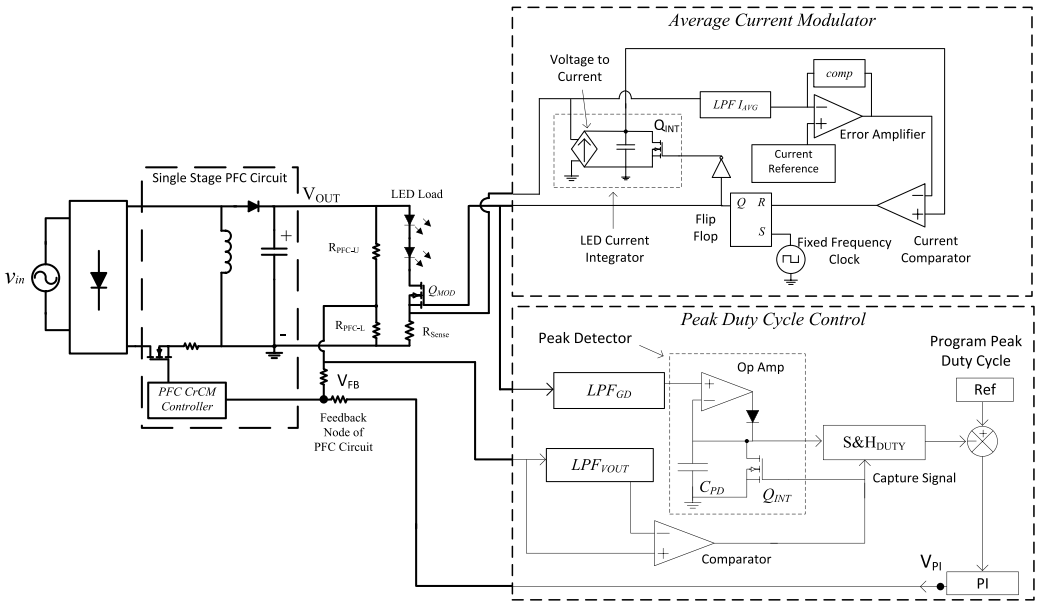


Fig. 6. Peak duty cycle control circuit with output voltage adjustment.

the required PFC stage capacitance, once the maximum and minimum LED current pulses are defined. This expression is given in

$$V_{\text{OUT pk–pk}} = (I_{\text{LED\_max}} - I_{\text{LED\_min}}) \cdot R_{\text{LED}} \tag{9}$$

$$C_{\text{out}} = \frac{I_{\text{LED\_avg}}}{2\pi \cdot f_{\text{line}} \cdot (I_{\text{LED\_max}} - I_{\text{LED\_min}}) \cdot R_{\text{LED}}} \tag{10}$$

High-amplitude current pulses can damage LEDs, and when left uncontrolled, they pose a danger to the long-term reliability of the devices. As such, it is important to limit the maximum LED current pulse amplitude. Considering a single-stage PFC circuit with a fixed energy storage capacitor and, therefore, a fixed output ripple, the maximum output voltage can be considered as an offset of the minimum voltage level. If the minimum voltage level is controlled close to its minimum permissible value in (5), the maximum voltage level can be limited accordingly. This in turn would limit the maximum LED current pulse amplitude.

It is noted that the minimum PFC voltage and minimum LED current pulse correspond with the peak duty cycle of the average current modulator at the modulation frequency. To control the minimum LED current pulse such that the maximum LED current pulse amplitude is limited, the average current modulator has been designed to control the peak duty cycle of the modulation switch. Using the peak duty cycle as a control variable in the modulation loop, the controller becomes independent of the LED load characteristics, ensuring proper operation regardless of the LED load.

Considering an LED load ($R_{\text{LED}} = 20\ \Omega$ and $V_{\text{fwd}} = 40$ V) that is powered by a single-stage PFC circuit and the average current modulator, the benefits of peak duty cycle control can be illustrated. The PFC circuit is assumed to have an output voltage ripple of 6 $V_{\text{pk}-\text{pk}}$ and the average current modulator is set to control the average LED current at 200 mA. If the minimum PFC voltage achieves the average LED current by modulating the LED current with a 70% duty cycle, the minimum LED current pulse will be 285 mA based on (2). The maximum LED current pulse will be 240 mA higher, from (9), at 525 mA, with a duty cycle of 38% from (2). With a peak duty cycle of 90%, the minimum LED current pulse will be 222 mA, and the maximum current pulse will be limited to 462 mA, down from 525 mA. If the peak duty cycle is set to 90%, the minimum current pulse can be controlled, which in turn limits the maximum current pulse. Therefore, it is desirable to set the peak duty cycle of $Q_{\text{MOD}}$ to as close to 100% as possible to limit the peak LED current. In this paper, peak duty cycle of 90% is used.

## IV. Peak Duty Cycle Control Methods

Two circuit configurations to control the peak duty cycle have been developed. One method adjusts the PFC output voltage to control the peak duty cycle. With this method, the average LED current is set by the current modulation circuit, and the PFC circuit is configured to control the output voltage. The other method adjusts the average LED current level within the current modulator to control the peak duty cycle. In this method, the average LED current is set by the PFC circuit, which is configured to control its output current. The output voltage is indirectly adjusted to achieve the desired peak duty cycle at the programmed current level. A brief discussion on the limitations of pulsed current in LEDs is included.

### A. Peak Duty Cycle Control–Output Voltage Adjustment

The first method of controlling the peak duty cycle of the modulation switch is suitable for nonisolated PFC circuits, where a direct connection can be made between the peak duty cycle circuit and the PFC controller, as shown in Fig. 6. The detected peak duty cycle and the desired peak duty cycle are compared to create an error voltage, which is added to the feedback voltage of the PFC circuit. In this way,

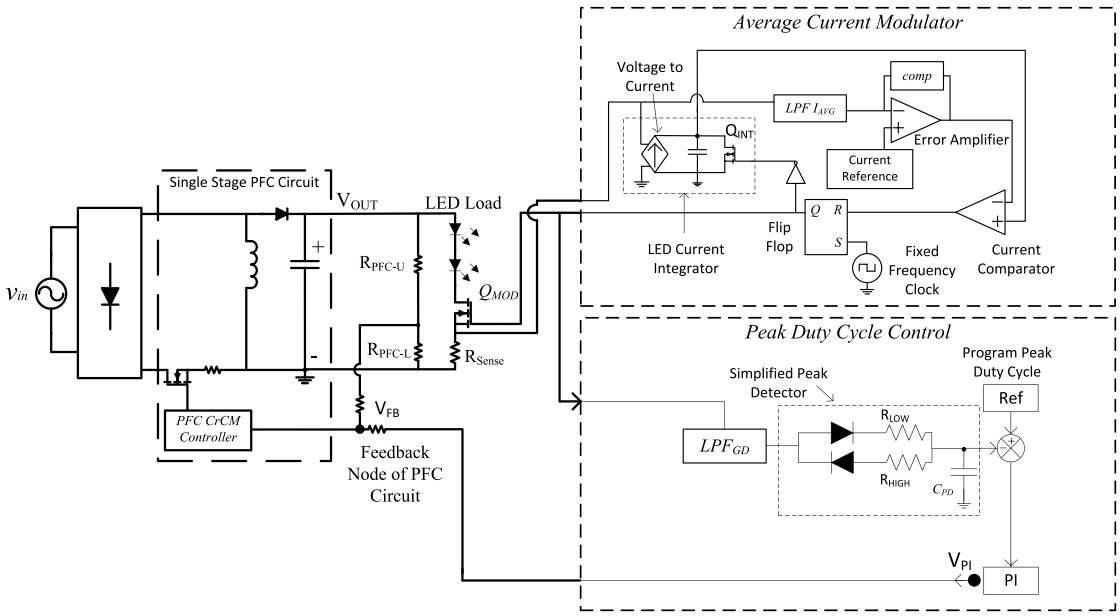


Fig. 7. Peak duty cycle control circuit with output voltage adjustment and simplified peak detector.

the voltage level of the PFC output is adjusted to ensure that the desired peak duty cycle is achieved. In this method, the LED current level is set by the average current modulator, not the PFC circuit.

Fig. 6 shows the control circuit that adjusts the output voltage to control the peak duty cycle, highlighting the components and circuit connections required for its operation. The average current modulator block is the same as the circuit shown in Fig. 4.

To detect the peak duty cycle, the PWM gate drive signal of the modulation switch ($Q_{\mathrm{MOD}}$) is filtered to produce a continuous waveform that represents the varying duty cycle of the average current modulator. This is accomplished by a low-pass filter with a cutoff frequency significantly lower than the modulation frequency, represented by $\mathrm{LPF_{GD}}$.

The peak duty cycle is detected from this waveform by a traditional peak detector circuit (diode, capacitor, and reset switch), which holds the maximum voltage applied to its input with a sample and hold circuit, $\mathrm{S\&H_{DUTY}}$. The capture signal, which instructs the sample and hold circuit to sample the peak detector voltage, is generated from the ripple voltage of the PFC output. Using the low-pass filter $\mathrm{LPF_{VOUT}}$ and the peak comparator, a pulse (the capture signal) is generated once the peak duty cycle is reached. In this way, the capture signal is able to sample the voltage of the peak detector when it holds a voltage representing the peak duty cycle of the modulation switch.

Once the peak duty cycle is detected, it is compared with a reference voltage representing the programmed peak duty cycle. The error voltage from this comparison is then used to adjust the output of the PFC converter. The error voltage is connected via a large resistor to the feedback node of the PFC controller. A scaled down version of the output voltage is also fed through a large resistor into the feedback node of the PFC controller.

When the peak duty cycle is below the desired level, the output voltage of the PI block ($V_{\mathrm{PI}}$) will increase, causing the voltage at the feedback node of the PFC circuit ($V_{\mathrm{FB}}$) to increase. The PFC controller responds by decreasing the output voltage ($V_{\mathrm{OUT}}$), which increases the peak duty cycle so that the same average current is achieved. When the peak duty cycle is above the desired level, the output voltage of the PI block will decrease, causing the feedback node voltage of the PFC circuit to decrease. The PFC controller responds by increasing the output voltage, which causes the peak duty cycle to decrease. In this way, the error voltage of the peak duty cycle comparison will adjust the dc voltage level of the PFC converter such that the minimum PFC voltage produces the desired peak duty cycle in the average current modulator.

The output voltage adjustment method requires four op-amps, one each for the peak detector, $\mathrm{LPF_{GD}}$, $\mathrm{LPF_{VOUT}}$, and the PI block. As well, it requires a comparator for the peak comparator and the sample, and holds IC for $\mathrm{S\&H_{DUTY}}$. The number of ICs can be reduced with a simplified peak detector, as explained below.

An improved method was developed to approximate the peak duty cycle without the use of a traditional peak detector or sample and hold circuit, which is shown in Fig. 7. With the improved method, the duty cycle waveform is fed into a simplified peak detector, which relies on two unidirectional sensing paths. The sensing paths, a forward (low impedance) path, and a reverse (high impedance) path, charge and discharge a capacitor to generate a voltage waveform representing the peak duty cycle. The path directions are controlled using diodes, and the resistors are used to control the impedance of each path.

At the peak of the duty cycle waveform, the simplified peak detector's output voltage is quickly charged to the voltage level representing the peak duty cycle by the forward sensing path. Through the rest of the low-frequency period, the peak detector

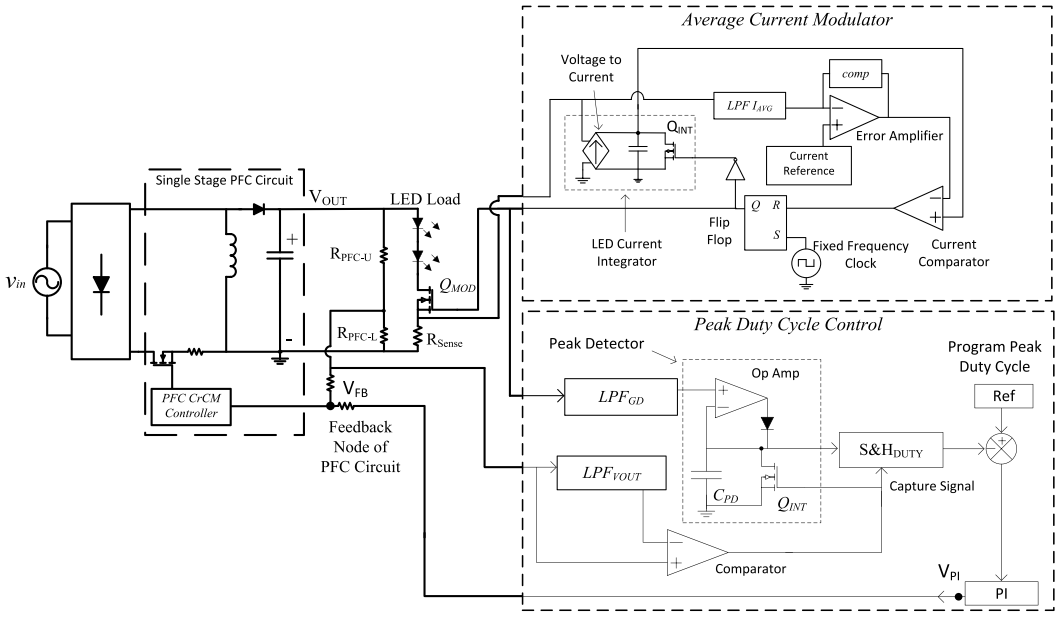


Fig. 8. Peak duty cycle control circuit with average current adjustment.

would ideally hold this voltage level, though for stability reasons, this is inadmissible. Instead, the reverse sensing path's high impedance causes the detector's capacitor to discharge slowly, such that the voltage of the detector does not change significantly over a single low-frequency period. As the duty cycle waveform reaches the voltage level representing the next peak duty cycle, the peak detector voltage is again quickly charged to this level.

The reverse sensing path is designed to discharge the capacitor over several low-frequency periods. This is required so that the controller can adjust the system in case the peak duty cycle voltage ever saturates, which is likely to occur during the start-up sequence. The capacitor voltage decrease within one low-frequency period will not significantly impact the steady-state operation of the average current modulator.

The simplified peak detector is able to produce a voltage that accurately represents the peak duty cycle of the average current modulator using a limited number of passive components. Using the simplified peak detector, the output voltage adjustment method requires only two op-amps, for $\mathrm{LPF_{GD}}$ and the PI block. The cost of the added diodes and resistors is negligible.

### *B. Peak Duty Cycle Control—Average Current Adjustment*

The second method of controlling the peak duty cycle of the modulation switch is suitable for both the isolated and nonisolated PFC circuits, as no connection is required between the PFC controller and the peak duty cycle circuit. The detected peak duty cycle and the desired peak duty cycle are compared to create an error voltage, the same as in the previously described method. Instead of adjusting the output voltage of the PFC circuit, the error voltage is used as the current reference for the average current modulator (which no longer has a fixed current reference). By adjusting the average LED current level, the desired peak duty cycle is ensured.

With this method, the dc LED current is set by the PFC controller. In steady-state operation, the current reference of the average current modulator will match the current reference of the PFC controller. Therefore, the average current adjustment method allows the average current modulator to easily work with dimming capable PFC circuits, such as those designed to work with common phase cut dimmers. Utilizing the previously described simplified peak detector, it is possible to configure the peak duty cycle control circuit as an integrated part of the average current modulator, with no external connections required.

The average current adjustment method is shown in Fig. 8, featuring the conventional peak detector with a sample and hold circuit. The LED load in this configuration is powered by a primary-side regulated (PSR) flyback PFC circuit. The average current modulator block is based on the circuit shown in Fig. 4, except that the fixed current reference has been replaced with a connection to the output of the PI block from the peak duty cycle comparison. The average current adjustment method using the conventional peak detector requires four op-amps, one each for the peak detector, $\mathrm{LPF_{GD}}$, $\mathrm{LPF_{VOUT}}$, and the PI block. As well, it requires a comparator for the peak comparator and the sample and hold IC for $\mathrm{S\&H_{DUTY}}$.

The PFC controller controls the dc component of the LED current from the primary side of the flyback transformer, and the average current modulator pulses the LED load. When the peak duty cycle is below the desired level, the output voltage of the PI block ($V_{\mathrm{PI}}$) will increase, increasing the current reference for the current modulator. As the average current level of the modulator increases, the peak duty cycle will increase to achieve this average current. When the peak duty cycle is above the desired level, the output voltage of the PI block will decrease, decreasing the average current level of the current modulator. As the average current level decreases,

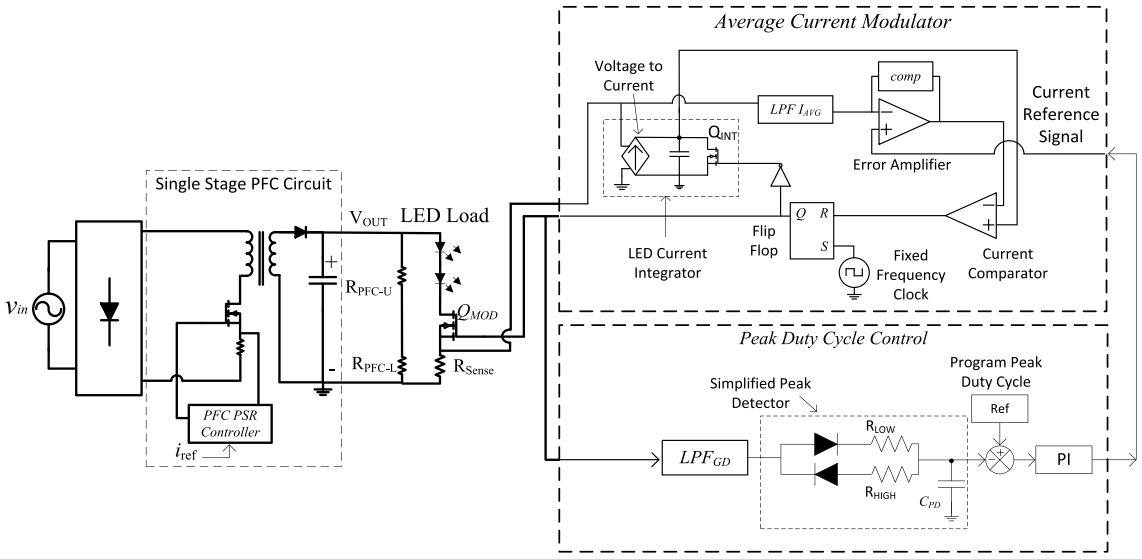


Fig. 9. Peak duty cycle control circuit with average current adjustment and simplified peak detector.

the peak duty cycle will decrease so that the programmed average current is achieved. As the peak duty cycle controls loop and the PFC controls loop balance, the PFC output voltage will be indirectly adjusted such that the desired peak duty cycle is achieved.

If the current reference of the PFC controller is changed, for example, during dimming applications, the dc current of the LED load will change accordingly. Through the control action described above, the average current modulator and the peak duty cycle circuit will adjust the average LED current level to obtain the desired peak duty cycle, at the average current level dictated by the PFC controller.

The peak duty cycle detection can be accomplished by either of the two ways previously described, with the traditional peak detector or with the simplified design. The circuit of the simplified peak detector connected to the average current modulator is shown in Fig. 9. The behavior of the PI block to control the peak duty cycle is the same as above. It is noted that using the simplified peak detector with the average current adjustment method, the peak duty cycle control can be added to the average current modulator control circuit without requiring any external connections. As well, with the simplified peak detector, the average current adjustment method requires only two op-amps, for $LPF_{GD}$ and the PI block. The cost of the added diodes and resistors is negligible.

### C. Dimming Functionality

It is possible to add dimming to the average current modulator, regardless of which peak duty cycle control circuit is used. With the output voltage adjustment method, the average LED current level is set by the current reference within the current modulator. Dimming control can be implemented by adjusting the current reference within the modulator. By changing the current reference, the average LED current level will change accordingly. The output voltage adjustment circuit adjusts the output voltage level of the PFC converter to ensure that the programmed peak duty cycle is achieved at every dimming level.

With the average current adjustment method, the average LED current level is set by the current reference within the PFC control circuit. Dimming control can be implemented by adjusting the current reference within the PFC control circuit. The average LED current level will change as the current reference of the PFC circuit changes. The average current adjustment circuit adjusts the current reference within the current modulator to ensure that the programmed peak duty cycle is achieved at every dimming level. As numerous PFC control circuits available on the market feature dimming capability, using the average current adjustment method offers the simplest way to add dimming functionality to the average current modulator.

## V. Advantage of Peak Duty Cycle Control and Design Procedure

By comparing the maximum LED current with different peak duty cycles, the advantage of the proposed peak duty cycle control method is shown. An analysis of an example LED driver, based on a buck–boost PFC stage designed to operate at ∼50 V/175 mA (8.75 W), will show that the maximum LED current is limited when the peak duty cycle is controlled. A simple design procedure is then presented using an example LED driver based on a flyback PFC stage designed to operate at ∼50 V/500 mA (25 W). These example drivers are the basis for the prototypes used in the experimental results section.

### A. Advantage of Peak Duty Cycle Control

The 8.75 W buck–boost example is used to emphasize the advantage of the proposed peak duty cycle control method. For the LED load, 14 units of the Cree XLAMP ML-C LED are used. At an average current of 175 mA, each LED has a series resistance of ∼2.67 Ω, with a forward voltage of ∼2.9 V.

TABLE I
PEAK DUTY CYCLE EXAMPLE

| Symbol | Quantity | Value | |
|---|---|---|---|
| | | Without Peak Duty Cycle Control | With Peak Duty Cycle Control |
| $I_{LED\_avg}$ | Average LED Current | 175 mA | 175 mA |
| $V_{OUT\ pk-pk}$ | Output Voltage Ripple | 8 V | 8 V |
| $C_{out}$ | PFC Capacitance | 56μF | 56μF |
| $I_{LED\_min}$ | Minimum LED Current | 250 mA | 195 mA |
| $V_{OUT\_min}$ | Minimum PFC Voltage | 49.95 V | 47.89 V |
| $V_{OUT\_max}$ | Maximum PFC Voltage | 57.95 V | 55.89 V |
| $I_{LED\_max}$ | Maximum LED Current | 464 mA | 409 mA |

Using 14 LEDs, the resultant LED load has a resistance of 37.38 Ω and a forward voltage of 40.6 V. In this example, it will be assumed that the average current modulator is used to condition a single-stage PFC circuit that has an 8 $V_{pk-pk}$ output voltage ripple. With a 60 Hz power source, the required energy storage capacitance is calculated from (8) to be 58 $\mu$F.

First, without the peak duty cycle control, it is assumed that the PFC output voltage level is such that the minimum LED current pulse amplitude is 250 mA. This pulse occurs at a duty cycle of 70% based on (1). According to (4), the minimum PFC output voltage is 49.95 V, while the maximum PFC output voltage is 57.95 V based on the peak-to-peak PFC circuit voltage ripple and (7). From (6), the maximum LED current pulse is 464 mA.

Now, if the peak duty cycle control is implemented with the average current modulator, the PFC output voltage will be adjusted to obtain the programmed high duty cycle. If a peak duty cycle of 90% is obtained, the amplitudes of the LED current pulses will be reduced. The minimum current pulse is 195 mA, dictated by the peak duty cycle. Subsequently, the minimum and maximum PFC voltage levels are recalculated to be 47.89 and 55.89 V, respectively. This leads to a new maximum current pulse of 409 mA.

Table I summarizes the conditions of the two driver systems, with and without the peak duty cycle control. The data show that while both the drivers have the same average LED current and use the same output capacitor, the maximum LED current is lower when the peak duty cycle control is used. By programming a high peak duty cycle (e.g., 90%), the maximum LED current amplitude is reduced without having to increase the PFC stage energy storage capacitance.

### *B. Design Procedure to Minimize PFC Capacitance*

The peak duty cycle control method allows the average current modulator to achieve its full potential by ensuring that the minimum LED current pulse is very close to the programmed average current. This control can be used to minimize the energy storage capacitance within the PFC circuit while ensuring that the maximum LED current does not damage the LED load. From (10), the required PFC capacitance can be calculated once the maximum LED current is defined (as the minimum LED current is defined by the peak duty cycle).

The maximum LED current is restricted by the current rating of the LED load. The maximum LED current pulse is chosen by selecting a minimum duty cycle of 50%, and is calculated from (2). A minimum duty cycle of 50% is selected for several reasons. Under the recommendation provided in Section II, the maximum LED current pulse will not damage the LED load as it will be rated for a maximum current equal to twice the average current. As the LED is capable of operating at this maximum LED current under dc operation, any light ripple induced by the LED nonlinearity is expected to be minimal.

The 25 W flyback example is used with this design procedure for the average current modulator. For the LED load, 20 units of the OSRAM Golden Dragon Plus LUW-W5AM LEDs are used. At an average LED current of 500 mA, each LED has a series resistance of ∼0.67 Ω and a forward voltage of 2.1 V. Using 20 LEDs, the resultant LED load has a resistance of 13.4 Ω and a forward voltage of 42 V.

With the peak duty cycle set at 90%, the minimum LED current pulse will be 555 mA from (1). The maximum LED current is selected using a minimum duty cycle of 50%, calculated to be 1 A from (2). Using (10), the capacitor value is calculated to be 198 $\mu$F. This is the minimum amount that the average current modulator, with peak duty cycle control, needs to ensure zero low-frequency LED current given the set minimum and maximum LED current pulses.

## VI. EXPERIMENTAL RESULTS

Two experimental prototypes have been built in the laboratory to showcase the operation of the average current modulator, highlighting both the output voltage adjustment method and average current adjustment method for peak duty cycle control. Both the prototypes use the simplified peak detection method to reduce the component count. The two prototypes are designed from the example cases of Section V.

### *A. 8.75-W Buck–Boost Prototype With Output Voltage Adjustment*

A nonisolated buck–boost prototype is designed to showcase the operation of the average current modulator with output voltage adjustment for peak duty cycle control. The output of this prototype is designed to operate at ∼50 V/175 mA for 8.75 W of power from a 60 Hz supply. The Cree MLCAWT-A1-0000-000WE7CT LED is used to configure the LED load. Rated for a maximum dc current of 350 mA, the LEDs exhibit a forward voltage of 2.9 V and a series resistance of 2.67 Ω at 175 mA. The LED load is configured with 14 LED chips, and thus the resistance of the entire LED load is 37.38 Ω.

A conventional single-stage PFC buck–boost LED driver was built and analyzed to provide a reference to measure the performance of the average current modulator. The buck–boost PFC circuit is designed and implemented with the FAN7529 Critical Conduction Mode PFC Controller [35]

TABLE II
CURRENT MODULATOR COMPONENT LIST

| Component | Part | Quantity | Manufacturer |
|---|---|---|---|
| Modulation MOSFET | IRFL014NPBFCT | 1 | International Rectifier |
| Current Sense Resistor | 0.1 Ohm | 1 | Standard |
| | PWM Controller UCC38C43 [36] | 1 | Texas Instruments |
| Control Circuit | Operational Amplifier | 4 | Texas Instruments |
| | NAND Gate | 1 | Texas Instruments |

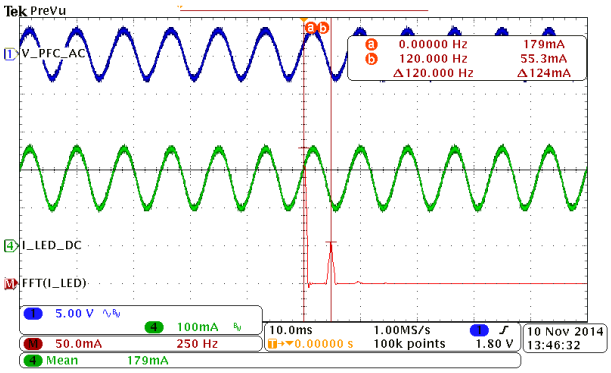


Fig. 10. Conventional buck–boost driver—LED current. CH1: PFC output voltage (ac coupled; 5 V/div; 10 ms/div). CH4: LED current (dc coupled; 100 mA/div; 10 ms/div). MATH: FFT of LED current (50 mA/div; 250 Hz/div).

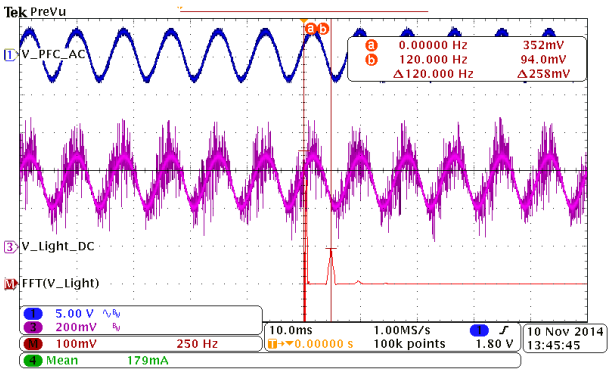


Fig. 11. Conventional buck–boost driver—LED light. CH1: PFC output voltage (ac coupled; 5 V/div; 10 ms/div). CH3: LED light (dc coupled; 200 mV/div; 10 ms/div). MATH: FFT of LED light (100 mV/div; 250 Hz/div).

from Fairchild. Waveforms of LED current and light are presented in Figs. 10 and 11, respectively. The fast-Fourier transform (FFT) of the LED current and light is used as a metric to compare the attenuation of low-frequency current ripple and light ripple of the LED load between the two power supplies. The energy storage capacitance is selected such that the PFC output will carry a voltage ripple of approximately 8 $V_{pk-pk}$, as in the first example of Section V. For an average output current of 175 mA, this is calculated from (8) to be 58 $\mu$F. A 56 $\mu$F capacitor is used in the lab.

The FFT analysis is done by the MATH function of the Tektronix DPO 3034 oscilloscope. The LED light is sensed by a light to voltage sensor, configured using a photodiode (OSRAM—SFH 2701) and a transimpedance

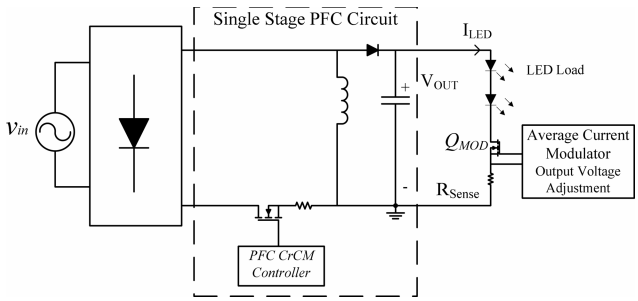


Fig. 12. Placement of average current modulator within buck–boost driver.

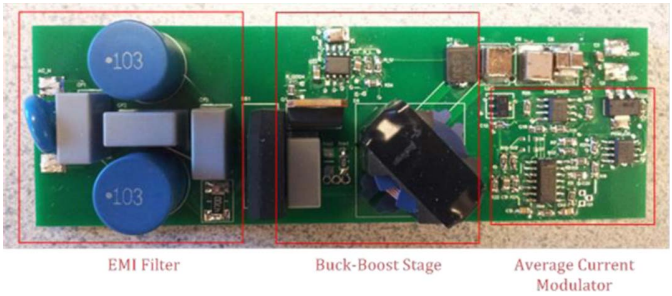


Fig. 13. Photo of buck–boost prototype with the average current modulator.

amplifier (TI—OPA381). The bandwidth of the sensor is set very high (~500 kHz), to accurately follow the high-frequency waveform of the LEDs.

With the conventional buck–boost LED driver, the LED load has a 120-Hz ripple current of 55.3 $mA_{rms}$ with a dc current of 179 mA or 43% modulation index defined as peak ripple value to average LED value (55.3 mA $\times$ 1.414/179 mA). Similarly, the light produced by the LED load has a 120 Hz modulation index of 37.7% (94 mV $\times$ 1.414/353 mV).

The average current modulator is connected to the LED driver in the laboratory to reduce the low-frequency current ripple of the LED load. The block diagram of the buck–boost PFC stage with the modulator added is shown in Fig. 12. A 10 nF capacitor is connected across the LED load to prevent voltage spikes caused by the modulation method. The voltage across this small capacitor is not discharged by the modulation method and, therefore, has no effect on efficiency. The modulator is set to a modulation frequency of 25 kHz. The components used to configure the modulator are listed in Table II. The 0.1 $\Omega$ resistor is used to minimize the power loss. The photo in Fig. 13 shows the buck–boost prototype with the average current modulator. A peak duty

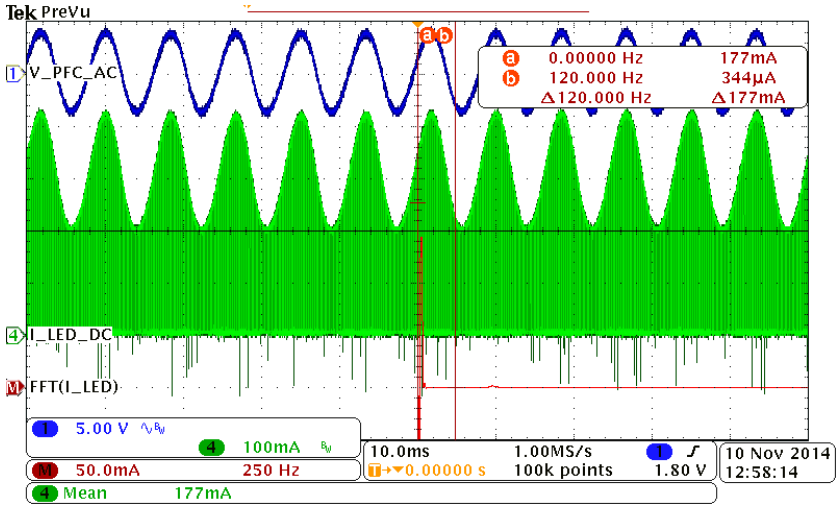


Fig. 14. Buck–boost output voltage ripple and LED current with average current modulator. CH1: PFC output voltage (ac coupled; 5 V/div; 10 ms/div). CH4: LED current (dc coupled; 100 mA/div; 10 ms/div). MATH: FFT of LED current (50 mA/div; 250 Hz/div).

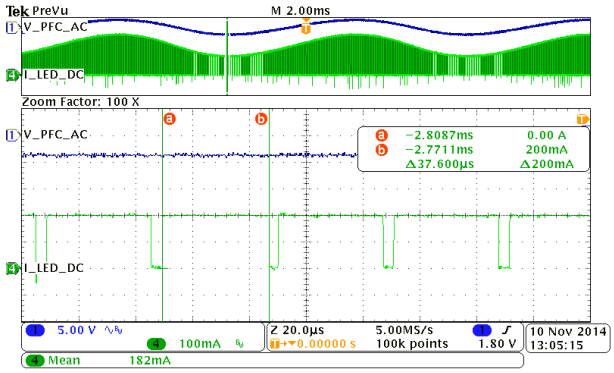


Fig. 15. LED current highlighting peak duty cycle. CH1: PFC output voltage (ac coupled; 5 V/div; 20 $\mu$s/div). CH4: LED current (dc coupled; 100 mA/div; 20 $\mu$s/div).

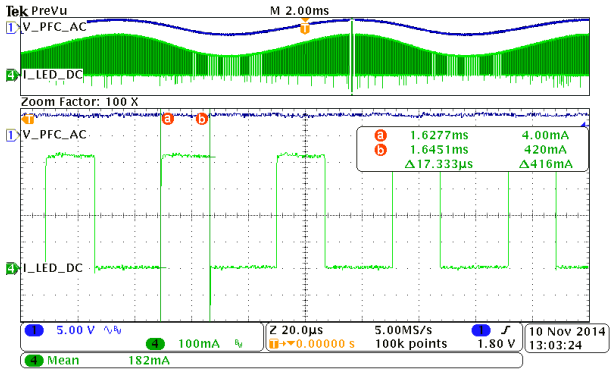


Fig. 16. LED current highlighting minimum duty cycle. CH1: PFC output voltage (ac coupled; 5 V/div; 20 $\mu$s/div). CH4: LED current (dc coupled; 100 mA/div; 20 $\mu$s/div).

cycle of 90% is programmed, and should occur at a current pulse of 195 mA. The peak duty cycle circuit is configured to adjust the output voltage to obtain this peak duty cycle. From the series resistance of the LED load, the current amplitude ripple is calculated to be 215 mA, leading to a maximum current pulse amplitude of 410 mA.

The waveform of the modulated LED current is presented in Fig. 14, along with its FFT result. The cursors in Fig. 14 highlight the dc and 120 Hz components of the FFT result. The varying duty cycles of the LED current are highlighted in Figs. 15 and 16, where the peak and minimum duty cycles have been isolated. The minimum current pulse of 200 mA, maximum current pulse of 420 mA, and current amplitude ripple of 220 mA all correspond to their calculated values.

Using the average current modulator, the 120-Hz component of the LED current has been reduced to 344 $\mu A_{rms}$, which leads to modulation index of 0.27% (344 $\mu$A $\times$ 1.414/177 mA). Use of the modulator has reduced the 120 Hz current ripple from 43% to 0.27%. It is important to note that the amplitude of the LED current pulses will vary at the low (twice line) frequency, but due to the modulation method, the LED current contains very little content at this low frequency.

The waveform of the modulated LED light is presented Fig. 17, along with its FFT result. The LED light modulation is highlighted in Figs. 18 and 19, where the peak and minimum duty cycles have been isolated.

Using the average current modulator, the 120-Hz component modulation index of the LED light is calculated as 9.1% (20.3 mV $\times$ 1.414/315 mV). Use of the modulator has reduced the 120 Hz light modulation index from 37.7% to 9.1%. This is below the limit proposed in [30] for low risk light flicker at 120 Hz. Due to the nonlinear relationship between LED current and luminous flux, the low-frequency light ripple has not been completely eliminated. It is noted that there has been a small decrease in the dc component of luminous flux with the use of the current modulator.

The measured efficiency of the LED drivers with and without the average current modulator is shown in Fig. 20, highlighting the low power loss associated with the proposed circuit. It is noted that there is $<$1% drop in efficiency between the conventional driver and with the added current modulator.

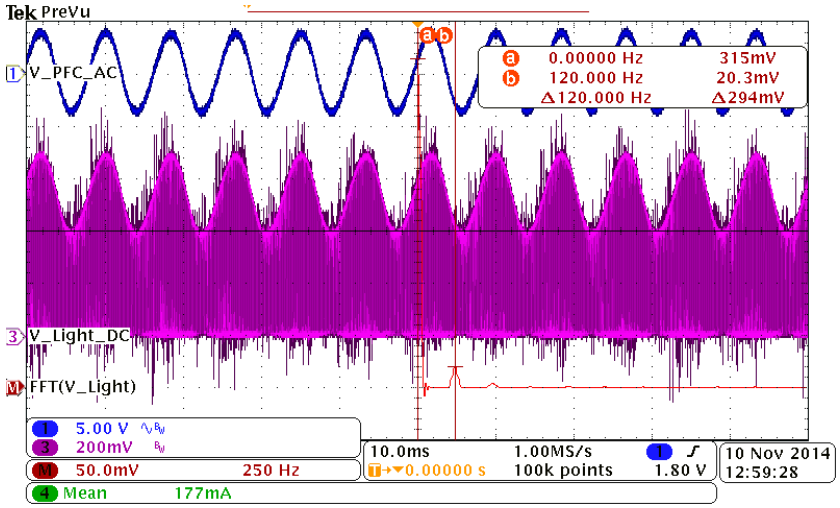


Fig. 17. Buck–boost output voltage ripple and LED light with average current modulator. CH1: PFC output voltage (ac coupled; 5 V/div; 10 ms/div). CH3: LED light (dc coupled; 200 mV/div; 10 ms/div). MATH: FFT of LED light (50 mV/div; 250 Hz/div).

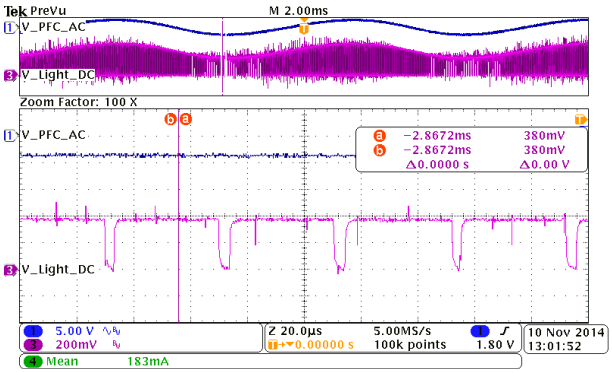


Fig. 18. LED light highlighting peak duty cycle. CH1: PFC output voltage (ac coupled; 5 V/div; 20 $\mu$s/div). CH3: LED light (dc coupled; 200 mV/div; 20 $\mu$s/div).

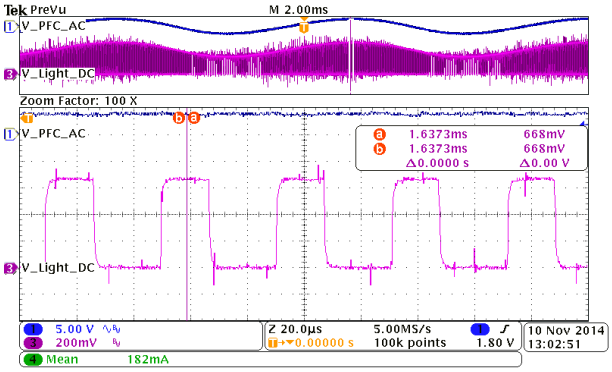


Fig. 19. LED light highlighting minimum duty cycle. CH1: PFC output voltage (ac coupled; 5 V/div; 20 $\mu$s/div). CH3: LED light (dc coupled; 200 mV/div; 20 $\mu$s/div).

The input current of the prototype was analyzed to ensure that high PF was achieved. The data in Fig. 21 show the measured PF of the buck–boost LED driver with and without the average current modulator. It is clear that there is very little if any difference between the PF of the two drivers. The waveforms in Fig. 22 show the input voltage and input current

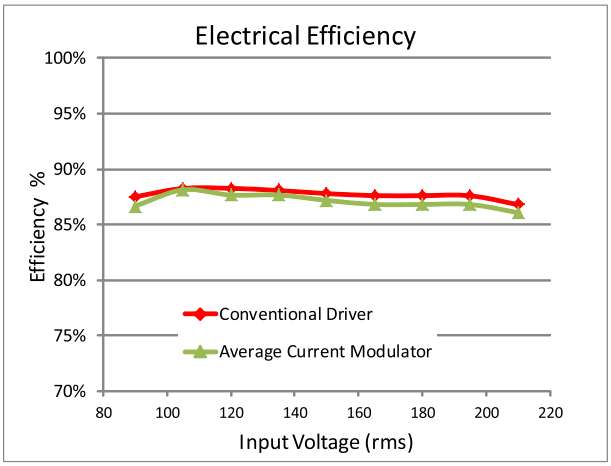


Fig. 20. Efficiency comparison of buck–boost PFC with and without average current modulator.

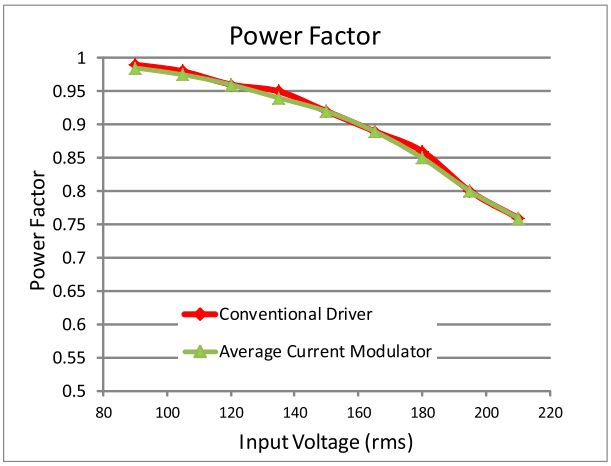


Fig. 21. PF comparison of buck–boost PFC with and without average current modulator.

of the buck–boost driver with the average current modulator at 120 $V_{rms}$ input. The input current shape matches the input voltage, illustrating a high PF.

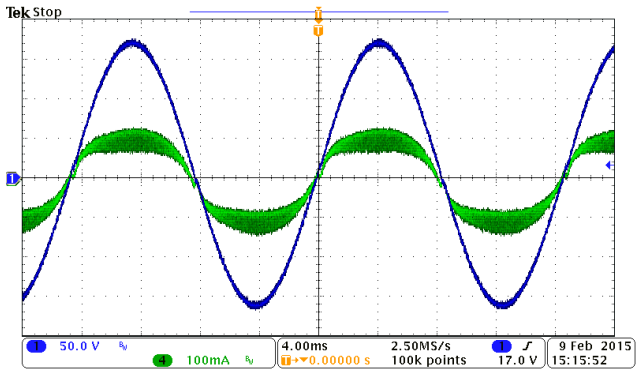


Fig. 22. Input waveforms of buck–boost driver with the average current modulator. CH1: input voltage (dc coupled; 50 V/div; 4 ms/div). CH4: input current (dc coupled; 100 mA/div; 4 ms/div).

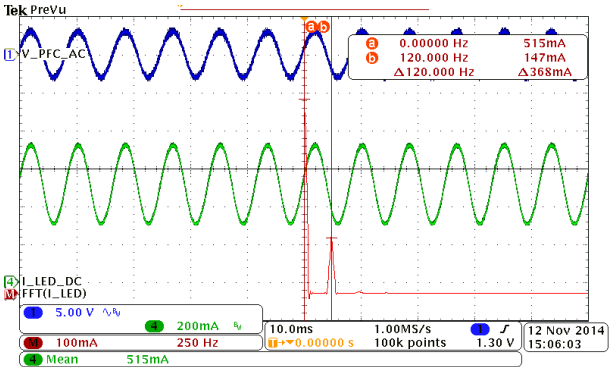


Fig. 23. Conventional flyback LED driver—LED current. CH1: PFC output voltage (ac coupled; 5 V/div; 10 ms/div). CH4: LED current (dc coupled; 200 mA/div; 10 ms/div). MATH: FFT of LED current (100 mA/div; 250 Hz/div).

The average current modulator with output voltage adjustment has been shown to reduce the low-frequency LED current ripple without requiring a change in the PFC circuit output capacitance. Similarly, the average current modulator can be used to reduce the output capacitance of a single-stage PFC LED driver without affecting the low-frequency LED current ripple.

The buck–boost prototype LED driver with the average current modulator has limited the low-frequency LED current to 344 $\mu A_{rms}$ using only a 56 $\mu$F capacitor. Without the average current modulator, the LED driver would require a 12 770 $\mu$F capacitor to limit the low-frequency LED current to 344 $\mu A_{rms}$. This value is calculated from (10).

### *B. 25-W (50 V/0.5 A) Flyback Prototype With Average Current Adjustment*

An isolated flyback prototype was designed to demonstrate the operation of the current modulator with an average current adjustment for peak duty cycle control. The output of this prototype is designed to operate at ~50 V/500 mA for a 25 W of power from a 60 Hz ac power supply. The OSRAM Golden Dragon Plus LUW-W5AM LED is used as the LED load. Rated for a maximum current of 1 A, the LEDs exhibit a forward voltage of 2.1 V and a series

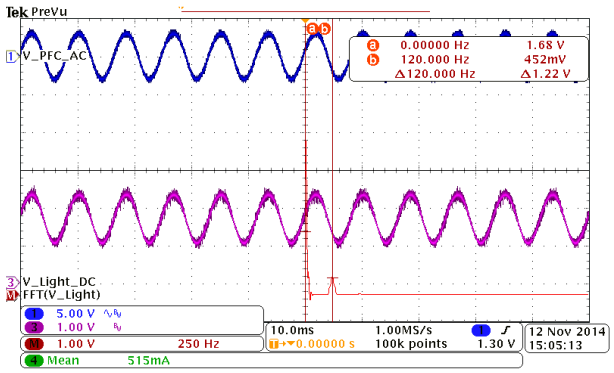


Fig. 24. Conventional flyback LED driver—LED light. CH1: PFC output voltage (ac coupled; 5 V/div; 10 ms/div). CH3: LED light (dc coupled; 1 V/div; 10 ms/div). MATH: FFT of LED light (1 V/div; 250 Hz/div).

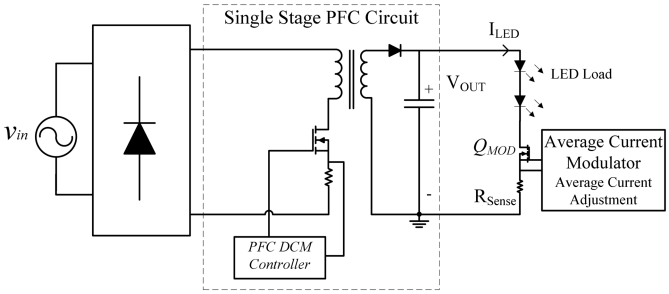


Fig. 25. Placement of average current modulator within flyback driver.

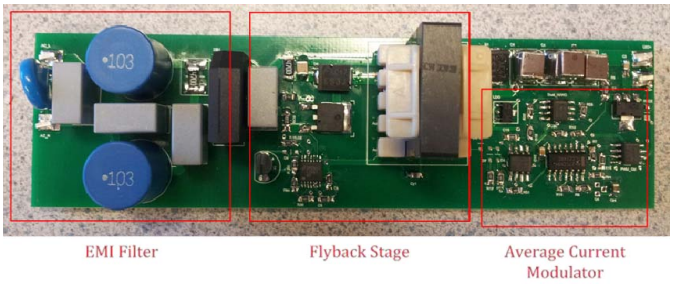


Fig. 26. Photo of flyback prototype with the average current modulator.

resistance of 0.67 Ω at 500 mA. The LED load is configured with 20 LED chips, thus the resistance of the entire LED load is 13.4 Ω.

A conventional single-stage PFC flyback LED driver was built and analyzed to provide a reference to measure the performance of the proposed average current modulator. The flyback PFC circuit is designed and implemented with the FL7732 PSR PFC Controller [37] from Fairchild. The waveforms of LED current and light are presented in Figs. 23 and 24, respectively. The FFT results of these waveforms provide a metric to compare the attenuation of low-frequency current and light ripple of the LED load between the two power supplies. The energy storage capacitance from the design procedure in Section V is used, which was calculated to be 198 $\mu$F. Three 68 $\mu$F capacitors are used in the lab for a total of 204 $\mu$F.

With the conventional flyback LED driver, the LED load has a 120 Hz ripple current of 147 $mA_{rms}$ with a

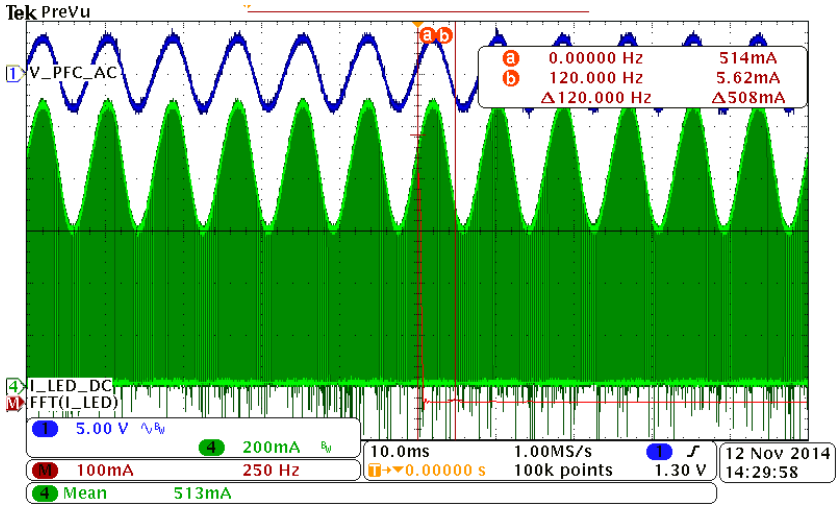


Fig. 27. Flyback output voltage ripple and LED current with average current modulator. CH1: PFC output voltage (ac coupled; 5 V/div; 10 ms/div). CH4: LED current (dc coupled; 200 mA/div; 10 ms/div). MATH: FFT of LED current (100 mA/div; 250 Hz/div).

dc current of 515 mA, or a modulation index of 40% (147 mA × 1.414/515 mA). Similarly, the modulation index for the LED light is 38% (452 mV × 1.414/1.68 V).

The average current modulator is connected to the LED driver in the laboratory to reduce the low-frequency current ripple of the LED load. The block diagram of the flyback PFC stage with the modulator added is shown in Fig. 25. A 10 nF capacitor is connected across the LED load to prevent the voltage spikes caused by the modulation method. The voltage across this small capacitor is not discharged by the modulation method and therefore has no effect on efficiency. The modulator is set to a modulation frequency of 25 kHz. The components used to configure the modulator are the same as before, listed in Table II. The photo in Fig. 26 shows the flyback prototype with the average current modulator. A peak duty cycle of 90% is programmed, which should occur at a current pulse of 555 mA. From the series resistance of the LED load, the current amplitude ripple is calculated to be 447 mA, leading to an estimated peak current pulse of ∼1 A.

The operation of the PFC flyback circuit is completely independent of the average current modulator, and there is no connection between the two circuits. The average LED current is dictated by the primary side flyback controller, while the average current modulator operates to eliminate the low-frequency LED current content. The peak duty cycle circuit in this method adjusts the modulator's current reference to achieve the desired peak duty cycle of 90%.

The waveform of the modulated LED current is presented in Fig. 27, along with its FFT result. The cursors in Fig. 27 highlight the dc and 120 Hz components of the FFT result. The varying duty cycles of the LED current are highlighted in Figs. 28 and 29, where the peak and minimum duty cycles have been isolated. The minimum current pulse of 588 mA, maximum current pulse of 1.07 A, and current amplitude ripple of 482 mA all correspond to their calculated values.

Using the average current modulator, the 120 Hz component of the LED current has been reduced to 5.62 $mA_{rms}$, with a current modulation index of 1.54% (5.62 mA × 1.414/514 mA). Use of the modulator has reduced

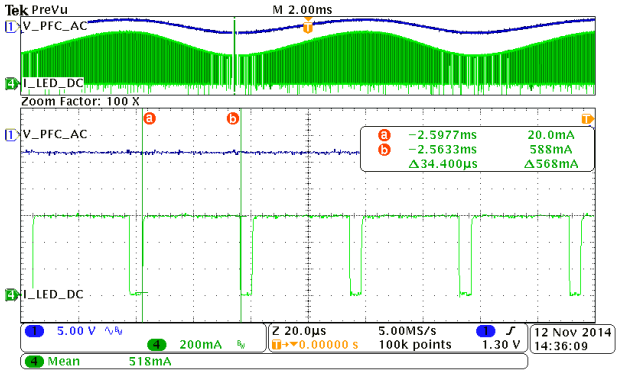


Fig. 28. LED current highlighting peak duty cycle. CH1: PFC output voltage (ac coupled; 5 V/div; 20 $\mu$s/div). CH4: LED current (dc coupled; 200 mA/div; 20 $\mu$s/div).

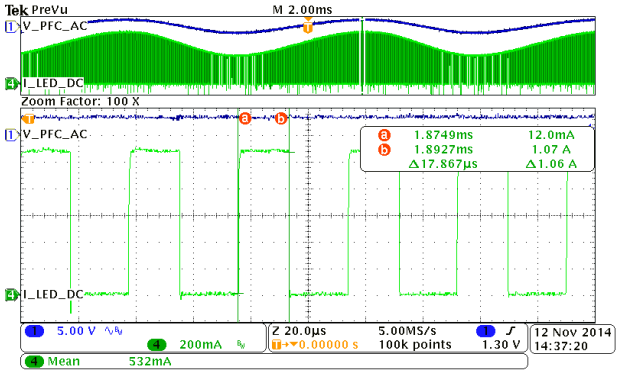


Fig. 29. LED current highlighting minimum duty cycle. CH1: PFC output voltage (ac coupled; 5 V/div; 20 $\mu$s/div). CH4: LED current (dc coupled; 200 mA/div; 20 $\mu$s/div).

the 120 Hz current modulation index from 40% to 1.54%. It is important to note that the amplitude of the LED current pulses will vary at the low (twice line) frequency, but due to the modulation method, the LED current contains very little content at this low frequency.

The waveform of the modulated LED light is presented in Fig. 30, along with its FFT result. The LED light modulation

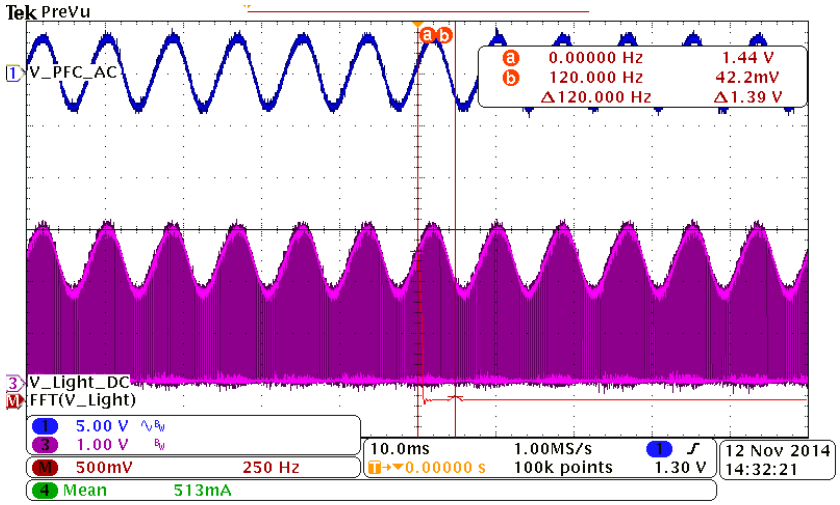


Fig. 30. Flyback output voltage ripple and LED light with average current modulator. CH1: PFC output voltage (ac coupled; 5 V/div; 10 ms/div). CH3: LED light (dc coupled; 1 V/div; 10 ms/div). MATH: FFT of LED light (500 mV/div; 250 Hz/div).

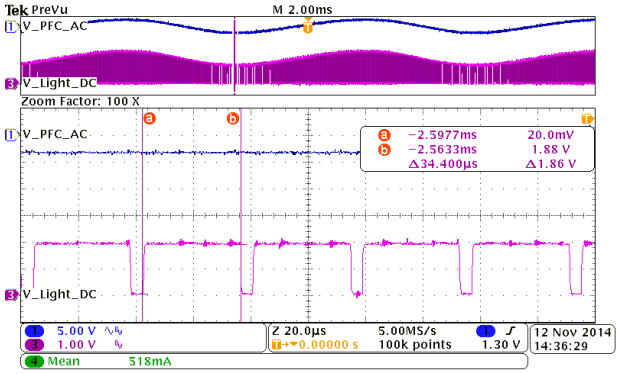


Fig. 31. LED light highlighting peak duty cycle. CH1: PFC output voltage (ac coupled; 5 V/div; 20 $\mu$s/div). CH3: LED light (dc coupled; 1 V/div; 20 $\mu$s/div).

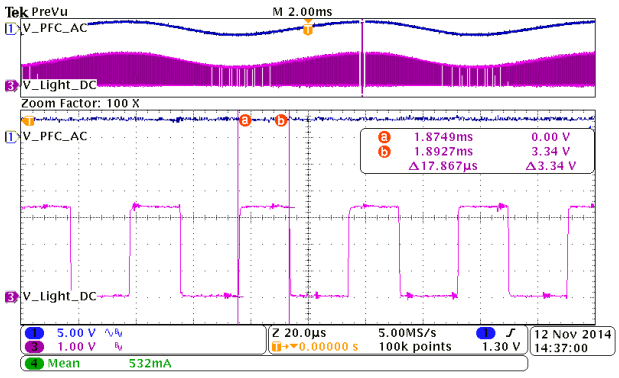


Fig. 32. LED light highlighting minimum duty cycle. CH1: PFC output voltage (ac coupled; 5 V/div; 20 $\mu$s/div). CH3: LED light (dc coupled; 1 V/div; 20 $\mu$s/div).

is highlighted in Figs. 31 and 32, where the peak and minimum duty cycles have been isolated.

Using the average current modulator, the 120 Hz component of the LED light modulation index is calculated to be 4.1% (42.2 mV $\times$ 1.414/1.44 V). Use of the average current modulator has reduced the 120 Hz light modulation index from 38% to 4.1%. This is well below the limit proposed

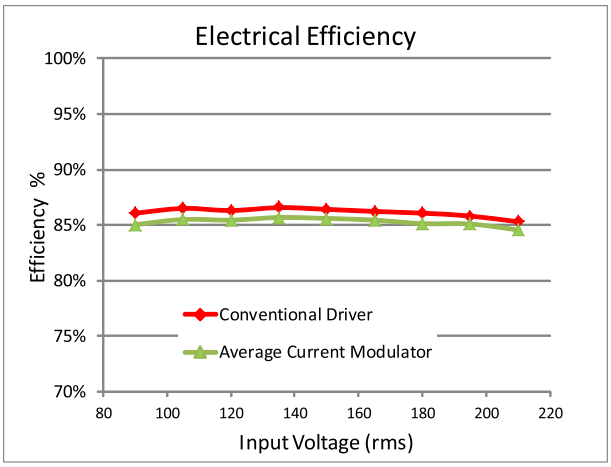


Fig. 33. Efficiency comparison of flyback driver with and without average current modulator.

in [30] for low risk light flicker at 120 Hz. Due to the nonlinear relationship between LED current and luminous flux, the low-frequency light ripple has not been completely eliminated. It is noted that there has been a small decrease in the dc component of luminous flux with the use of the current modulator.

The measured efficiency of the LED drivers with and without the average current modulator is shown in Fig. 33, highlighting the low power loss associated with the proposed circuit. It is noted that there is $<$1% drop in efficiency with the added current modulator. From the data in Figs. 20 and 33, it is demonstrated that the average current modulator can be utilized in low- and medium-power applications with minimal power loss.

The input current of the prototype was analyzed to ensure that high PF was achieved. The data in Fig. 34 show the measured PF of the flyback LED driver with and without the average current modulator. It is clear that there is very little if any difference between the PF of the two drivers. The waveforms in Fig. 35 show the input voltage and input current of the flyback driver with the average current

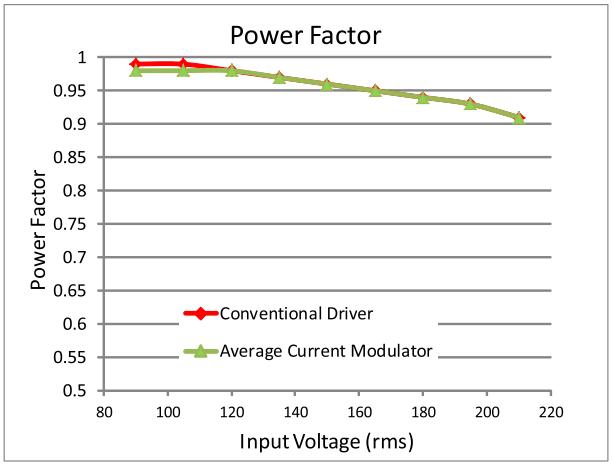


Fig. 34. PF comparison of flyback driver with and without average current modulator.

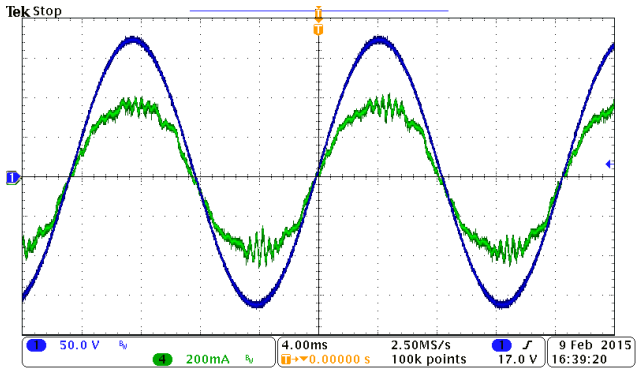


Fig. 35. Input waveforms of flyback driver with the average current modulator. CH1: input voltage (dc coupled; 50 V/div; 4 ms/div). CH4: input current (dc coupled; 200 mA/div; 4 ms/div).

modulator at 120 $V_{rms}$ input. The input current shape matches the input voltage, illustrating a high PF.

The average current modulator with average current adjustment has been shown to reduce the low-frequency LED current ripple without requiring a change in the PFC circuit output capacitance. Similarly, the average current modulator can be used to reduce the output capacitance of a single-stage PFC LED driver without affecting the low-frequency LED current ripple.

The flyback prototype LED driver with the average current modulator has limited the low-frequency LED current to 5.62 $mA_{rms}$ using only a 204 $\mu$F capacitor. Without the average current modulator, the LED driver would require a 6410 $\mu$F capacitor to limit the low-frequency LED current to 5.62 $mA_{rms}$. This value is calculated from (10).

## VII. Conclusion

The average current modulation method proposed within this paper presents a novel control technique for driving LEDs from single-stage PFC circuits. It provides minimized low-frequency LED current with reduced PFC energy storage capacitance, allowing the use of ceramic or film-type capacitors for a long lifespan operation. A peak duty cycle control method is implemented within the average current modulator to limit the maximum LED current pulse, preventing damage to the LED load. Experimental results of lab-tested prototypes show that the low-frequency current ripple can be limited to 1.5% or less, and that the low-frequency light ripple is limited below the tolerated boundaries defined by the industry. Requiring only a single low-voltage MOSFET, current sense resistor, and simple control circuit, the component cost is kept very low. Limited power loss leads to an efficiency drop of <1% compared with conventional LED drivers. Minimal change in the PF is observed between the conventional driver and with the average current modulator. The prototypes built illustrate that this high performance can be achieved for low and medium power levels, with both isolated and nonisolated power circuits.

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