A Flicker-Free Single-Stage Offline LED Driver With High Power Factor

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***Abstract*— A conventional offline single-stage light-emitting diode (LED) driver with a high power factor usually produces a significant twice-line-frequency ripple LED current, where the ripple LED current is presented as flickering to human eye. This paper introduces a ripple cancellation method to remove the twice-line-frequency voltage ripple for an offline single-stage LED driver with a power factor correction. Consequently, a dc LED current can be produced to achieve flicker-free LED driving performance. At the same time, the required storage capacitor for the proposed LED driver can be greatly reduced, and the circuit implementation to achieve ripple cancellation is simple. Thus, the overall cost of the proposed LED driver is low. The proposed LED driver also features high efficiency because of its power structure. A 35-W Flyback experimental prototype and a 10-W Buck–Boost experimental prototype have been built to validate the proposed design and demonstrate its optimal performance.**

***Index Terms*— Flicker-free light-emitting diode (LED) driving, high power factor, ripple cancellation, single-stage power conversion.**

I. Introduction

LIGHT-EMITTING diodes (LEDs) become an increasingly popular light source choice because of their high efficacy, low power consumption, and long lifespan compared with conventional incandescent alternatives. The LED lighting market is anticipated to continue to experience strong growth. It is predicted that ~70% of $100 billion lighting market will be occupied by LED lighting by 2020 [1]–[3].

However, LEDs are especially susceptible to flickering due to their low intrinsic resistance. A very small ripple voltage applied to an LED results in a significant ripple current, which is almost proportionally presented as flicker. It was revealed that excessive flicker is very harmful to human health, which can lead to fatigue, headache, malaise, vision impairment, and other health related issues [4]. It was advised that the percent of flicker should be restricted to a certain level so that the lighting environment can be considered low risk [6]. For an offline LED driver, the most significant flicker commonly occurs at twice the line frequency. In North America, where the line frequency is 60 Hz, flicker at 120 Hz should be restricted within 10% of the averaged lighting output to be considered low risk. Similarly, in Europe and Asia, where the line frequency is 50 Hz, flicker at 100 Hz should be restricted with 8% of the averaged lighting output.

LED light fixture manufacturers face a dilemma to choose between the single-stage LED driver and the two-stage LED driver. High efficiency and low cost can be achieved with the single-stage LED driver. However, the downside of the single-stage LED driver is the significant flicker it produces. It is not very likely that the single-stage LED driver can achieve the above suggested low-risk flicker criteria with reasonable output capacitors. The two-stage LED driver, depending on how it is designed, can usually significantly reduce the level of flicker. It can even naturally achieve the so-called flicker-free LED driving. However, the additional power stage increases the component cost and reduces the efficiency of the overall system.

Because of the large economic impact and the related health concerns of LED lighting, there is an urge to come up with a solution that can combine the advantages from both the single-stage LED driver (low cost) and the two-stage LED driver (no flicker) while avoiding their respective drawbacks.

The method of integrating the first power factor correction (PFC) stage and the second LLC stage LED driving was presented in [7]. It achieved a reduced component count compared with a standard two-stage LED driver. However, this method has a few limitations. First of all, the shared MOSFETs need to be very carefully driven so that they can achieve PFC for the first stage and dc–dc conversion for the second stage at the same time. A lot of restrictions are applied to drive these MOSFETs. It is difficult to achieve design optimization for each stage. Second, the intermediate dc bus voltage cannot be well regulated. Under the high line input and the light load output condition, the dc bus voltage can be very high, which imposes too much voltage stress on the related power components.

The method of active energy storage LED driving was presented in [8]. A bidirectional dc–dc converter works as an active energy storage device, and is connected in parallel with the LED load. This method can achieve a dc LED current output and reduce output storage capacitor. However, in a half line cycle, the amount of energy that is converted back and forth by the bidirectional dc–dc converter is equal to $T \times P_{\text{out}}/\pi$, where T is the period of a half line cycle. This means, on average, P_{out}/π amount of power is converted three times before it reaches to the output, which introduces significant power loss. In addition, the bidirectional dc–dc converter needs high-voltage rating MOSFETs to implement, which also increases component cost.

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The method of injecting harmonics input current was presented in [9] and [10]. The low-frequency LED ripple current can be reduced with this method. It is a cost-effective solution, since no change is needed on the power stage circuit. The limitation of this method is that flicker cannot be completely eliminated, and at the same time, the power factor is significantly reduced.

The method of combining input current regulation and active energy storage was presented in [11]. The input current is regulated to be a constant instead of following the input voltage in this scheme, which results a lower amount of energy imbalance between the input side and the output side in a half line cycle. The active energy storage circuit (bidirectional converter) processes less power as compared with how much it processed in [8]. However, this method also scarifies power factor performance, and the amount of power loss introduced by the active energy storage circuit is still significant.

The method of ripple cancellation to achieve a high power factor and a dc LED current driving performance was presented in [12] and [13]. A ripple cancellation converter (RCC) has been used to produce an opposite low-frequency ripple voltage to cancel the ripple voltage from the PFC. A dc LED voltage as well as a dc LED current can be obtained with this method while maintaining a high power factor. However, this method suffers from the following problems: 1) high voltage stress for the RCC; and 2) a grounding issue exists in this method because the PFC output also serves as the input voltage for the RCC. Only Buck–Boost or isolated topologies can be used to build the RCC.

These previously presented solutions show advantages over the conventional designs to some extent. However, on the other hand, they all have limitations or introduce new issues. In this paper, a new ripple cancellation method for the single-stage LED driving is proposed. Compared with the method presented in [12] and [13], an isolated auxiliary voltage, which is much smaller than the PFC main output, is produced by the PFC. The auxiliary voltage, instead of the PFC main output, is used as the input voltage for the RCC. This arrangement introduces several advantages. First of all, the grounding issue has been solved. As a result, the RCC can be built with, but not limited to, Buck topology to achieve a higher efficiency and a lower cost instead of using Buck–Boost or any isolated topologies. The voltage stress for the RCC is also greatly reduced because of its lower input voltage. Lower voltage rating power components can be used in the RCC to reduce cost. Furthermore, integrated switching regulators, which include MOSFETs, controller, and gate driver in a single chip, are widely available to implement the low-cost RCC. Another very practical advantage with using Buck topology to build the RCC is achieving a very good ripple cancellation result. With Buck topology, in general, the control loop can be designed faster than other isolated topologies that need an optocoupler in the feedback or a Buck–Boost converter with an right half plane zero (under continuous conduction mode) in the control loop. This way, the Buck RCC can track its twice line frequency reference voltage relatively better.

The proposed LED driver combines the advantages from both the single-stage and the two-stage LED drivers.

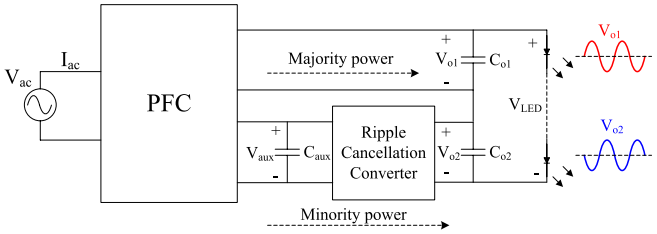


Fig. 1. Generic power stage structure of the proposed ripple cancellation LED driver.

More importantly, this solution is straightforward and does not introduce new issues. A Flyback-based experimental prototype and a Buck–Boost-based experimental prototype have been built to verify the proposed method.

This paper is organized as follows. Section II describes the operating principle of the proposed ripple cancellation LED driver and its advantages. Section III discusses the critical design considerations of the proposed LED driver. The experimental result is shown in Section IV. Finally, the conclusion is drawn in Section V.

II. Operating Principle

In this section, the detailed operation of the proposed LED driver as well as its advantages will be discussed.

A. Power Stage Structure

For a single-stage LED driver with a high power factor, its output voltage usually has a large ripple at twice the line frequency. This ripple voltage produces an even more significant ripple current through LEDs. The fundamental concept of the proposed LED driver is to cancel the twice line frequency ripple voltage from a single-stage LED driver. An opposite ripple voltage is produced by another miniature power converter and is connected in series with the PFC output. As a result, a dc voltage is obtained and applied to the LEDs to produce a dc LED current.

Fig. 1 shows the generic power stage structure of the proposed ripple cancellation LED driver. A PFC transfers the energy from the input to the output, and also achieves a high power factor for the system. The PFC can be built with topologies, such as Flyback or Buck–Boost, since their output voltages are not limited by their input voltages, which can be as low as required to drive LEDs. The PFC has two outputs: 1) a main output V_{o1}; and 2) an auxiliary output V_{aux}. The main output V_{o1} delivers the majority of the output power. As a result, it contains a large voltage ripple at twice the line frequency. V_{aux} is the input voltage for the followed RCC. The key point is to control the ripple voltage of the RCC output voltage V_{o2} so that it has the same magnitude, but out of phase, to the low-frequency ripple voltage of the main output V_{o1}. As a result, the low-frequency ripple voltage from V_{o1} is cancelled. It should be noted that the portion of power delivered to the output through V_{o2} has been processed twice. This part of power is first processed by the PFC, and then processed by the RCC. In order to achieve high efficiency,

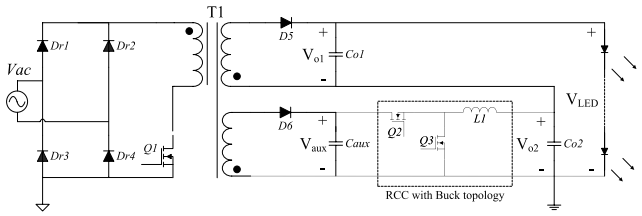


Fig. 2. Power stage of the proposed Flyback-based ripple cancellation LED driver.

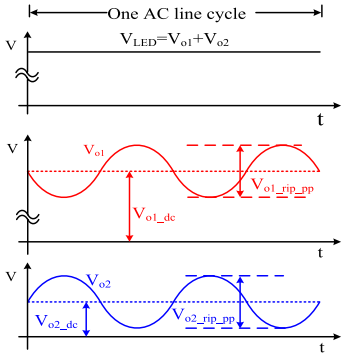


Fig. 3. Critical waveforms of the proposed LED driver.

the power delivered to the output through V_{o2} should be minimized.

Fig. 2 shows the power stage implementation of the proposed ripple cancellation LED driver based on Flyback topology. The RCC is implemented with Buck topology to achieve low cost and optimal performance. The RCC can also be implemented by other power topologies as necessary.

Fig. 3 shows the critical waveforms of the proposed ripple cancellation LED driver. Because a high power factor is achieved with the proposed LED driver, the input power waveform contains a large ripple at twice the line frequency. This low-frequency ripple is passed to the main output of the PFC and creates a same frequency ripple voltage on V_{o1}. V_{o1} can be expressed as

$$V_{o1}(t) = V_{o1\_dc} + V_{o1\_rip}(t). \tag{1}$$

In (1), V_{o1_dc} and $V_{o1\_rip}(t)$ represent the dc component and the twice line frequency ripple of V_{o1}, respectively. On the other hand, the output voltage of the RCC V_{o2} has an opposite low-frequency ripple voltage to V_{o1}. V_{o2} can be expressed as

$$V_{o2}(t) = V_{o2\_dc} + V_{o2\_rip}(t). \tag{2}$$

In (2), V_{o2_dc} and $V_{o2\_rip}(t)$ represent the dc component and the twice line frequency ripple of V_{o2}, respectively. It should be noted that V_{o2_dc} is much smaller than V_{o1_dc} in a design. Because the higher V_{o2_dc} is, the more power is processed by the RCC, and the lower the overall efficiency will be. V_{o2_dc} should be designed just enough to provide bias voltage to keep V_{o2} positive.

Since $V_{o1\_rip}(t)$ and $V_{o2\_rip}(t)$ are the same in amplitude and opposite in sign, their relationship can be expressed as

$$V_{o1\_rip}(t) = -V_{o2\_rip}(t). \tag{3}$$

The sum of V_{o1} and V_{o2}, which is the voltage applied to the LED load, can be expressed as

$$V_{LED} = V_{o1}(t) + V_{o2}(t) = (V_{o1\_dc} + V_{o2\_dc}) + [V_{o1\_rip}(t) + V_{o2\_rip}(t)]. \tag{4}$$

Substitution of (3) into (4) leads to

$$V_{LED} = V_{o1}(t) + V_{o2}(t) = V_{o1\_dc} + V_{o2\_dc}. \tag{5}$$

Equation (5) reveals that the voltage applied to the LED load is a dc voltage and is equal to the sum of V_{o1_dc} and V_{o2_dc}.

B. System Efficiency

Another advantage of the proposed LED driver is its high efficiency. Most of the output power is delivered directly by the PFC through V_{o1}, and this part of power has only been processed once. Only the part of power that is delivered to the output through V_{o2} has been processed twice, and this portion is very small in a typical design.

Assuming that the PFC delivers power to the output via V_{o1} and V_{aux} with the same efficiency, the theoretical overall efficiency of the proposed LED driver can be then expressed as

$$\eta_{pd} = \frac{P_{out}}{P_{in}} = \frac{P_{LED}}{\frac{P_{o1\_avg}}{\eta_{pfc}} + \frac{P_{o2\_avg}}{\eta_{pfc} \times \eta_{RCC}}}. \tag{6}$$

In (6), η_{pd}, η_{pfc}, and η_{RCC} represent the overall efficiency of the proposed LED driver, the efficiency of the PFC, and the efficiency of the RCC, respectively. P_{LED}, P_{o1_avg}, and P_{o2_avg} represent the total output power for the LED load, the average power delivered to the LED load via V_{o1}, and the average power delivered to the LED load via V_{o2}, where P_{LED}, P_{o1_avg}, and P_{o2_avg} can be also expressed as

$$P_{LED} = (V_{o1\_dc} + V_{o2\_dc}) \times I_{LED} \tag{7}$$

$$P_{o1\_avg} = V_{o1\_dc} \times I_{LED} \tag{8}$$

$$P_{o2\_avg} = V_{o2\_dc} \times I_{LED}. \tag{9}$$

Substitution of (7)–(9) into (6) leads to

$$\eta_{pd} = \frac{P_{out}}{P_{in}} = \frac{V_{o1\_dc} + V_{o2\_dc}}{\frac{V_{o1\_dc}}{\eta_{pfc}} + \frac{V_{o2\_dc}}{\eta_{pfc} \times \eta_{RCC}}}. \tag{10}$$

In order to keep $V_{o2}(t)$ always positive, V_{o2_dc} must be larger than the amplitude of the peak low-frequency ripple of V_{o1}. As a design guideline, V_{o2_dc} can be designed to be

$$V_{o2\_dc} = 1.1 \times \frac{1}{2} V_{o1\_rip\_pp}. \tag{11}$$

Then, (10) can be rewritten as

$$\eta_{pd} = \eta_{pfc} \times \frac{\left(\frac{1}{RF}\right)}{\left(\frac{1}{RF} - 1.1\right) + \frac{1.1}{\eta_{RCC}}} \tag{12}$$

where RF is the ripple factor (RF) and is defined as

$$RF = \frac{V_{o1\_rip\_pp}}{V_{LED}}. \tag{13}$$

Equation (12) can also be further presented as

$$\eta_{pd} = \eta_{pfc} \times \eta_{eq} \tag{14}$$

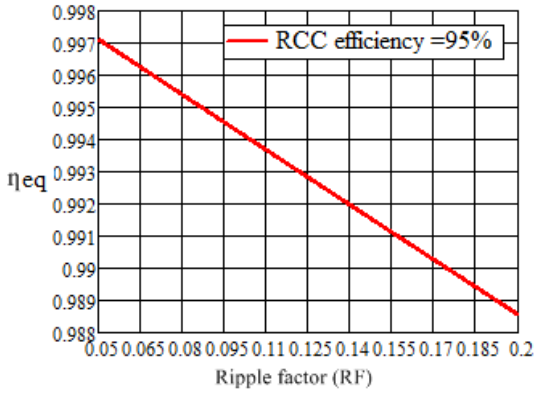


Fig. 4. Relationship between RF and η_{eq}.

where

$$\eta_{eq} = \frac{\left(\frac{1}{RF}\right)}{\left(\frac{1}{RF} - 1.1\right) + \frac{1.1}{\eta_{RCC}}}. \quad (15)$$

In (14), the overall efficiency of the proposed LED driver is presented as a multiplication of the single-stage PFC efficiency, η_{PFC}, and an equivalent efficiency, η_{eq} as defined in (15). Since the proposed LED driver does not has impact on the efficiency of the PFC itself, it is η_{eq} that should be increased to achieve a higher overall efficiency. As shown in (15), the RF has the effect to change η_{eq}. Fig. 4 plots the relationship between η_{eq} and the RF when η_{RCC} is 0.95.

The RF changes from 0.05 to 0.2 in Fig. 4, which means that the peak-to-peak (pk–pk) twice line frequency ripple voltage changes from 2.5 to 10 V when the LED voltage is 50 V. As the RF increases, η_{eq} decreases and so does the overall efficiency of the proposed LED driver. This is because a higher V_{o2_dc} is needed in the design to cover the higher V_{o2} voltage ripple (the same in amplitude as V_{o1} voltage ripple), and leads to more power being processed by the RCC. Therefore, in order to achieve high efficiency, the RF should be carefully selected. When the efficiency of the RCC is quite high, the RF can be selected to be quite large without reducing much system efficiency. For example, when η_{RCC} is 0.95, η_{eq} is as high as 0.988 even the RF is 0.2. When the efficiency of the RCC is moderate, a smaller RF should be selected.

With η_{eq} to be 0.98 and assuming the efficiency of the PFC is 90%, the overall efficiency of the proposed LED driver will be 88.9%, or 1.1% lower. On the other hand, in a two-stage (a Flyback PFC followed by a Buck converter) solution [34], the overall efficiency will be 85.5% assuming the efficiency of the Buck converter is also 95%. Therefore, the proposed LED driver can achieve high efficiency much easier than a conventional two-stage LED driver.

C. Implementation Cost

Another advantage of the proposed LED driver comes from the low-cost implementation of the RCC. Since the RCC only processes a small portion of the output power (generally 10% or less) and its voltage stress is also much lower than the LED voltage, integrated switching regulators, which includes MOSFETs, controller, and gate driver, are widely available

TABLE I
COMPONENT COMPARISON BETWEEN THE SECOND-STAGE DC–DC AND THE RCC

Components	Second stages DC/DC	RCC
Buck MOSFET	Discrete MOSFET with up to 70V rating	15V input, 1A output integrated switching regulator such as TPS54620, FAN2013, LM2651
Buck diode	Discrete diode with up to 70V rating	
Buck high side driver	FA5650 high side and low side driver	
Buck PWM controller	UC2843	
Buck inductor	RCP1317NP-470MMT, 47uH, 69mohm, 13.5mm diameter, 17.5mm (high)	IHLP2020CZER4R7M11. 4.7uH, 54mohm, 5.2mm x 5.5mm x 3mm (high)
Buck output capacitor	470μF, 63V electrolytic	20μF/16V ceramic

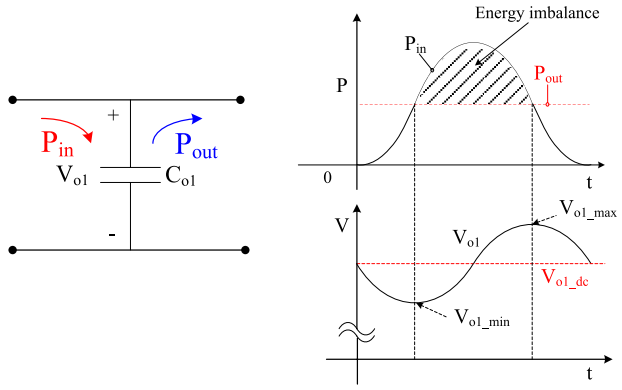


Fig. 5. Energy imbalance between input and output and the resulted V_{o1} ripple.

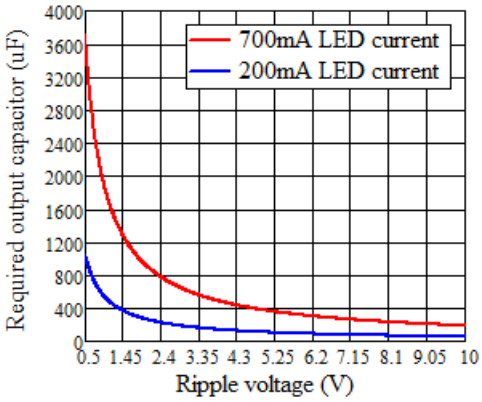
to implement the RCC. Comparatively, in a conventional two-stage LED driver, the second-stage dc–dc converter needs to process 100% of the output power, and withstand a voltage stress no less than the LED voltage. Discrete components are usually needed to build the second-stage dc–dc converter. In addition, the passive components, such as the filter inductor and capacitor used in the RCC, are also smaller than they are used in the second-stage dc–dc converter. Therefore, the proposed LED driver can achieve much lower cost. Table I shows the component comparison between the second-stage dc–dc converter and the RCC under 50 V/0.7-A output application as an example.

D. Storage Capacitor Requirement

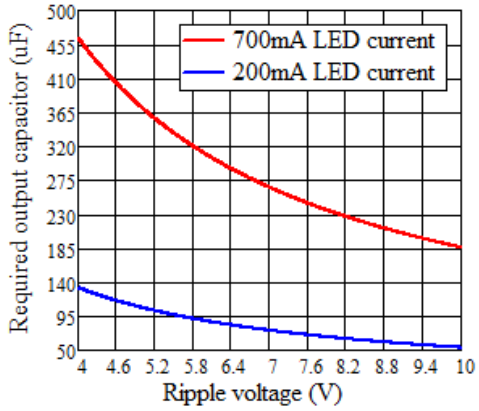
Another advantage of the proposed LED driver is the significant reduction on the storage capacitor. The capacitor C_{o1} of the PFC output V_{o1} is used to buffer the energy imbalance between the input and the output in a half-line cycle as shown

TABLE II
REQUIRED CAPACITOR FOR A CONVENTIONAL SINGLE-STAGE LED DRIVER TO LIMIT 10% RIPPLE CURRENT

Item	$R_i(\Omega)$	$V_F(V)$	Required LEDs	$R_{i\_total}(\Omega)$	Output	P-P ripple voltage (V) causing 10% ripple current	Required capacitor
LED load 1	0.28	2.69	17	4.76	49.0V/0.7A	0.68Vpp	2700μF
LED load 2	0.21	2.65	18	3.78	50.3V/0.7A	0.52Vpp	3570 μF



(a)



(b)

Fig. 6. Required capacitance for C_{o1} under different pk–pk V_{o1} ripple amplitude. (a) pk–pk ripple amplitude change from 0.5 to 10 V. (b) Zoomed-in-view of (a).

in Fig. 5. The higher value of the capacitance, the smaller amplitude will be the twice line frequency ripple on V_{o1}. The twice line frequency ripple of V_{o1}, $V_{o1\_rip\_pp}$ and the output capacitor C_{o1} of the PFC have an approximate relationship of

$$C_{o1} \approx \frac{I_{LED}}{2 \times \pi \times f_{line} \times V_{o1\_rip\_pp}}. \quad (16)$$

Equation (16) reveals that if a higher $V_{o1\_rip\_pp}$ is allowed in the design, a lower capacitance of C_{o1} can be used. For the proposed LED driver, the twice line frequency ripple voltage from V_{o1} is not directly applied to the LED load. Ripple cancellation is achieved and it is a dc voltage that is applied to the LED load. Therefore, $V_{o1\_rip\_pp}$ can be designed to be fairly large, such as 10 V pk–pk, without causing a large current ripple. In other words, a much smaller capacitor C_{o1} can be used in the proposed LED driver. The required capacitance for C_{o1} under different amplitudes of V_{o1} ripple voltage is plotted in Fig. 6.

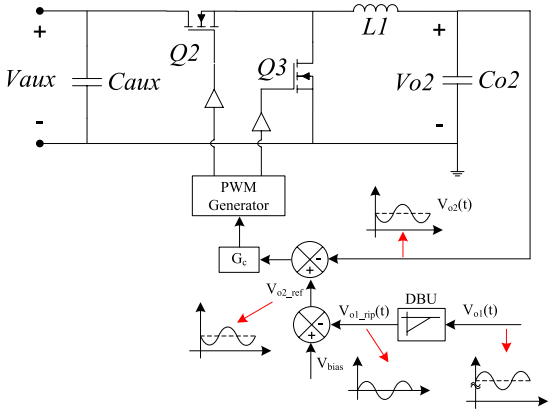


Fig. 7. Control diagram of the RCC.

When the pk–pk ripple voltage of V_{o1} is designed to be 10 V, the output capacitor can be reduced below 200 μF under the 700-mA LED current curve. The output capacitor can be even reduced to 53 μF under the 200-mA LED current curve. For low-voltage applications, this amount of capacitance can be implemented by low-cost and long lifespan ceramic capacitors.

Comparatively, for a conventional single-stage LED driver, the low-frequency ripple voltage is directly applied to the LED load. This ripple voltage further produces a much more excessive ripple LED current because of the low resistance of the LED load. Therefore, much larger storage capacitor is required to limit the low-frequency ripple voltage and current in a conventional single-stage LED driver design.

Table II shows the parameter of two LED loads. From the left to the right, listing the intrinsic resistance of each LED, its forward voltage, the number of LEDs to make the LED load, the total resistance of the LED load, the operating condition of the LED load, the pk–pk ripple voltage that can cause 10% of ripple current, and the required capacitor to limit ripple current to 10%. Both LED loads are driven under the condition of 50 V/0.7 A by a conventional single-stage LED driver. For the LED load 1, the ripple voltage should be controlled below 0.68 V to achieve <10% ripple current. For the LED load 2, the ripple voltage should be controlled below 0.52 V. This means a capacitor value of 2700 or 3570 μF [the required capacitor can be calculated with (16)] is needed to limit the 120-Hz LED ripple current to 10%. With the ripple cancellation method proposed in this paper, a capacitor with a value of 200 μF can achieve even lower twice line frequency ripple current. Therefore, the requirement on the storage capacitor is significantly reduced with the proposed design.

E. Control of Ripple Cancellation Converter

Fig. 7 illustrates the way to achieve the RCC control. The PFC output $V_{o1}(t)$ is sensed and sent to the

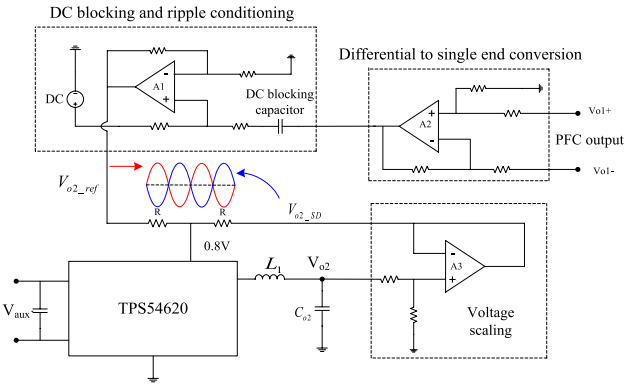


Fig. 8. Detailed circuit implementation of the RCC.

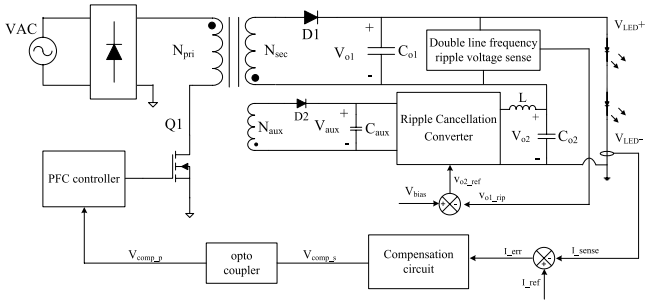


Fig. 9. Control diagram of the proposed Flyback ripple cancellation LED driver.

dc blocking unit (DBU). The DBU blocks the dc component of the signal while allowing the twice line frequency ripple go through. The output of the DBU is the twice line frequency ripple $V_{o1\_rip}(t)$. $V_{o1\_rip}(t)$ is further inverted and added with a dc bias voltage V_{bias}, and the result, V_{o2_ref}, becomes the reference voltage for the RCC. With a well designed feedback loop, the output voltage of the RCC, V_{o2}, should be able to tightly follow its reference voltage. Therefore, V_{o2} contains an opposite twice line frequency ripple voltage to that of V_{o1}, thus achieving ripple cancellation. Fig. 8 shows the detailed circuit implementation of the RCC. TPS54620, which is an integrated Buck converter including MOSFETs, gate driver, and controller, is used as the voltage controller. Similar alternative, such as LM2651 or FAN2013, can also be used. Three general purpose amplifiers TLV274CDR are used to sense and condition the twice line frequency ripple voltage of V_{o1} and generate the reference voltage for the RCC.

F. LED Current Regulation

Fig. 9 shows the current control diagram of the proposed LED driver. The change of compensation signal V_{comp_p} at the primary side results in a change of the rms input current (also means the input power). Furthermore, the change of the input current leads to the change of the output voltage V_{o1}. It should be noted that the dc voltage of V_{o2} is unchanged in the design. It is the dc voltage change of V_{o1} that leads to the change of the dc LED current. With the LED current regulation loop, V_{o1_dc} settles to the value that produces an LED current that is exactly equal to its reference.

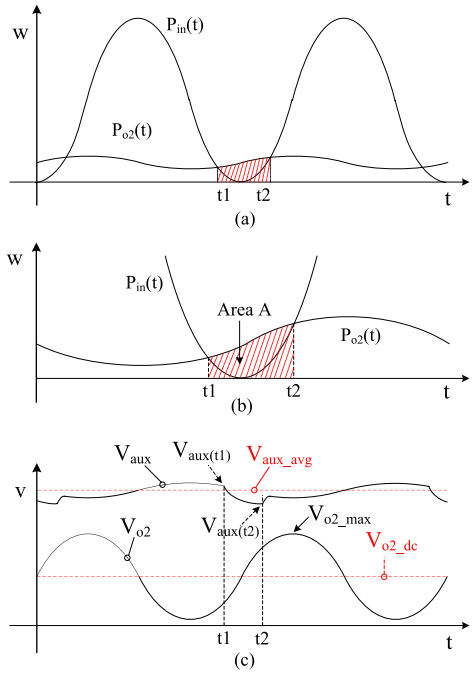


Fig. 10. Design consideration for C_{aux}. (a) Waveform of the input power and the required power to maintain V_{o2}. (b) Zoomed-in-view of (a). (c) Relationship of the waveform V_{aux} and V_{o2}.

III. Critical Design Parameter

In this section, the critical design parameters of the proposed LED driver are discussed.

A. PFC Output Capacitor C_{o1}

For the proposed LED driver, the capacitance of C_{o1} does not have a direct impact on the flicker. Therefore, it is desirable to use a small C_{o1} to achieve the lowest possible cost or even electrolytic capacitor free design. However, a smaller C_{o1} leads to a larger V_{o1} ripple. Furthermore, the larger V_{o1} ripple leads to more power processed by the RCC and lower overall efficiency. The capacitance of C_{o1} should be carefully selected in order to achieve an overall optimized design. As a design guideline, it is a good idea to make η_{eq} no less than 0.985. As shown in Fig. 4, when the efficiency of the RCC is 95%, the RF can be as high as 0.2 and η_{eq} is still $>$0.985. In a 50 V/0.7-A LED driving application, RF of 0.2 means that a 10 V pk-pk V_{o1} ripple voltage is allowed in the design. According to (16), C_{o1} can be selected to be 185 or 200 μF as a closest standard value, which is very small with respect to the power level.

Fig. 10 shows the key waveforms that is used to explain the design consideration for C_{aux}. As referring to Fig. 10(a), the instantaneous PFC input power is always higher than the RCC output power except when the input power is close to zero. The power needed to sustain the RCC operation can be supplied by the PFC input power directly. Therefore, C_{aux} do not need to store energy most of the time in a half-line cycle. C_{aux} does serve as an energy storage capacitor when the instantaneous PFC input power is lower than the RCC output power. During this time interval, C_{aux} provides the difference.

Therefore, C_{aux} should be selected accordingly to avoid too much voltage dip.

The required power to maintain V_{o2} is the sum of V_{o2} output power, and the power causing C_{o2} voltage changes. Since C_{o2} is very small in a typical design, the power causing C_{o2} changes is ignored in the discussion. For simplification and for leaving margin to design C_{aux}, it can be assumed that during the time interval $[t_1 - t_2]$, the energy needed to maintain V_{o2} is solely provided by C_{aux}. Area A in Fig. 10(b) represents the amount of energy that is used to maintain V_{o2} during the time $[t_1 - t_2]$. Area A can be expressed as

$$A_{\text{Area}} = \int_{t1}^{t2} P_{\text{o2}}(t)dt. \tag{17}$$

It should be noted that during $[t_1 - t_2]$, $V_{\text{o2}}(t)$ swings at the vicinity of its averaged value. Therefore, area A can be approximately presented as

$$A_{\text{Area}} \approx P_{\text{o2\_avg}} \times (t_2 - t_1) \tag{18}$$

where time t_1 and t_2 can be obtained by the equations

$$\begin{cases} P_{\text{o2}}(t_1) = P_{\text{in}}(t_1) \\ P_{\text{o2}}(t_2) = P_{\text{in}}(t_2) \end{cases} \tag{19}$$

or for simplicity, t_1 and t_2 can also be obtained by the following equations:

$$\begin{cases} P_{\text{o2\_avg}} = P_{\text{in}}(t_1) \\ P_{\text{o2\_avg}} = P_{\text{in}}(t_2). \end{cases} \tag{20}$$

Then, the length of $[t_1 - t_2]$ can be written as

$$t_2 - t_1 = \frac{\arccos\left[1 - \frac{P_{\text{o2\_avg}}}{2P_{\text{LED}}}\right]}{2\pi \times f_{\text{line}}}. \tag{21}$$

On the contrary, as it is shown in Fig. 10(c), the energy drawn from C_{aux} causes the voltage drop on C_{aux}. The area A can also be presented as the energy changes on C_{aux} during time interval $[t_1 - t_2]$. Therefore

$$A_{\text{Area}} = \frac{1}{2}C_{\text{aux}}[V_{\text{aux}}(t_1)]^2 - \frac{1}{2}C_{\text{aux}}[V_{\text{aux}}(t_2)]^2. \tag{22}$$

In (22), $V_{\text{aux}}(t_1)$ and $V_{\text{aux}}(t_2)$ represent the instantaneous voltage of $V_{\text{aux}}(t)$ at t_1 and t_2, respectively. Combining (18) and (22) yields

$$C_{\text{aux}} = \frac{P_{\text{o2\_avg}} \times (t_2 - t_1)}{\frac{1}{2}[V_{\text{aux}}(t_1) + V_{\text{aux}}(t_2)] \times [V_{\text{aux}}(t_1) - V_{\text{aux}}(t_2)]}. \tag{23}$$

Equation (23) can be also rewritten approximately as

$$C_{\text{aux}} \approx \frac{P_{\text{o2\_avg}} \times (t_2 - t_1)}{V_{\text{aux\_avg}} \times [V_{\text{aux}}(t_1) - V_{\text{aux}}(t_2)]}. \tag{24}$$

Because the RCC is built with Buck topology, its input voltage must be higher than its output voltage, which imposes the restriction on V_{aux}. As a design guideline, the criteria should be selected to be

$$V_{\text{aux}}(t_2) > 1.1V_{o2\_\max}. \tag{25}$$

TABLE III
FLYBACK EXPERIMENTAL PROTOTYPE CIRCUIT PARAMETERS

Flyback PFC Section	
Transformer turns ratio N_{pri}:N_{sec}:N_{aux}	38:15:4
Primary side winding inductance (L_{pri})	470μH
Main MOSFETs Q1	STF11NM80
PFC controller	FA5601N
Output capacitor C_{o1}	470μF, 63V
Ripple Cancellation Converter Section	
RCC input capacitor C_{aux}	160 μF, 16V
RCC output capacitor C_{o2}	20 μF, 16V
RCC output inductor L	4.7 μH
Switching Regulator	TPS54620
LED Load Section	
LED load	23 LEDs connect in series PN: LR W5AM-HZJZ-1-Z

Combining (21) and (23)–(25), the restriction of design C_{aux} is obtained as

$$C_{\text{aux}} \geq \frac{P_{\text{o2\_avg}} \times \arccos\left[1 - \frac{P_{\text{o2\_avg}}}{2P_{\text{LED}}}\right]}{2\pi \times f_{\text{line}} \times V_{\text{aux\_avg}} \times (V_{\text{aux\_avg}} - 1.1V_{\text{o2\_max}})}. \tag{26}$$

B. RCC Output Capacitor C_{o2}

The capacitor C_{o2} for the output V_{o2} is used to filter the high switching frequency ripple instead of using as storage capacitor Therefore, a $10 \sim 20$-μF ceramic capacitor can be used to filter out the switching frequency ripple, together with the inductor.

IV. EXPERIMENTAL RESULT

In this section, the experimental results are shown to validate the proposed LED driver. A 35-W, 50 V/0.7-A Flyback experimental prototype has been built to validate the proposed LED driving method. The circuit diagram of the experimental prototype is shown in Fig. 9. Table III shows the critical circuit parameters.

The Flyback PFC operates under boundary conduction mode to achieve a high power factor, low switching losses, and low switching current. The RCC is built with an integrated switching regulator, TPS54620, to reduce cost and simplify the design.

The key waveforms of the proposed Flyback experimental prototype are shown in Fig. 11. For the Flyback PFC main output, the 120-Hz output ripple voltage is 4 V. The RCC produces a 180° phase shifted 4 V pk–pk 120-Hz ripple voltage. Therefore, these two voltages have their 120-Hz ripple cancelled. A twice line frequency ripple free dc LED voltage and dc LED current are produced.

A ripple current comparison has also been performed between the proposed LED driver and a conventional single-stage LED driver. Their waveforms are shown in Figs. 12 and 13. The PFCs used in both the designs are identical and their output capacitor are the same 470-μF electrolytic capacitors. In order to accurately measure the

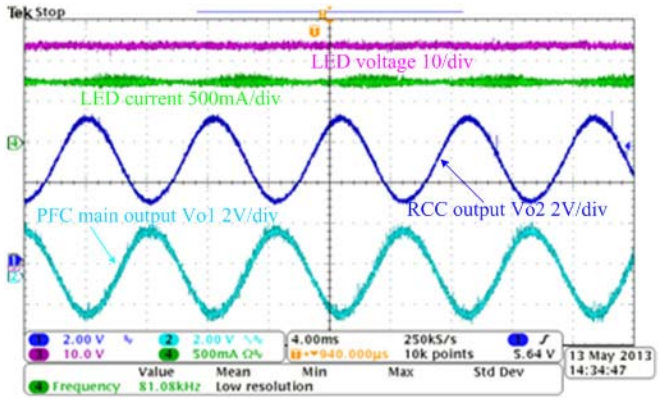
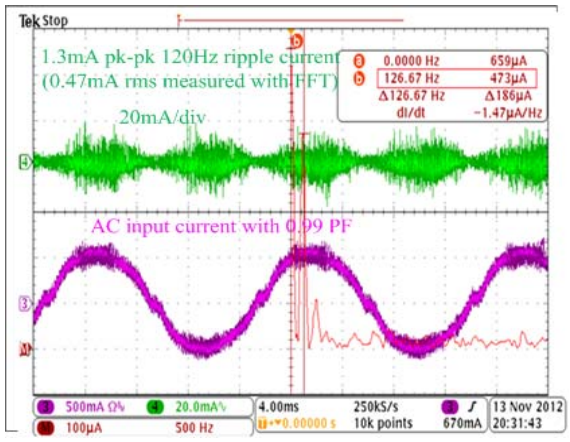
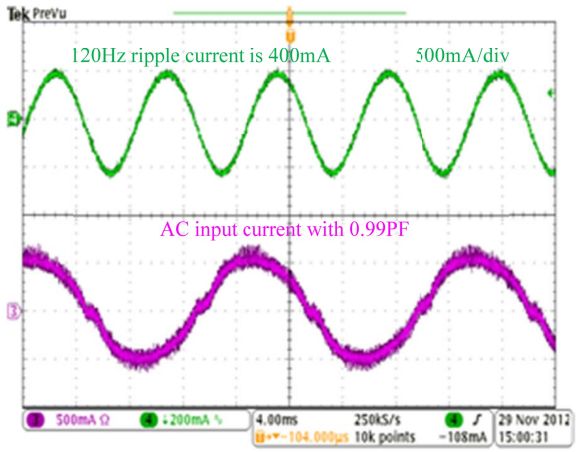


Fig. 11. Key waveforms of the proposed Flyback LED driver prototype ($V_{\text{in}} = 110$ V_{rms}, $V_{\text{LED}} = 50$ V, and $I_{\text{LED}} = 0.7$ A).



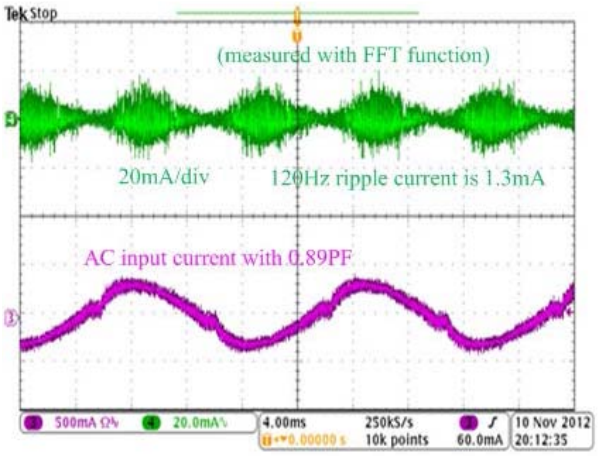
(a)



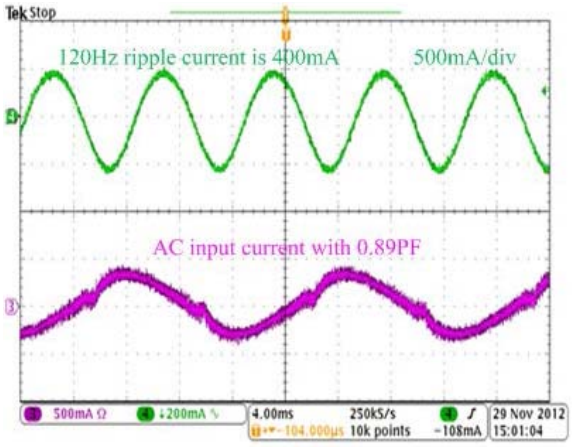
(b)

Fig. 12. Ripple current comparison between the proposed LED driver and the conventional single-stage LED driver ($V_{\text{in}} = 110$ V_{rms}, $V_{\text{LED}} = 50$ V, and $I_{\text{LED}} = 0.7$ A). (a) Proposed ripple cancellation LED driver. (b) Conventional Flyback LED driver.

120-Hz ripple current out of the high switching frequency noise, the FFT function in the oscilloscope was used for measurement. Under both 110 and 220 V_{rms} input voltages, the rms 120-Hz ripple current is measured to be 0.47 mA, which reflects a 1.3-mA pk–pk 120-Hz ripple current.



(a)



(b)

Fig. 13. Ripple current comparison between the proposed LED driver and the conventional single-stage LED driver ($V_{\text{in}} = 220$ V_{rms}, $V_{\text{LED}} = 50$ V, and $I_{\text{LED}} = 0.7$ A). (a) Proposed ripple cancellation LED driver. (b) Conventional Flyback LED driver.

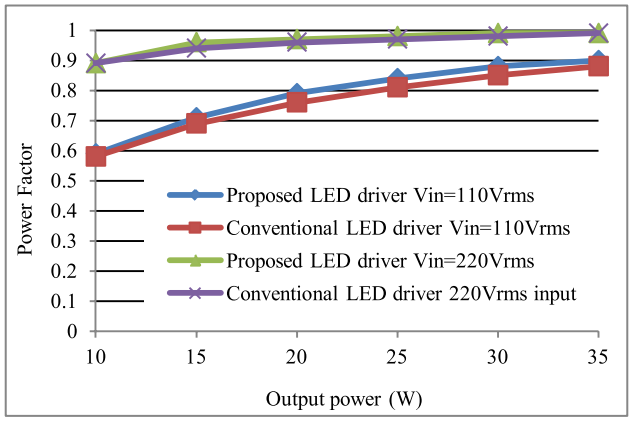


Fig. 14. Power factor of the proposed LED driver and the conventional LED driver.

Comparatively, the 120-Hz ripple current produced by the conventional single-stage LED driver is 400-mA pk–pk. The proposed ripple cancellation LED driver can reduce the LED current ripple by 265 times.

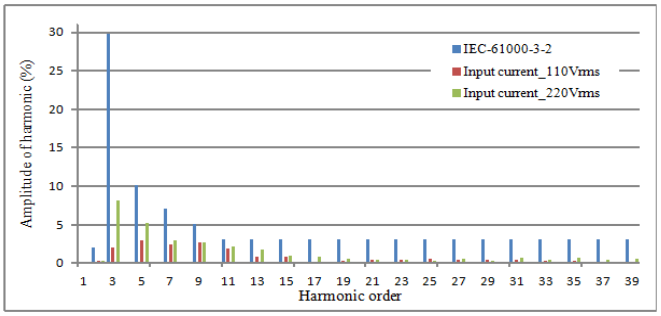


Fig. 15. Measured harmonic content of the input current.

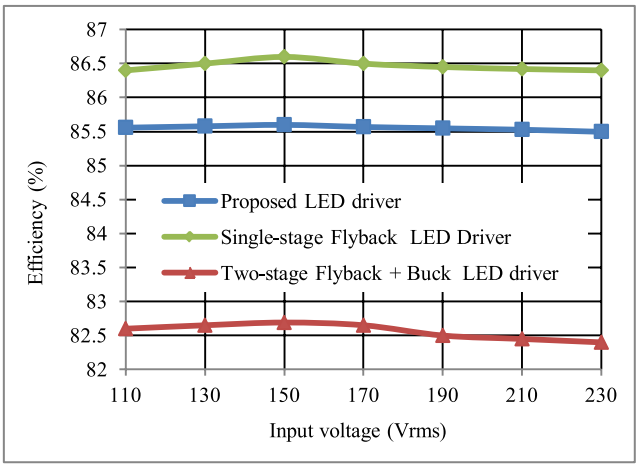


Fig. 16. Efficiency comparison between different designs at full load (50 V/0.7 A).

The power factor of the proposed the LED driver and the conventional LED driver have been shown in Fig. 14. It has demonstrated that the proposed LED driver can achieve a comparable power factor performance as a conventional design. The input current harmonics with the proposed LED driver have also been measured and shown in Fig. 15.

The efficiency comparison between the conventional single-stage LED driver, the proposed LED driver, and the conventional two-stage LED driver has been shown in Fig. 16. Identical PFCs are used in three designs. The RCC in the proposed LED driver has an averaged 90% efficiency. The second-stage dc–dc converter in the two-stage LED driver has a 96% efficiency.

Even the RCC efficiency is much lower than the second-stage dc–dc converter, the overall efficiency of the proposed LED driver is still 3% higher than the two-stage LED driver while only 1% lower than the single-stage LED driver. This is because the RCC only processes a small amount of total power and the loss it introduced is small compared with the overall system loss. The photo of the proposed Flyback experimental prototype is shown in Fig. 17.

Another 10-W, 50 V/0.2-A output Buck–Boost experimental prototype has also been built to verify the possibility of using ceramic storage capacitor. Fig. 18 shows the circuit diagram and Table IV shows the key circuit parameters.

One more benefit from the Buck–Boost-based ripple cancellation LED driver is the possibility of integrating the

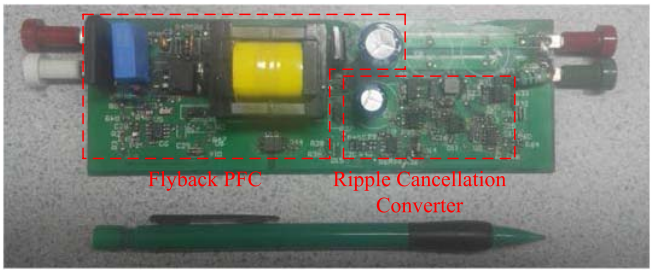


Fig. 17. Photo of the Flyback experimental prototype.

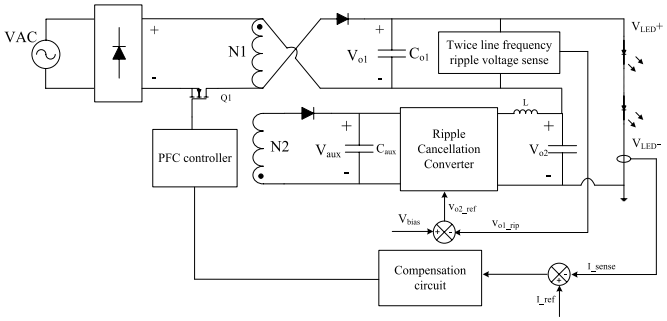


Fig. 18. Circuit diagram of the proposed Buck–Boost LED driver prototype.

TABLE IV
BUCK–BOOST EXPERIMENTAL PROTOTYPE CIRCUIT PARAMETERS

Buck-Boost PFC Section	
Inductor turns ratio N1: N2	42:13
Inductor (winding N1)	985μH
Main MOSFET Q1	STP3NK80Z
Controller	FL7732
Output capacitor C_{o1}	3 x 20μF
Ripple Cancellation Converter Section	
RCC input capacitor C_{aux}	20μF, 16V
RCC output capacitor C_{o2}	4.7μF, 16V
RCC output inductor L	22μH
Switching controller	FAN8303
Load Section	
LED load	26 LEDs connect in series PN: LR W5AM-HZJZ-1-Z

PFC controller, compensation circuit, and the RCC into a single chip. Thus, the Buck–Boost implementation of the proposed LED driver can be very cost effective.

The key waveforms of the Buck–Boost experimental prototype are shown in Fig. 19. In this design, the output capacitor has been intentionally reduced to 60 μF so that a reasonable amount of ceramic capacitors can be used in the design. The twice line frequency ripple voltage on V_{o1} is 9 V pk–pk. The RCC also produces an opposite 9 V pk–pk ripple voltage to cancel the ripple voltage from V_{o1}. As a result, the twice line frequency ripple LED voltage has been substantially reduced.

The produced ripple currents and light flicker are compared between the conventional Buck–Boost LED driver and the proposed Buck–Boost LED driver. The result is shown in Fig. 20. Both LED drivers are connected with the same 60-μF ceramic output capacitors and output 200-mA average LED current. With the conventional Buck–Boost LED driver,

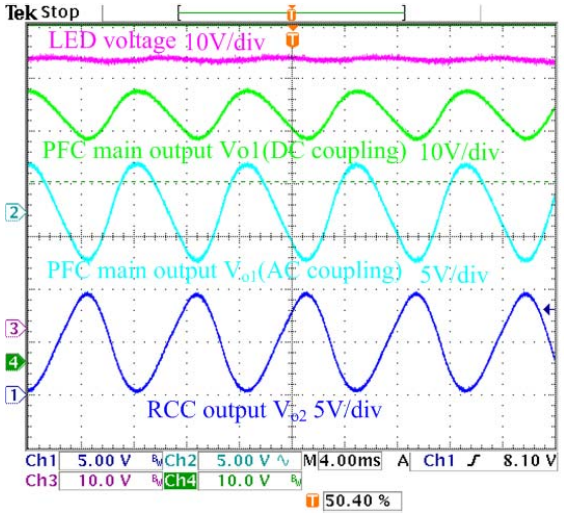


Fig. 19. Key waveforms of the proposed Buck–Boost LED driver ($V_{\text{in}} = 110$ V_{rms}, $V_{\text{LED}} = 50$ V, and $I_{\text{LED}} = 0.2$ A).

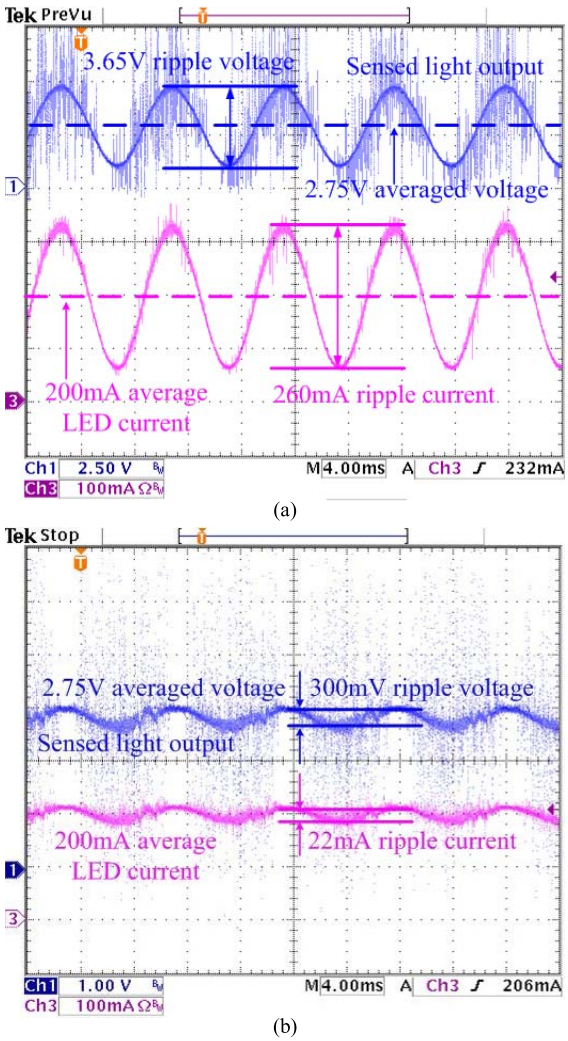


Fig. 20. Ripple current and light flickering comparison between the proposed LED driver and the conventional LED driver. (a) Conventional Buck-Boost LED driver. (b) Proposed Buck-Boost LED driver.

the pk–pk twice line frequency ripple current is as high as 260 mA, which means 65% ripple current. Comparatively, with the proposed LED driver, the pk–pk ripple current is

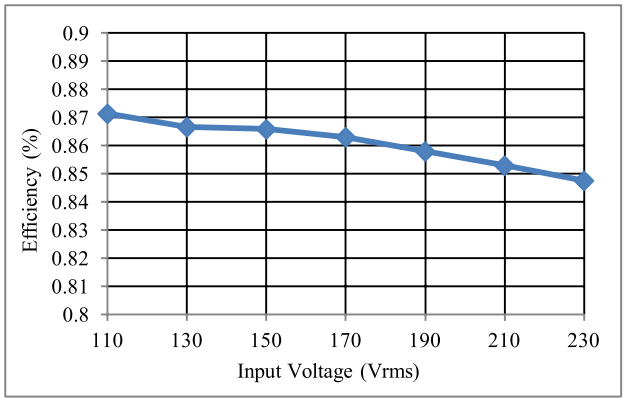


Fig. 21. Efficiency of the Buck–Boost experimental prototype at full load (50 V/0.2 A).

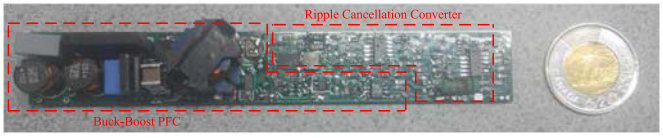


Fig. 22. Photo of the Buck–Boost experimental prototype.

reduced to be 22 mA, which means 5.5% ripple current. The proposed Buck–Boost prototype achieved 12 times ripple current reduction. The light outputs produced by the LEDs are also shown and presented as voltage quantities. With the conventional Buck–Boost LED driver, the light ripple is presented as 3.65 V, while the averaged light output is presented as 2.75 V, which means 66% flicker. With the proposed LED current, the light ripple is presented as 300 mV, while the averaged light output is also 2.75 V, which means 5.4% flicker. The flicker ratio between these two technologies is also ∼12 times. The ripple currents are almost proportionally presented as flicker. The ripple current as well as flicker can be further reduced with the proposed Buck–Boost LED driver when the RCC has better reference tracing performance.

The efficiency of the Buck–Boost prototype is shown in Fig. 21. The photo of the Buck–Boost experimental prototype is shown in Fig. 22.

V. Conclusion

A ripple cancellation LED driving method is proposed in this paper. A miniature converter is used to generate an opposite twice line frequency ripple voltage to compensate the ripple voltage from the main output of the PFC. As a result, a dc LED voltage, a dc LED current are obtained and therefore achieved flicker-free LED driving.

A 35-W, 50 V/0.7-A Flyback LED driver prototype and a 10-W, 50 V/0.2-A Buck–Boost LED driver prototype have been implemented and tested to validate the proposed LED driving method. With the proposed LED driver, the required output capacitor can also be greatly reduced, which means a reduction on the component cost. The output capacitors for the 10-W Buck–Boost prototype have even been reduced to 60 μF, and can be implemented by ceramic capacitors for long lifespan. The proposed LED driver also achieves a high efficiency, which is very close to a conventional

single-stage LED driver while much higher than a conventional two-stage LED driver. Because the RCC only processes a very small portion of the total output power and experiences very low voltage stress, the implementation cost for the RCC is very low. The overall component cost of the proposed LED driver is close to a conventional single-stage LED driver while much lower than a conventional two-stage LED driver.

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